

# SN65LBC174, SN75LBC174 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVERS

SLLS162D – JULY 1993 – REVISED SEPTEMBER 2003

- Meets or Exceeds the Standard EIA-485
- Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments
- Supports Data Rates up to and Exceeding Ten Million Transfers Per Second
- Common-Mode Output Voltage Range of  $-7\text{ V}$  to  $12\text{ V}$
- Positive- and Negative-Current Limiting
- Low Power Consumption . . .  $1.5\text{ mA}$  Max (Output Disabled)
- Functionally Interchangeable With SN75174

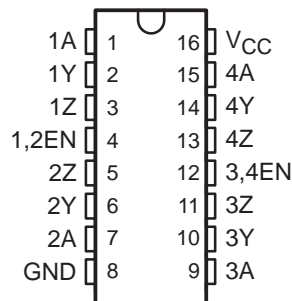
## description

The SN65LBC174 and SN75LBC174 are monolithic, quadruple, differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of the Electronics Industry Association Standard EIA-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown protection, making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultralow power consumption and inherent robustness.

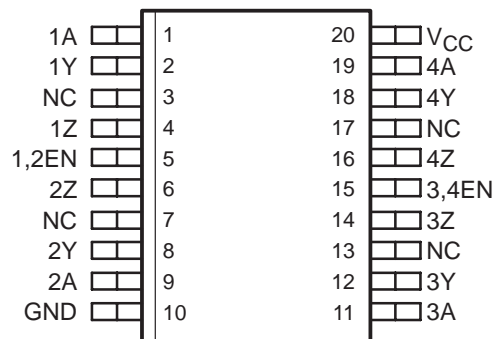
Both the SN65LBC174 and SN75LBC174 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC174 and SN75LBC174 are available in the 16-terminal DIP package (N) and the 20-terminal wide-body small outline intergrated circuit (SOIC) package (DW).

The SN75LBC174 is characterized for operation over the commercial temperature range of  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . The SN65LBC174 is characterized over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**N PACKAGE  
(TOP VIEW)**



**DW PACKAGE  
(TOP VIEW)**



NC – No internal connection

**FUNCTION TABLE  
(each driver)**

INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level,  
X = irrelevant, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



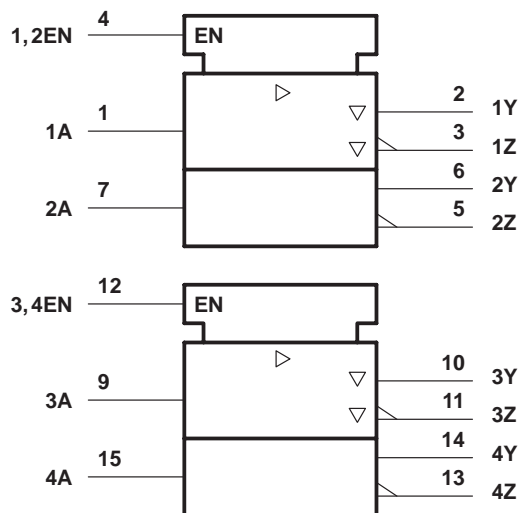
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001–2003, Texas Instruments Incorporated

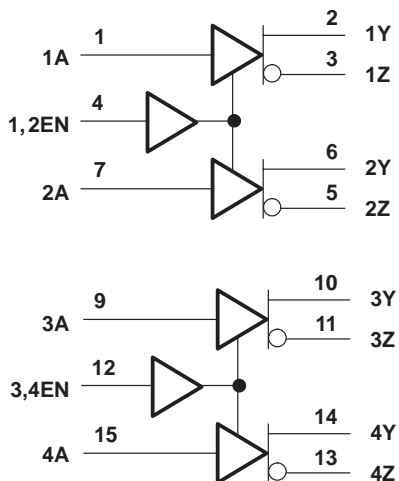
# SN65LBC174, SN75LBC174 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVERS

SLLS162D – JULY 1993 – REVISED SEPTEMBER 2003

## logic symbol†

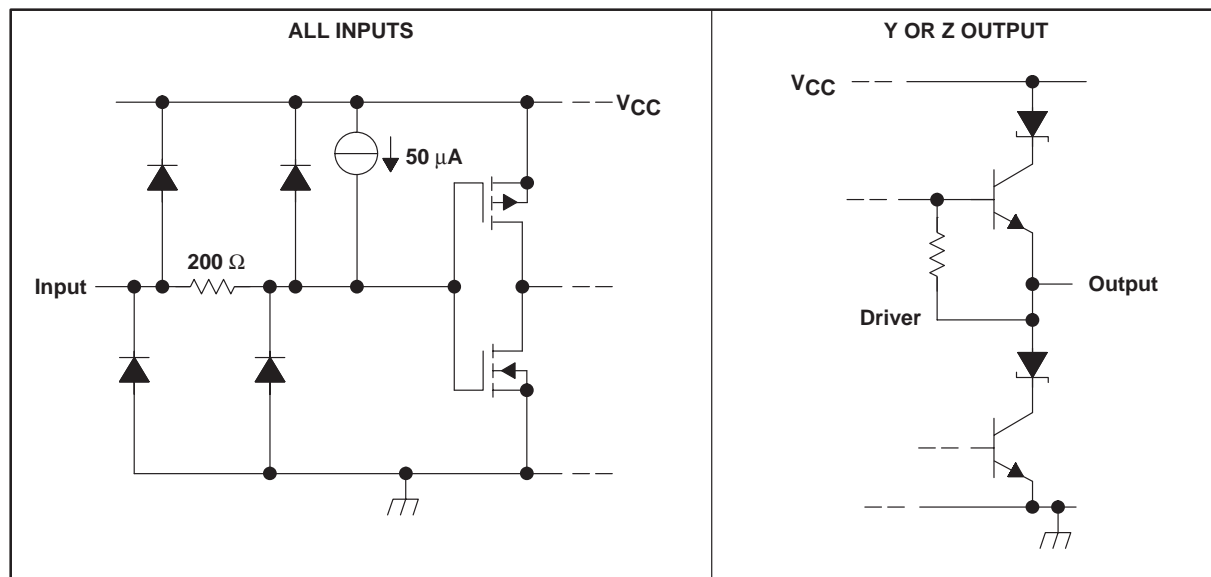


## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Terminal numbers shown are for the N package.

## schematic of inputs and outputs



# SN65LBC174, SN75LBC174 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVERS

SLLS162D – JULY 1993 – REVISED SEPTEMBER 2003

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 7 V
Output voltage range, $V_O$	–10 V to 15 V
Voltage range at A, 1/2EN, 3/4EN	–0.3 V to $V_{CC} + 0.5$ V
Continuous total power dissipation	Internally limited‡
Operating free-air temperature range, $T_A$ : SN65LBC174	–40°C to 85°C
SN75LBC174	0°C to 70°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature.

NOTE 1: All voltage values are with respect to GND.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
High-level input voltage, $V_{IH}$		2			V
Low-level input voltage, $V_{IL}$		0.8			V
Voltage at any bus terminal (separately or common-mode), $V_O$	Y or Z	12			V
		–7			
High-level output current, $I_{OH}$	Y or Z	–60			mA
Low-level output current, $I_{OL}$	Y or Z	60			mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature, $T_A$	SN65LBC174	–40			°C
	SN75LBC174	0	70		

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$
	POWER RATING	ABOVE $T_A = 25^\circ\text{C}$	POWER RATING	POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

# SN65LBC174, SN75LBC174 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVERS

SLLS162D – JULY 1993 – REVISED SEPTEMBER 2003

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = -18 mA				-1.5	V
V <sub>OD</sub>	Differential output voltage‡	R <sub>L</sub> = 54 Ω, See Figure 1	SN65LBC174	1.1	1.8	5	V
			SN75LBC174	1.5	1.8	5	
		R <sub>L</sub> = 60 Ω, See Figure 2	SN65LBC174	1.1	1.7	5	
			SN75LBC174	1.5	1.7	5	
Δ V <sub>OD</sub>	Change in magnitude of common-mode output voltage§					±0.2	V
V <sub>OC</sub>	Common-mode output voltage	R <sub>L</sub> = 54 Ω, See Figure 1				3 -1	V
Δ V <sub>OC</sub>	Change in magnitude of common-mode output voltage§					±0.2	V
I <sub>O</sub>	Output current with power off	V <sub>CC</sub> = 0, V <sub>O</sub> = -7 V to 12 V				±100	μA
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = -7 V to 12 V				±100	μA
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 2.4 V				-100	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0.4 V				-100	μA
I <sub>OS</sub>	Short-circuit output current	V <sub>O</sub> = -7 V to 12 V				±250	mA
I <sub>CC</sub>	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

† All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

‡ The minimum V<sub>OD</sub> specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal transmission distance.

§ Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
t <sub>d(OD)</sub>	Differential output delay time	R <sub>L</sub> = 54 Ω, See Figure 3			2	11	20	ns
t <sub>t(OD)</sub>	Differential output transition time				10	15	25	ns
t <sub>PZH</sub>	Output enable time to high level	R <sub>L</sub> = 110 Ω, See Figure 3				20	30	ns
t <sub>PZL</sub>	Output enable time to low level	R <sub>L</sub> = 110 Ω, See Figure 5				21	30	ns
t <sub>PHZ</sub>	Output disable time from high level	R <sub>L</sub> = 110 Ω, See Figure 4				48	70	ns
t <sub>PLZ</sub>	Output disable time from low level	R <sub>L</sub> = 110 Ω, See Figure 5				21	30	ns



PARAMETER MEASUREMENT INFORMATION

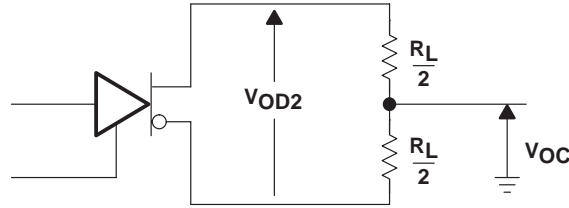


Figure 1. Differential and Common-Mode Output Voltages

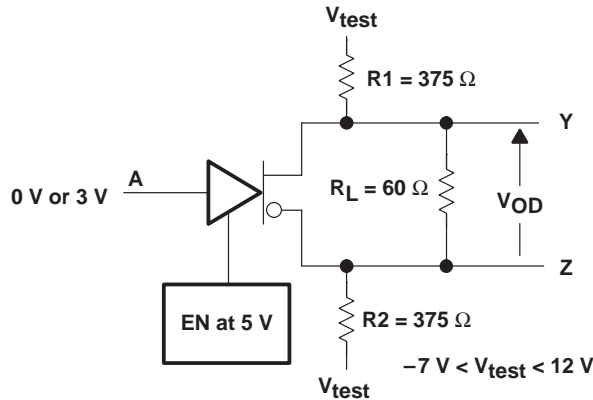
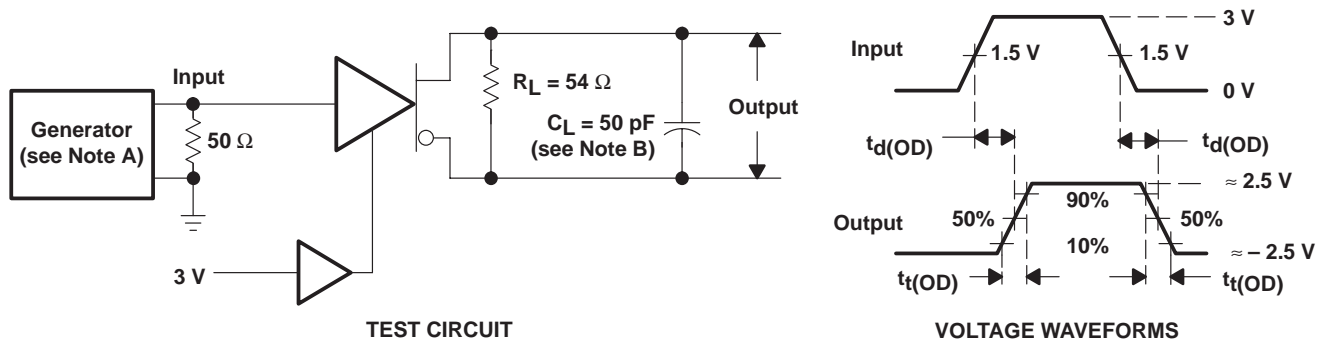


Figure 2. Driver  $V_{OD}$  Test Circuit



- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, duty cycle = 50%,  $t_r \leq 5$  ns,  $t_f \leq 5$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.

Figure 3. Time Waveforms for Driver Differential Output Test Circuit Delay and Transition

# SN65LBC174, SN75LBC174 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVERS

SLLS162D – JULY 1993 – REVISED SEPTEMBER 2003

## PARAMETER MEASUREMENT INFORMATION

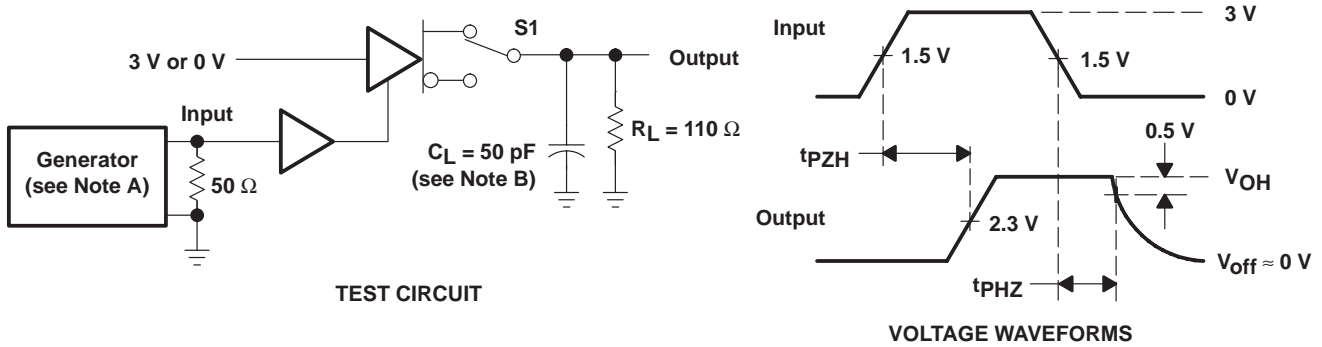
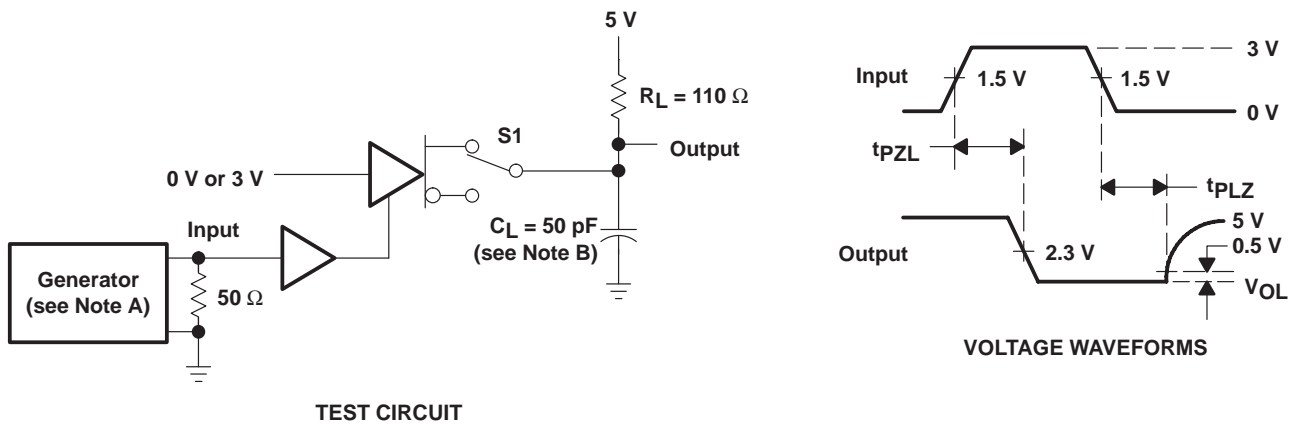


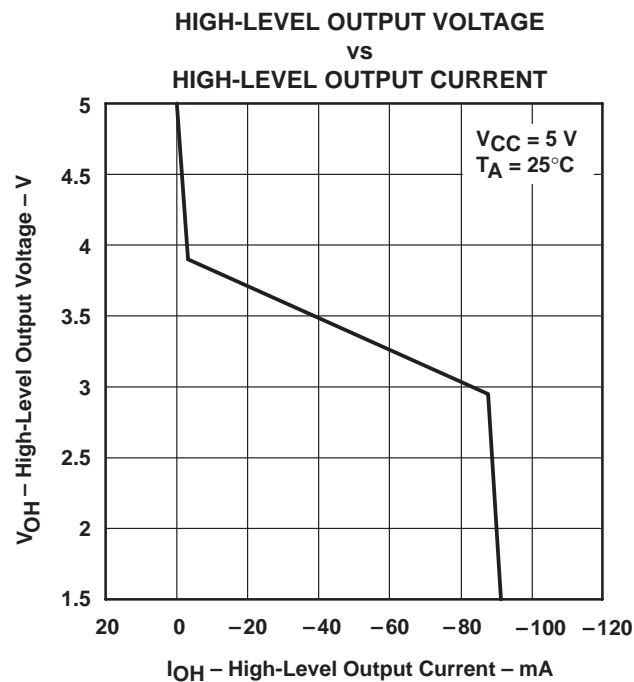
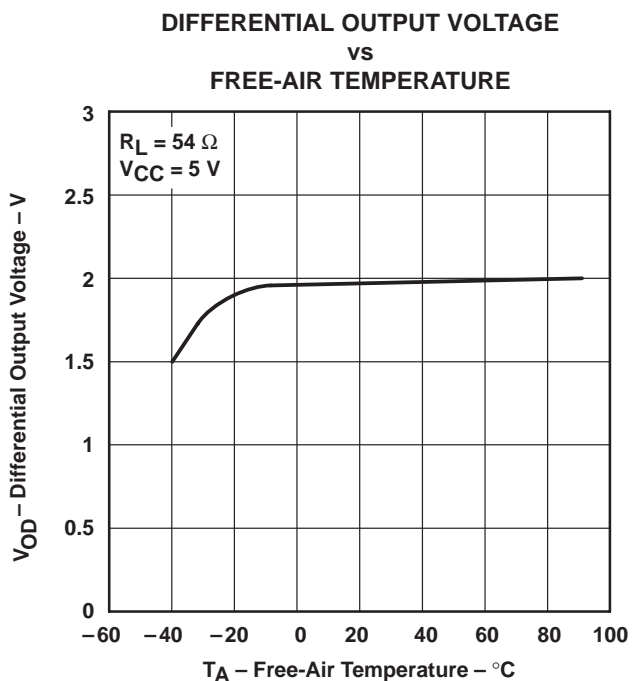
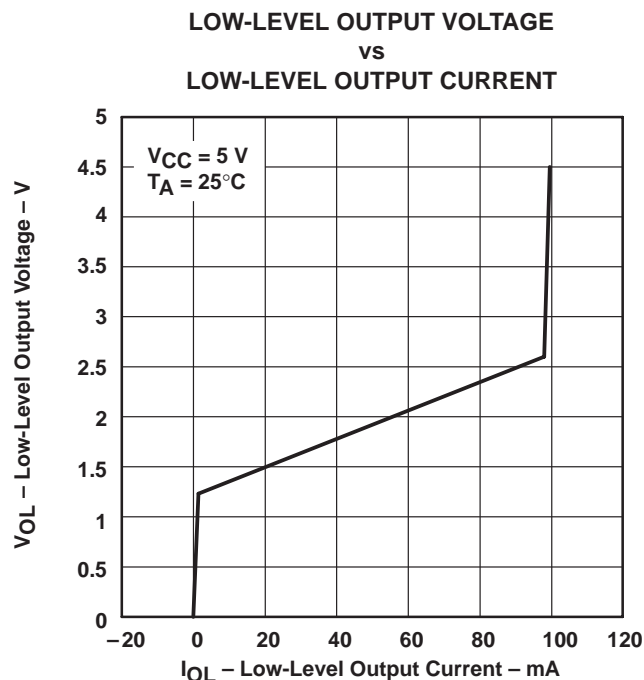
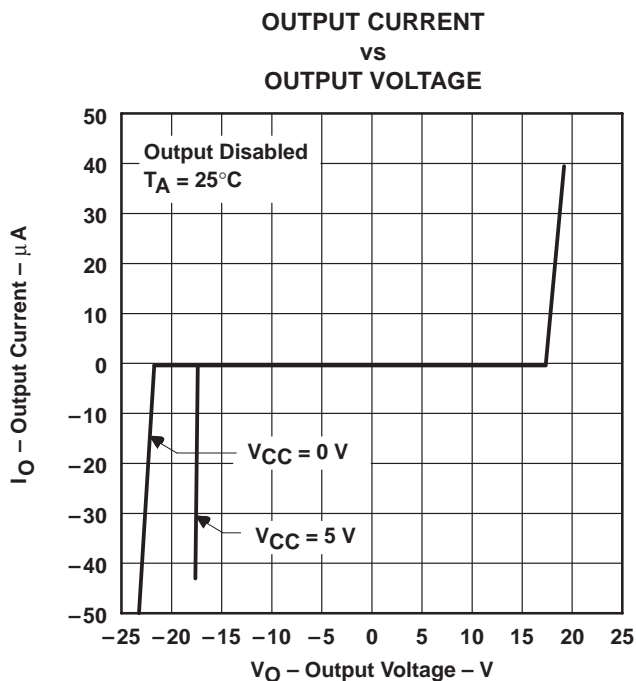
Figure 4.  $t_{pZH}$  and  $t_{pHZ}$  Test Circuit and Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, duty cycle = 50%,  $t_r \leq 5$  ns,  $t_f \leq 5$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.

Figure 5.  $t_{pZL}$  and  $t_{pLZ}$  Test Circuit and Waveforms

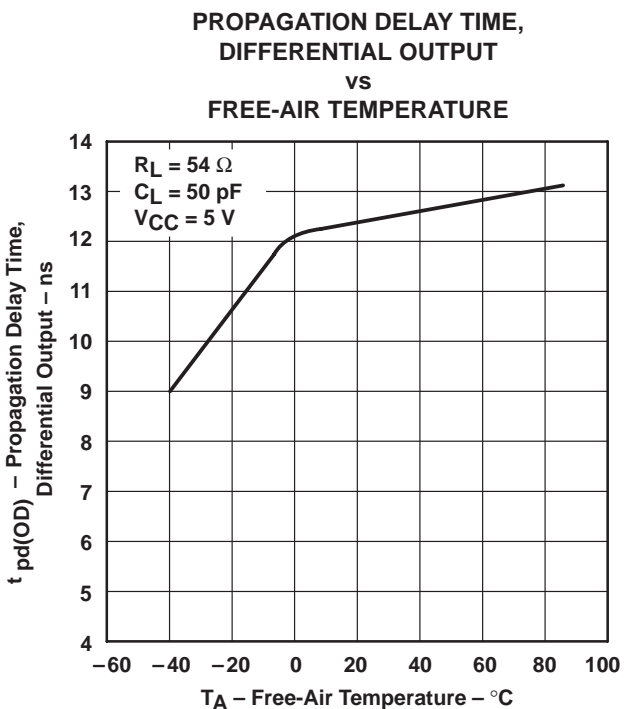
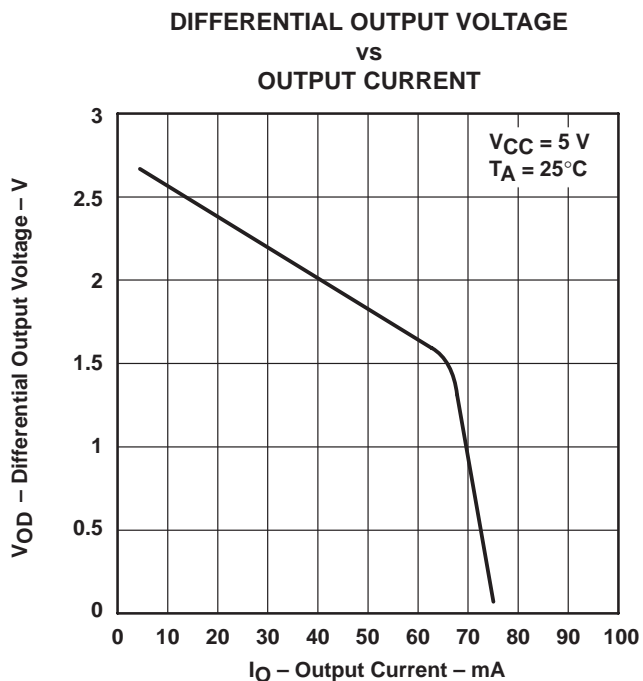
TYPICAL CHARACTERISTICS



# SN65LBC174, SN75LBC174 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVERS

SLLS162D – JULY 1993 – REVISED SEPTEMBER 2003

## TYPICAL CHARACTERISTICS





**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC174DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65LBC174	<a href="#">Samples</a>
SN65LBC174DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65LBC174	<a href="#">Samples</a>
SN65LBC174N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	SN65LBC174N	<a href="#">Samples</a>
SN75LBC174DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC174	<a href="#">Samples</a>
SN75LBC174DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC174	<a href="#">Samples</a>
SN75LBC174N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN75LBC174N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN75LBC174 :**

- Military: [SN55LBC174](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LBC174DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LBC174DWR	SOIC	DW	20	2000	367.0	367.0	45.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated