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October 2013

FDPF3N50NZ

N-Channel UniFETTM II MOSFET 500 V, 3 A, 2.5 Ω

Features

- $R_{DS(on)}$ = 2.1 Ω (Typ.) @ V_{GS} = 10 V, I_D = 1.5 A
- Low Gate Charge (Typ. 6.2 nC)
- Low C_{rss} (Typ. 2.5 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability
- · ESD Improved Capability
- · RoHS Compliant

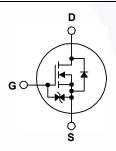
Applications

- · LCD/LED TV
- · Uninterruptible Power Supply
- Lighting
- · AC-DC Power Supply

Description

UniFETTM II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballats





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FDPF3N50NZ	Unit	
V _{DSS}	Drain to Source Voltage			500	V	
V _{GSS}	Gate to Source Voltage		±25	V		
	Drain Current	- Continuous (T _C = 25°C)		3*	^	
ID	Drain Current	- Continuous (T _C = 100°C)		1.8*	A	
I _{DM}	Drain Current	- Pulsed	(Note 1)	12*	Α	
E _{AS}	Single Pulsed Avalanche En	(Note 2)	113	mJ		
I _{AR}	Avalanche Current		(Note 1)	3	Α	
E _{AR}	Repetitive Avalanche Energy	1	(Note 1)	5.4	mJ	
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	10	V/ns	
D	Dawer Discipation	(T _C = 25°C)		27	W	
P_{D}	Power Dissipation	- Derate above 25°C		0.21	W/°C	
T _J , T _{STG}	Operating and Storage Temp	erature Range		-55 to +150	°C	
T _L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C	

^{*}Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter FDPF3N50NZ		Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	°C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDPF3N50NZ	FDPF3N50NZ	TO-220F	Tube	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A$, $V_{GS} = 0V$, $T_C = 25^{\circ}C$	500	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	-	0.5	-	V/°C
	Zero Gate Voltage Drain Current	V _{DS} = 500V, V _{GS} = 0V	-	-	1	μА
I _{DSS}	Zero Gate voltage Drain Current	$V_{DS} = 400V, V_{GS} = 0V, T_{C} = 125^{\circ}C$	-	-	10	μΑ
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25V, V_{DS} = 0V$	-	-	±10	μΑ

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10V, I _D = 1.5A	-	2.1	2.5	Ω
g _{FS}	Forward Transconductance	V _{DS} = 20V, I _D = 1.5A	-	1.9	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance		V 051/1/ 01/	-	210	280	pF
Coss	Output Capacitance		$V_{DS} = 25V, V_{GS} = 0V$ f = 1MHz		30	45	pF
C _{rss}	Reverse Transfer Capacitance				2.5	5	pF
Q _{g(tot)}	Total Gate Charge at 10V			- \	6.2	9	nC
Q _{gs}	Gate to Source Gate Charge		$V_{DS} = 400V I_{D} = 3A$	-	1.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		$V_{GS} = 10V$ (Note 4)	-	3.1	-	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	10	30	ns
t _r	Turn-On Rise Time	$V_{DD} = 250V, I_D = 3A$	-	15	40	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10V, R_{GEN} = 25 Ω	-	26	60	ns
t _f	Turn-Off Fall Time	(Note 4)	-	17	45	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	3	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	12	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = 3A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 3A	-	190	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	-	0.52	_	μС

Notes:

- Repetitive Rating: Pulse width limited by maximum junction temperature
- 2. L = 25mH, I_{AS} = 3A, V_{DD} = 50V, R_{G} = 25 Ω , Starting T_{J} = 25 $^{\circ}$ C
- 3. $I_{SD} \leq$ 3A, di/dt \leq 200A/ μ s, $V_{DD} \leq$ BV $_{DSS}$, Starting T $_{J}$ = 25°C
- 4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

Figure 1. On-Region Characteristics

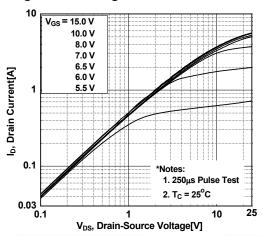


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

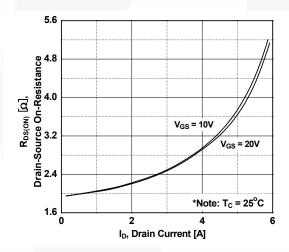


Figure 5. Capacitance Characteristics

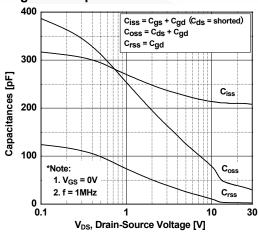


Figure 2. Transfer Characteristics

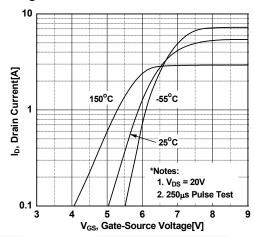


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

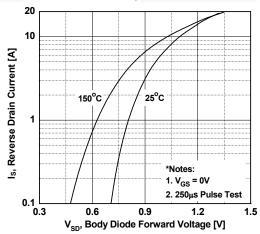
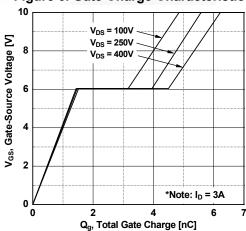


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

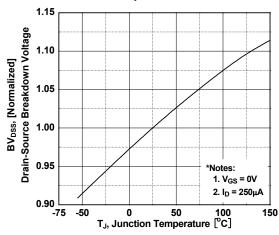


Figure 8. On-Resistance Variation vs. Temperature

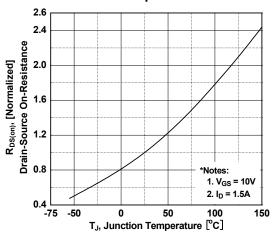


Figure 9. Maximum Safe Operating Area vs. Case Temperature-FDPF3N50NZ

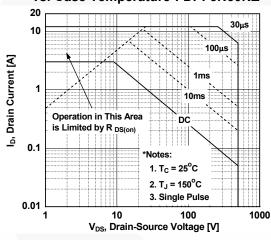


Figure 10. Maximum Drain Current

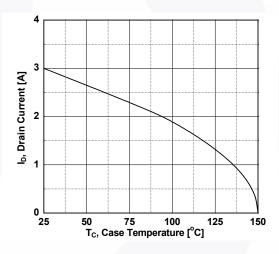
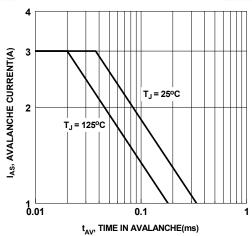


Figure 11. Unclamped Inductive Switching Capability



Typical Characteristics (Continued)

Figure 12. Transient Thermal Response Curve- FDPF3N50NZ

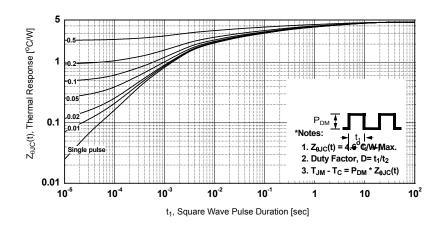


Figure 13. Gate Charge Test Circuit & Waveform

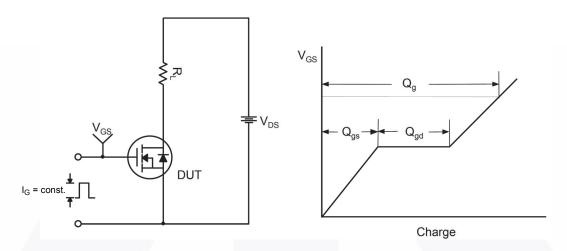


Figure 14. Resistive Switching Test Circuit & Waveforms

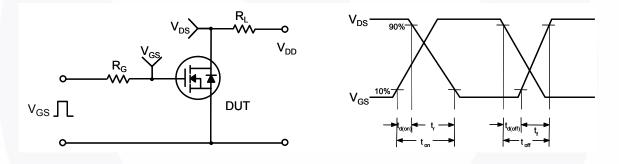
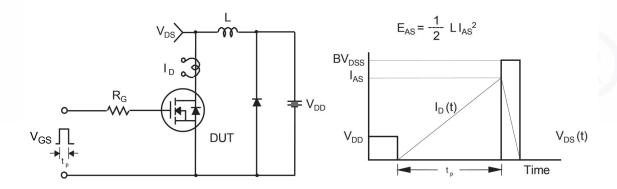


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms



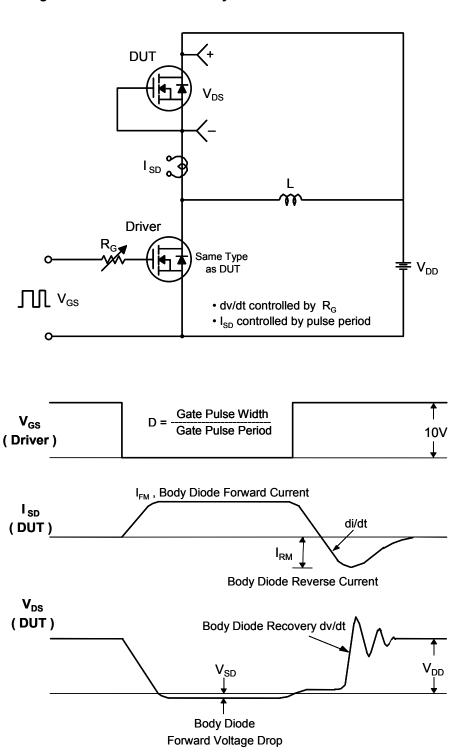


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

TO-220F 3L

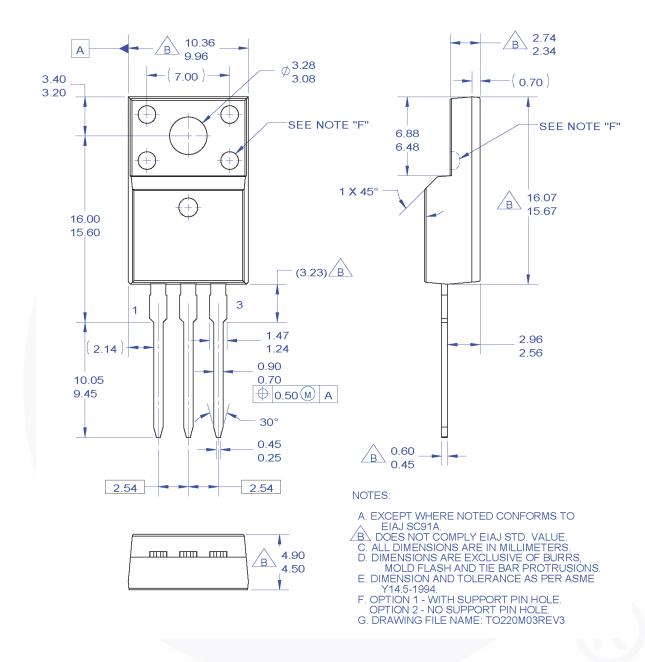


Figure 17. TO220, Molded, 3LD, Full Pack, EIAJ SC91, Straight Lead

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Dimension in Millimeters





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