# 3-V TO 5.5-V MULTICHANNEL RS-232 1-MBit/s LINE DRIVER/RECEIVER

**Check for Samples: TRS3237E**

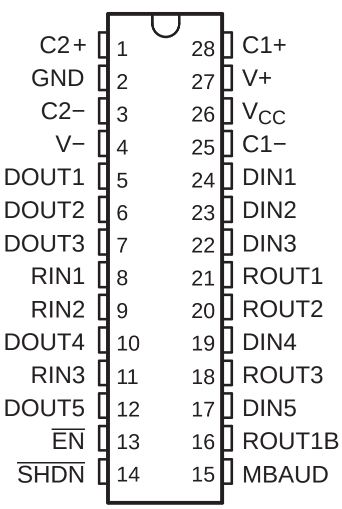
## FEATURES

- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V $V_{CC}$ Supply
- Operates From 250 kbits/s to 1 Mbit/s
- Low Standby Current . . . 1 μA Typical
- External Capacitors . . . 4 × 0.1 μF
- Accepts 5-V Logic Input With 3.3-V Supply
- Designed to Be Interchangeable With Industry Standard '3237E Devices
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection for RS-232 I/O Pins
  - ±15 kV – Human-Body Model (HBM)
  - ±8 kV – IEC61000-4-2, Contact Discharge
  - ±15 kV – IEC61000-4-2, Air-Gap Discharge

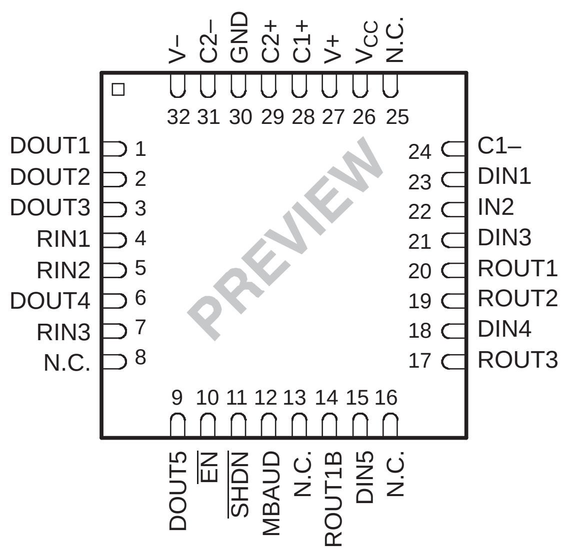
## APPLICATIONS

- Battery-Powered, Hand-Held, and Portable Equipment
- PDAs and Palmtop PCs
- Notebooks, Sub-Notebooks, and Laptops
- Digital Cameras
- Mobile Phones and Wireless Devices

DB, DW, OR PW PACKAGE
(TOP VIEW)




RHB PACKAGE
(TOP VIEW)




N.C.– Not internally connected

## DESCRIPTION/ORDERING INFORMATION

The TRS3237E consists of five line drivers, three line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. This device operates at data signaling rates of 250 kbit/s in normal operating mode (MBAUD = GND) and 1Mbit/s when MBAUD = $V_{CC}$. The driver output slew rate is a maximum of 30 V/μs.

The TRS3237E transmitters are disabled and the outputs are forced into high-impedance state when the device is in shutdown mode ($\overline{SHDN}$ = GND) and the supply current falls to less than 1 μA. Also, during shutdown, the onboard charge pump is disabled; V+ is lowered to $V_{CC}$, and V– is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting enable ($\overline{EN}$) high. ROUT1B remains active all the time, regardless of the $\overline{EN}$ and $\overline{SHDN}$ condition.

The TRS3237EC is characterized for operation from 0°C to 70°C. The TRS3237EI is characterized for operation from –40°C to 85°C.

**Table 1. ORDERING INFORMATION(1)**

| $T_A$ | PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | SSOP – DB | Reel of 2000 | TRS3237ECDBR | TRS3237EC |
| | SOIC – DW | Reel of 2000 | TRS3237ECDWR | TRS3237EC |
| | TSSOP – PW | Reel of 2000 | TRS3237ECPWR | RS37EC |
| | QFN – RHB | Reel of 2000 | TRS3237ECRHBR | PREVIEW |
| –40°C to 85°C | SSOP – DB | Reel of 2000 | TRS3237EIDBR | TRS3237EI |
| | SOIC – DW | Reel of 2000 | TRS3237EIDWR | TRS3237EI |
| | TSSOP – PW | Reel of 2000 | TRS3237EIPWR | RS37EI |
| | QFN – RHB | Reel of 2000 | TRS3237EIRHBR | PREVIEW |

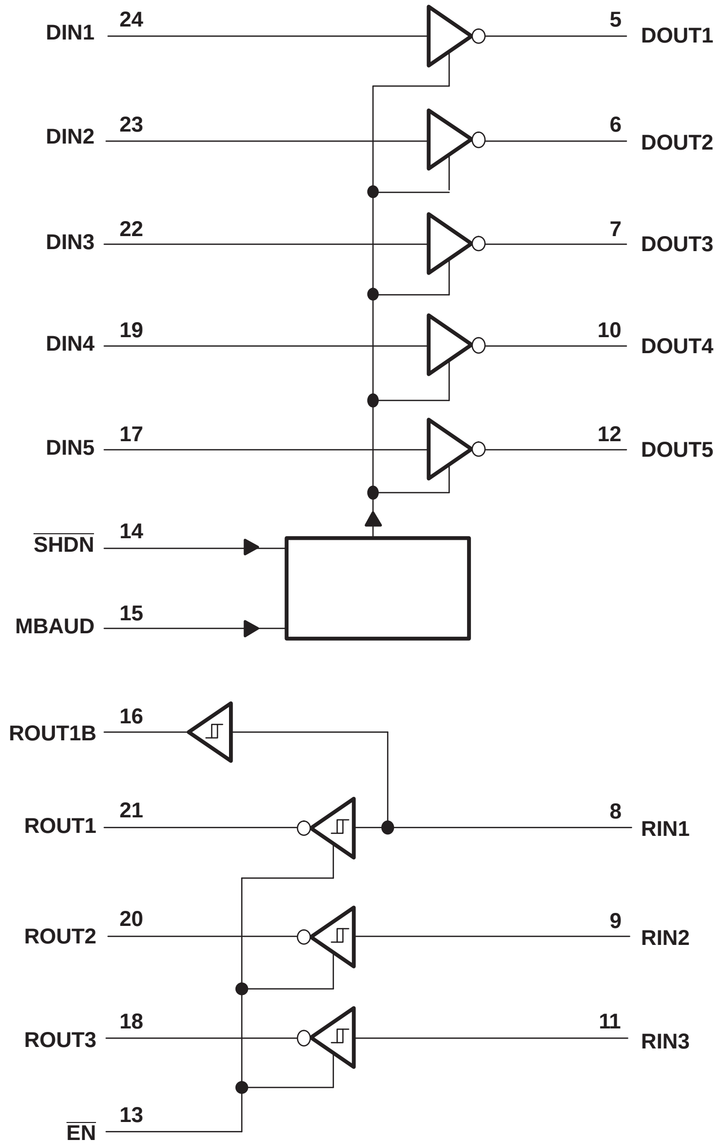
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

**Table 2. FUNCTION TABLE**

| INPUTS | | OUTPUTS | | |
|---|---|---|---|---|
| $\overline{SHDN}$ | $\overline{EN}$ | DOUT | ROUT | ROUT1B |
| 0 | 0 | Z(1) | Active | Active |
| 0 | 1 | Z(1) | Z(1) | Active |
| 1 | 0 | Active | Active | Active |
| 1 | 1 | Active | Z(1) | Active |

(1) Z = high impedance (off)

## LOGIC DIAGRAM (POSITIVE LOGIC)



## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range(2) | | –0.3 | 6 | V |
| V+ | Positive-output supply voltage range(2) | | –0.3 | 7 | V |
| V– | Negative-output supply voltage range(2) | | 0.3 | –7 | V |
| V+ – V– | Supply voltage difference(2) | | | 13 | V |
| $V_I$ | Input voltage range | Driver ($\overline{SHDN}$, MBAUD, $\overline{EN}$) | –0.3 | 6 | V |
| | | Receiver | –25 | 25 | |
| $V_O$ | Output voltage range | Driver | –13.2 | 13.2 | V |
| | | Receiver | –0.3 | $V_{CC}$ + 0.3 | |
| | Short-circuit duration | DOUT to GND | Unlimited | | |
| $\theta_{JA}$ | Package thermal impedance(3) | | | 62 | °C/W |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS(1)

See Figure 5

| | | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Supply voltage | | $V_{CC}$ = 3.3 V | 3 | 3.3 | 3.6 | V |
| | | | $V_{CC}$ = 5 V | 4.5 | 5 | 5.5 | |
| $V_{IH}$ | Driver and control high-level input voltage | DIN, $\overline{SHDN}$, MBAUD, $\overline{EN}$ | $V_{CC}$ = 3.3 V | 2 | | 5.5 | V |
| | | | $V_{CC}$ = 5 V | 2.4 | | 5.5 | |
| $V_{IL}$ | Driver and control low-level input voltage | DIN, $\overline{SHDN}$, MBAUD, $\overline{EN}$ | | 0 | | 0.8 | V |
| $V_I$ | Receiver input voltage | | | –25 | | 25 | V |
| $T_A$ | Operating free-air temperature | | TRS3237EC | 0 | | 70 | °C |
| | | | TRS3237EI | –40 | | 85 | |

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC}$ = 3 V to 5 V.

## ELECTRICAL CHARACTERISTICS(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP(2) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_I$ | Input leakage current | DIN, $\overline{SHDN}$, MBAUD, $\overline{EN}$ | | | 9 | 18 | μA |
| $I_{CC}$ | Supply current ($T_A$ = 25°C) | | No load, $\overline{SHDN}$ = $V_{CC}$ | | 0.5 | 2 | mA |
| | | Shutdown supply current | $\overline{SHDN}$ = GND | | 1 | 10 | μA |
| | | | $\overline{SHDN}$ = RIN = GND, DIN = GND or $V_{CC}$ | | 10 | 300 | nA |

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC}$ = 3 V to 5 V.
(2) All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.

## DRIVER SECTION ELECTRICAL CHARACTERISTICS(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(2) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | DOUT at $R_L$ = 3 kΩ to GND, | DIN = GND | 5 | 5.4 | | V |
| $V_{OL}$ | Low-level output voltage | DOUT at $R_L$ = 3 kΩ to GND, | DIN = $V_{CC}$ | –5 | –5.4 | | V |
| $I_{IH}$ | High-level input current | $V_I$ = $V_{CC}$ | | | ±0.01 | ±1 | μA |
| $I_{IL}$ | Low-level input current | $V_I$ at GND | | | ±0.01 | ±1 | μA |
| $I_{OS}$ | Short-circuit output current(3) | $V_{CC}$ = 3.6 V or 3.3 V, | $V_O$ = 0 V | | | ±60 | mA |
| $r_o$ | Output resistance | $V_{CC}$, $V_+$, and $V_–$ = 0 V, | $V_O$ = ±2 V | 300 | 50k | | Ω |

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC}$ = 3 V to 5 V.
(2) All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

## DRIVER SECTION SWITCHING CHARACTERISTICS(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP(2) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | Maximum data rate | $C_L$ = 1000 pF, MBAUD = GND | $R_L$ = 3 kΩ, 1 DIN switching, See Figure 1 | | 250 | | | kbit/s |
| | Maximum data rate | $C_L$ = 1000 pF, $V_{CC}$ = 4.5 V to 5.5 V, MBAUD = $V_{CC}$ | $R_L$ = 3 kΩ, 1 DIN switching, See Figure 1 | | 1000 | | | kbit/s |
| | Maximum data rate | $C_L$ = 250 pF, $V_{CC}$ = 3 V to 4.5 V, MBAUD = $V_{CC}$ | $R_L$ = 3 kΩ, 1 DIN switching, See Figure 1 | | 1000 | | | kbit/s |
| $t_{sk(p)}$ | Pulse skew(3) | $C_L$ = 150 pF to 2500 pF, $R_L$ = 3 kΩ to 7 kΩ, MBAUD = $V_{CC}$ or GND, See Figure 2 | | | | 100 | | ns |
| SR(tr) | Slew rate, transition region (see Figure 1) | $V_{CC}$ = 3.3 V, $R_L$ = 3 kΩ to 7 kΩ, $T_A$ = 25°C | $C_L$ = 150 pF to 1000 pF | MBAUD = GND | 6 | | 30 | V/μs |
| SR(tr) | Slew rate, transition region (see Figure 1) | $V_{CC}$ = 3.3 V, $R_L$ = 3 kΩ to 7 kΩ, $T_A$ = 25°C | $C_L$ = 150 pF to 1000 pF | MBAUD = $V_{CC}$ | 24 | | 150 | V/μs |
| SR(tr) | Slew rate, transition region (see Figure 1) | $V_{CC}$ = 3.3 V, $R_L$ = 3 kΩ to 7 kΩ, $T_A$ = 25°C | $C_L$ = 150 pF to 2500 pF, | MBAUD = GND | 4 | | 30 | V/μs |

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC}$ = 3 V to 5 V.
(2) All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

## RECEIVER SECTION ELECTRICAL CHARACTERISTICS[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | TEST CONDITIONS | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.6 | $V_{CC}$ – 0.1 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1 mA | | | 0.4 | V |
| $V_{IT+}$ | Positive-going input threshold voltage | $V_{CC}$ = 3.3 V | | 1.5 | 2.4 | V |
| | | $V_{CC}$ = 5 V | | 2 | 2.4 | |
| $V_{IT-}$ | Negative-going input threshold voltage | $V_{CC}$ = 3.3 V | 0.6 | 1.1 | | V |
| | | $V_{CC}$ = 5 V | 0.8 | 1.5 | | |
| $V_{hys}$ | Input hysteresis ($V_{IT+}$ – $V_{IT-}$) | | | 0.5 | | V |
| $I_{oz}$ | Output leakage current | $\overline{EN}$ = $V_{CC}$ | | ±0.05 | ±10 | μA |
| $r_i$ | Input resistance | $V_I$ = ±3 V to ±25 V | 3 | 5 | 7 | kΩ |

(1) Test conditions are C1–C4 = 0.1 mF at $V_{CC}$ = 3 V to.5 V.
(2) All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.

## RECEIVER SECTION SWITCHING CHARACTERISTICS[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

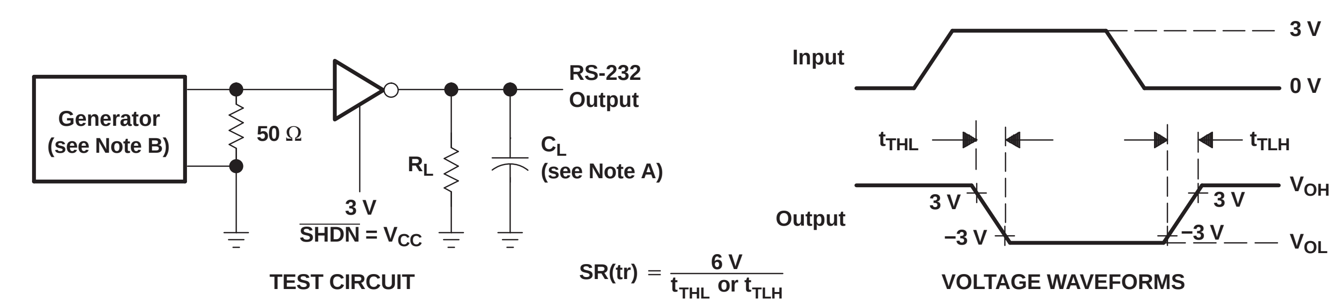
| PARAMETER | | TEST CONDITIONS | TYP[2] | UNIT |
|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $C_L$ = 150 pF, See Figure 3 | 150 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | $C_L$ = 150 pF, See Figure 3 | 150 | ns |
| $t_{en}$ | Output enable time | $C_L$ = 150 pF, $R_L$ = 3 kΩ, See Figure 4 | 2.6 | μs |
| $t_{dis}$ | Output disable time | $C_L$ = 150 pF, $R_L$ = 3 kΩ, See Figure 4 | 2.4 | μs |
| $t_{sk(p)}$ | Pulse skew[3] | See Figure 3 | 50 | ns |

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC}$ = 3 V to 5 V.
(2) All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

## ESD PROTECTION

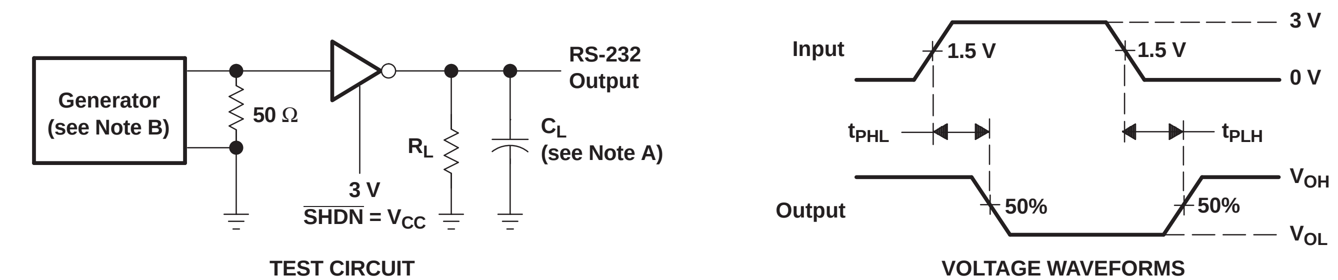
| PIN | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|
| DOUT, RIN | IEC61000-4-2, Contact Discharge | ±8 | kV |
| | IEC61000-4-2, Air-Gap Discharge | ±15 | |

## PARAMETER MEASUREMENT INFORMATION



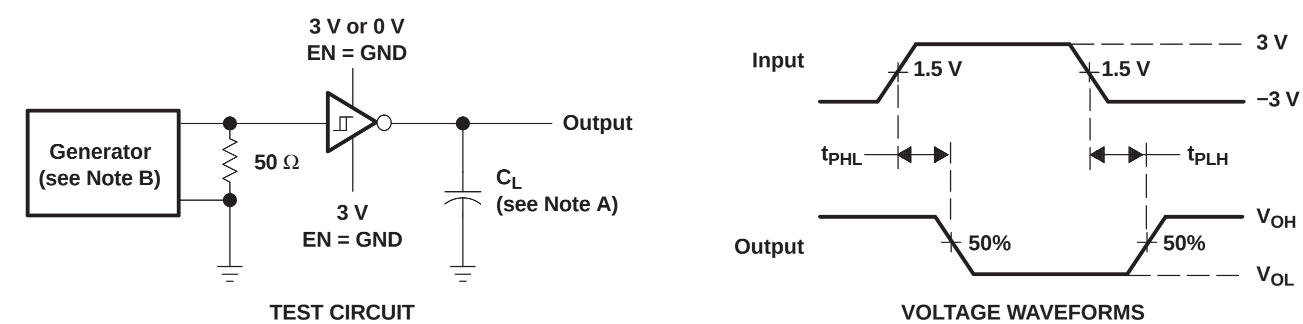

NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 1. Driver Slew Rate**




NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

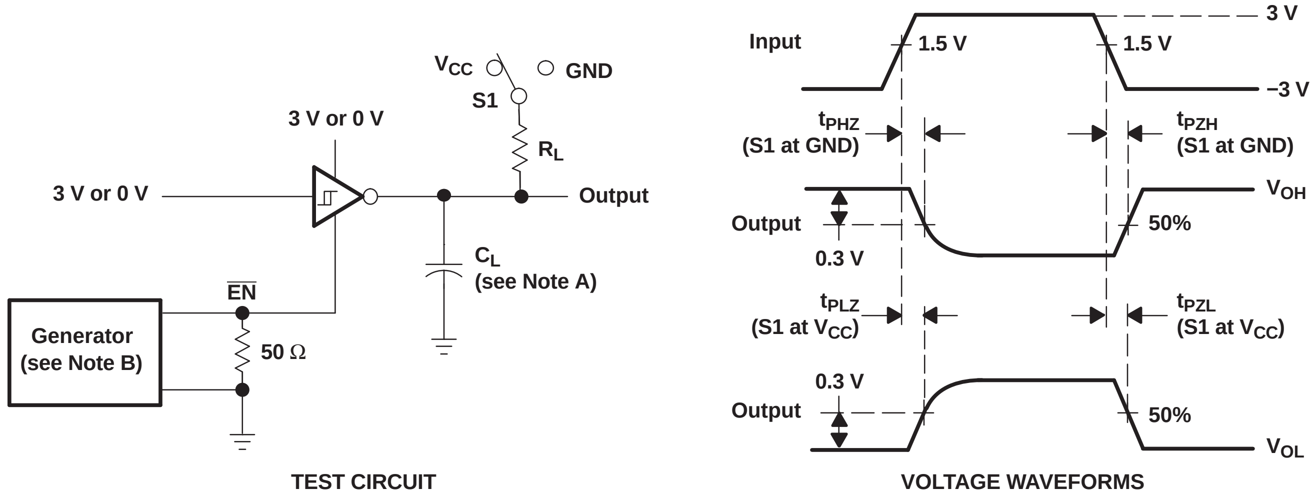
**Figure 2. Driver Pulse Skew**




NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

**Figure 3. Receiver Propagation Delay Times**

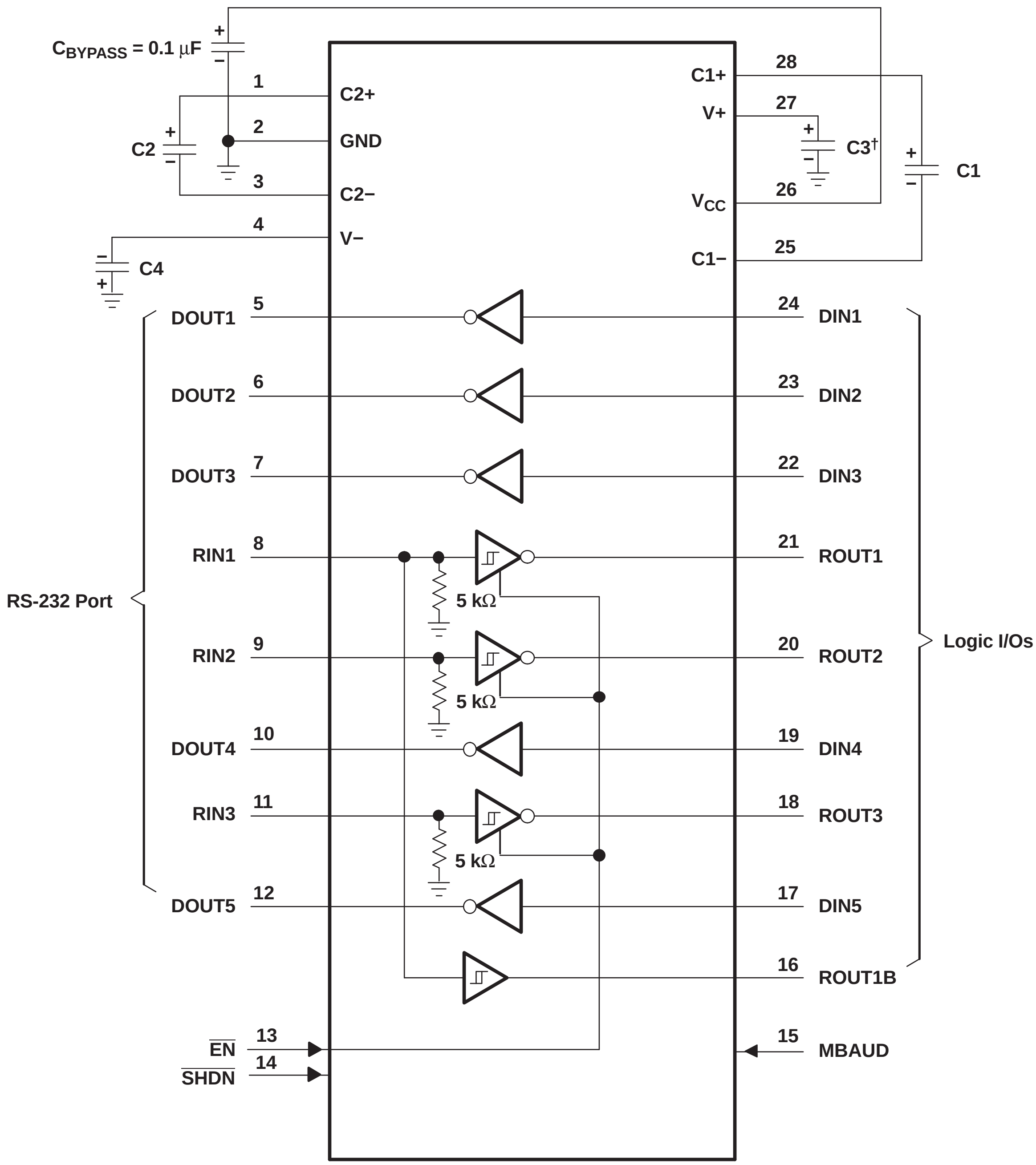
## PARAMETER MEASUREMENT INFORMATION (continued)




NOTES:
- A. $C_L$ includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
- C. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
- D. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

**Figure 4. Receiver Enable and Disable Times**

## APPLICATION INFORMATION




† C3 can be connected to $V_{CC}$ or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

**$V_{CC}$ vs CAPACITOR VALUES**

| $V_{CC}$ | C1 | C2, C3, and C4 |
|---|---|---|
| 3.3 V ± 0.15 V | 0.1 µF | 0.1 µF |
| 3.3 V ± 0.3 V | 0.22 µF | 0.22 µF |
| 5 V ± 0.5 V | 0.047 µF | 0.33 µF |
| 3 V to 5.5 V | 0.22 µF | 1 µF |

**Figure 5. Typical Operating Circuit and Capacitor Values**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TRS3237ECDB | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TRS3237EC | Samples |
| TRS3237ECDBR | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TRS3237EC | Samples |
| TRS3237ECDWR | ACTIVE | SOIC | DW | 28 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TRS3237EC | Samples |
| TRS3237ECPWR | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RS37EC | Samples |
| TRS3237EIDB | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TRS3237EI | Samples |
| TRS3237EIDBR | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TRS3237EI | Samples |
| TRS3237EIDWR | ACTIVE | SOIC | DW | 28 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TRS3237EI | Samples |
| TRS3237EIPWR | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | RS37EI | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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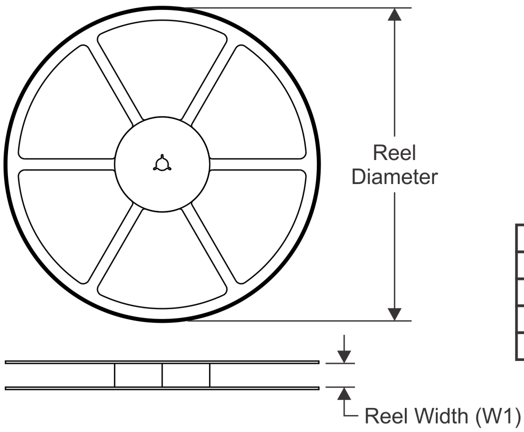
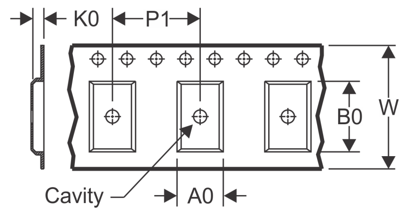
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

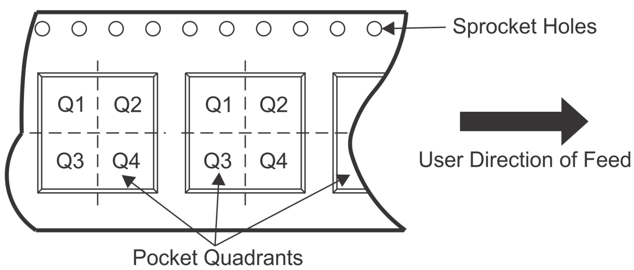



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

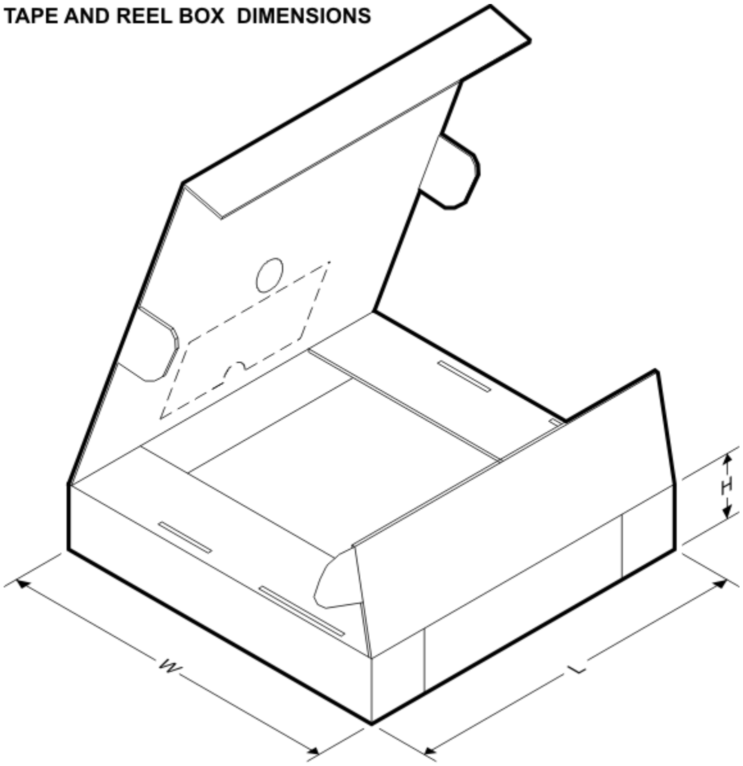
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRS3237ECDBR | SSOP | DB | 28 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TRS3237ECDWR | SOIC | DW | 28 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |
| TRS3237ECPWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TRS3237EIDBR | SSOP | DB | 28 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TRS3237EIDWR | SOIC | DW | 28 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |
| TRS3237EIPWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

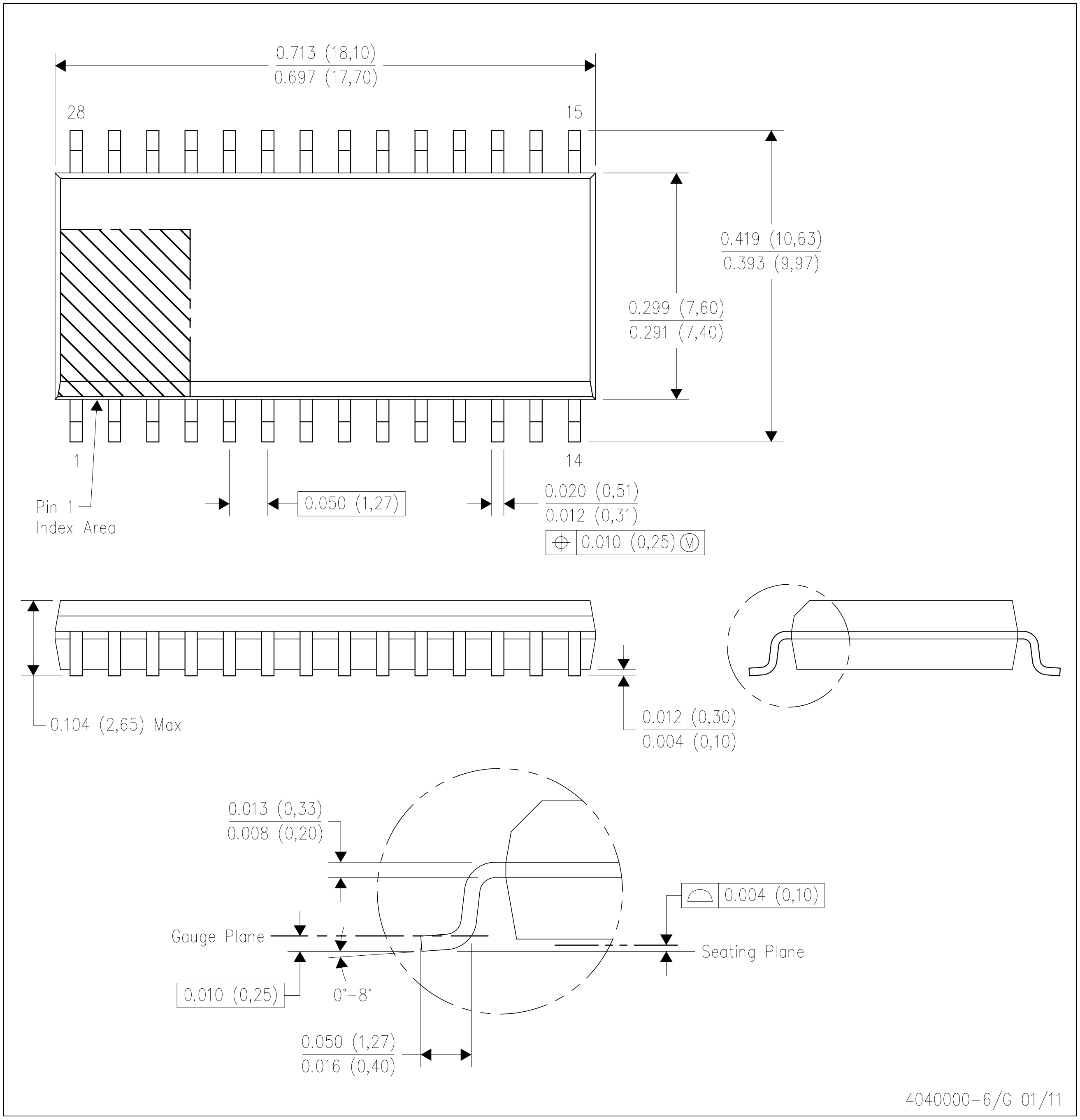
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

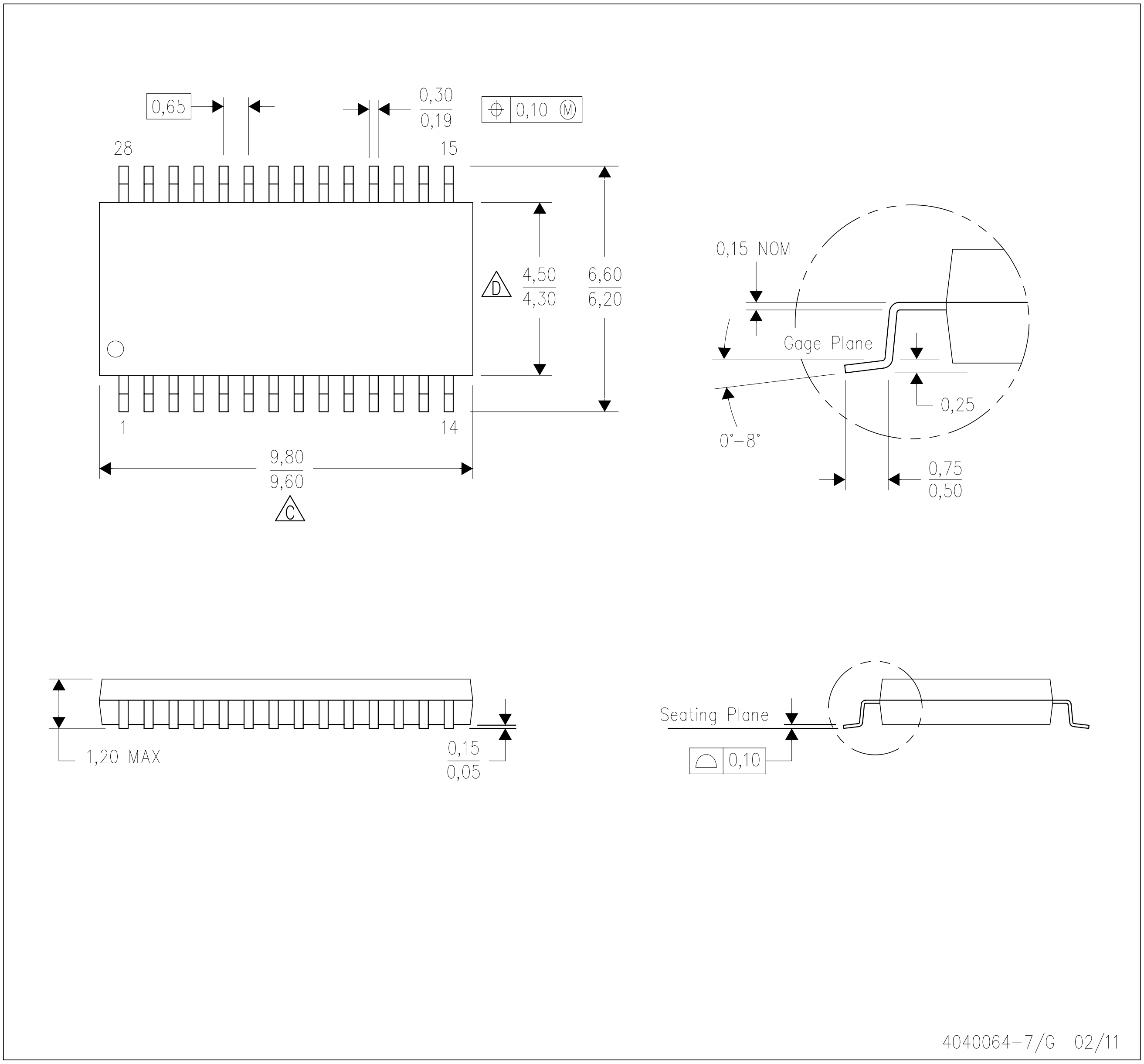
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TRS3237ECDBR | SSOP | DB | 28 | 2000 | 367.0 | 367.0 | 38.0 |
| TRS3237ECDWR | SOIC | DW | 28 | 1000 | 350.0 | 350.0 | 66.0 |
| TRS3237ECPWR | TSSOP | PW | 28 | 2000 | 367.0 | 367.0 | 38.0 |
| TRS3237EIDBR | SSOP | DB | 28 | 2000 | 367.0 | 367.0 | 38.0 |
| TRS3237EIDWR | SOIC | DW | 28 | 1000 | 350.0 | 350.0 | 66.0 |
| TRS3237EIPWR | TSSOP | PW | 28 | 2000 | 367.0 | 367.0 | 38.0 |

DW (R-PDSO-G28) PLASTIC SMALL OUTLINE



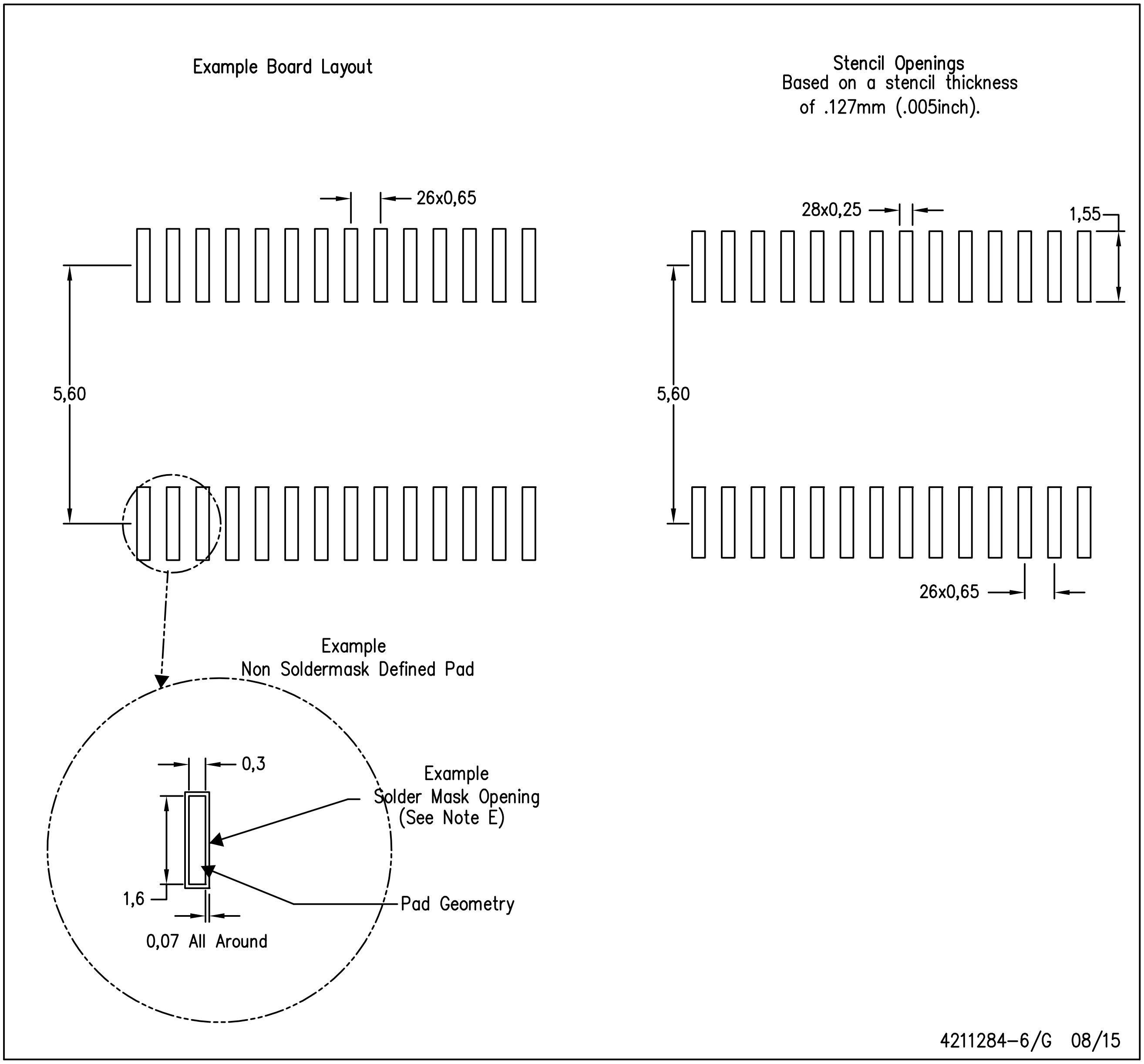

NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AE.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE

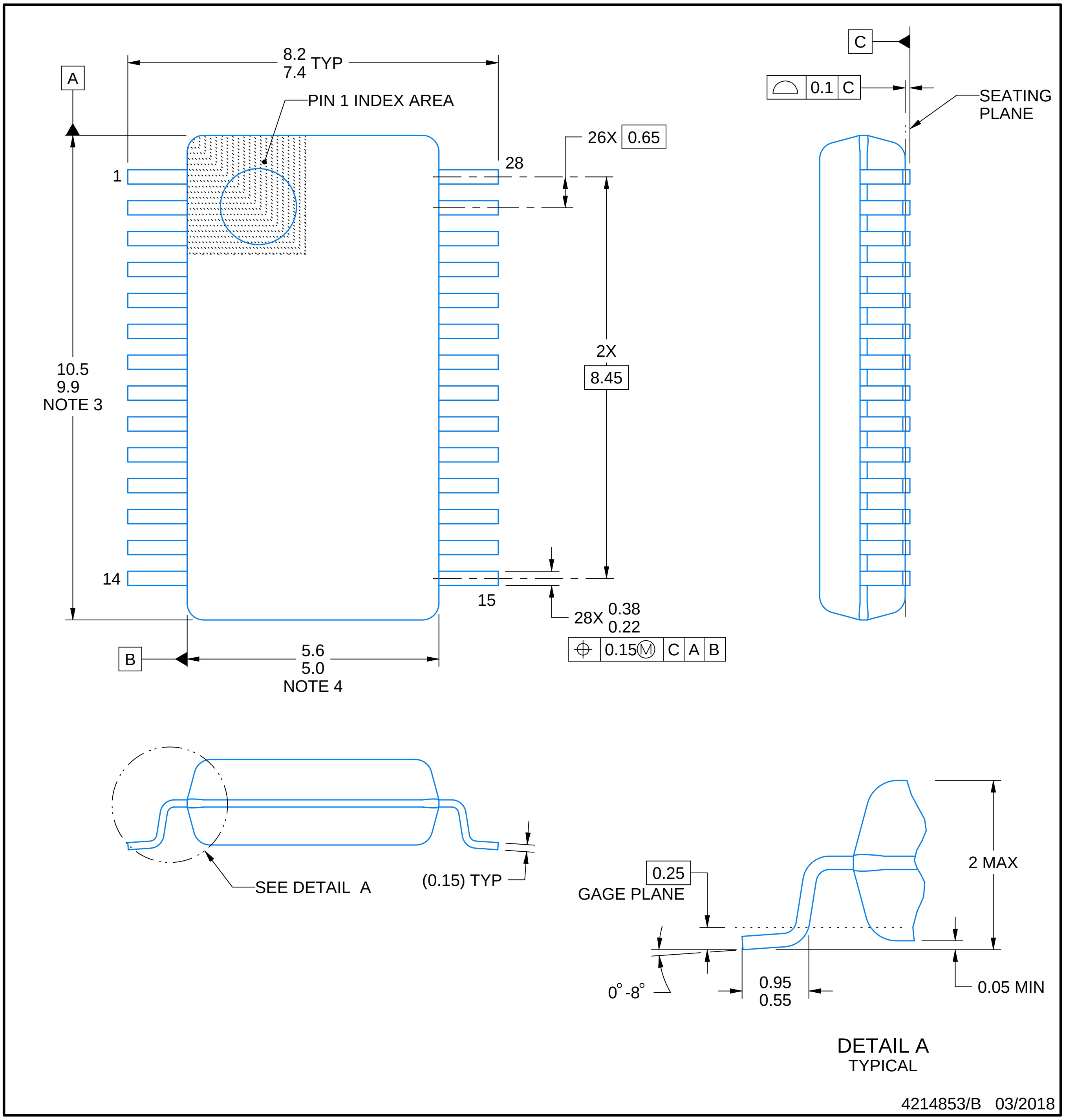



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# PACKAGE OUTLINE

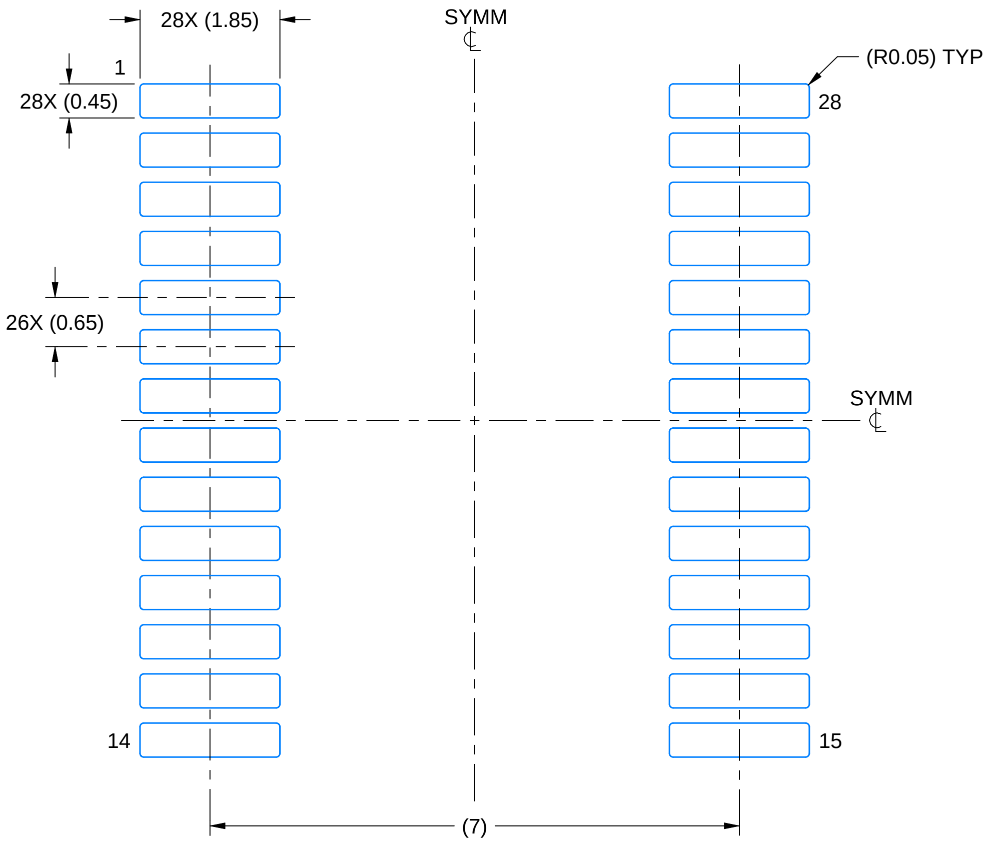
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

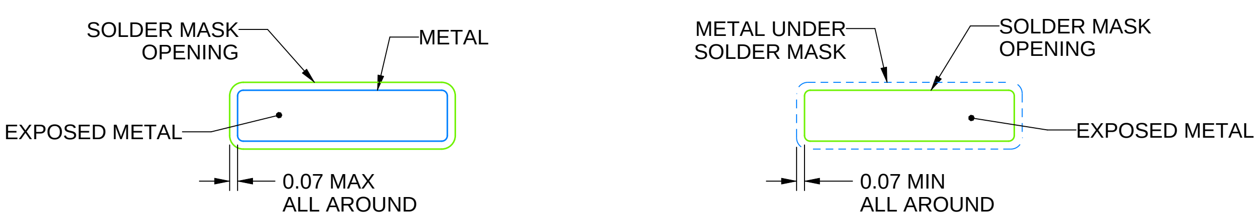



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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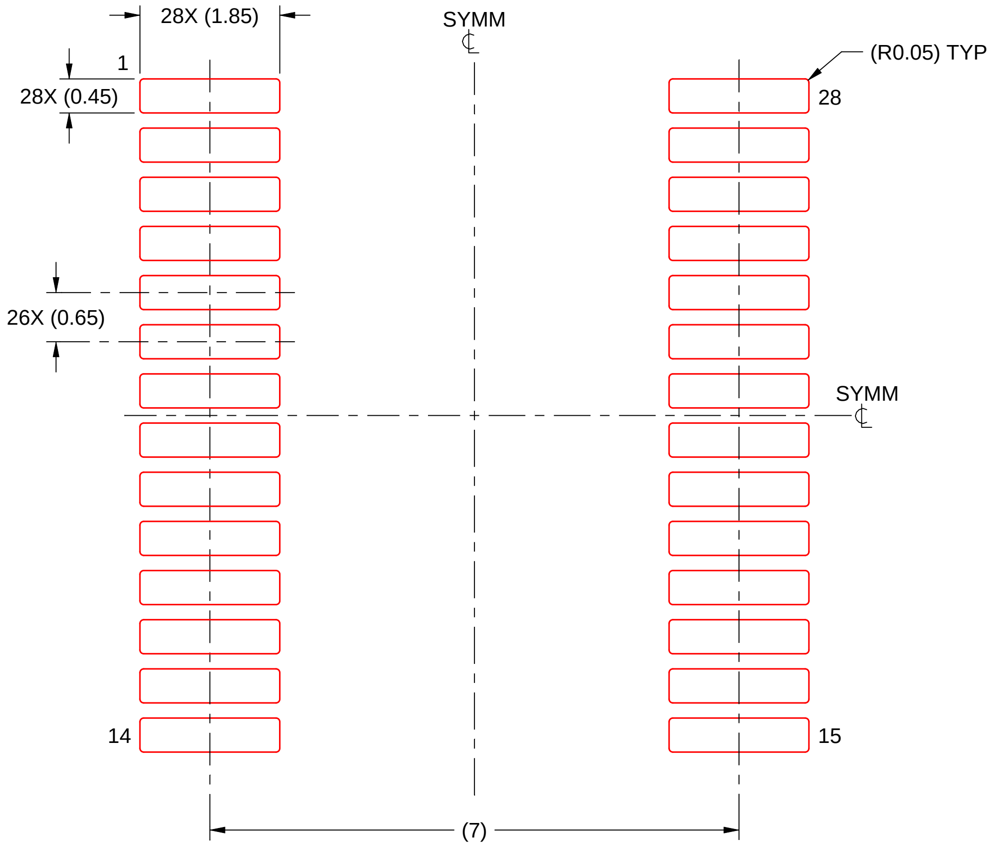
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.