19-0731; Rev 0; 1/07

EVALUATION KIT AVAILABLE

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

General Description

The MAX9742 stereo Class D audio power amplifier delivers up to 2 x 16W into 4Ω loads. The MAX9742 features high-power efficiency (92% with 8Ω loads), eliminating the need for a bulky heatsink and conserving power. The MAX9742 operates from a 20V to 40V single supply or a ±10V to ±20V dual supply. Features include fully differential inputs, comprehensive click-and-pop suppression, low-power shutdown mode, and an externally adjustable gain. Short-circuit and thermal-overload protection prevent the device from being damaged during a fault condition.

The MAX9742 is available in a thermally efficient 36-pin TQFN (6mm x 6mm x 0.8mm) package and is specified over the -40°C to +85°C extended temperature range.

Applications

CRT TVs

Flat-Panel Display TVs

Audio Docking Stations

Multimedia Monitors

Features

- **2 x 16W Output Power (R_L = 4Ω, THD+N = 10%)**
- **High Efficiency: Up to 92% with R_L = 8Ω**
- **Mute and Shutdown Modes**
- **Differential Inputs Suppress Common-Mode Noise**
- **Adjustable Gain**
- **Integrated Click-and-Pop Suppression**
- **Low 0.06% THD+N at 3.5W, R_L = 8Ω**
- **Output Short-Circuit and Thermal Protection**
- **Available in Space-Saving, 6mm x 6mm, 36-Pin TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9742ETX+	-40°C to +85°C	36 TQFN-EP*	T3666-3

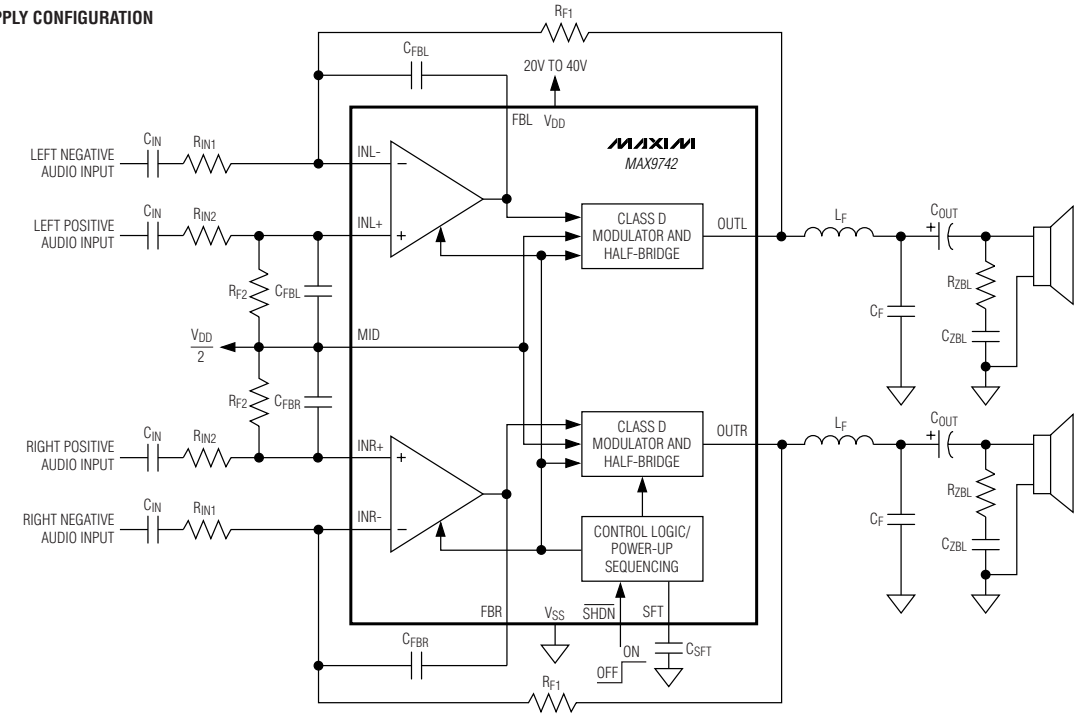
+Denotes lead-free package.

***EP = Exposed paddle.*

Pin Configuration located at end of data sheet.

Simplified Block Diagrams

SINGLE-SUPPLY CONFIGURATION



Simplified Block Diagrams continued at end of data sheet.

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to V_{SS}, NSENSE .....-0.3V to +45V
MID, LGND, LV_{DD}, REGM, REGP, OUTR, OUTL to V_{SS} .....-0.3V to +45V
MID, LGND, LV_{DD}, REGM, REGP, OUTR, OUTL to V_{DD}.....-45V to +0.3V
REGLS to V_{SS} .....-0.3V to +12V
MID to REGP, REGM.....(V_{REGM} - 0.3V) to (V_{REGP} + 0.3V)
REGP to REGM.....-0.3V to +12V
LV_{DD} to LGND.....-0.3V to +6V
$\overline{SHDN}$ to LGND.....-0.3V to +4V
SFT to LGND .....-0.3V to +6V
FB_, IN_+, IN_-, REFCUR to REGP, REGM.....(V_{REGM} - 0.3V) to (V_{REGP} + 0.3V)
BOOTR to OUTR .....-0.3V to +12V
BOOTL to OUTL .....-0.3V to +12V
OUTR, OUTL Shorted to LGND.....Continuous
Continuous Power Dissipation (T_A = +70°C) (Note 1)
Single-Layer Board:
36-Pin TQFN (derate 26.3mW/°C above +70°C) 2.11W
Multilayer Board:
36-Pin TQFN (derate 35.7mW/°C above +70°C) 2.86W
Junction-to-Ambient Thermal Resistance (θ_{JA})
Single-Layer Board:
36-Pin TQFN.....38°C/W
Multilayer Board:
36-Pin TQFN.....28°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....1.4°C/W
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Actual power capabilities are dependent on PCB layout. See the *Thermal Considerations* section.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single-Supply, Single-Ended Output

(V_{DD} = 24V, V_{SS} = V_{SUB} = LGND = 0V, $V_{\overline{SHDN}}$ = 3.3V, V_{MID} = 12V, C_{VDD} = 660µF, C_{MID1} = 10µF, C_{MID2} = 10µF, R1 = R2 = R3 = 10kΩ, C_{SFT} = 0.47µF, C_{OUT} = 1000µF, C_{FB_1} = 150pF, C_{FB_2} = 10pF, C_{BOOT} = 0.1µF, C_{REGP} = C_{REGM} = 1µF, $R_{IN\_}$ = 30.1kΩ, R_{F1A} = 121kΩ, R_{F1B} = 562kΩ, R_{F2} = 681kΩ, R_{REF} = 68kΩ, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	(Note 3)	20		40	V
Supply Current	I_{DD}	No load, output filter removed		15		mA
Mute Mode Supply Current		No load, V_{SFT} = 0V (outputs not switching)		8		mA
Shutdown Current		No load, $V_{\overline{SHDN}}$ = 0V		0.8	1.3	mA
Switching Frequency	f_{SW}			300		kHz
Power-Supply Rejection Ratio (Note 4)	PSRR	V_{DD} = 24V + 500mV_{P-P}, f = 1kHz		68		dB
Crosstalk (Notes 5 and 6)		L to R, R to L, R_L = 8Ω, P_{OUT} = 1W, f = 1kHz		-78		dB
Continuous Output Power (Notes 5, 6, and 7)	P_{OUT}	R_L = 8Ω, f_{IN} = 1kHz, THD+N = 10%		9.5		W
		R_L = 8Ω, f_{IN} = 1kHz, THD+N = 10%, V_{DD} = 35V		20.5		
		R_L = 4Ω, f_{IN} = 1kHz, THD+N = 10%		16		
Efficiency (Notes 5, 6, and 7)		R_L = 8Ω, P_{OUT} = 9.5W, THD+N = 10%		92		%

ELECTRICAL CHARACTERISTICS—Single-Supply, Single-Ended Output (continued)

(V_{DD} = 24V, V_{SS} = V_{SUB} = LGND = 0V, $V_{\overline{SHDN}}$ = 3.3V, V_{MID} = 12V, C_{VDD} = 660µF, C_{MID1} = 10µF, C_{MID2} = 10µF, R1 = R2 = R3 = 10kΩ, C_{SFT} = 0.47µF, C_{OUT} = 1000µF, C_{FB_1} = 150pF, C_{FB_2} = 10pF, C_{BOOT} = 0.1µF, C_{REGP} = C_{REGM} = 1µF, $R_{IN\_}$ = 30.1kΩ, R_{F1A} = 121kΩ, R_{F1B} = 562kΩ, R_{F2} = 681kΩ, R_{REF} = 68kΩ, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz, BW = 22Hz to 22kHz (Notes 5, 6, and 7)	R_L = 8Ω, P_{OUT} = 3.5W		0.06		%
			R_L = 4Ω, P_{OUT} = 5W		0.08		
Signal-to-Noise Ratio	SNR	P_{OUT} = 9.5W, R_L = 8Ω, BW = 22Hz to 22kHz (Notes 5 and 6)	Unweighted		88		dB
			A-weighted		93		
Half-Bridge Switch On-Resistance	$R_{DS(ON)}$				0.4	0.7	Ω
Switch Rise and Fall Times		No load (Note 4)			50		ns
IN_ Input Bias Current				-1		+1	µA
MID Input Bias Current	I_{MID}	V_{DD} = 24V, no load				50	µA
Shutdown-to-Full Operation	t_{SON}				68		ms
Power-On to Full Operation	t_{PU}	$V_{\overline{SHDN}}$ = 3.3V			1.5		s
Thermal-Overload Threshold Temperature	T_{SH}	Junction temperature			150		°C
Short-Circuit Output Current	I_{SC}	OUT_ shorted to V_{DD} or V_{SS}		2.9	4.5		A
Click-and-Pop	K_{CP}	Peak voltage, 32-samples per second, A-weighted (Notes 4 and 8)	Into shutdown		-38		dBV
			Out of shutdown		-40		
DIGITAL INPUTS ($\overline{SHDN}$) (Note 9)							
Logic-Input Low Voltage	V_{IL}					0.4	V
Logic-Input High Voltage	V_{IH}			2.4			V
Input Leakage Current				-1		+1	µA

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V_{DD} = 15V, V_{SS} = V_{SUB} = -15V, $V_{\overline{SHDN}}$ = 3.3V, V_{MID} = LGND = 0V, C_{VDD} = C_{VSS} = 1000µF, C_{BYP} = 1µF, C_{SFT} = 0.22µF, C_{FB_1} = 150pF, C_{FB_2} = 10pF, C_{BOOT} = 0.1µF, C_{REGP} = C_{REGM} = 1µF, $R_{IN\_}$ = 30.1kΩ, R_{F1A} = 121kΩ, R_{F1B} = 562kΩ, R_{F2} = 681kΩ, R_{REF} = 68kΩ, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Voltage Range	V_{DD}	(Note 3)	10		20	V
Negative Supply Voltage Range	V_{SS}	(Note 3)	-20		-10	V
Positive Supply Mute Mode Current		No load, V_{SFT} = 0V (outputs not switching)		8	11	mA
Negative Supply Mute Mode Current		No load, V_{SFT} = 0V (outputs not switching)	-12	-8		mA

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V_{DD} = 15V, V_{SS} = V_{SUB} = -15V, $V_{\overline{SHDN}}$ = 3.3V, V_{MID} = LGND = 0V, C_{VDD} = C_{VSS} = 1000µF, C_{BYP} = 1µF, C_{SFT} = 0.22µF, C_{FB_1} = 150pF, C_{FB_2} = 10pF, C_{BOOT} = 0.1µF, C_{REGP} = C_{REGM} = 1µF, $R_{IN\_}$ = 30.1kΩ, R_{F1A} = 121kΩ, R_{F1B} = 562kΩ, R_{F2} = 681kΩ, R_{REF} = 68kΩ, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Positive Supply Current	I_{DD}	No load, output filter removed			23	36	mA
Negative Supply Current	I_{SS}	No load, output filter removed		-36	-23		mA
Positive Supply Shutdown Current		No load, $V_{\overline{SHDN}}$ = 0V			0.001	1	µA
Negative Supply Shutdown Current		No load, $V_{\overline{SHDN}}$ = 0V		-1	-0.03		µA
Output Offset Voltage		Output referred, affected by $R_{IN\_}$ and $R_{F\_}$ tolerances (Note 4)			5	30	mV
IN_ Input Bias Current				-1		+1	µA
Power-Supply Rejection Ratio (Note 4)	PSRR	V_{DD} = 10V to 20V			97		dB
		V_{SS} = -10V to -20V			100		
		V_{DD} = 15V + 500mV_{P-P}, f = 1kHz			67		
		V_{SS} = -15V + 500mV_{P-P}, f = 1kHz			64		
Crosstalk (Notes 5 and 6)		L to R, R to L, R_L = 8Ω, P_{OUT} = 1W, f = 1kHz			-61		dB
Continuous Output Power	P_{OUT}	f_{IN} = 1kHz, THD+N = 10% (Notes 5, 6, and 7)	R_L = 8Ω		14		W
			R_L = 8Ω, V_{DD} = 18V, V_{SS} = -18V		21		
			R_L = 4Ω, V_{DD} = 12V, V_{SS} = -12V		9.5		
Efficiency (Notes 5, 6, and 7)		R_L = 8Ω, P_{OUT} = 15W, THD+N = 10%			93		%
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz, BW = 22Hz to 22kHz (Notes 5, 6, and 7)	R_L = 8Ω, P_{OUT} = 5W		0.06		%
			R_L = 4Ω, P_{OUT} = 10W		0.08		
Signal-to-Noise Ratio	SNR	P_{OUT} = 14W, R_L = 8Ω, BW = 22Hz to 22kHz (Notes 5 and 6)	Unweighted		89		dB
			A-weighted		94		
Shutdown-to-Full Operation	t_{SON}				68		ms
Short-Circuit Output Current	I_{SC}	OUT_ shorted to V_{DD} or V_{SS}		2.9	4.5		A
Click-and-Pop	K_{CP}	Peak voltage, 32-samples per second, A-weighted (Notes 4 and 8)	Into shutdown		-36		dBV
			Out of shutdown		-36		

ELECTRICAL CHARACTERISTICS—Single-Supply, BTL Configuration

(V_{DD} = 24V, V_{SS} = V_{SUB} = LGND = 0V, $V_{\overline{SHDN}}$ = 3.3V, V_{MID} = 12V, C_{VDD} = 660µF, C_{MID1} = 10µF, C_{MID2} = 10µF, R1 = R2 = R3 = 10kΩ, C_{SFT} = 0.47µF, C_{OUT} = 1000µF, C_{FB_1} = 150pF, C_{FB_2} = 10pF, C_{BOOT} = 0.1µF, C_{REGP} = C_{REGM} = 1µF, $R_{IN\_}$ = 30.1kΩ, R_{F1A} = 121kΩ, R_{F1B} = 562kΩ, R_{F2} = 681kΩ, R_{REF} = 68kΩ, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Offset Voltage		(Note 4)			7		mV
Power-Supply Rejection Ratio (Note 4)	PSRR	V_{DD} = 20V to 40V			88		dB
		V_{DD} = 24V + 500mV_{P-P}, f = 1kHz			77		
Continuous Output Power	P_{OUT}	R_L = 8Ω, f_{IN} = 1kHz, THD+N = 10%, (Notes 6, 10, and 11)			32		W
Efficiency		R_L = 8Ω, P_{OUT} = 10W, THD+N = 10%, (Notes 5 and 6)			83		%
Total Harmonic Distortion Plus Noise (Notes 6, 10, and 11)	THD+N	f_{IN} = 1kHz, BW = 22Hz to 22kHz, R_L = 8Ω, P_{OUT} = 10W			0.08		%
Signal-to-Noise Ratio	SNR	P_{OUT} = 32W, R_L = 8Ω, BW = 22Hz to 22kHz (Notes 6, 10, and 11)	Unweighted		90		dB
			A-weighted		96		
Shutdown-to-Full Operation	t_{SON}				68		ms
Click-and-Pop	K_{CP}	Peak voltage, 32-samples per second, A-weighted (Notes 4, 11, and 12)	Into shutdown		-47		dBV
			Out of shutdown		-32		

Note 2: All devices are 100% production tested at +25°C. All temperature limits are guaranteed by design.

Note 3: Supply pumping may occur at high output powers with low audio frequencies. Use proper supply bypassing to prevent the device from entering overvoltage protection due to supply pumping. See the *Supply Pumping Effects* and the *Supply Undervoltage and Overvoltage Protection* sections.

Note 4: Amplifier inputs AC-coupled to ground.

Note 5: For R_L = 4Ω, L_F = 22µH and C_F = 0.68µF. For R_L = 6Ω, L_F = 33µH and C_F = 0.47µF. For R_L = 8Ω, L_F = 47µH and C_F = 0.33µF.

Note 6: Testing performed with four-layer PCB.

Note 7: Both channels driven in phase.

Note 8: Testing performed with an 8Ω resistor connected between LC filter output and ground. Mode transitions are controlled by $\overline{SHDN}$. K_{CP} level is calculated as 20log[(peak voltage during mode transition, no input signal) / $1V_{RMS}$].

Note 9: Digital input specifications apply to both single-supply and dual-supply operation.

Note 10: Channels driven 180° out-of-phase. Load connected between LC filter outputs.

Note 11: L_F = 22µH and C_F = 0.68µF.

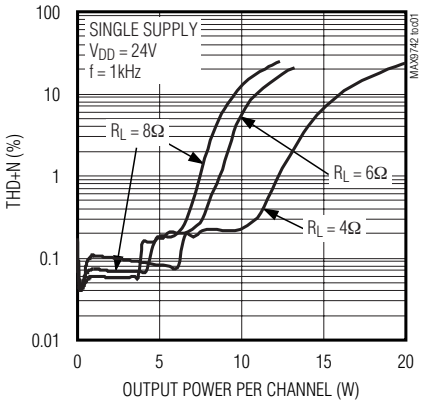
Note 12: Testing performed with an 8Ω resistor connected between LC filter outputs. Mode transitions are controlled by $\overline{SHDN}$. K_{CP} level is calculated as 20log[(peak voltage during mode transition, no input signal) / $1V_{RMS}$].

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

Typical Operating Characteristics

(24V single-supply mode, ±15V dual-supply mode, both channels driven in phase, THD+N measurement bandwidth = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted. See Figure 1 for test circuits, see *Typical Application Circuits/Functional Diagrams* for test circuit component values.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



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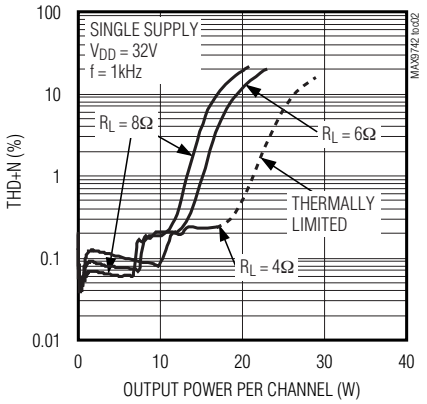

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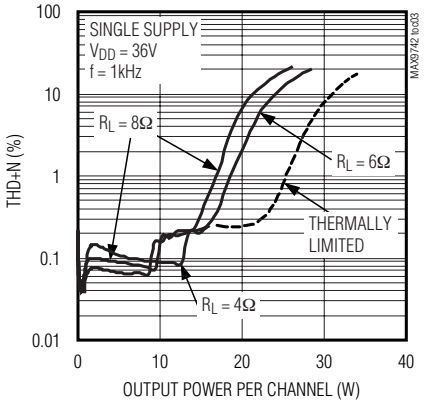

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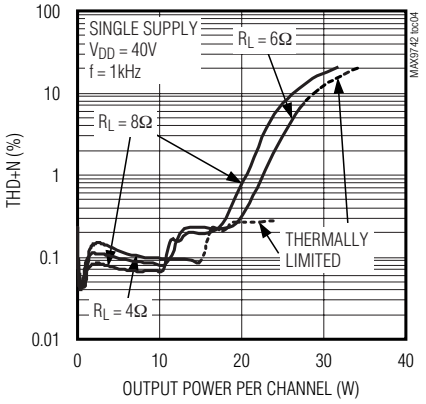

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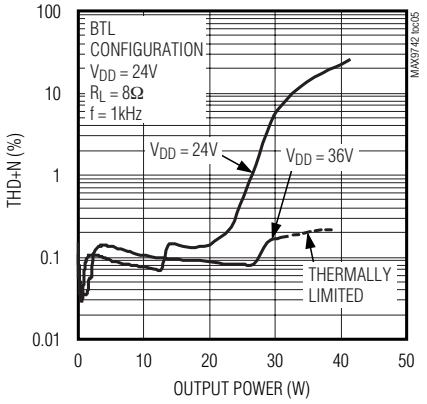

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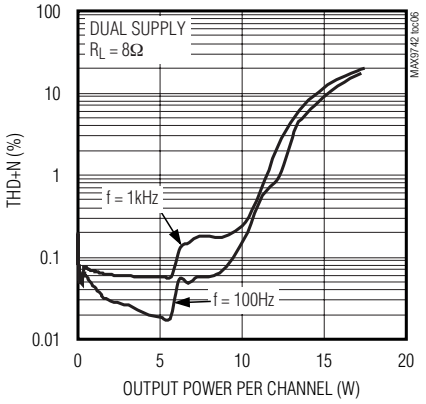

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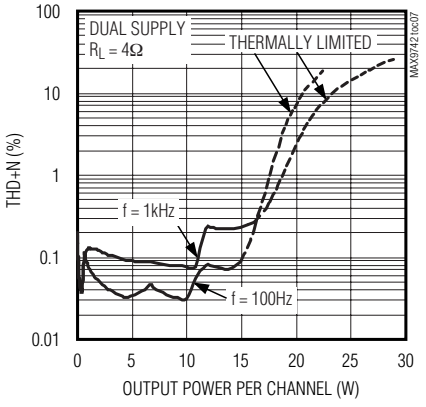

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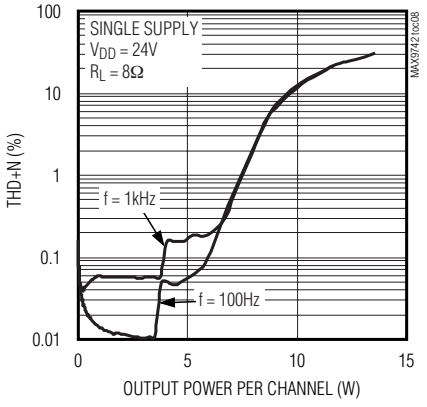

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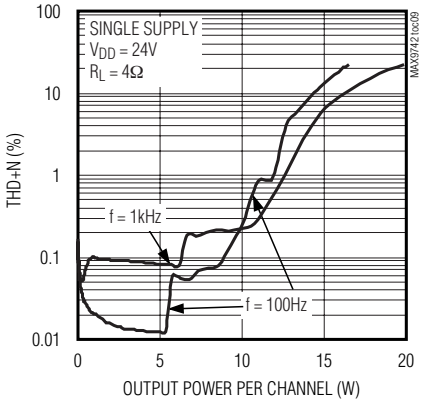
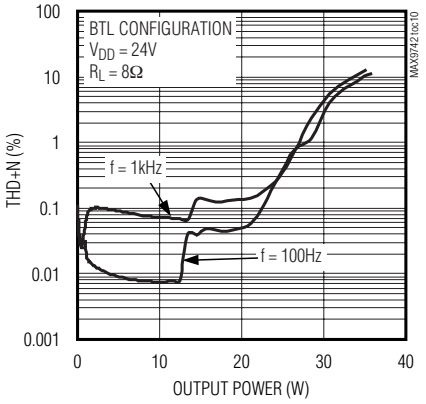


Typical Operating Characteristics (continued)

(24V single-supply mode, ±15V dual-supply mode, both channels driven in phase, THD+N measurement bandwidth = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted. See Figure 1 for test circuits, see *Typical Application Circuits/Functional Diagrams* for test circuit component values.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



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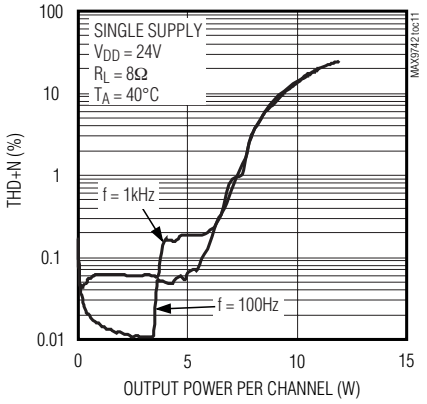

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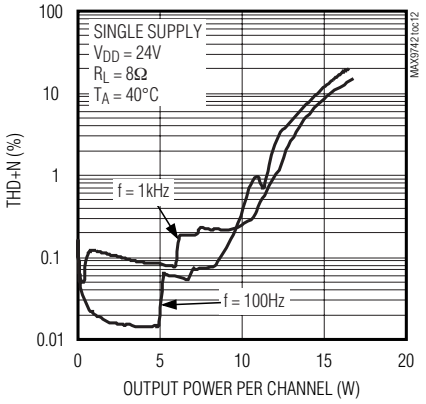

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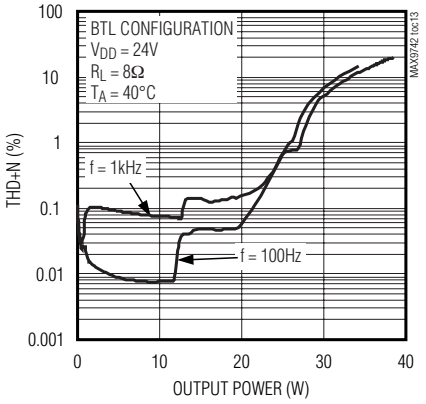
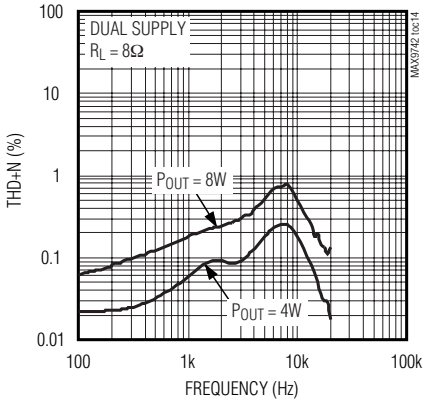


TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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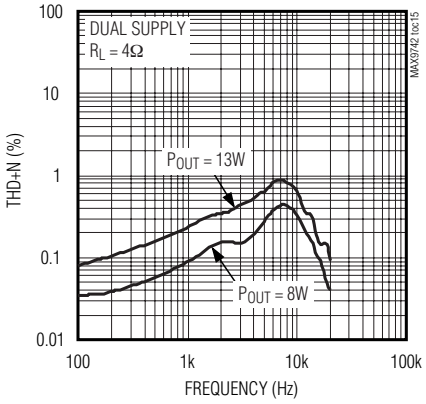

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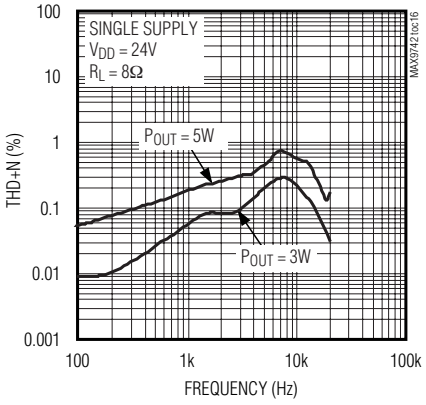
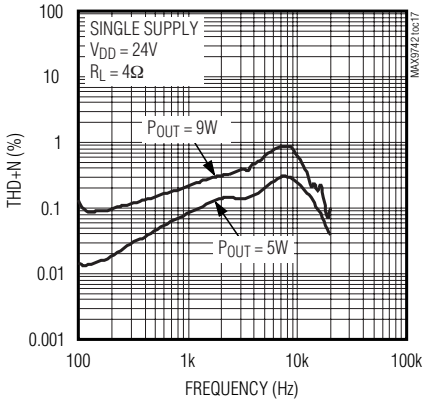
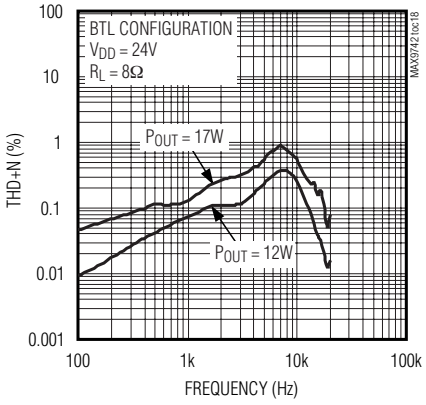


TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY

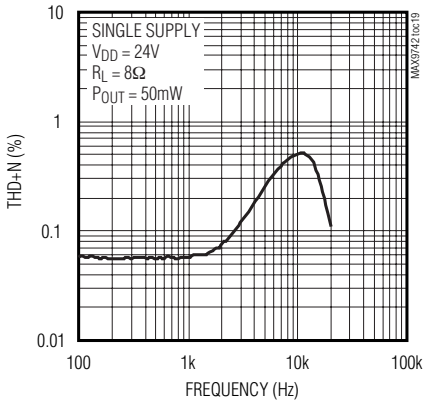


Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

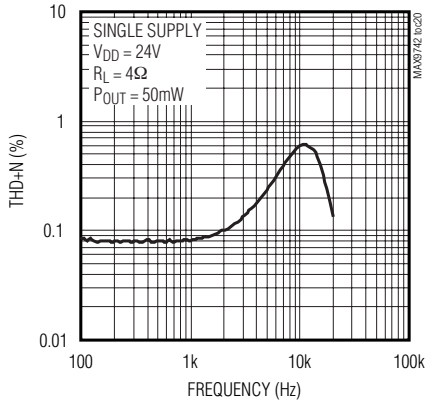
Typical Operating Characteristics (continued)

(24V single-supply mode, ±15V dual-supply mode, both channels driven in phase, THD+N measurement bandwidth = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted. See Figure 1 for test circuits, see *Typical Application Circuits/Functional Diagrams* for test circuit component values.)

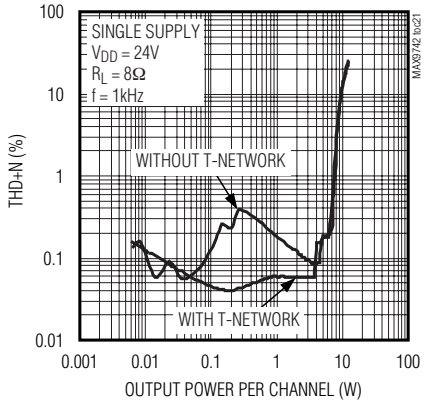
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



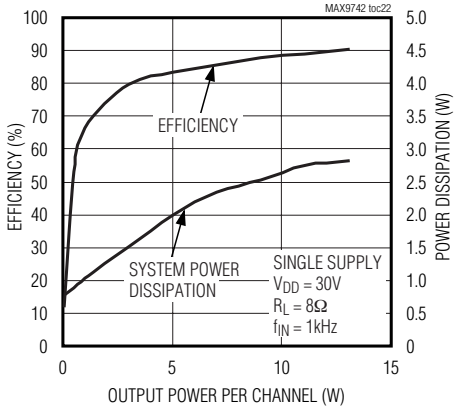
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



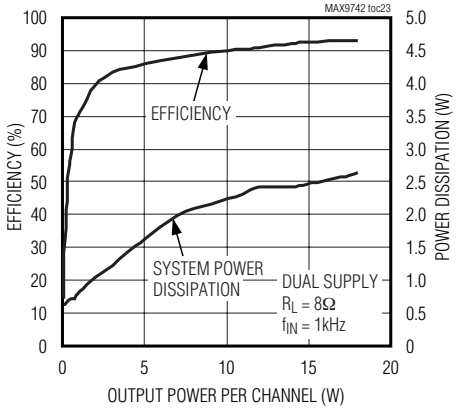
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER WITH AND WITHOUT T-NETWORK



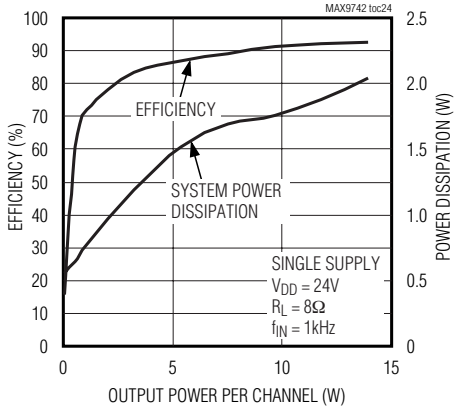
EFFICIENCY AND POWER DISSIPATION vs. OUTPUT POWER



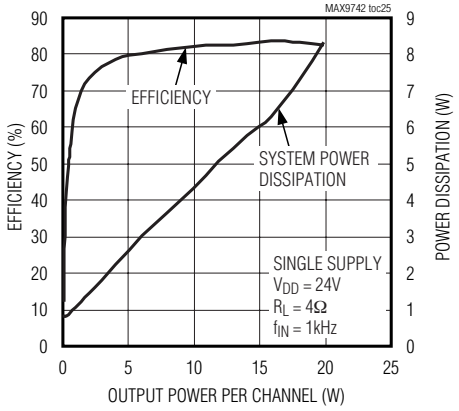
EFFICIENCY AND POWER DISSIPATION vs. OUTPUT POWER



EFFICIENCY AND POWER DISSIPATION vs. OUTPUT POWER



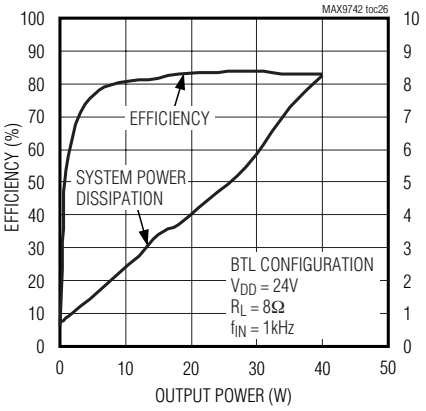
EFFICIENCY AND POWER DISSIPATION vs. OUTPUT POWER



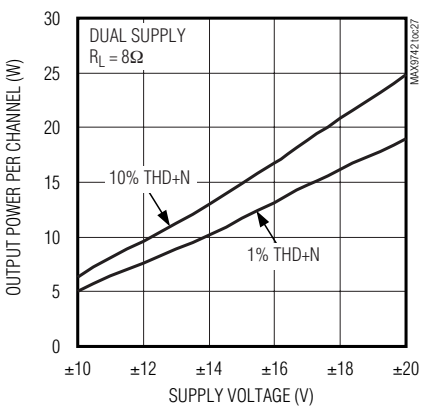
Typical Operating Characteristics (continued)

(24V single-supply mode, ±15V dual-supply mode, both channels driven in phase, THD+N measurement bandwidth = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted. See Figure 1 for test circuits, see *Typical Application Circuits/Functional Diagrams* for test circuit component values.)

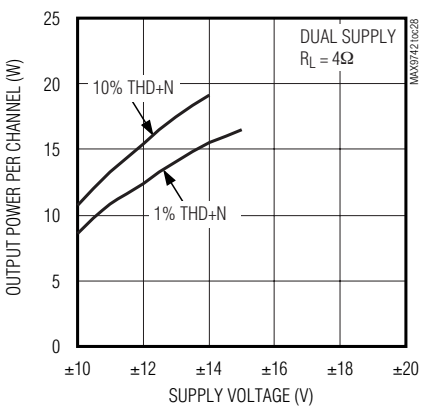
EFFICIENCY AND POWER DISSIPATION vs. OUTPUT POWER



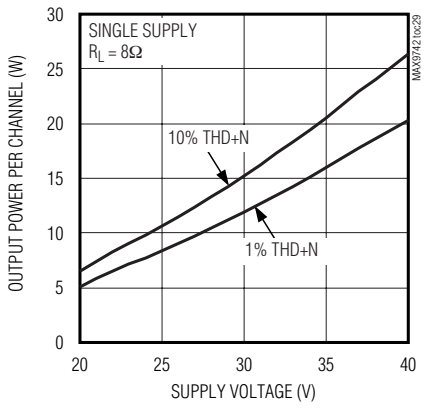
OUTPUT POWER vs. SUPPLY VOLTAGE



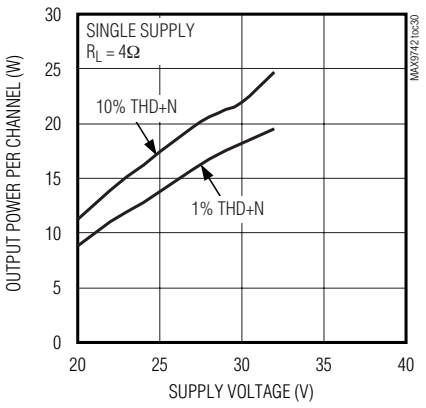
OUTPUT POWER vs. SUPPLY VOLTAGE



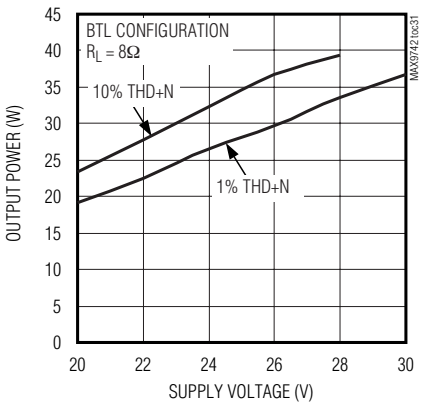
OUTPUT POWER vs. SUPPLY VOLTAGE



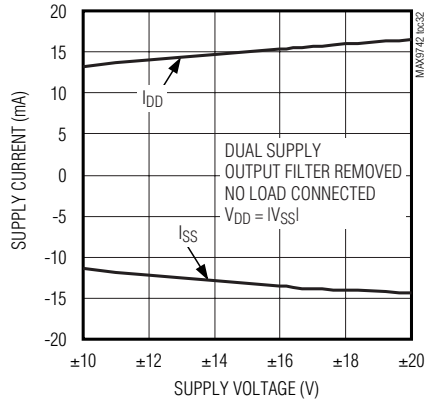
OUTPUT POWER vs. SUPPLY VOLTAGE



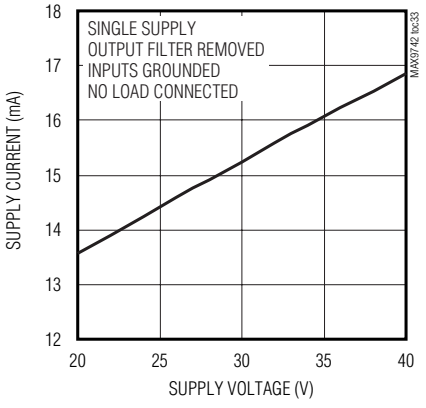
OUTPUT POWER vs. SUPPLY VOLTAGE



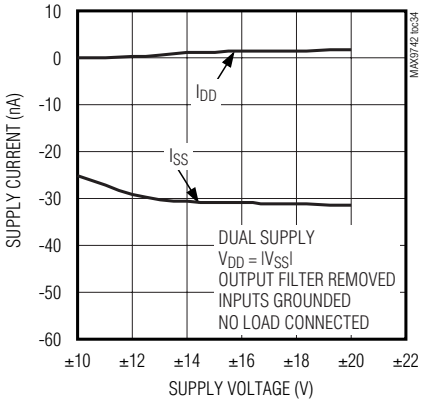
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE

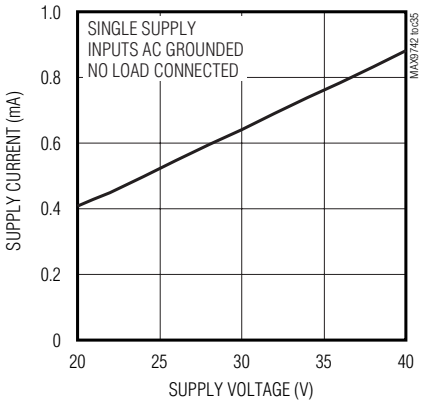


Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

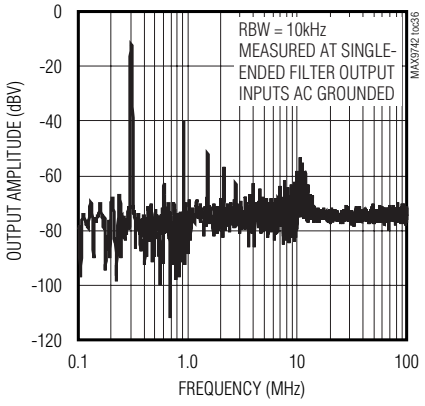
Typical Operating Characteristics (continued)

(24V single-supply mode, ±15V dual-supply mode, both channels driven in phase, THD+N measurement bandwidth = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted. See Figure 1 for test circuits, see *Typical Application Circuits/Functional Diagrams* for test circuit component values.)

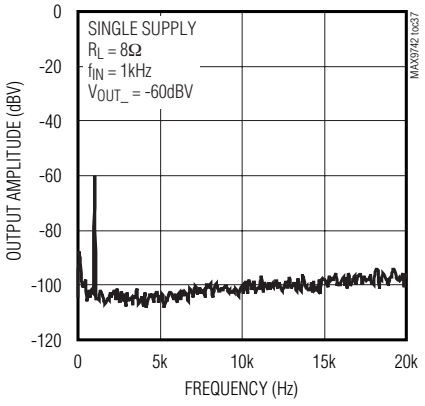
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



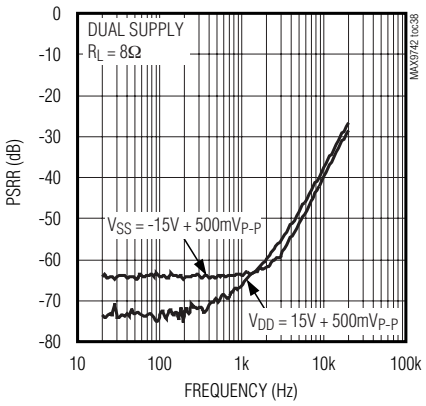
WIDEBAND OUTPUT SPECTRUM



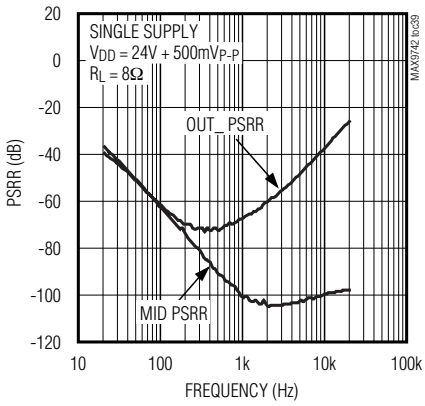
OUTPUT SPECTRUM FFT



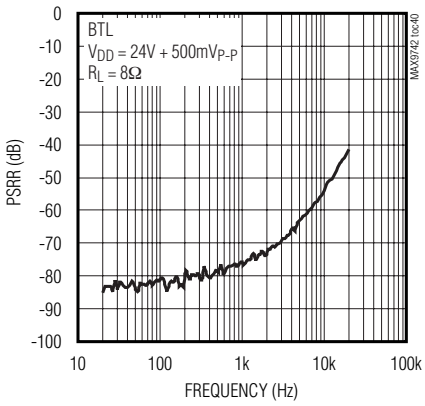
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



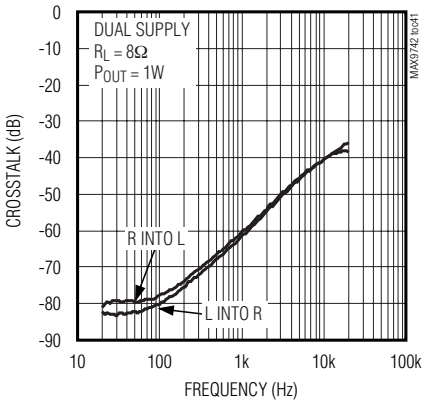
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



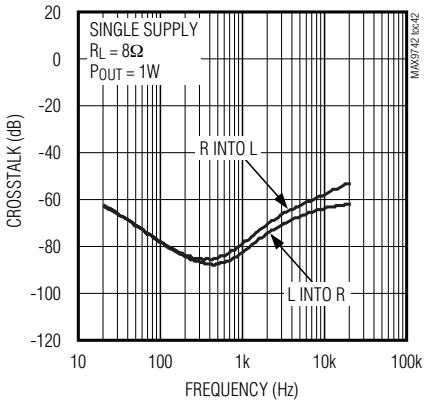
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



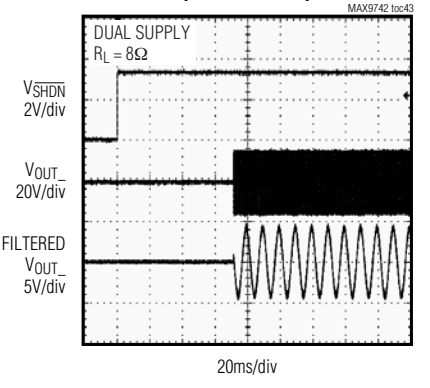
CROSSTALK vs. FREQUENCY



CROSSTALK vs. FREQUENCY



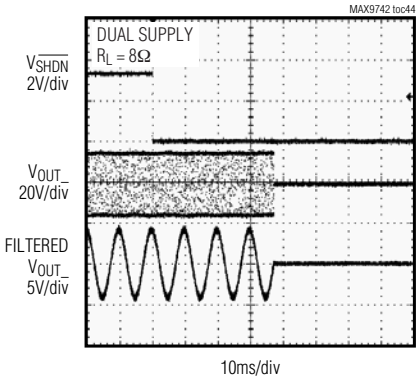
EXITING SHUTDOWN (DUAL SUPPLY)



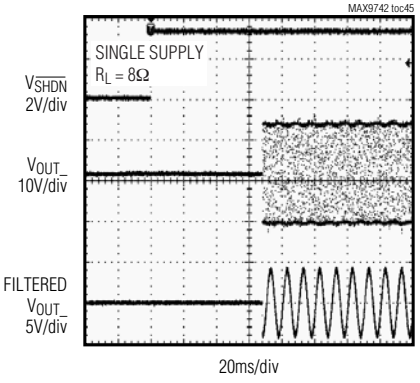
Typical Operating Characteristics (continued)

(24V single-supply mode, ±15V dual-supply mode, both channels driven in phase, THD+N measurement bandwidth = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted. See Figure 1 for test circuits, see *Typical Application Circuits/Functional Diagrams* for test circuit component values.)

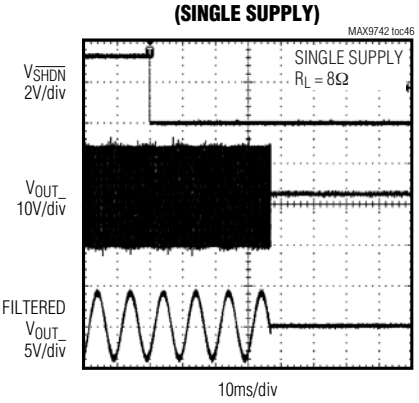
ENTERING SHUTDOWN



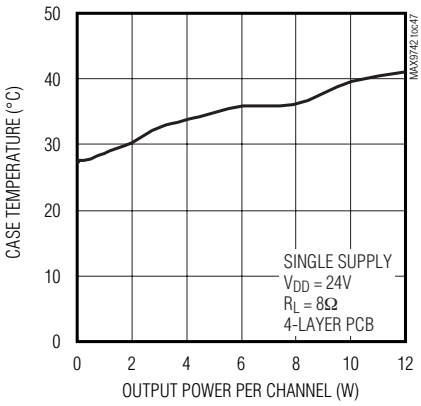
EXITING SHUTDOWN



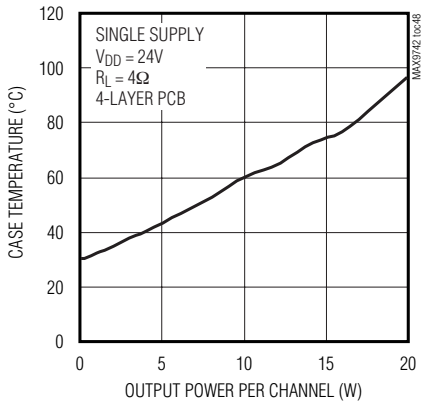
ENTERING SHUTDOWN (SINGLE SUPPLY)



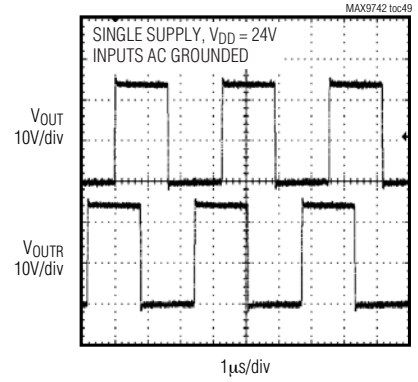
CASE TEMPERATURE vs. OUTPUT POWER



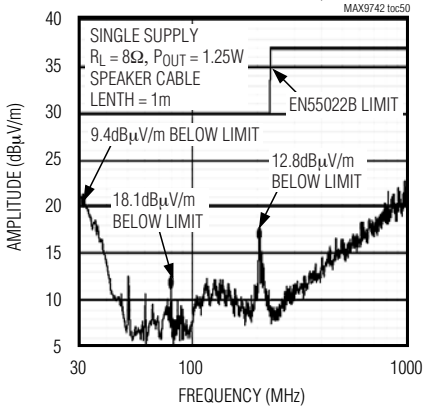
CASE TEMPERATURE vs. OUTPUT POWER



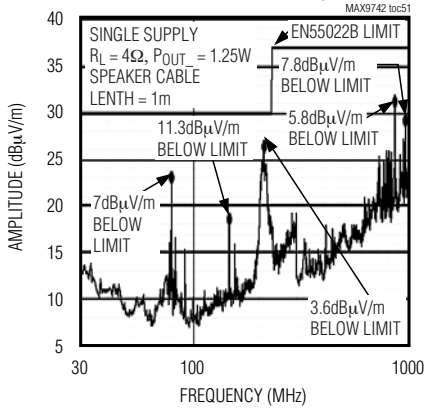
OUTPUT WAVEFORM



EMI AMPLITUDE vs. FREQUENCY



EMI AMPLITUDE vs. FREQUENCY



Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

Pin Description

PIN	NAME	FUNCTION
1, 6, 18, 27, 28, 36	N.C.	No Connection. Not internally connected.
2, 3	OUTL	Left Speaker Output
4	SUB	Device Substrate. Connect SUB to V_{SS}.
5	BOOTL	Left-Channel Bootstrap Capacitor Terminal. Connect a 0.1µF capacitor between BOOTL and OUTL.
7	INL+	Left-Channel Positive Input
8	INL-	Left-Channel Negative Input. Connect an external feedback capacitor between INL- and FBL. See the *Feedback Capacitor ($C_{FB\_}$)* section.
9	FBL	Left-Channel Feedback Capacitor Terminal. Connect an external feedback capacitor between FBL and INL-. See the *Feedback Capacitor ($C_{FB\_}$)* section.
10	REGM	-5V Internal Regulator Output. Regulator output voltage is with respect to MID. Bypass REGM with a 1µF capacitor to signal ground plane (SGND). See the *Supply Bypassing/Layout* section.
11	MID	Midsupply Bias Voltage Input. The MID input biases the internal preamplifiers to the average value of the V_{DD} and V_{SS} supply inputs. For dual-supply operation, connect to the signal ground plane (SGND). For single-supply operation, apply a voltage to MID equal to 0.5 x V_{DD} through an external resistive voltage-divider and decoupling network (see the *Setting V_{MID}* section). See the *Typical Application Circuits/Functional Diagrams* and *Supply Bypassing/Layout* sections.
12	REGP	5V Internal Regulator Output. Regulator output voltage is with respect to MID. Bypass REGP with a 1µF capacitor to the signal ground plane (SGND). See the *Supply Bypassing/Layout* section.
13	REFCUR	Reference Current Resistor Terminal. Connect an external resistor from REFCUR to REGP to set the switching frequency and output short-circuit current-limit value. Use resistor values greater than or equal to 58kΩ and less than or equal to 75kΩ. See the *Setting the Switching Frequency and Output Current Limit (R_{REF})* section.
14	SFT	Soft-Start Capacitor Terminal/Mute Input. Connect a 0.22µF capacitor between SFT and PGND to utilize the soft-start power-up sequence. Drive SFT low to mute the outputs.
15	LGND	Logic Ground. Connect LGND to signal ground (SGND) and power ground (PGND) planes. See the *Supply Bypassing/Layout* section.
16	LV_{DD}	Internal 5V Logic Supply. Bypass LV_{DD} to LGND with a 0.1µF capacitor.
17	$\overline{SHDN}$	Active-Low Shutdown Input. Drive $\overline{SHDN}$ high for normal operation. Drive $\overline{SHDN}$ low to place the device into shutdown mode.
19	FBR	Right-Channel Feedback Capacitor Terminal. Connect an external feedback capacitor between FBR and INR-. See the *Feedback Capacitor ($C_{FB\_}$)* section.
20	INR-	Right-Channel Negative Input. Connect an external feedback capacitor between INR- and FBR. See the *Feedback Capacitor ($C_{FB\_}$)* section.
21	INR+	Right-Channel Positive Input
22	NSENSE	Negative Supply Sense Input. NSENSE is internally connected to V_{SS}. Connect a 1µF bypass capacitor between NSENSE and REGLS.
23	REGLS	7V Internal Regulator Output. REGLS output voltage is with respect to V_{SS}. Bypass REGLS with a 1µF capacitor to NSENSE.

Pin Description (continued)

PIN	NAME	FUNCTION
24	BOOTR	Right-Channel Bootstrap Capacitor. Connect a 0.1µF capacitor between BOOTR and OUTR.
25, 26	OUTR	Right Speaker Output
29, 30, 34, 35	V_{DD}	Positive Power-Supply Input. Bypass V_{DD} to LGND with a 0.1µF plus additional bulk capacitance. See the *Supply Pumping Effects* section.
31, 32, 33	V_{SS}	Negative Power-Supply Input. For dual-supply operation, connect to negative power-supply voltage and bypass V_{SS} to LGND with a 0.1µF plus additional bulk capacitance. For single-supply operation, connect to LGND.
EP	EP	Exposed Paddle. EP is internally connected to device substrate. Connect EP to V_{SS} through a large section of copper to maximize power dissipation.

Test Circuits

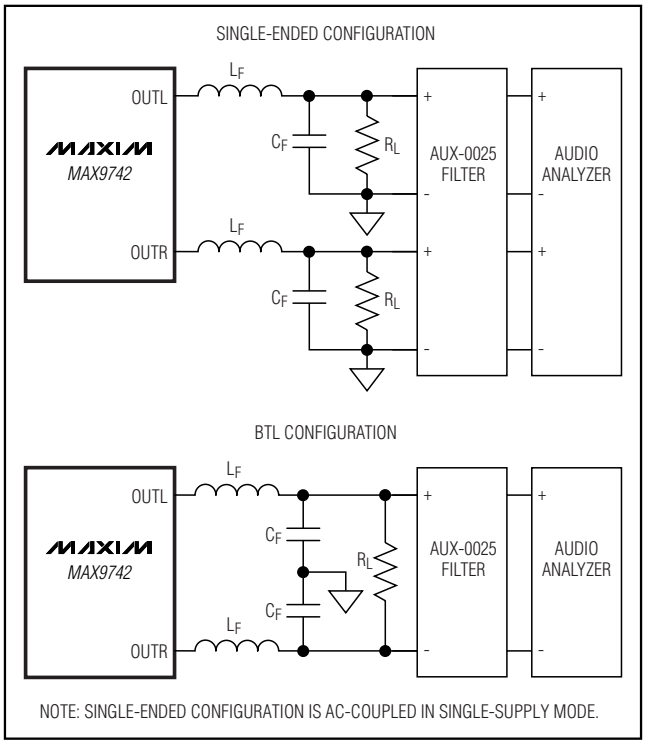


Figure 1. Test Circuits for Single-Ended and BTL Configurations

Detailed Description

The MAX9742 is a two-channel, single-ended Class D stereo amplifier capable of providing 16W of output power on each channel into 4Ω loads in single- or dual-supply operation. The amplifier can also provide 32W of output power in a mono bridge-tied-load (BTL) configuration. The device offers Class AB audio performance with Class D efficiency.

The differential input architecture reduces common-mode noise pickup. The device can also be configured for single-ended input signals.

The connection of external feedback components allows custom gain settings.

Class D Operation and Efficiency

Class D amplifiers are switch-mode devices capable of significantly higher power efficiencies in comparison to linear amplifiers. The output stage of the MAX9742 consists of a half-bridge speaker driver (see Figure 2). The high efficiency of a Class D amplifier is attributed to the region of operation of the output stage transistors. In a Class D amplifier, the output transistors act as current-steering switches by switching the output between V_{DD} and V_{SS} (ground for single-supply operation). Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead. The theoretical best

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

efficiency of a linear amplifier is 78%; however, that efficiency is only exhibited at peak output powers. Under normal operating levels (typical music reproduction levels), efficiency falls below 30%, whereas the MAX9742 still exhibits 80% efficiency under the same conditions.

Since the output transistors switch the output to either V_{DD} or V_{SS} (ground for single-supply operation), the resulting output of a Class D amplifier is a high-frequency square wave. This square wave is pulse-width-modulated by the audio input signal. In the MAX9742, the pulse-width modulation (PWM) is accomplished by comparing the input audio signal to an internally generated triangle wave oscillator. The resulting duty cycle of the square wave is proportional to the level of the input signal. When the input signal is at 0V, the duty cycle of the MAX9742 output is equal to 50%. To extract the amplified audio signal from this PWM waveform, the output of the MAX9742 is fed to an external LC lowpass filter (see the *Single-Ended LC Output Filter Design (L_F and C_F)* section). The LC filter works as an averaging circuit for the PWM output voltage waveform. The resulting averaged output voltage is equal to the amplified audio signal. Figure 3a illustrates the resulting PWM output waveform due to the varying input signal level, and Figure 3b shows the recovered amplified input signal after filtering.

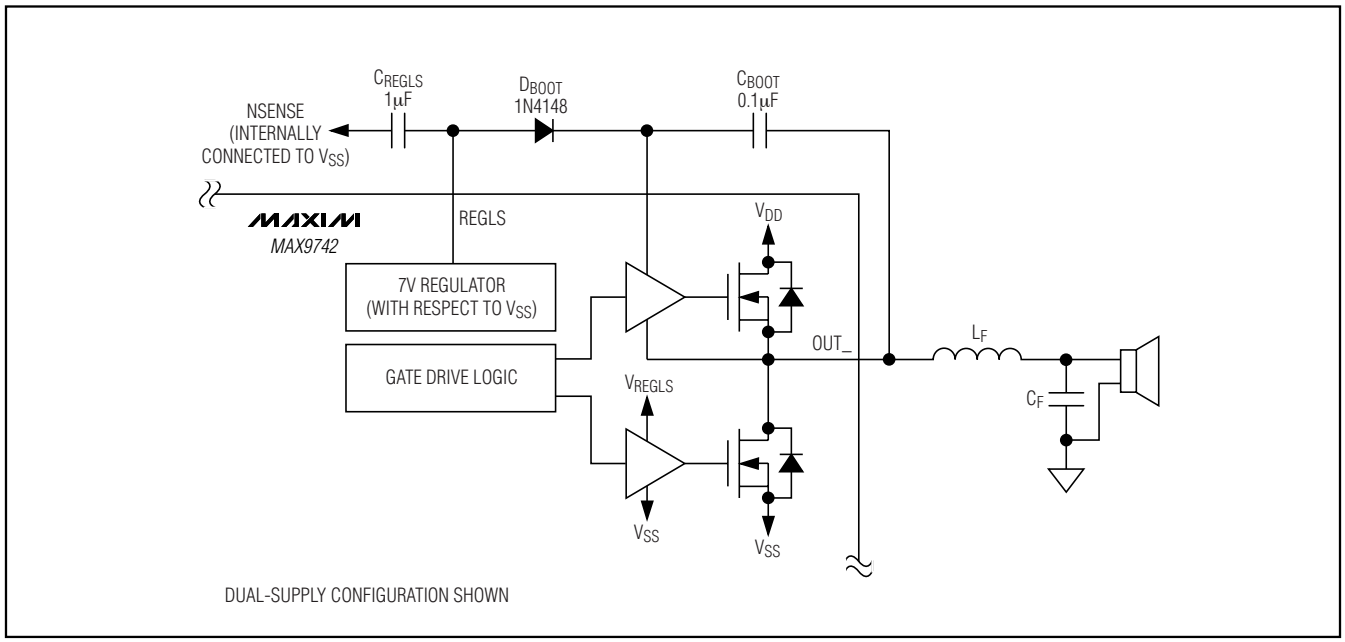


Figure 2. Simplified Block Diagram of the MAX9742 Output Stage

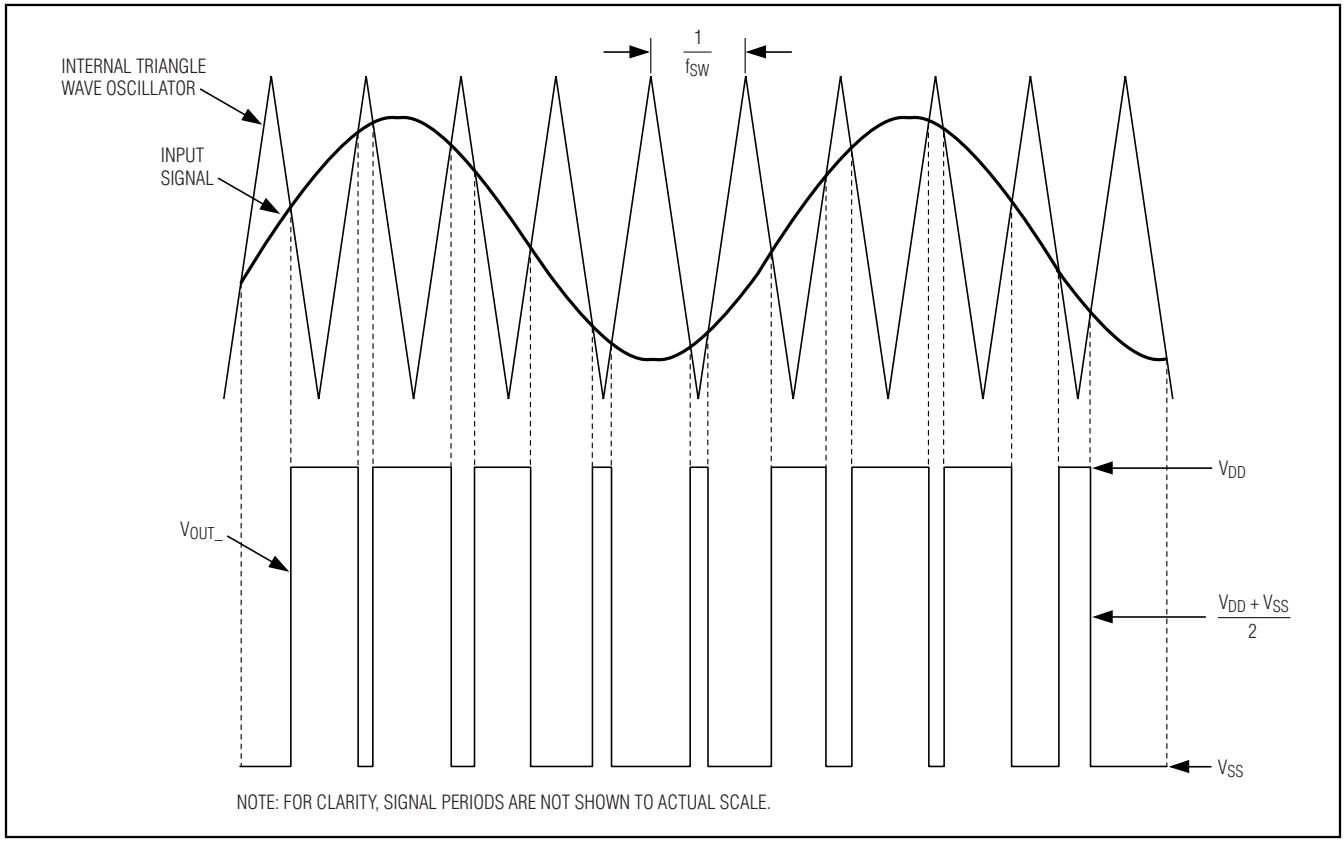


Figure 3a. MAX9742 Output with an Applied Input Signal

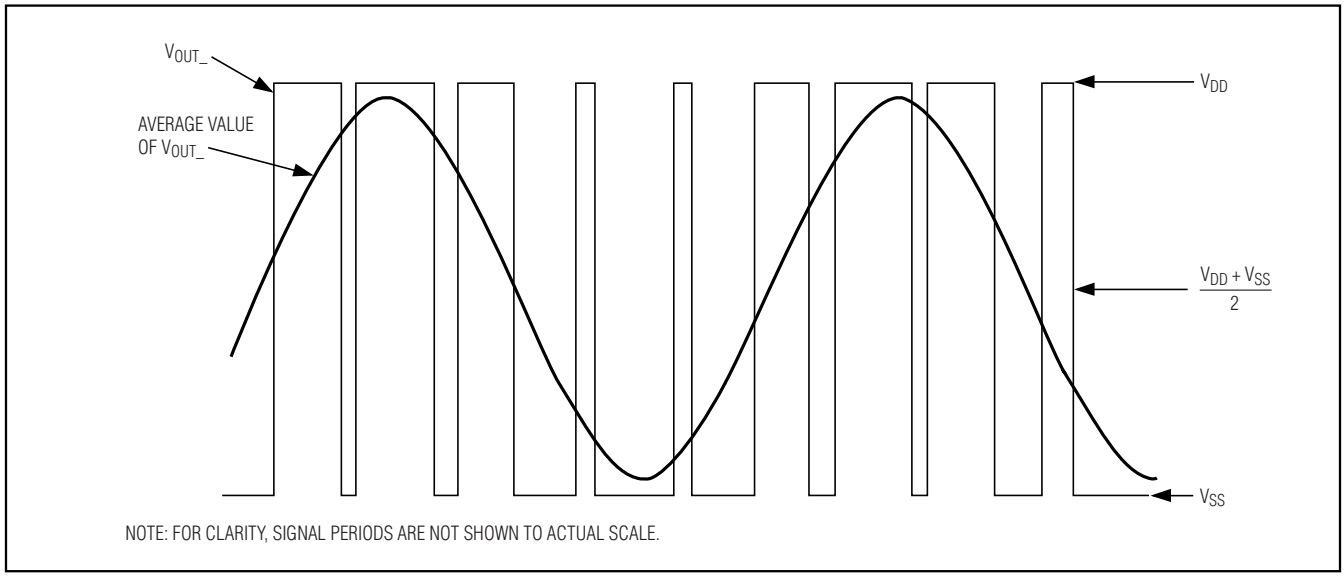


Figure 3b. MAX9742 Output with Resulting Output After Filtering

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

Shutdown Mode

The MAX9742 features a low-power shutdown mode that reduces quiescent current consumption to less than 0.5mA in single-supply mode and less than 1µA in dual-supply mode. Drive $\overline{SHDN}$ low to place the device into shutdown mode. Connect $\overline{SHDN}$ to a logic-high for normal operation.

The maximum voltage that may be applied to the $\overline{SHDN}$ input is 4V (see the *Absolute Maximum Ratings* section). If the $\overline{SHDN}$ input must be controlled by a 5V logic signal, limit the maximum voltage that can be applied to the $\overline{SHDN}$ input to 4V through an external resistive divider.

Click-and-Pop Suppression

The MAX9742 features comprehensive click-and-pop suppression that minimizes audible transients on start-up and shutdown. While in shutdown, the half-bridge output transistor switches are turned off, causing each output to go high impedance. During startup, or power-up, the input amplifiers are muted and an internal loop sets the modulator bias voltages to the correct levels, minimizing audible clicks and pops when the output half-bridge is enabled. The value of the soft-start capacitor, C_{SFT}, affects the click-and-pop performance and startup time of the MAX9742 (see the *Soft-Start Capacitor (C_{SFT})* section). To maximize click-and-pop suppression when powering up an audio system, drive $\overline{SHDN}$ or SFT (see the *Mute Function* section) to 0V until the rest of the circuitry in the system has had enough time to stabilize. This ensures the MAX9742 is the last device to be activated in the system and prevents transients caused by circuitry preceding the MAX9742 from being amplified at the outputs.

Mute Function

The MAX9742 features a clickless/popless mute mode. When the device is muted, the outputs stop switching, muting the speaker. The mute function only affects the output stage and does not shutdown the device. To mute the MAX9742, drive SFT to ground. Figure 4 shows how an external transistor (MOSFET or BJT) can be used to easily mute the MAX9742.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX9742. When the junction temperature exceeds approximately +160°C, the thermal protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by approximately 15°C. This results in a pulsing output under continuous thermal-overload conditions.

Supply Undervoltage and Overvoltage Protection

The MAX9742 features an undervoltage protection function that prevents the device from operating if V_{DD} is less than +7V with respect to V_{MID} input or if V_{SS} is greater than -7V with respect to V_{MID}. This feature prevents improper operation when insufficient supply voltages are present. Once the supply voltage exceeds the undervoltage threshold, the MAX9742 is turned on and the amplifiers are powered, provided that $\overline{SHDN}$ is high and the outputs are unmuted.

The MAX9742 also features an overvoltage protection function that prevents the device from operating if the potential difference between V_{DD} and V_{SS} exceeds +46V. This feature prevents the MAX9742 from damaging itself due to excessive supply pumping effects (see the *Supply Pumping Effects* section). The device returns to normal operation once the potential difference between V_{DD} and V_{SS} drops below +46V.

Applications Information

Output Dynamic Range

Dynamic range is the difference between the noise floor of the system and the output level at 10% THD+N. It is essential that a system's dynamic range be known before setting the maximum output gain. Output clipping occurs if the output signal is greater than the dynamic range of the system.

Use the THD+N vs. Output Power graph in *Typical Operating Characteristics* to identify the system's dynamic range. Given the system's supply voltage, find the output power that causes 10% THD+N for a given load. Use the following equation to determine the peak-

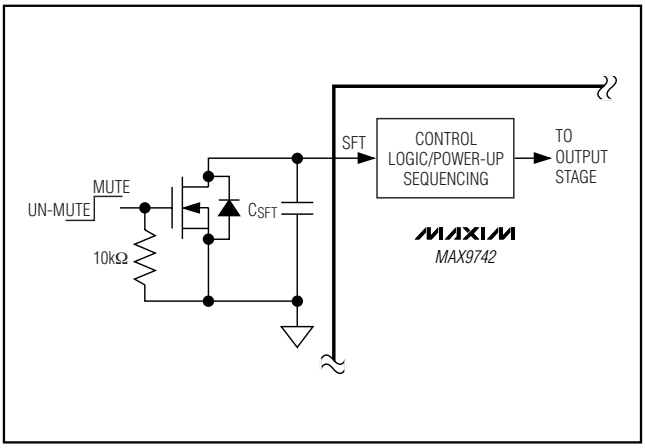


Figure 4. MAX9742 Mute Circuit

to-peak output voltage that causes 10% THD+N for a given load.

$$V_{OUT\_P-P} = 2\sqrt{2\left(P_{OUT\_10\%} \times R_L\right)}\ (V)$$

where $P_{OUT\_10\%}$ is the output power that causes 10% THD+N, R_L is the load resistance, and V_{OUT_P-P} is the peak-to-peak output voltage. Determine the voltage gain (A_V) necessary to attain this output voltage based on the maximum peak-to-peak input voltage (V_{IN_P-P}):

$$A_V = \frac{V_{OUT\_P-P}}{V_{IN\_P-P}}\ (V/V)$$

Set the closed-loop voltage gain of the MAX9742 less than or equal to A_V to prevent clipping of the output, unless audible clipping is acceptable for the application.

Input Amplifier

The external feedback networks of the MAX9742 input amplifiers allow custom gain settings while maximizing dynamic range. The input amplifiers also accommodate a variety of standard amplifier configurations including differential input, single-ended input, and summing amplifiers. Due to the output current limitations of the internal input amplifiers, always select feedback resistors (R_{F1}, see the *Typical Application Circuits/Functional Diagrams*) with values greater than or equal to 400kΩ. To preserve gain accuracy, avoid using feedback resistors with values greater than 1MΩ. For proper operation, limit common-mode input voltages to ±3V.

Differential Input Configuration

The *Typical Application Circuits/Functional Diagrams* show each channel of the MAX9742 configured as differential input amplifiers. A differential input offers improved noise immunity over a single-ended input. In systems that include high-speed digital circuitry, high-frequency noise can couple into the amplifier's input traces. The signals appear at the amplifier's inputs as common-mode noise. A differential input amplifier amplifies the difference of the two inputs, and signals common to both inputs are subtracted out. When configured for differential inputs, the voltage gain of the MAX9742 is set by:

$$A_V = \frac{R_{F1}}{R_{IN1}}\ (V/V)$$

where A_V is the desired voltage gain in V/V. R_{IN1} should be equal to R_{IN2}, and R_{F1} should be equal to R_{F2}.

When using the differential input configuration, the common-mode rejection ratio (CMRR) is primarily limited by the external resistor tolerances. Ideally, to achieve the highest possible CMRR, the resistors should be perfectly matched and the following condition should be met:

$$\frac{R_{F1}}{R_{IN1}} = \frac{R_{F2}}{R_{IN2}}$$

To ensure the MAX9742 input amplifiers operate as fully differential integrators, connect a capacitor between IN_+ and MID whose value is equal to C_F (see the *Feedback Capacitor (CFB_)* section).

Single-Ended Input

Each channel of the MAX9742 can be configured as a single-ended input amplifier by connecting IN_+ to MID (through an external resistor, R_{OS}) and driving IN_- with the input source (see Figure 5). In this configuration, the MAX9742 is configured as a single-ended amplifier whose voltage gain is equal to:

$$A_V = -\frac{R_F}{R_{IN}}\ (V/V)$$

where A_V is the desired voltage gain in V/V.

To minimize output offset voltages due to input bias currents, connect a resistor, R_{OS}, (see Figure 5) between IN_+ and MID. Select the value of R_{OS} so that the DC resistances looking out of inputs of the amplifier (IN_+ and IN_-) are equal. For example, when using the dual-supply configuration with a DC-coupled input source, the value of R_{OS} should be equal to $R_F \| R_{IN}$.

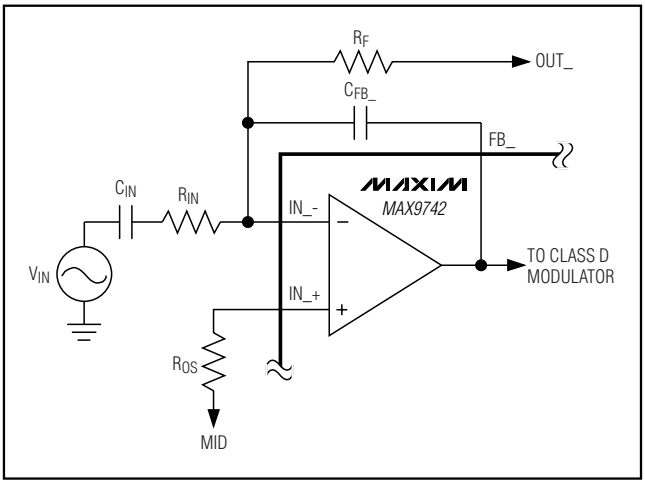


Figure 5. Single-Ended Input Configuration

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

Summing Configuration (Audio Mixer)

Figure 6 shows the MAX9742 configured as a summing amplifier, which allows multiple audio sources to be linearly mixed together. Using this configuration, the output of the MAX9742 is equal to the weighted sum of the input signals:

$$V_{OUT\_} = -\left(V_{IN1}\frac{R_F}{R_{IN1}} + V_{IN2}\frac{R_F}{R_{IN2}} + V_{IN3}\frac{R_F}{R_{IN3}}\right)$$

As shown in the above equation, the weighting or amount of gain applied to each input signal source is determined by the ratio of R_F and the respective input resistor (R_{IN1}, R_{IN2}, R_{IN3}) connected to each signal source. Select R_F and $R_{IN\_}$ so that the dynamic range of the MAX9742 is not exceeded when the input signals are at their maximum values and in phase with each other (see the *Output Dynamic Range* section).

To minimize output offset voltages due to input bias currents, connect a resistor, R_{OS}, (see Figure 6) between IN_+ and MID. Select the value of R_{OS} such that the DC resistances looking out of inputs of the amplifier (IN_+ and IN_-) are equal. For example, when using the dual-supply configuration with a DC-coupled input source, the value of R_{OS} should be equal to $R_F||R_{IN1}||R_{IN2}||\ ||R_{INn}$.

Mono Bridge-Tied-Load (BTL) Configuration

The MAX9742 also accommodates a mono bridge-tied-load (BTL) configuration that can be used in single-supply and dual-supply applications. In the BTL configuration, the speaker load is driven differentially by connecting the half-bridge outputs as a full H-bridge driver. To drive the speaker differentially, the inputs of both channels must be driven by the same audio signal with one channel 180° out-of-phase with the other channel. Figure 7 shows the connections required for BTL operation.

The advantages of BTL operation include reduced component count due to the elimination of the output-coupling capacitors when using single-supply operation, a 6dB increase in gain due to the load being driven differentially, increased output power into a single load, and the minimization of the supply-pumping since each half bridge is driven 180° out-of-phase (see the *Supply Pumping Effects* section). For single-supply applications, the output-coupling capacitors are not needed for BTL operation since the DC voltage present at each half-bridge output is equal in value and applies to each side of the load. This means no DC voltage appears across the load, and therefore, no DC current flows into the speaker.

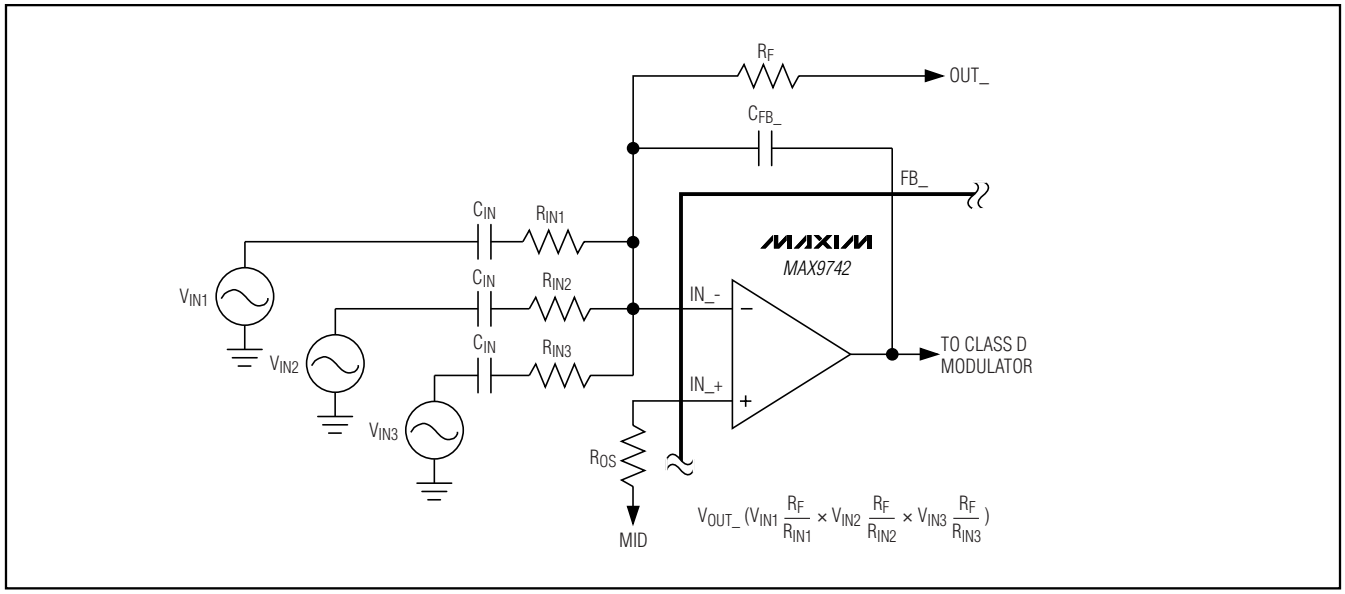


Figure 6. Summing Amplifier Configuration

Since each half-bridge output stage is only capable of driving loads as small as 4Ω and each half-bridge sees half of the differential load resistance when configured for BTL, only use the BTL configuration with loads greater than or equal to 8Ω. The MAX9742 may be thermally limited when using the BTL configuration with high supply voltages due to the decreased load resistance seen by each half bridge. For optimum performance, the PCB should be thermally optimized to achieve the continuous output powers required for the application (see the *Thermal Considerations* section).

Component Selection

Feedback Capacitor ($C_{FB\_}$)

To maximize dynamic range, an external feedback capacitor ($C_{FB\_}$) is needed to generate an error signal for the Class D modulator. The feedback capacitor configures the input amplifier stage as an integrator whose output is equal to an error signal consisting of the sum of the integrated input audio and PWM output signals. The integrator provides a noise-shaping function for the closed-loop response of the amplifier.

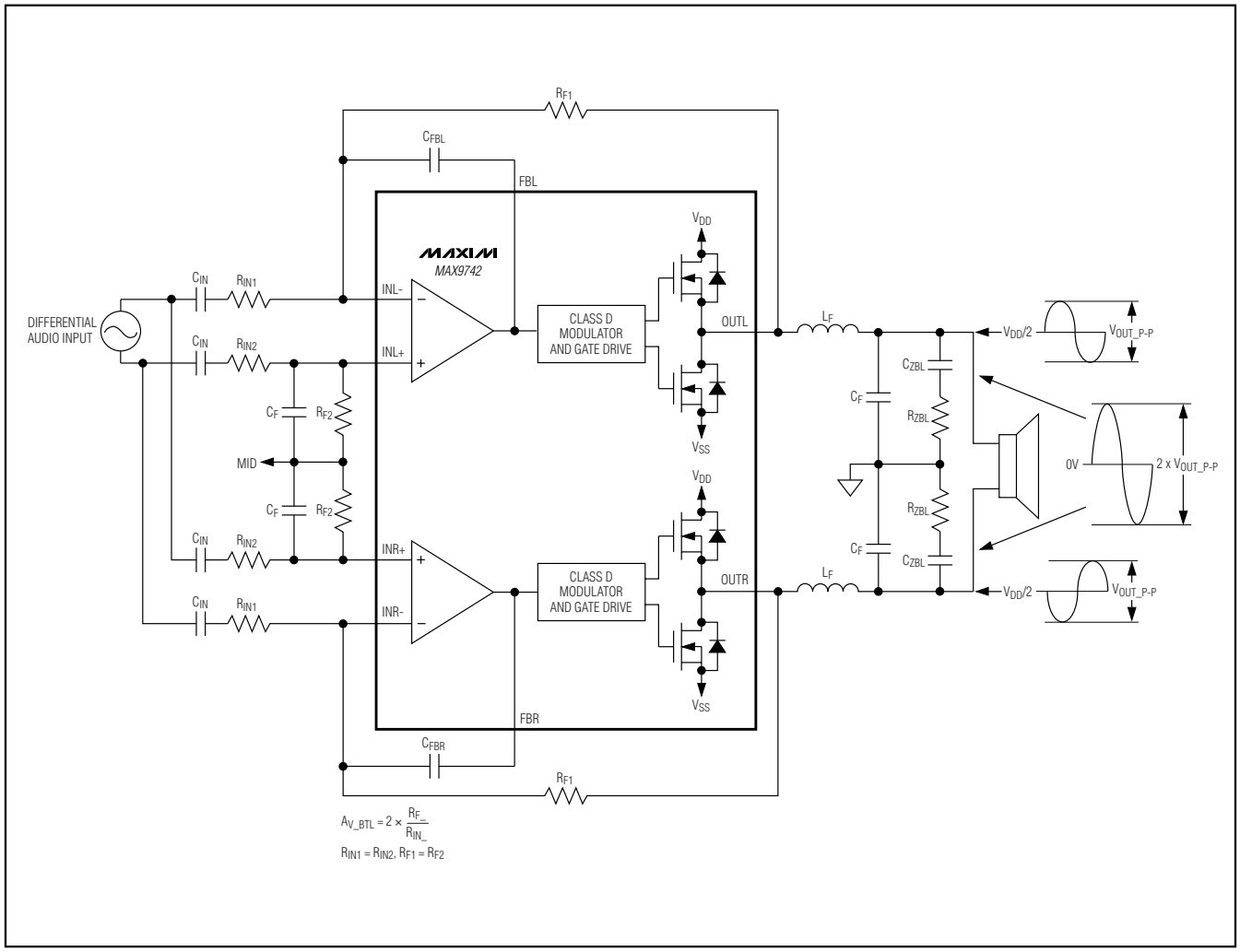


Figure 7. Input Signal Source and Load Connections for BTL Operation

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

To guarantee stability and minimize distortion, select the external feedback resistor ($R_{F\_}$) and capacitor ($C_{FB\_}$) so that the following conditions are met:

$$R_{F\_} \times C_{FB\_} \geq \frac{21.5}{f_{SW}} \text{ and } R_{F\_} > 400k\Omega$$

where f_{SW} is the output switching frequency determined by R_{REF} (see the *Setting the Switching Frequency and Output Current Limit (R_{REF})* section).

Setting the Switching Frequency and Output Current Limit (R_{REF})

Resistor R_{REF} determines the output switching frequency (f_{SW}) and the output short-circuit current-limit value (I_{SC}). Set f_{SW} and I_{SC} with the following equations:

$$f_{SW} = \frac{1}{3.3\mu s \times \frac{68k\Omega}{R_{REF}}} \text{ (Hz)}$$

$$I_{SC} = 3.6A \times \frac{68k\Omega}{R_{REF}} \text{ (A)}$$

For example, selecting a 68kΩ resistor for R_{REF} results in a switching frequency of 303kHz and an output short-circuit current limit of 4.5A.

To prevent damage to the MAX9742 during output short-circuit conditions and to utilize its full output power capabilities, use resistor values greater than or equal to 58kΩ and less than or equal to 75kΩ for R_{REF}.

Input-Coupling Capacitor

The AC-coupling capacitors (C_{IN}) and input resistors ($R_{IN\_}$) form highpass filters that remove any DC bias from an input signal (see the *Typical Application Circuits/Functional Diagrams*). C_{IN} prevents any DC components from the input-signal source from appearing at the amplifier outputs. The -3dB point of the highpass filter, assuming zero source impedance due to the input signal source, is given by:

$$f_{-3dB} = \frac{1}{2\pi \times R_{IN} \times C_{IN}} \text{ (Hz)}$$

Choose C_{IN} so that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response. Use capacitors with low-voltage coefficient dielectrics. Aluminum electrolytic, tantalum, or film dielectric capacitors are good choices for AC-coupling capacitors. Capacitors with high-voltage coefficients, such as ceramics (non-C0G dielectrics), can result in increased distortion at low frequencies.

Single-Ended LC Output Filter Design (L_F and C_F)

An LC output filter is needed to extract the amplified audio signal from the PWM output (see Figure 8). The LC circuit forms an LCR lowpass filter (neglecting voice coil inductance) with the impedance of the speaker. To provide a maximally flat-frequency response, the LCR filter should be designed to have a Butterworth response and should be optimized for a specific speaker load. Table 1 provides some recommended standard L_F and C_F component values for 4Ω, 6Ω, and 8Ω speaker loads. The component values given in Table 1 provide an approximate -3dB cutoff frequency (f_C) of 40kHz. The following paragraph provides information on calculating filter component values for cutoff frequencies other than 40kHz and speaker loads not listed in Table 1.

The LCR filter has the following 2nd order transfer function:

$$H(s) = \frac{\frac{1}{L_F \times C_F}}{s^2 + \frac{1}{R_{SPKR} \times C_F} s + \frac{1}{L_F \times C_F}}$$

where L_F is the value of the filter inductor, C_F is the value of the filter capacitor, and R_{SPKR} is the DC resistance of the speaker. The voice coil inductance of the speaker has been neglected to simplify filter calculations (see the *Zobel Network* section). The above transfer function is presented in the general 2nd order transfer function format given below:

$$H(s) = \frac{\omega_n^2}{s^2 + 2 \times \zeta \times \omega_n \times s + \omega_n^2}$$

where w_n is the natural frequency in radians/s and ζ is the damping ratio of the 2nd order system. For an ideal Butterworth response, ζ is equal to 0.707 and ω_C is equal to the -3dB cutoff frequency, ω_c. Using the above transfer functions and converting to Hertz, the -3dB cutoff frequency of the filter is:

$$f_C = \frac{1}{2 \times \pi \times \sqrt{L_F \times C_F}} \text{ (Hz)}$$

Using the transfer functions and the equation for f_C, the following expressions for L_F and C_F can be derived:

$$C_F = \frac{1}{4 \times \pi \times f_C \times R_{SPKR} \times \zeta} \text{ (F)}$$

$$L_F = \frac{1}{4 \times \pi^2 \times f_C^2 \times C_F} \text{ (H)}$$

Since the frequency response of the output filter is dependent on the speaker resistance, it is best to optimize the LC filter for a particular load resistance. To calculate the component values of the LC filter for a given speaker load resistance, first select an appropriate cutoff frequency for the filter. The cutoff frequency should be high enough so that upper audio frequency band attenuation is kept to a minimum while providing sufficient attenuation at the switching frequency (f_{SW}) of the MAX9742. Once the cutoff frequency is determined, calculate C_F using the DC resistance of the speaker (R_{SPKR}) and a damping ratio (ζ) equal to 0.707. Finally, calculate L_F using the resulting C_F value.

When selecting C_F, use capacitors with DC voltage ratings greater than V_{DD}.

When selecting L_F, it is important to take into account the DC resistance, current capabilities, and upper frequency limitations of the inductor. Choosing an inductor with minimum DC resistance minimizes I^2R losses due to the filter inductor and therefore preserves power efficiency. The inductor current rating should be greater than the maximum peak output current to prevent the inductor from going into saturation. Output inductor saturation introduces nonlinearities into the output signal and therefore increases distortion. The upper frequency limit of the inductor should also be taken into account. The load connected to the output of the half-bridge (LC filter and speaker) should remain inductive at the switching frequency of the MAX9742. If not, a significant amount of high-frequency energy is dissipated in the resistive load, therefore, increasing the supply current to excessive levels. To prevent this from occurring, select an output inductor whose self-resonant frequency is substantially higher than the switching frequency of the MAX9742.

To minimize possible EMI radiation, place the LC filter near the MAX9742 on the PCB.

Table 2 provides some suggested inductor manufacturers.

BTL LC Output Filter Design

When using the BTL configuration, optimize the output filter for fully differential operation (see Figure 9 and Table 3). Follow the design criteria provided for the single-ended filter except use half the value of the BTL resistance for the output filter calculations. This is because each half-bridge output sees half of the BTL resistance. For example, with a BTL resistance of 8Ω the ideal filter component values are C_F = 0.7µF and L_F = 22.5µH for a maximally flat differential filter response with an approximate cutoff frequency of 40kHz. Rounding to the nearest standard component values yields C_F = 0.68µF and L_F = 22µH. Also connect ground-terminated Zobel networks on each side of the speaker load (see the *Zobel Network* section). Ground terminating the Zobel networks prevents excessive peaking in the common-mode frequency response of the filter.

Table 1. Recommended LC Filter Component Values for Various Speaker Loads (f_C = 40kHz)

DC RESISTANCE OF SPEAKER (Ω)	L_F (µH)	C_F (µF)
4	22	0.68
6	33	0.47
8	47	0.33

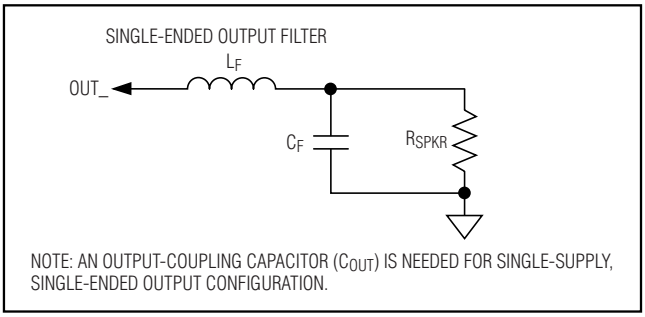


Figure 8. Single-Ended LC Output Filter

Table 2. Suggested Inductor Manufacturers

MODEL	MANUFACTURER	DIMENSIONS	WEBSITE
DO3340P	Coilcraft	12.95mm x 9.4mm x 11.43mm	www.coilcraft.com
CDRH127	Sumida	12.3mm x 12.3mm x 8mm	www.sumida.com
11RHBP	Toko	11mm x 11mm x 13.75mm	www.tokoam.com
SLF12575	TDK	12.5mm x 12.5mm x 7.5mm	www.component.tdk.com

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

To maximize the performance of the differential output filter and minimize EMI radiation, keep the ground connections of the C_F capacitors close together on the PCB and place the filter near the MAX9742.

The component ratings for C_F and L_F follow the same requirements mentioned in the *Single-Ended LC Output Filter Design (L_F and C_F)* section.

Zobel Network

For speaker loads that have appreciable amounts of voice coil inductance (> 33µH), peaking in the frequency response of the output may occur near the cutoff frequency of the LC filter, which may cause the device to go into current limit at high output powers. This peaking is due to the resonant circuit formed by the LC output filter and complex impedance of the speaker. To nullify the peaking in the frequency response, connect a Zobel network (series RC circuit) in parallel with the speaker load as shown in Figure 10. The Zobel circuit reduces the peaking by dampening the reactive behavior of the speaker. For the single-ended output configuration, use the following equations to calculate the component values for the Zobel network:

$$R_{ZBL} = 1.2 \times R_{SPKR} \ (\Omega)$$

$$C_{ZBL} = \frac{1}{2\pi \times R_{SPKR} \times f_C} \ (F)$$

where R_{ZBL} is the value of the Zobel resistor, C_{ZBL} is the value of the Zobel capacitor, R_{SPKR} is the DC resistance of the speaker, and f_C is the cutoff frequency of the LC filter. For the BTL configuration, use half of the BTL resistance for the Zobel network calculations. Connect a ground-terminated Zobel network on each side of the BTL resistance to prevent excessive peaking in the common-mode response of the output filter. For most applications, R_{ZBL} should have a minimum power rating of 1/4W or greater. C_{ZBL} should have a voltage rating greater than or equal to V_{DD}.

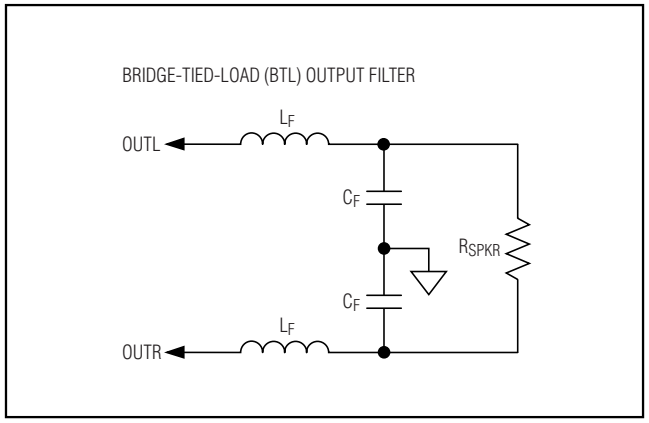


Figure 9. BTL LC Output Filter

Table 3. Recommended Differential LC Filter Component Values for an 8Ω BTL Speaker Load (f_C = 40kHz)

DC Resistance of Speaker (Ω)	L_F (µH)	C_F (µF)
8	22	0.68

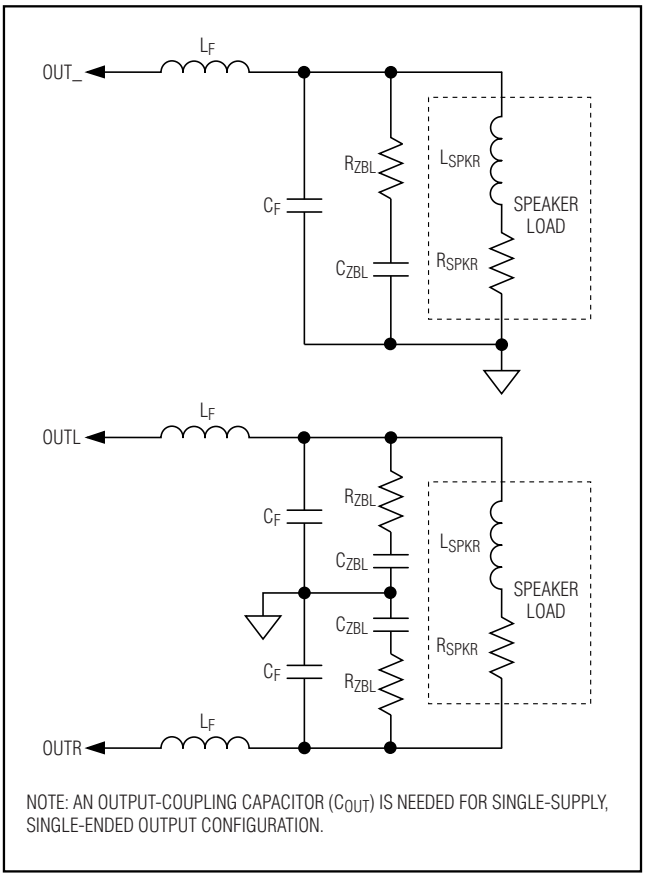


Figure 10. Zobel Network Connections for High-Inductance Speakers

Bootstrap Diode (D_{BOOT})

To provide sufficient gate drive voltage to the high-side transistor of the half-bridge output stage, an external diode (D_{BOOT}) and capacitor (C_{BOOT}) are needed for the internal bootstrapping circuitry (see Figure 2). To maintain high power efficiencies and maximum output power at low audio frequencies, use fast-recovery switching diodes for D_{BOOT}. Silicon diodes equivalent to 1N914, BAS16, or 1N4148 work well.

Capacitor (C_{BOOT})

For most applications, use a C_{BOOT} capacitor ≥ 0.1µF and ≤ 0.22µF. For proper operation, use capacitors with low ESR and voltage ratings greater than 7V for C_{BOOT}.

Output-Coupling Capacitors (C_{OUT}, Single-Ended, Single-Supply Operation)

The MAX9742 requires output-coupling capacitors for single-supply operation. Since the MAX9742 outputs switch between V_{DD} and ground in single-supply operation, there is a DC component equal to 0.5 x V_{DD} present at the outputs. The output-coupling capacitor blocks this DC component, preventing DC current from flowing into the load. The output capacitor and the load resistance of the speaker form a highpass filter. The -3dB point of the highpass filter can be approximated by:

$$f_{-3dB} = \frac{1}{2\pi \times R_{SPKR} \times C_{OUT}} \text{ (Hz)}$$

where f_{-3dB} is the -3dB cutoff frequency of the filter, R_{SPKR} is the DC resistance of the speaker, and C_{OUT} is the value of the output-coupling capacitor. As with the input capacitor, choose C_{OUT} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response. Select capacitors with low ESR to minimize power losses. Since the output-coupling capacitor has a large amplitude AC current (resulting average output current due to the LC filter) flowing through it at high output powers, it is important to select an output-coupling capacitor that has an appropriate ripple current rating. To prevent damage to the output-coupling capacitor, use the following equation to calculate the required RMS ripple current rating for C_{OUT}:

$$I_{RMS\_RIPPLE} = \frac{V_{DD}}{2.83 \times R_{SPKR}} \text{ (A)}$$

where I_{RMS_RIPPLE} is the minimum required RMS ripple current rating for C_{OUT} and R_{SPKR} is the DC resistance of the speaker. The ripple current ratings of capacitors are frequency dependent, so be sure to select a capacitor based on its ripple current rating within the audio frequency range.

Select output-coupling capacitors with DC voltage ratings greater than V_{DD}.

In single-supply operation with single-ended outputs, the leakage current of C_{OUT} can affect the startup time of the MAX9742. To minimize startup time delays due to C_{OUT}, use capacitors with leakage current ratings less than 1µA for C_{OUT}. See the *Startup Time Considerations* section for more information on optimizing the startup time of the MAX9742.

Setting V_{MID}

The voltage present at the MID input biases the internal amplifiers and should be set to the average value of V_{DD} and V_{SS} for maximum dynamic range. For dual-supply operation, connect MID to ground. For single-supply operation, set MID to 0.5 x V_{DD} through an external resistive divider. To minimize power dissipation while providing enough input bias current for the MID input, select divider-resistors with values greater than or equal to 10kΩ and less than or equal to 20kΩ. Connect a decoupling network between MID and the SGND plane (see the *Supply Bypassing/Layout* section) to provide a sufficient low- and high-frequency AC ground for the internal amplifiers. Figure 11 shows the recommended decoupling networks for bypassing the MID input.

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

Multiple-Pole MID Network vs. Single-Pole VMID Network for Increased PSRR Performance (Single-Supply Operation)

A multiple-pole MID network improves PSRR performance over a single-pole network. Since the input amplifiers of the MAX9742 are biased at V_{MID}, any noise coupled into the MID input using the MID bias network supply appears at the outputs of the MAX9742. Increasing the number of poles in the MID network provides further attenuation of low-frequency noise at the MID input, and therefore, improving the AC PSRR performance of the MAX9742. Figure 11 shows the recommended single-pole and two-pole MID input bias networks. Figure 12 illustrates the differences of the MAX9742's low-frequency AC PSRR performance with the single-pole and two-pole networks shown in Figure 11.

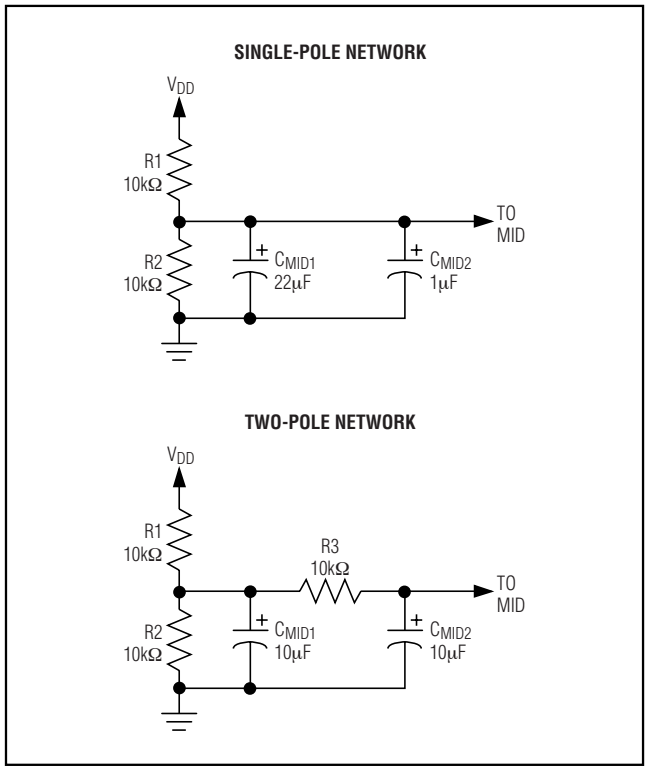


Figure 11. Recommended MID Input Bias Networks

Soft-Start Capacitor (C_{SFT})

The soft-start capacitor determines the timing for the soft-start power-up sequencing that minimizes audible clicks-and-pops during power-up/power-down transitions and when entering/exiting shutdown mode. Connect a capacitor between SFT and ground for proper operation. For optimum performance, this capacitor should equal 0.22µF. Using capacitor values much smaller than these values degrade click-and-pop performance and values much greater lengthen startup time.

Startup Time Considerations

At the beginning of the soft-start sequence, the MAX9742 ensures $V_{OUT\_}$ is approximately equal to V_{MID} before continuing the soft-start sequence. For single-supply operation with single-ended outputs, the output-coupling capacitors (C_{OUT}) are first gradually charged up to V_{MID} before continuing soft-start sequencing. This gradual charging up of C_{OUT} minimizes audible transients that may appear across the

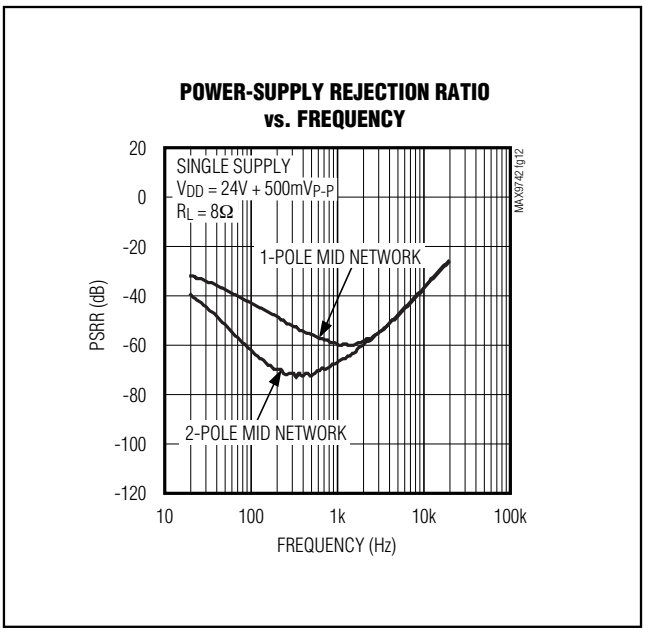


Figure 12. Comparison of MAX9742 AC PSRR with Single-Pole and Two-Pole MID Networks

speaker loads during mode transitions. After C_{OUT} is charged up to V_{MID}, the MAX9742 concludes the soft-start sequence by precharging C_{REGLS}, C_{BOOT}, and C_{IN}. Once the soft-start sequence is complete, the MAX9742 begins normal operation.

For dual-supply operation, the startup time of the MAX9742 is primarily dependent on the value of C_{SFT} since it controls the rate of the soft-start sequencing.

In single-supply operation, the overall startup time is affected by the values of C_{MID1}, C_{MID2}, C_{SFT}, C_{OUT} (single-ended outputs) and the value of the resistors used to bias the MID input. This is because soft-start power-up sequencing is dependent on the charging-up of the MID input bias network and the charging rate of C_{OUT}. As with dual-supply operation, the startup time is also affected by the value of C_{SFT} since it controls the rate of the soft-start sequencing. Using the component values shown in Figure 11 and a C_{SFT} capacitor value of 0.22µF yields a typical single-supply power-up time of 1.5s.

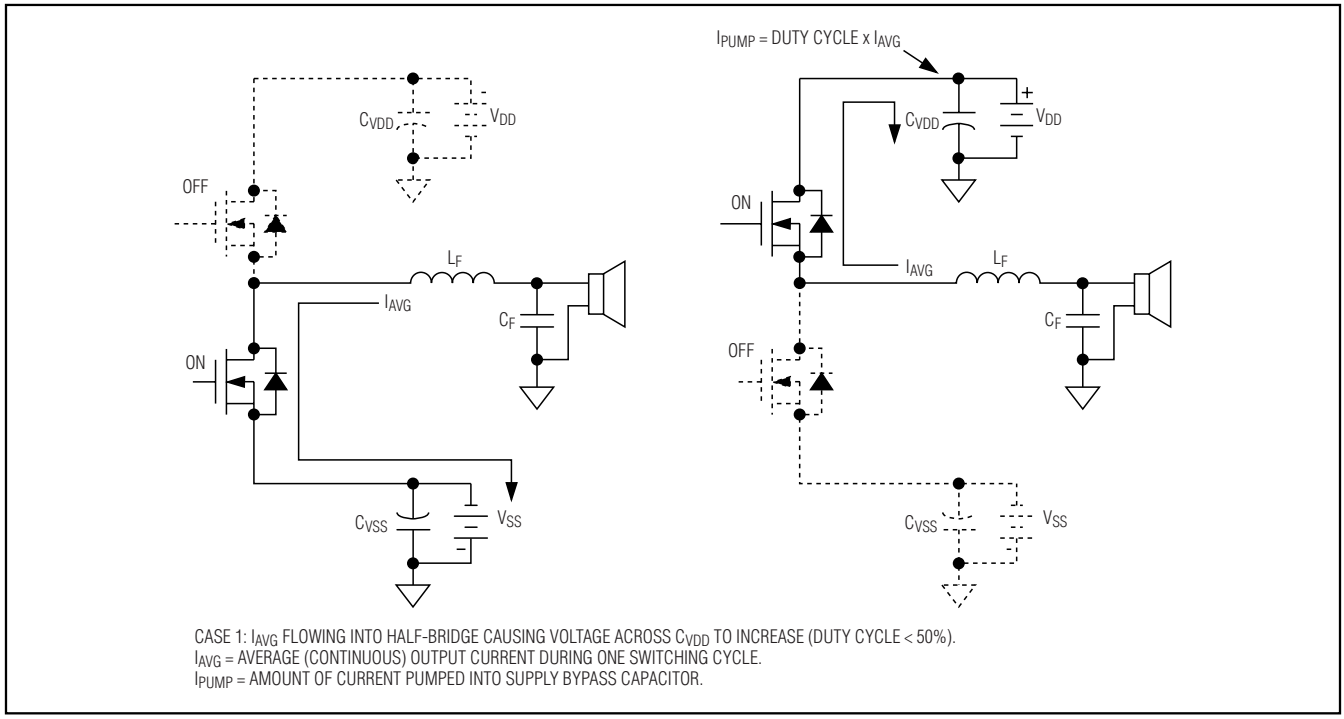
For single-supply operation with single-ended outputs, the leakage current of C_{OUT} can also affect the startup time of the MAX9742. To minimize startup time delays due to C_{OUT}, use capacitors with leakage current ratings less than 1µA for C_{OUT}.

Supply Pumping Effects

When using the MAX9742 in the single-ended output configuration, the power-supply voltages (V_{DD} and V_{SS}) may increase if the supplies cannot sink current. This "supply pumping" is primarily due to the inductive loading of the LC filter and the voice coil inductance of the speaker. The inductive load connected to the output of the device prevents the output current from changing instantaneously. When the MAX9742 drives this inductive load, a continuous current flows at the output whose value is equal to the running average of the output switching currents, or in other words, the amplified audio signal. This averaged current continues to flow during both switching cycles of the half-bridge, which means that some of the current is pumped back towards the opposite power supply. If the respective supply cannot sink this current, it flows into supply bypass capacitor causing the voltage across the capacitor to increase.

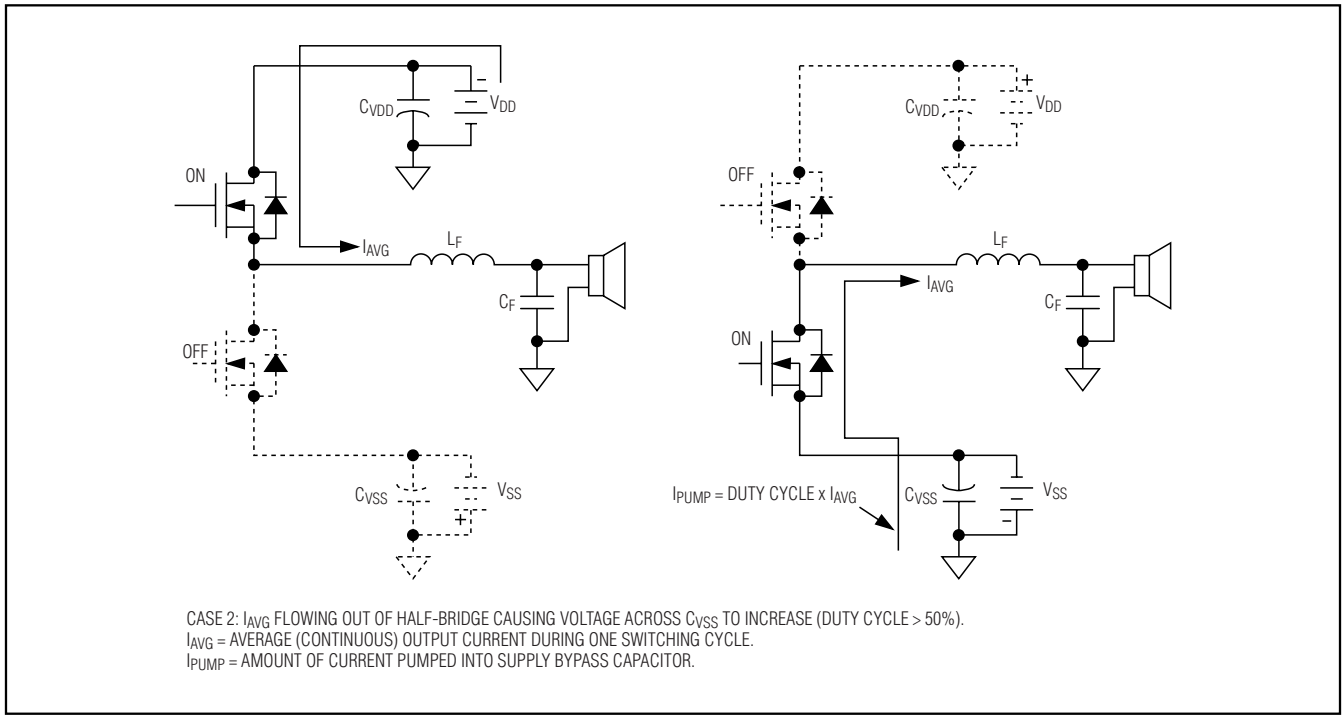
The amount of current pumped back into the opposite supply is proportional to the duty cycle of the switching period. For example, if the magnitude of the average (continuous) current during a single switching cycle is equal to -1A and the duty cycle of the output is equal to 25%, this means the V_{SS} supply provides 0.75A of current while the V_{DD} supply must sink 0.25A. Since the V_{DD} supply cannot sink this current, it flows into the bypass capacitor causing the V_{DD} supply voltage to be pumped up. Figures 13a and 13b illustrates the continuous output current flow that causes the supply pumping action.

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs



CASE 1: I_{AVG} FLOWING INTO HALF-BRIDGE CAUSING VOLTAGE ACROSS C_{VDD} TO INCREASE (DUTY CYCLE < 50%).
I_{AVG} = AVERAGE (CONTINUOUS) OUTPUT CURRENT DURING ONE SWITCHING CYCLE.
I_{PUMP} = AMOUNT OF CURRENT PUMPED INTO SUPPLY BYPASS CAPACITOR.

Figure 13a. Continuous Output Current Flow for Positive Supply Pumping



CASE 2: I_{AVG} FLOWING OUT OF HALF-BRIDGE CAUSING VOLTAGE ACROSS C_{VSS} TO INCREASE (DUTY CYCLE > 50%).
I_{AVG} = AVERAGE (CONTINUOUS) OUTPUT CURRENT DURING ONE SWITCHING CYCLE.
I_{PUMP} = AMOUNT OF CURRENT PUMPED INTO SUPPLY BYPASS CAPACITOR.

Figure 13b. Continuous Output Current Flow for Negative Supply Pumping

Worst-case supply pumping occurs at high output powers with low-frequency signals and small load resistances. Since the period is longer for low-frequency signals, the continuous output current has more time to pump up the supply rails during each cycle of the audio signal. Additionally, for most stereo audio sources the low-frequency audio content (bass) is primarily monophonic. This means both output channels are basically equal in magnitude and in phase at low frequencies causing twice as much pump-up current to flow into the supply bypass capacitors and therefore doubling the supply pump-up voltages. Assuming purely sinusoidal output signals, the worst-case supply voltage increase due to supply pumping can be approximated using the following equation:

$$V_{PUMP\_MAX} = \left(\frac{V_{SUPPLY}}{2\pi^2}\right) \times \left(\frac{1}{f_{OUT} \times R_{SPKR} \times C_{SUPPLY}}\right)$$

where V_{PUMP_MAX} is the magnitude increase of the supply rail, V_{SUPPLY} is the nominal voltage magnitude of the respective supply, f_{OUT} is the frequency of the audio signal, and C_{SUPPLY} is the value of the respective supply bypass capacitor. The above equation shows that increasing the value of the supply bypass capacitor decreases the supply voltage variations due to supply pumping. Using large bypass capacitors helps minimize supply voltage variations by providing sufficient supply decoupling at low output frequencies. To prevent the MAX9742 from entering supply overvoltage protection mode at low output frequencies (as low as 20Hz), use supply bypass capacitors with values of at least 1000µF for dual-supply operation and 660µF for single-supply operation.

Alternate Methods for Mitigating Supply Pumping

Using the BTL configuration minimizes the supply pumping effect since the outputs are driven 180° out-of-phase with each other. Driving the outputs 180° out-of-phase causes each half-bridge to pump up and draw current from opposite supplies, which reduces the magnitude of the of the supply pumping.

For the single-ended output configuration, the supply pumping can be minimized by driving the channels 180° out-of-phase and reversing the polarity of one speaker connection (see Figure 14). Reversing the polarity of one speaker minimizes any adverse affects on the audio quality by ensuring that the physical displacement of the speaker cones matches the physical displacement of the speakers when driven with in phase signals.

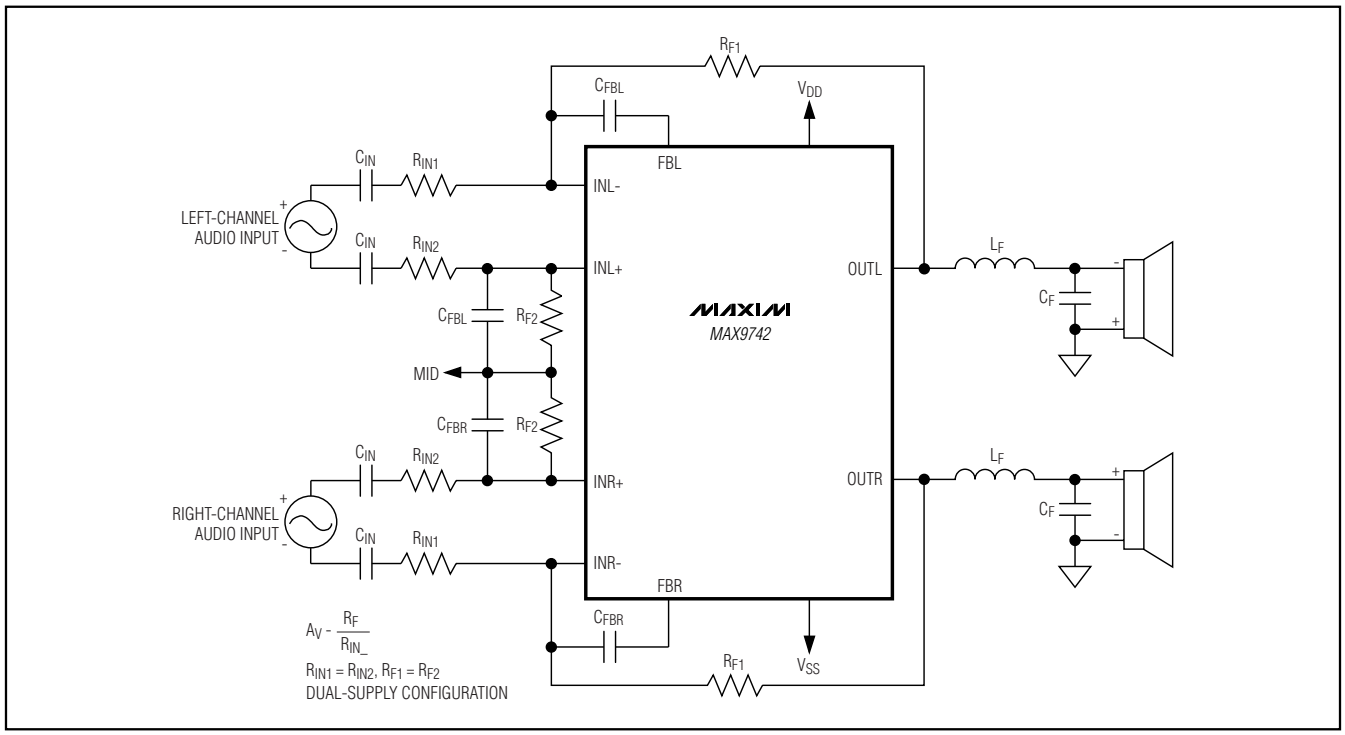


Figure 14. Circuit Configuration for Minimizing Supply Pumping

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

T-Network for Low THD Performance at Low Output Powers (Optional)

If low THD+N performance is needed at low-output powers, replace the feedback resistor (R_{F1}) in each channel with the T-network shown in Figure 15. The T-network provides additional attenuation of audio band noise, therefore, providing improved THD+N performance at lower output powers. Use the following expressions to select R_{IN1}, R_{IN2}, R_{F1a}, R_{F1b}, and R_{F2}:

$$R_{IN1} = \frac{R_{F1a} + R_{F1b}}{A_V} = \frac{121k\Omega + 562k\Omega}{A_V} = \frac{683k\Omega}{A_V} (\Omega)$$

$$R_{IN1} = R_{IN2} (\Omega)$$

$$R_{F2} = R_{F1a} + R_{F1b} (\Omega)$$

where A_V is the desired voltage gain in V/V. To maximize CMRR and minimize gain mismatch between channels, use the closest 1% tolerance resistor values available for R_{IN1}, R_{IN2}, R_{F1a}, R_{F1b}, and R_{F2}.

See the THD+N vs. Output Power With and Without T-Network plot in the *Typical Operating Characteristics* for a comparison of the THD+N performance with and without the optional T-network.

Output Limiting Diodes (Optional)

In applications where the output can be driven to clipping, a pair of diodes around the feedback capacitor helps reduce distortion. Clipping is most likely to happen when driving high-impedance speakers with lower supply voltages, for example, 8Ω loads with a 24V single supply. Diodes such as BAV99, a dual series silicon switching diode, are a good choice. Connect these diodes around the feedback capacitor as shown in Figure 16.

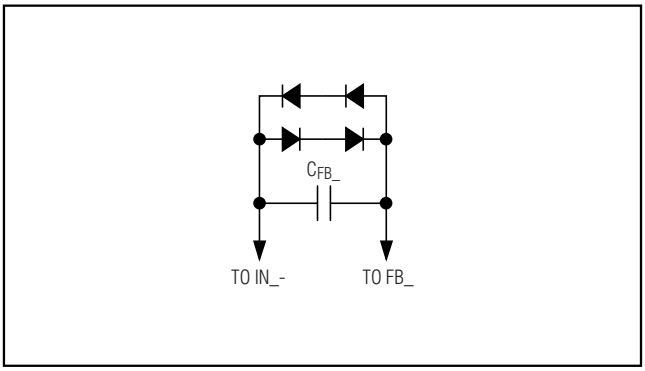


Figure 16. Connection of Output Limiting Diodes

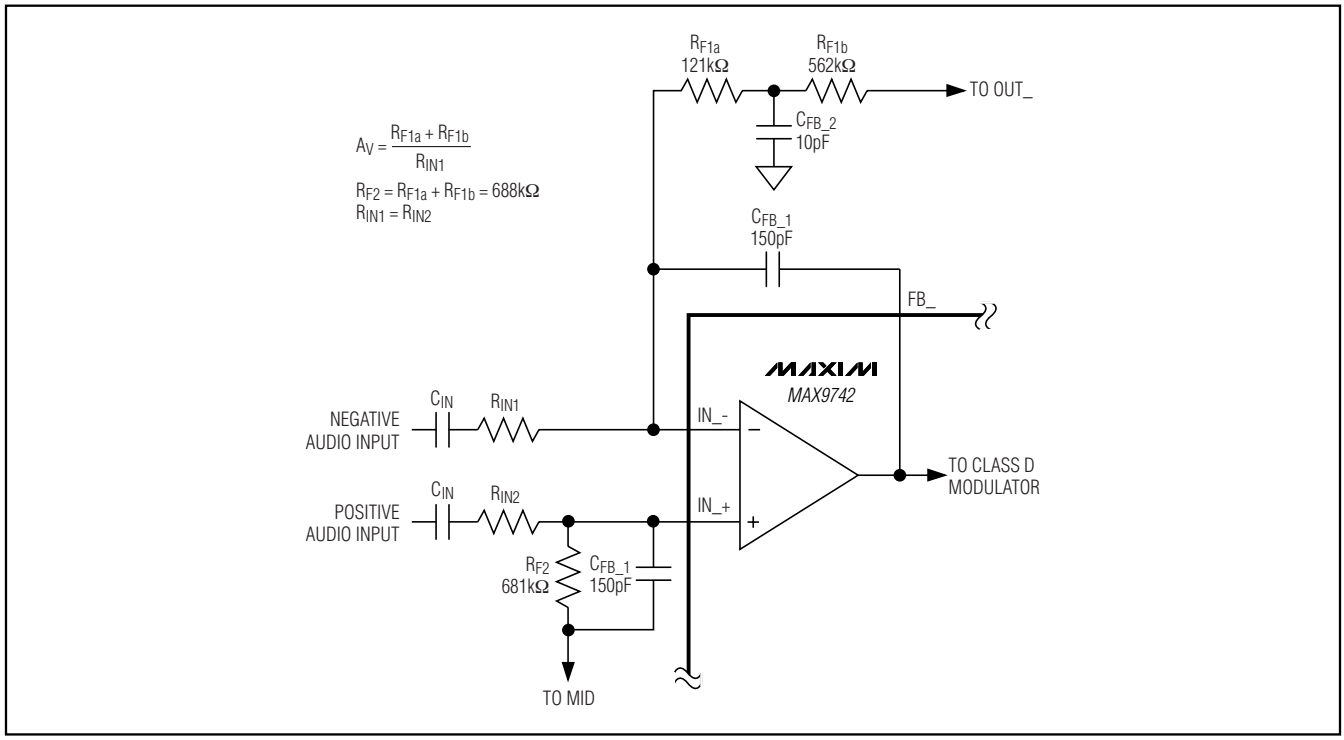


Figure 15. Optional T-Network for Minimizing THD+N at Low Output Powers

Supply Bypassing/Layout

To maximize output power and minimize distortion, proper layout and supply bypassing is essential. To prevent ground-loop-induced noise and minimize noise due to parasitic ground inductance, use separate ground planes for input-signal ground connections (SGND plane) and output-power ground connections (PGND plane). For dual-supply applications, connect MID to the SGND plane. For single-supply operation, connect MID to an external voltage-divider and bypass MID to the SGND plane with a decoupling network (see Figure 11). This provides a sufficient low- and high-frequency AC ground for the internal amplifiers. Connect the SGND and PGND planes together at a single point in the PCB near the MAX9742. Minimize the parasitic trace inductances and resistances associated with the V_{DD} and V_{SS} connections, by using wide traces of minimal length.

Proper power-supply bypassing is essential to ensure low distortion operation and to prevent excessive supply pumping when using the single-ended output configuration. For dual-supply operation, bypass V_{DD} and V_{SS} to PGND with 1000µF aluminum electrolytic capacitors. V_{DD} and V_{SS} should also be bypassed to PGND with 0.1µF capacitors as physically close as possible to V_{DD} and V_{SS} pins to provide sufficient high-frequency decoupling. Also, connect an additional 1µF capacitor between V_{DD} and V_{SS}. For single-supply operation, bypass V_{DD} to PGND with two 330µF capacitors. V_{DD} should also be bypassed to PGND with an additional 0.1µF capacitor as physically close as possible to the V_{DD} pin.

The MAX9742 includes voltage regulators for the internal amplifiers, logic circuitry, and gate-drive circuitry that require external bypassing. Bypass REGP and REGM to the SGND plane with 1µF capacitors. Bypass REGLS to NSENSE with a 1µF capacitor. Bypass LV_{DD} to LGND with a 0.1µF capacitor. The voltage rating requirements of the external bypass capacitors must be taken into account. This is especially important when selecting the REGP and REGM bypass capacitors since the ground-referenced voltages present at these regulator outputs are dependent on the voltage applied to the MID input. The minimum required voltage ratings for the regulator bypass capacitors are summarized in Table 4.

Thermal Considerations

Class D amplifiers provide much better efficiency and thermal performance than a comparable Class AB amplifier. However, the system's thermal performance must be considered with realistic expectations along with its many parameters.

Continuous Sine Wave vs. Music

When a Class D amplifier is evaluated in the lab, often a continuous sine wave is used as the signal source. While this is convenient for measurement purposes, it represents a worst-case scenario for thermal loading on the amplifier. It is not uncommon for a Class D amplifier to enter thermal shutdown if driven near maximum output power with a continuous sine wave. The PCB must be optimized for best dissipation (see the *PCB Thermal Considerations* section). Audio content, both music and voice, has a much lower RMS value relative to its peak output power. Therefore, while an audio signal may reach similar peaks as a continuous sine wave, the actual thermal impact on the Class D amplifier is highly reduced. If the thermal performance of a system is being evaluated, it is important to use actual audio signals instead of sine waves for testing. If sine waves must be used, the thermal performance is less than the system's actual capability for real music or voice.

PCB Thermal Considerations

The exposed paddle is the primary route for conducting heat away from the IC. With a bottom-side exposed paddle, the PCB and its copper becomes the primary heatsink for the Class D amplifier. Solder the exposed paddle to a copper polygon. Add as much copper as possible from this polygon to any adjacent pin on the Class D amplifier as well as to any adjacent components, provided these connections are at the same potential.

Table 4. Minimum Required Voltage Ratings for Regulator Bypass Capacitors

CAPACITOR	VOLTAGE RATING (V)
C_{REGP}	V_{MID} + 5
C_{REGM}	V_{MID} - 5
C_{REGLS}	7
C_{LVDD}	5

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These copper paths must be as wide as possible. Each of these paths contributes to the overall thermal capabilities of the system.

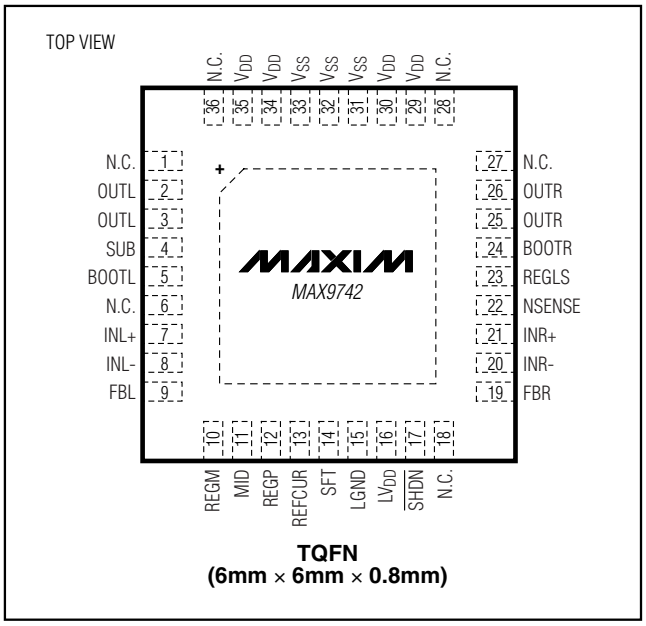
The copper polygon to which the exposed paddle is attached should have multiple vias to the opposite side of the PCB, where they connect to another copper polygon. Make this polygon as large as possible within the system's constraints for signal routing.

Additional improvements are possible if all the traces from the device are made as wide as possible. Although the IC pins are not the primary thermal path out of the package, they do provide a small amount. The total improvement would not exceed approximately 10%, but it could make the difference between acceptable performance and thermal problems.

Auxiliary Heatsinking

If operating in higher ambient temperatures, it is possible to improve the thermal performance of a PCB with the addition of an external heatsink. The thermal resistance to this heatsink must be kept as low as possible to maximize its performance. With a bottom-side exposed paddle, the lowest resistance thermal path is on the bottom of the PCB. The topside of the IC is not a significant thermal path for the device, and therefore, is not a cost-effective location for a heatsink. Place the inductor of the external LC output filter in close proximity to the IC. This not only helps minimize EMI radiation at the output traces, but also helps draw heat away from the MAX9742.

Pin Configuration

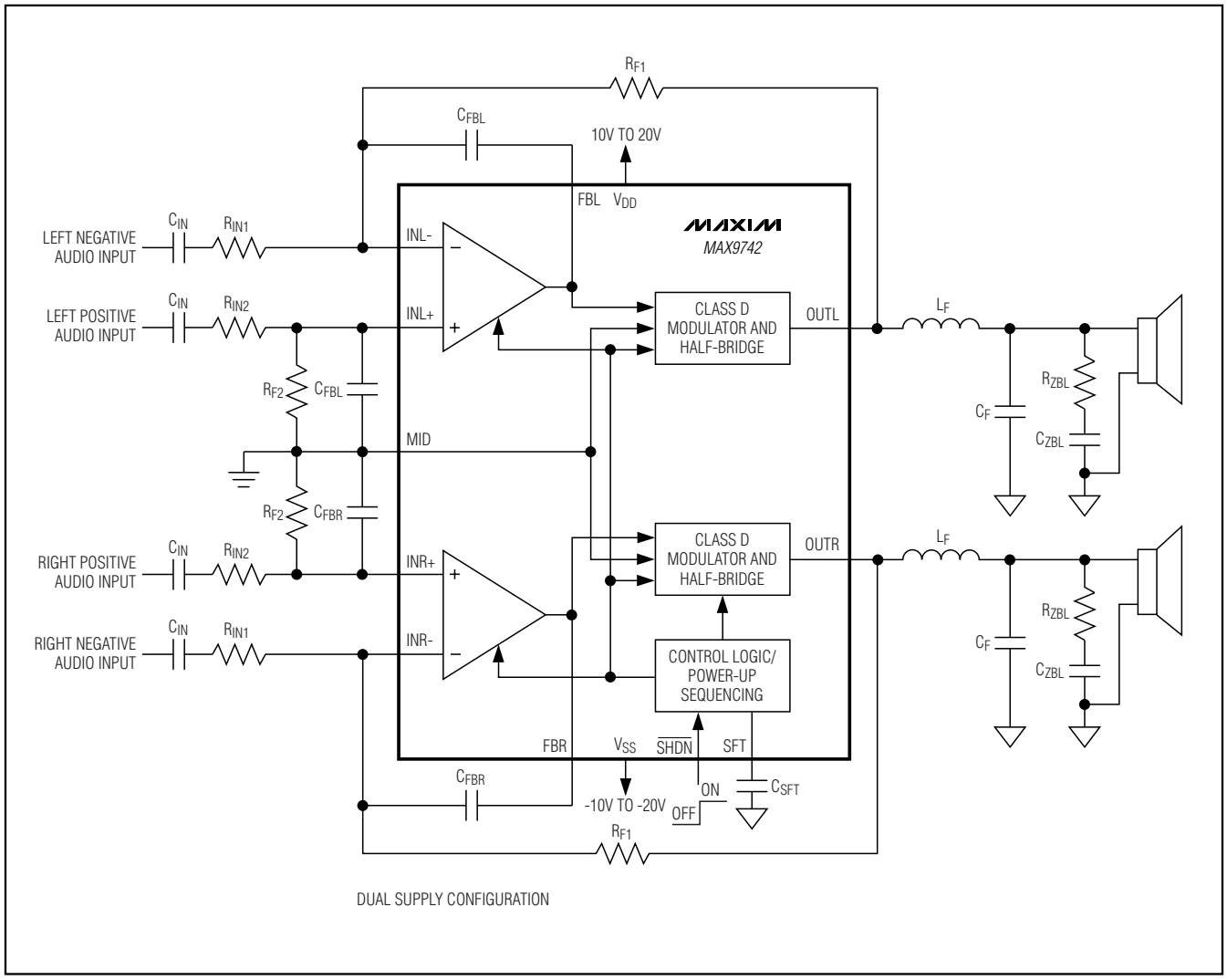


TQFN
(6mm × 6mm × 0.8mm)

Chip Information

PROCESS: BCD

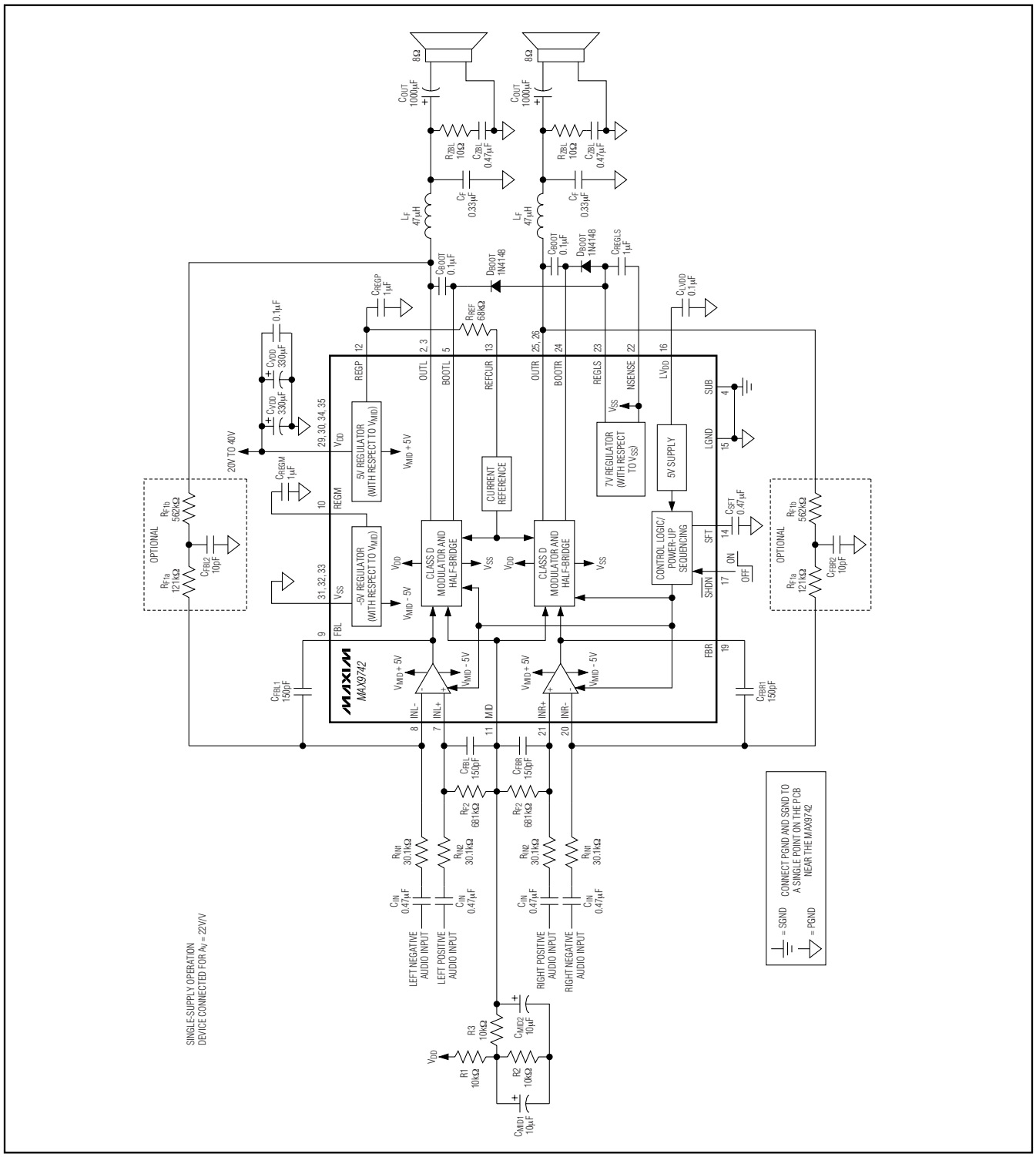
Simplified Block Diagram (continued)



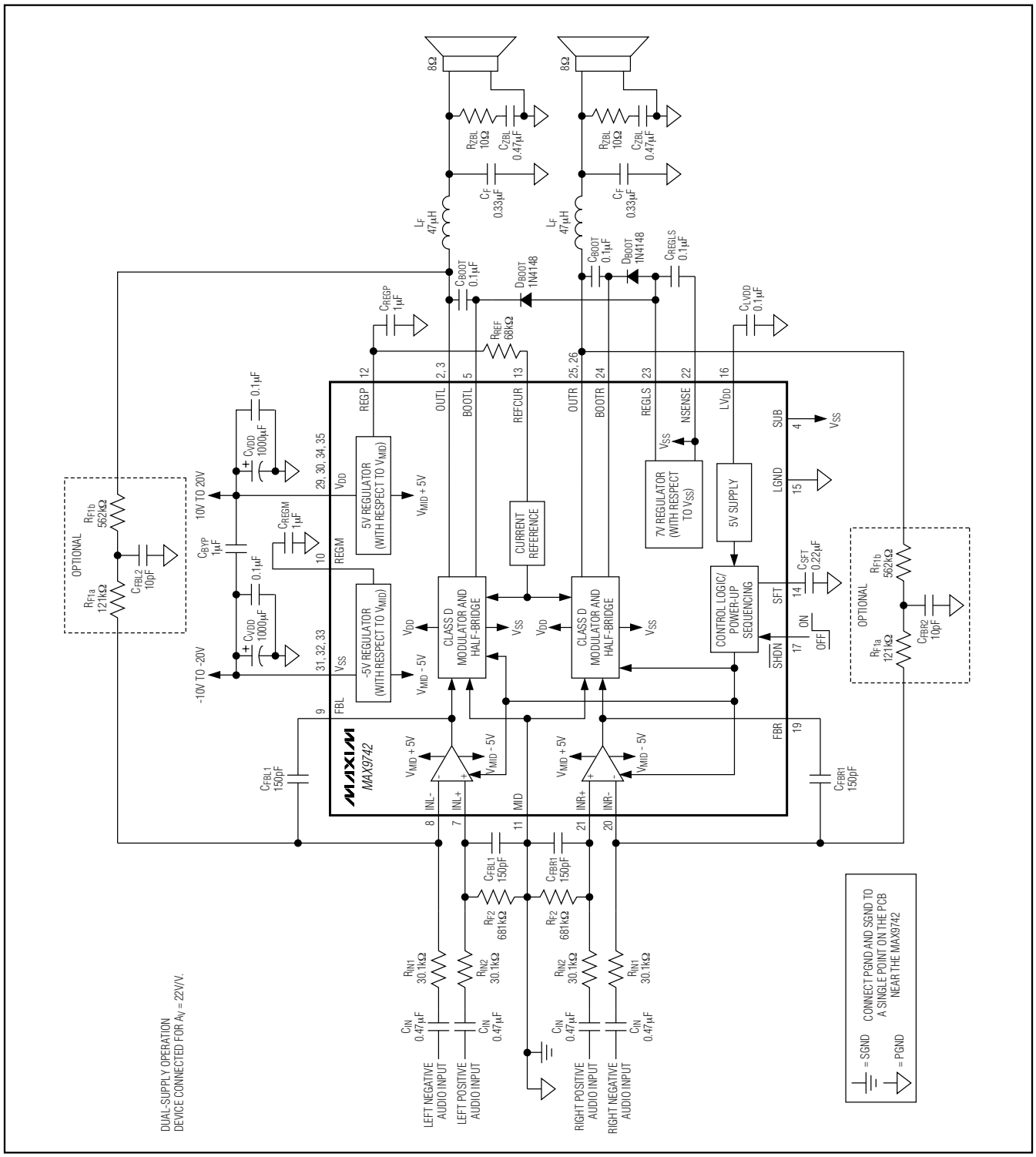
DUAL SUPPLY CONFIGURATION

Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

Typical Application Circuits/Functional Diagrams

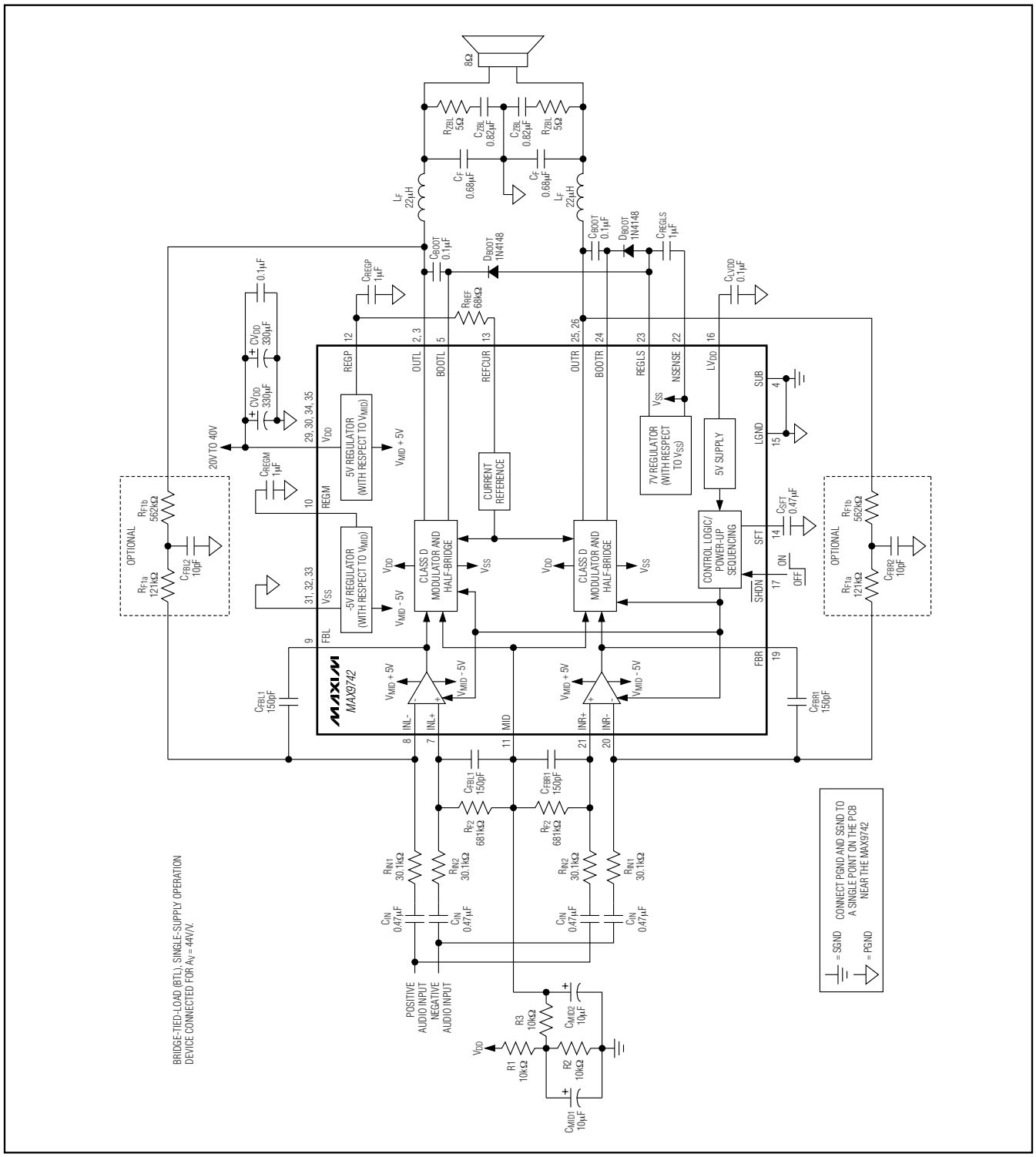


Typical Application Circuits/Functional Diagrams (continued)



Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

Typical Application Circuits/Functional Diagrams (continued)

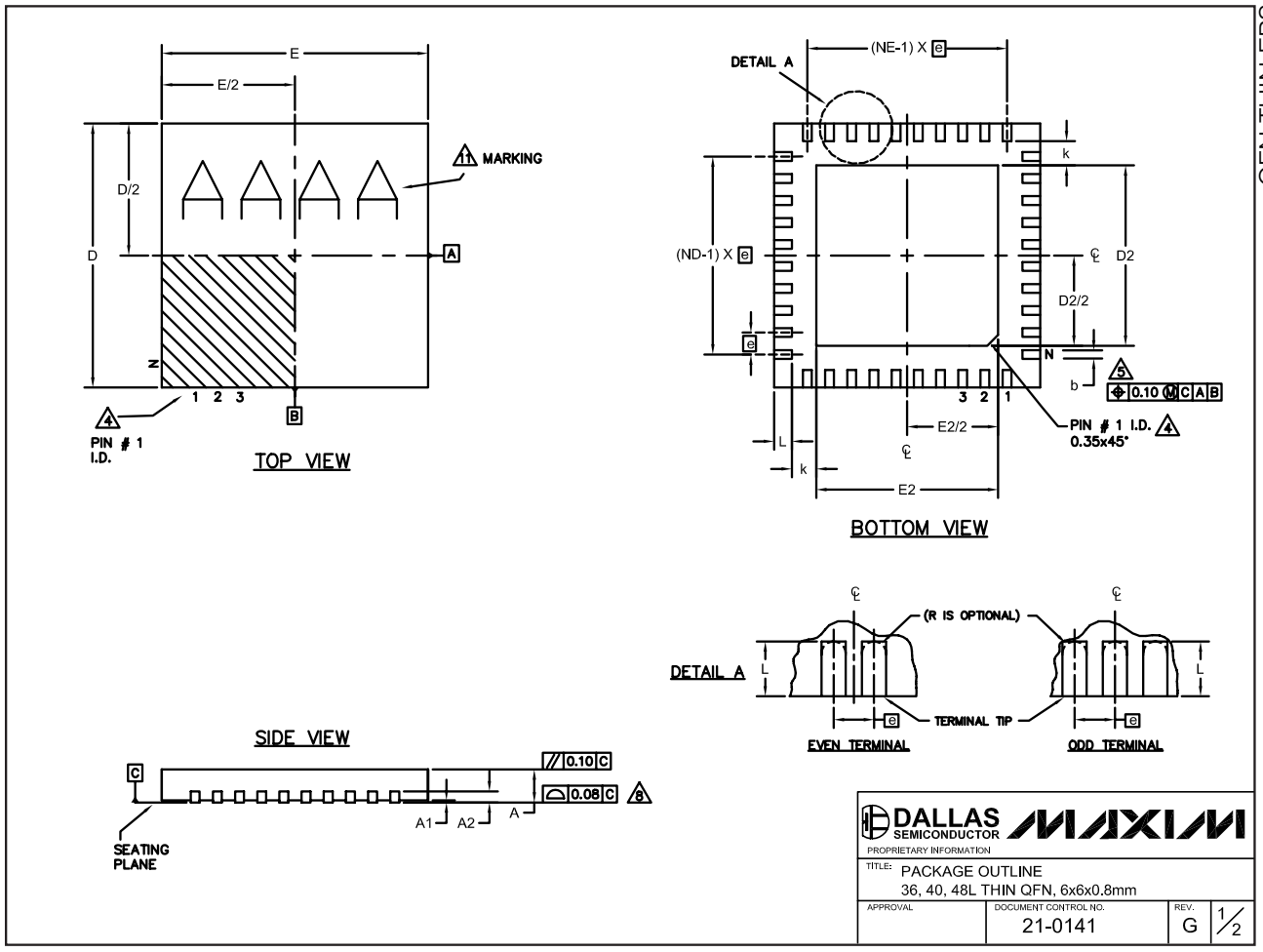


Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



Single-/Dual-Supply, Stereo 16W, Class D Amplifier with Differential Inputs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	G	2/2

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