Overvoltage Protector IC with Reverse Current Protection

NO.EA-313-181010

OUTLINE

The R5528Z001A is a CMOS-based overvoltage protector IC with reverse current protection that use an NMOS pass transistor to achieve ultra-low on resistance (Typ. 54mΩ). Overvoltage protection threshold is as high as 6.8V±3%. Also, continuous current capability is as high as 3A.

Internally, the R5528Z001A consists of a reverse current protection circuit, a soft-start circuit, a startup debounce circuit, an undervoltage lockout (UVLO) circuit, and a thermal shutdown circuit.

The R5528Z001A is offered in a small and thin WLCSP-9-P1 package which achieves the smallest possible footprint solution on boards where area is limited.

FEATURES

- Input Voltage Range (V_{IN}) ································ 2.3V to 36V
- Output Current (I_{OUT})······································ Max. DC 3A
- Switch On Resistance (R_{ON}) ····························· 54mΩ (V_{IN} = 5.0V, I_{OUT} = 100mA)
- OVP Threshold Accuracy ································· 6.8V±3%
- PG Function
- Reverse Current Protection Circuit
- Soft-start Circuit
- Startup Debounce Circuit ································· 15ms
- Thermal Shutdown Circuit
- Package··· WLCSP-9-P1 (1.27 mm x 1.27 mm x 0.64 mm)

APPLICATIONS

- Smartphones, Tablet PCs
- Portable devices

BLOCK DIAGRAMS

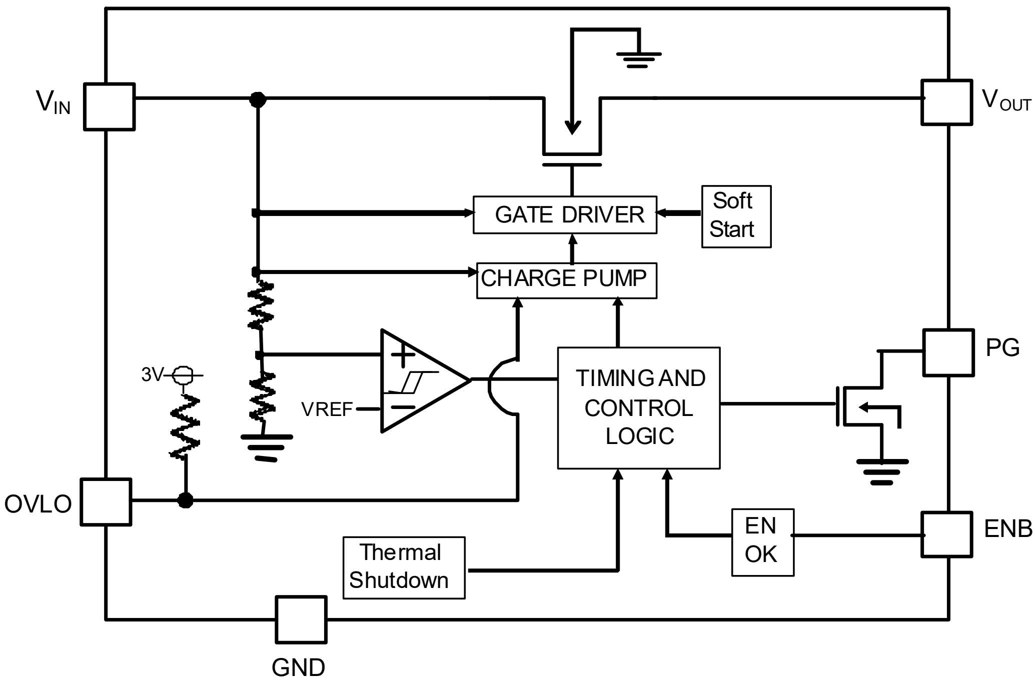


Figure 1. R5528Z001A

SELECTION GUIDE

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5528Z001A-E2-F	WLCSP-9-P1	5,000pcs	Yes	Yes

PIN CONFIGULATIONS

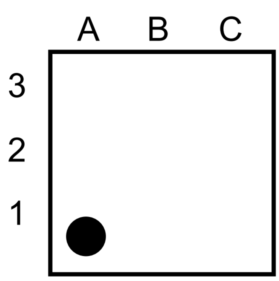


Figure 2. Top View

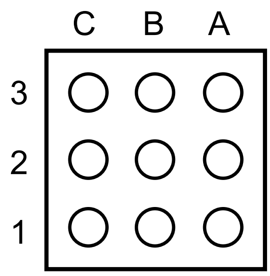


Figure 3. Bottom View

PIN DESCRIPTION

Pin No.	Symbol	Pin Description
A1	PG	Open Drain Flag Output Pin PG is driven low after input voltage is stable between minimum V_{IN} and $V_{IN\text{-}OVLO}$ after debounce (delay).
A2	OVLO	Overvoltage Lockout Input Pin Applying a voltage less than OVLO threshold (V_{OVLO_TH}) to the overvoltage lockout input pin can turn off a switch. When the overvoltage lockout input pin is Open, it outputs an OVLO open voltage (V_{OVLO_OP}).
A3	ENB	Active-Low ENB Input Pin
B1, C1	V_{IN}	Input Pin
B2	I.C	Internally Connected to Ground Unconnected or connected to GND
B3, C3	V_{OUT}	Output Pin
C2	GND	Ground Pin

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	-0.3 to 40	V
V_{OUT}	Output Voltage	-0.3 to 8.0	V
V_{ENB}	ENB Pin Input Voltage	-0.3 to 6.5	V
V_{PG}	PG Pin Voltage	-0.3 to 6.5	V
V_{OVLO}	OVLO Pin Input Voltage	-0.3 to 6.5	V
I_{PG}	PG Pin Current	14	mA
I_{OUT}	Output Current	3.0	A
P_D	Power Dissipation (High Wattage Land Pattern)*1	1190	mW
Topt	Operating Temperature Range	-40 to +85	°C
Tstg	Storage Temerature	-55 to +125	°C

*1 Refer to *POWER DISSIPATION* for detailed information.

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

V_{IN} = 2.3V to 36V, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} =1µF, unless otherwise noted. Typical values are V_{IN} = 5V and Ta = 25°C.

The specifications surrounded by [ ] are guaranteed by Design Engineering at - 40ºC ≤ Ta ≤ 85ºC.

(Ta=25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage		2.3		36	V
I_{IN}	Input Supply Current	V_{ENB} = 0V, V_{IN} = 5V, I_{OUT} = 0mA		50	120	µA
I_{IN_DIS}	Input Disable Current	V_{ENB} = 0V, V_{IN} = 5V, V_{OVLO} = 0V		40	120	µA
I_{IN_Q}	Input Shutdown Current	V_{ENB} = 5V, V_{IN} = 5V, V_{OUT} = 0V		1.0	12	µA
$I_{OUT\text{-}DIS}$	Output Disable Current	V_{ENB} = 0V, V_{OUT} = 5V, V_{IN} = 5V, V_{OVLO} < $V_{OVLO\text{-}TH}$			3	µA
		V_{ENB} = 0V, V_{OUT} = 5V, V_{IN} > $V_{IN\text{-}OVLO}$				
$I_{OUT\text{-}SD}$	Output Shutdown Current	V_{ENB} = 5V, V_{OUT} = 5V, V_{IN} = 5V			5.5	µA
R_{ON}	On Resistance	V_{IN} = 5V, I_{OUT} = 100mA		54	100	mΩ
$V_{IN\text{-}OVLO}$	Overvoltage Protection Threshold	V_{IN} rising	6.6	6.8	7.0	V
		V_{IN} falling	6.4			V
C_{OUT}	OUT Load Capacitance				1000	µF
V_{OVLO_OP}	OVLO Open voltage	V_{ENB} = 0V, V_{IN} = 5.0V		3.0	3.6	V
R_{OVLO_PU}	OVLO Pull-up Resistance			500		kΩ
V_{OVLO_TH}	OVLO Force Off Voltage		0.6	1.0	1.4	V
V_{IH}	ENB Input High Voltage		1.4			V
V_{IL}	ENB Input Low Voltage				0.4	V
I_{ENB}	ENB Input Leakage		-1		1	µA
V_{OL}	PG Output Low Voltage	I_{SINK} = 1mA			0.4	V
V_{PG_LEAK}	PG Leakage Current	V_{IO} = 3.3V*2	-1		1	µA
t_{DEB}	IN Debounce Time	starts when 2.3V < V_{IN}(5V) < $V_{IN\text{-}OVLO}$ and ends when charge-pump is turned on*3	10	15	35	ms
t_{SS}	Soft-start Time	starts when 2.3V < V_{IN} < $V_{IN\text{-}OVLO}$ and ends when V_{OUT} = 90% of V_{IN}		30		ms
t_{ON}	Turn-on Time During Soft-start	V_{IN} = 5V, R_L = 50Ω, C_L = 10uF, starts when V_{OUT} = 20% of V_{IN} and ends when V_{OUT} = 80% of V_{IN}*3	1.5	-		ms
t_{OFF}	Turn-off Time	R_L = 50Ω, starts when V_{IN} > $V_{IN\text{-}OVLO}$ (2V/µs) and ends when V_{OUT} = 80% of V_{IN}		1.5		µs
		starts when V_{ENB} is switched from "L" to "H", ends when V_{OUT} = 80% of V_{IN}, R_L = 50Ω		84		
T_{SHDN}	Thermal Shut Down			150		°C
T_{HYST}	Thermal Hysteresis			20		°C
V_{UVREL}	UVLO Release Voltage	V_{IN} rising		2.05	2.3	V
V_{UVHYS}	UVLO Hysteresis	V_{IN} falling		0.15		V

All test items listed under *ELECTRICAL CHARACTERISTICS* are done under the pulse load condition (Tj≈Ta=25ºC) except Soft-Start Time and Turn-off Time and UVLO Hysteresis.

*2 Refer to *TYPICAL APPLICATION AND TECHNICAL NOTES.*

*3 Refer to *TIMING CHART*.

TIMING CHART

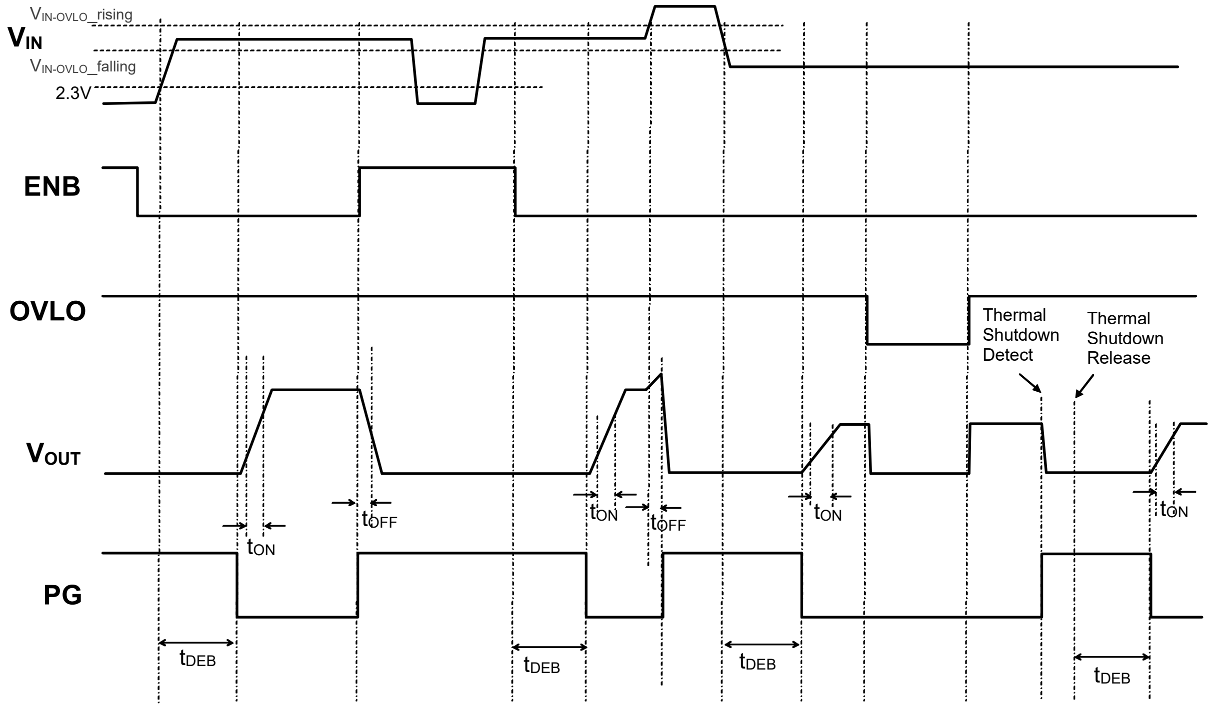


Figure 4. Timing Chart

TYPICAL APPLICATIONS AND TECHNICAL NOTES

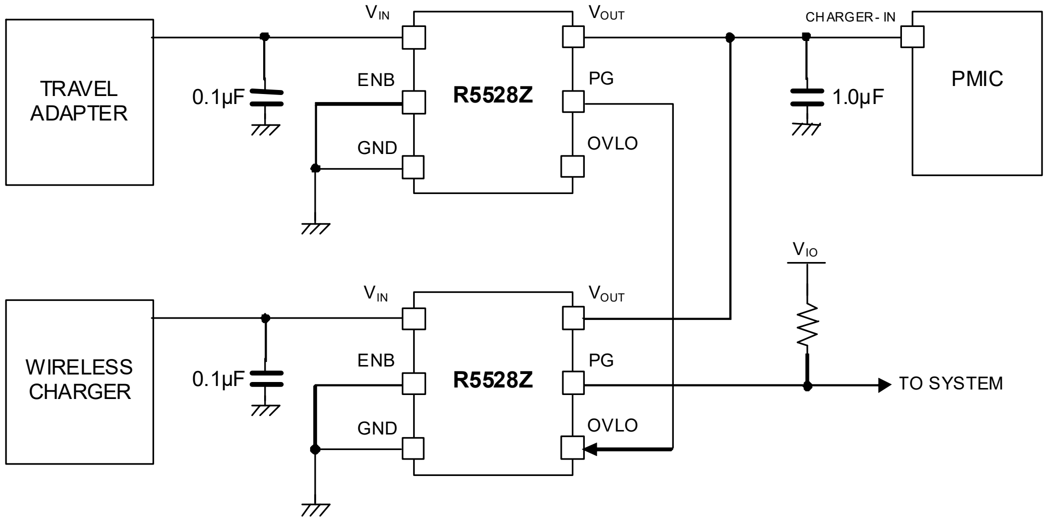


Figure 5. Typical Applications

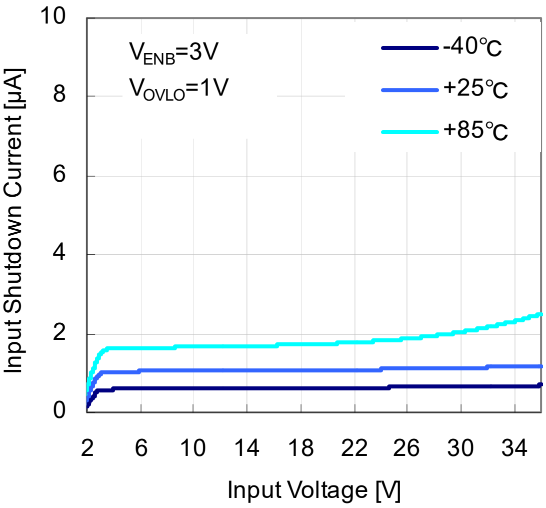
Technical Notes

The R5528Z001A does not require any bypass capacitor between V_{IN} and GND. However, connecting a 0.1µF or more capacitor between V_{IN} and GND may improve the performance against the noise.

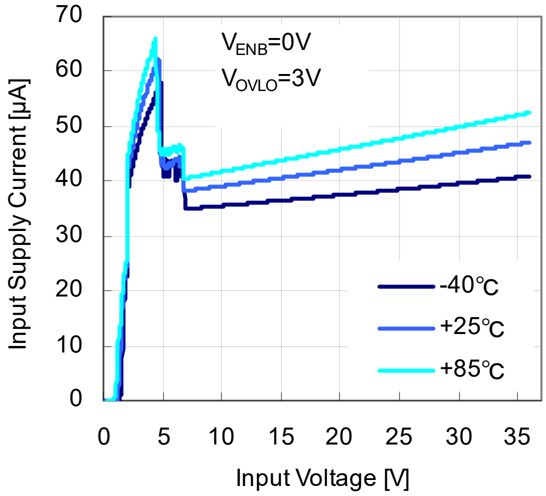
If there's any possibility of generating spike noise due to the parasitic element (inductance) of V_{IN}, connect an appropriate-sized capacitor between V_{IN} and GND.

TYPICAL CHARACTERISTIC

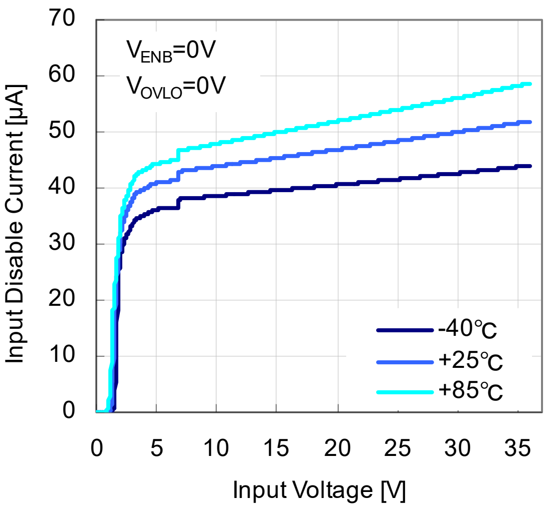
1) Input Shutdown Current VS. Input Voltage
R5528Z001A



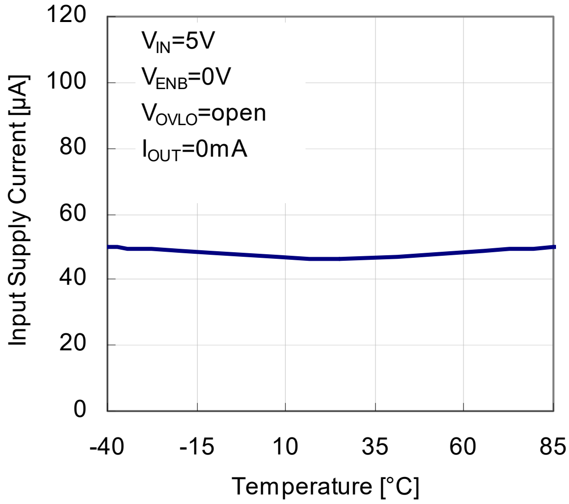
2) Input Supply Current VS. Input Voltage
R5528Z001A



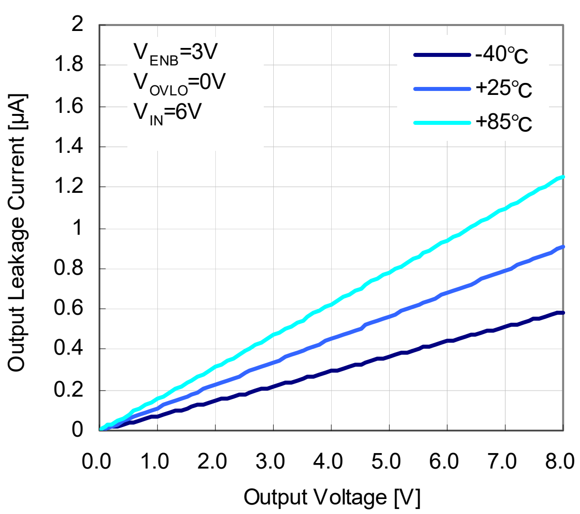
3) Input Disable Current VS. Input Voltage
R5528Z001A



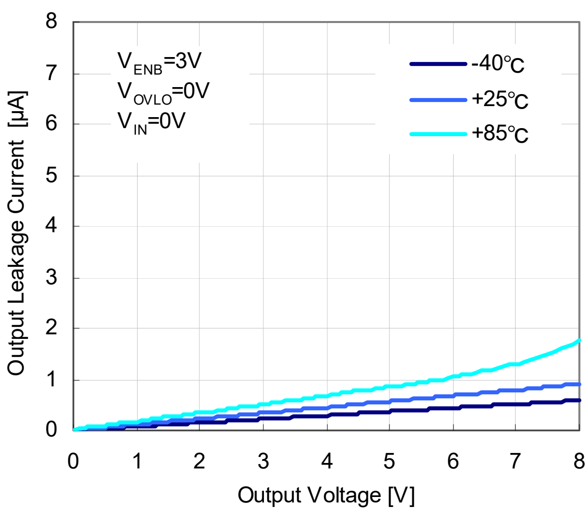
4) Input Supply Current VS. Temperature
R5528Z001A



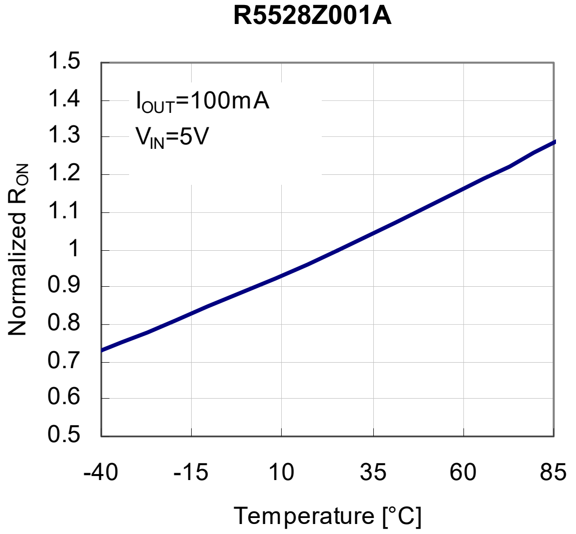
5) Output Leakage Current (6V) VS. Output Voltage
R5528Z001A



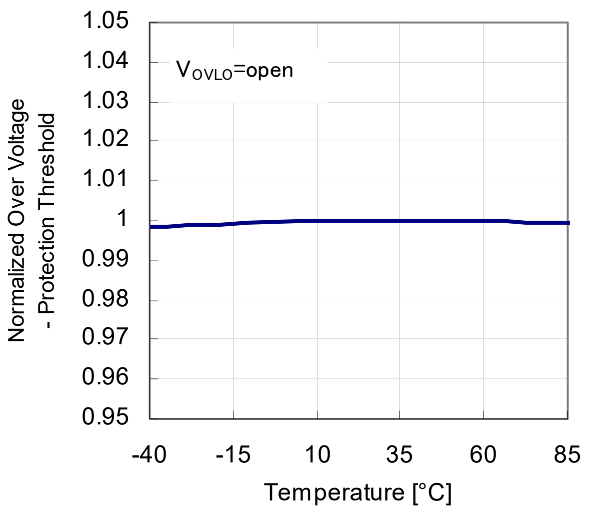
6) Output Leakage Current (0V) VS. Output Voltage
R5528Z001A



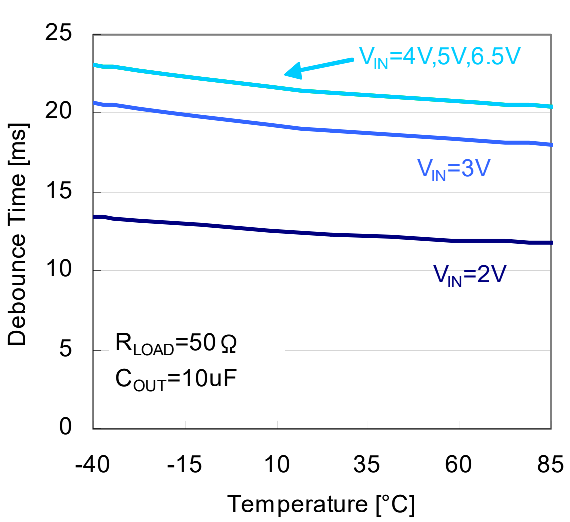
7) Normalized On-Resistance VS. Temperature



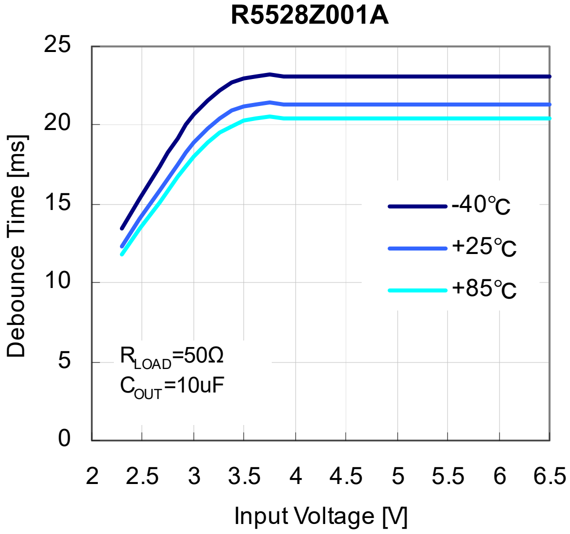
8) Normalized Overvoltage Protection Threshold (IN rising) VS. Temperature



9) Debounce Time VS. Temperature



10) Debounce Time VS. Input Voltage



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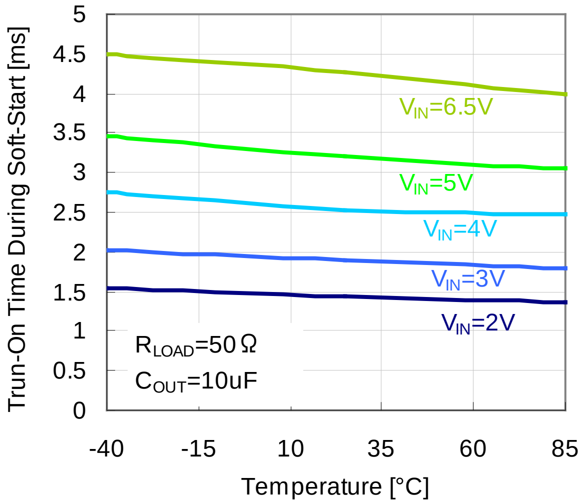
11) Trun-On Time VS. Temperature

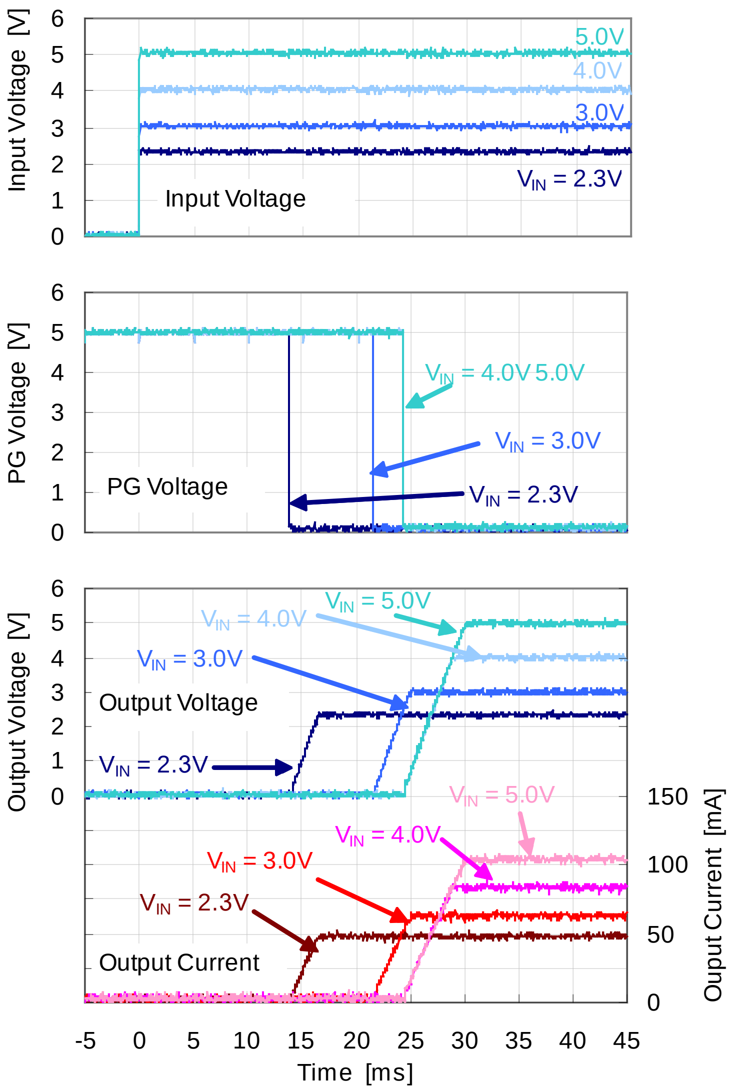
R5528Z001A



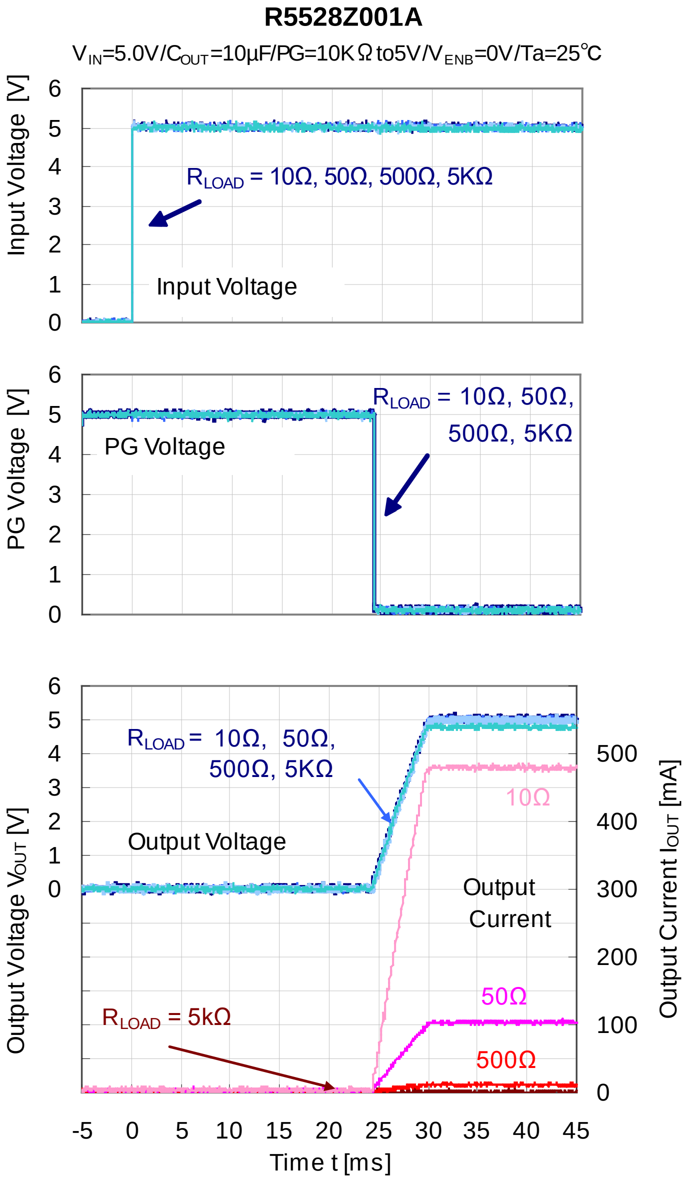
12) Power-Up Responce (V_{IN} = 2.3V/ 3.0V/ 4.0V/ 5.0V)

R5528Z001A

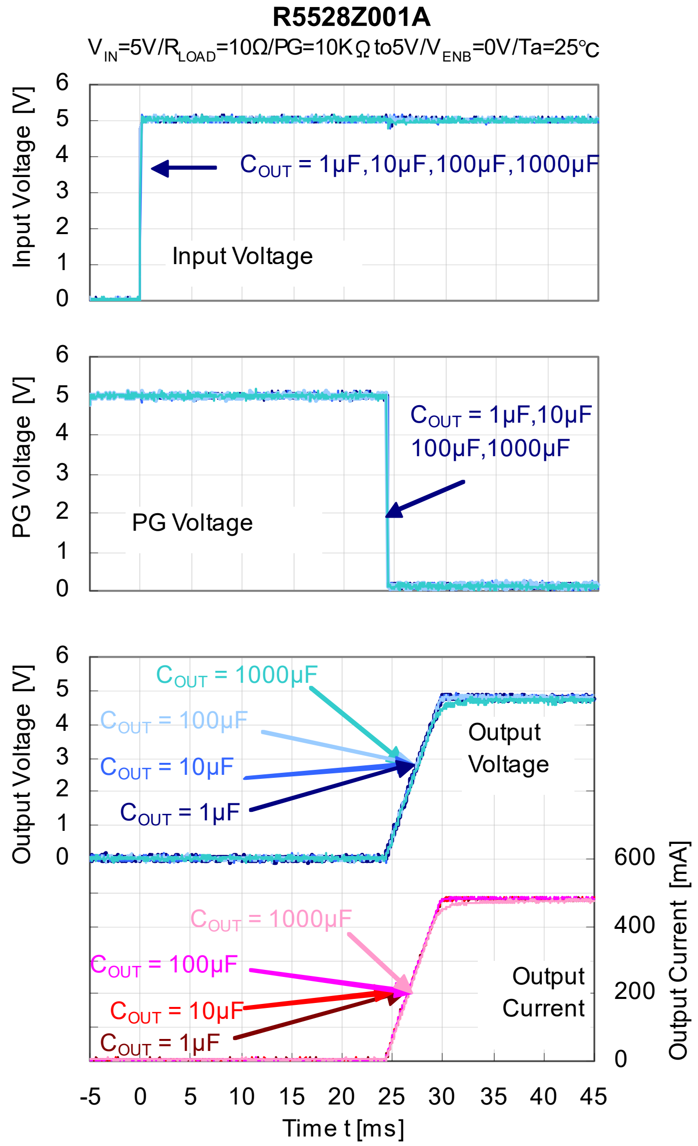
R_{LOAD}=50Ω/C_{OUT}=10µF/PG=10KΩto5V/V_{ENB}=0V/Ta=25°C



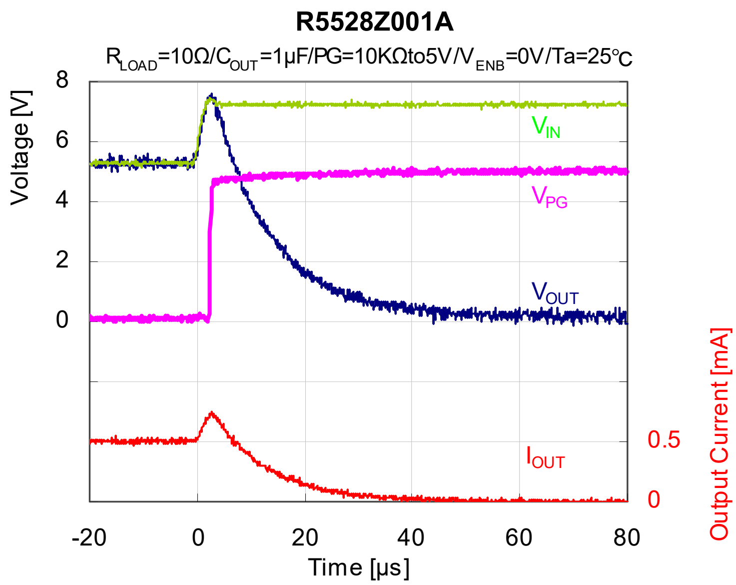
13) Power-Up Responce (R_{LOAD} = 10Ω/ 50Ω/ 500Ω/ 5KΩ)



14) Power-Up Responce (C_{OUT} = 1µF/ 10µF/ 100µF/ 1000µF)



15) Overvoltage Fault Response



Ver. A

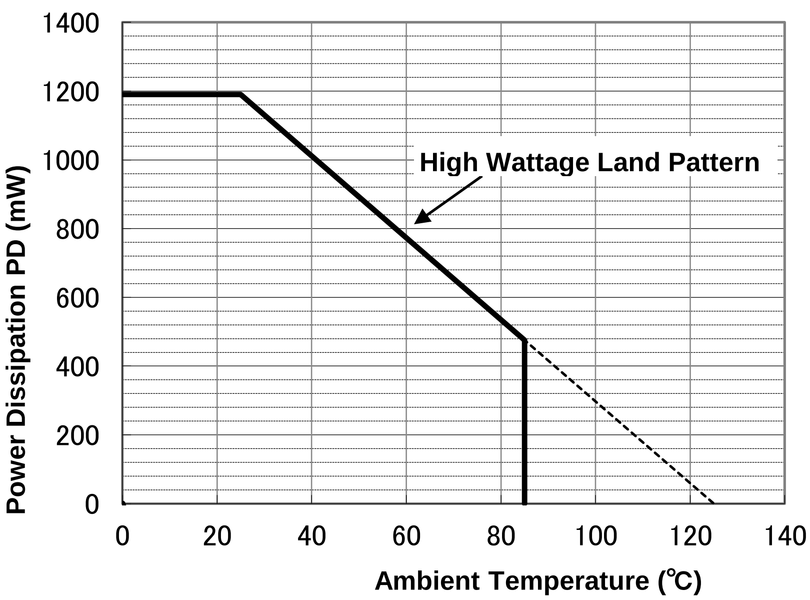
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

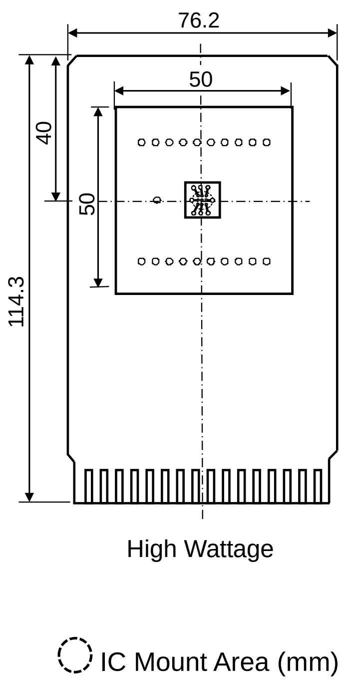
	High Wattage Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-layers)
Board Dimensions	76.2 mm × 114.3 mm × 1.6 mm
Copper Ratio	Outer Layers (First and Fourth Layers): Approx. 60% Inner Layers (Second and Third Layers): 100%

Measurement Result (Ta = 25°C, Tjmax = 125°C)

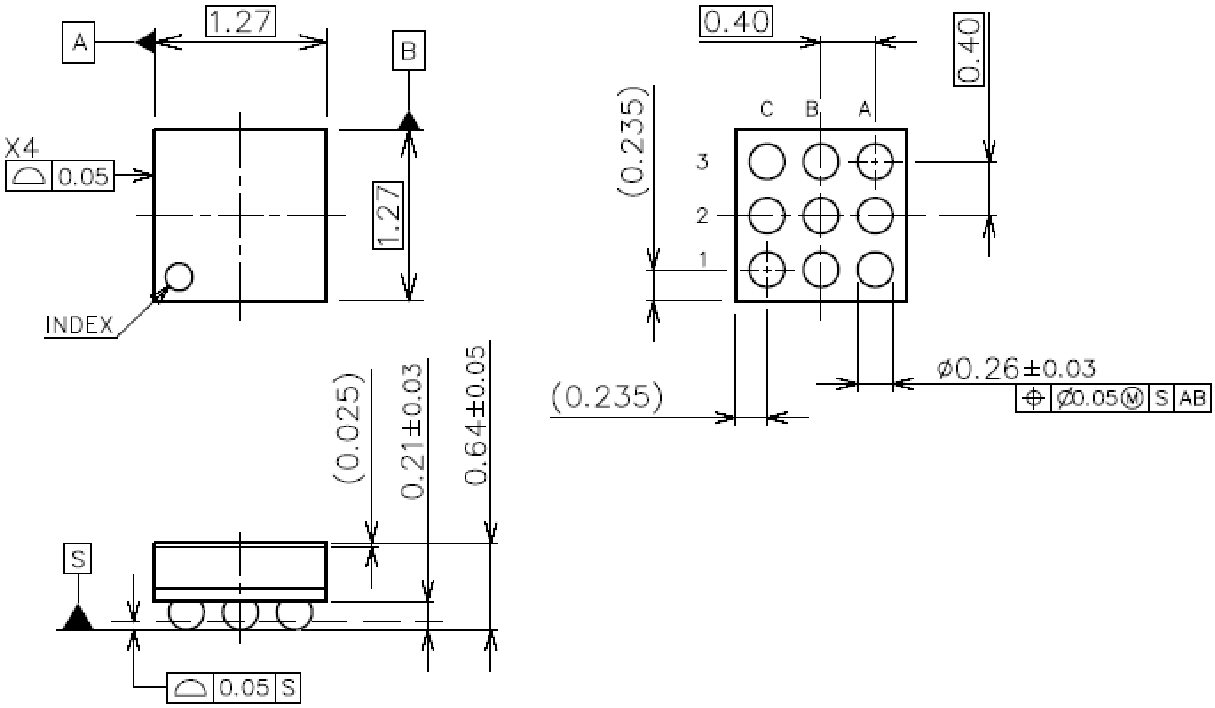
	High Wattage Land Pattern
Power Dissipation	1190 mW
Thermal Resistance	θja = (125 − 25°C) / 1.19 W = 84°C/W



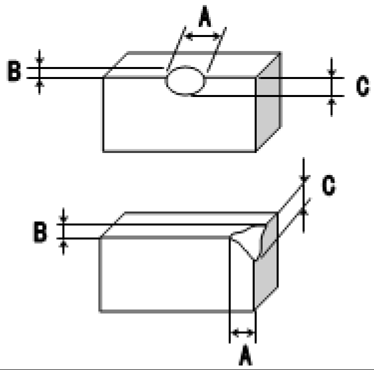
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



WLCSP-9-P1 Package Dimensions (Unit: mm)

No.	Inspection Items	Inspection Criteria	Figure
1	Package chipping	A≥0.2mm is rejected B≥0.2mm is rejected C≥0.2mm is rejected And, Package chipping to Si surface and to bump is rejected.	
2	Si surface chipping	A≥0.2mm is rejected B≥0.2mm is rejected C≥0.2mm is rejected But, even if A≥0.2mm, B≤0.1mm is acceptable.	
3	No bump	No bump is rejected.	
4	Marking miss	To reject incorrect marking, such as another product name marking or another lot No. marking.	
5	No marking	To reject no marking on the package.	
6	Reverse direction of marking	To reject reverse direction of marking character.	
7	Defective marking	To reject unreadable marking. (Microscope: X15/ White LED/ Viewed from vertical direction)	
8	Scratch	To reject unreadable marking character by scratch. (Microscope: X15/ White LED/ Viewed from vertical direction)	
9	Stain and Foreign material	To reject unreadable marking character by stain and foreign material. (Microscope: X15/ White LED/ Viewed from vertical direction)	

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