



Low-Voltage Single SPDT MICRO FOOT[®] Analog Switch

DESCRIPTION

The DG3000 is a single-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed (t_{ON} : 24 ns, t_{OFF} : 9 ns), low on-resistance ($R_{DS(on)}$: 1.4 Ω) and small physical size (MICRO FOOT, 6-bump), the DG3000 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG3000 is built on Vishay Siliconix's low voltage J12 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed for DG3000.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For MICRO FOOT analog switching products manufactured with tin/silver/copper (Sn/Ag/Cu) device terminations, the lead (Pb)-free "-E1" suffix is being used as a designator.

FEATURES

- MICRO FOOT[®] Chip Scale Package (1.07 x 1.57 mm)
- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - $R_{DS(on)}$: 1.4 Ω
- Fast Switching - t_{ON} : 24 ns, t_{OFF} : 9 ns
- Low Power Consumption
- TTL/CMOS Compatible



RoHS*
Available

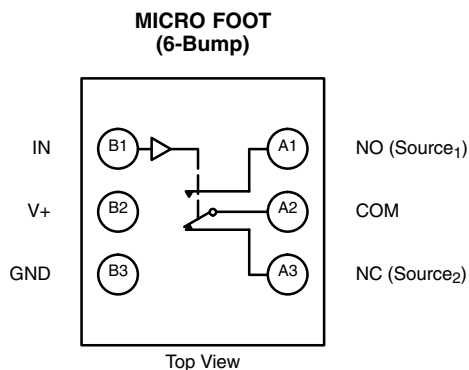
BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- PCM Cards
- PDA

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: 3000
xxx = Date/Lot Traceability Code

TRUTH TABLE

Logic	NC	NO
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 °C to 85 °C	MICRO FOOT: 6-Bump 3 x 2, 0.5 mm Pitch 165 μ m nom. bump height (Eutectic, SnPb)	DG3000DB-T1
	MICRO FOOT: 6-Bump 3 x 2, 0.5 mm pitch, 238 μ m nom. bump height (Lead (Pb)-free, Sn/Ag/Cu)	DG3000DB-T1-E1

* Pb containing terminations are not RoHS compliant, exemptions may apply.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Limit	Unit
Referenced V_+ to GND	- 0.3 to + 6 V	V
IN, COM, NC, NO ^a	- 0.3 V to ($V_+ + 0.3$ V)	
Continuous Current (Any Terminal)	± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)	± 200	
Storage Temperature (D Suffix)	- 65 to 150	$^\circ\text{C}$
Package Reflow Conditions^b		
VPR (Eutectic)	215	$^\circ\text{C}$
IR/Convection (Eutectic)	220	
IR/Convection (Lead (Pb)-free)	250	
Power Dissipation (Packages) ^c	6-Bump, 3 x 2 MICRO FOOT ^d	mW

Notes:

a. Signals on NC, NO, or COM or IN exceeding V_+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. Refer to IPC/JEDEC (J-STD-020A). No hand/manual solder rework recommended.

c. All bumps soldered to PC Board.

d. Derate 3.1 mW/ $^\circ\text{C}$ above 70°C .**SPECIFICATIONS ($V_+ = 2$ V)**

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2 V, ± 10 %, VIN = 0.4 V or 1.6 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 1.8 V, V _{COM} = 1 V, I _{NO} , I _{NC} = 10 mA	Room Full ^d		17	20 22.5	Ω
r _{ON} Flatness ^d	r _{ON} Flatness	V+ = 1.8 V, V _{COM} = 0 to V+, I _{NO} , I _{NC} = 10 mA	Room		14		
Switch Off Leakage Current ^f	I _{NO(off)} I _{NC(off)}	V+ = 2.2 V V _{NO} , V _{NC} = 0.5 V/1.5 V, V _{COM} = 1.5 V/0.5 V	Room Full ^d	- 700 - 11		700 11	pA nA
	I _{COM(off)}		Room Full ^d	- 700 - 11		700 11	pA nA
Channel-On Leakage Current ^f	I _{COM(on)}	V+ = 2.2 V, V _{NO} , V _{NC} = V _{COM} = 0.5 V/1.5 V	Room Full ^d	- 700 - 11		700 11	pA nA
Digital Control							
Input High Voltage	V _{INH}		Full	1.6			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Capacitance ^d	C _{in}		Full		5		pF
Input Current ^d	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 1.5 V, R _L = 300 Ω, C _L = 35 pF Figures 1 and 2	Room Full ^d		61	76 79	ns
Turn-Off Time	t _{OFF}		Room Full ^d		17	33 36	
Break-Before-Make Time	t _d		Room	1	45		
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 3	Room		2		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		- 61		dB
Crosstalk ^d	X _{TALK}		Room		- 67		
NO, NC Off Capacitance ^d	C _{NO(off)} C _{NC(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		31		pF
Channel-On Capacitance ^d	C _{ON}		Room		98		
Power Supply							
Power Supply Range	V+	V _{IN} = 0 or V+		1.8		2.2	V
Power Supply Current ^d	I+				0.1	1	μA
Power Consumption	P _C					2.2	μW



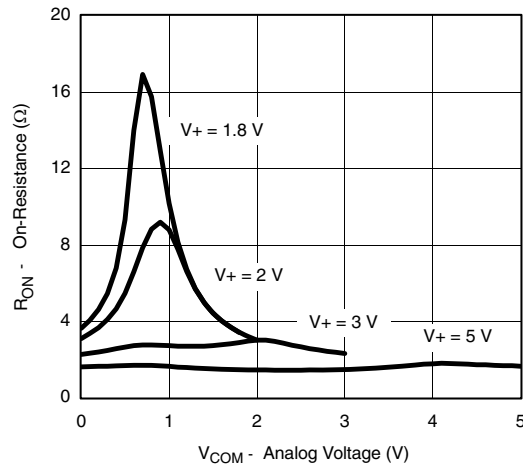
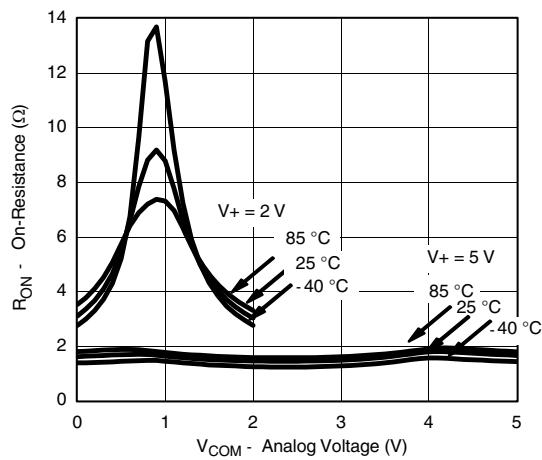
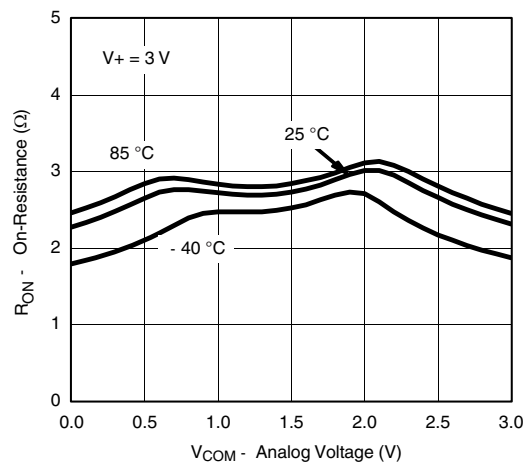
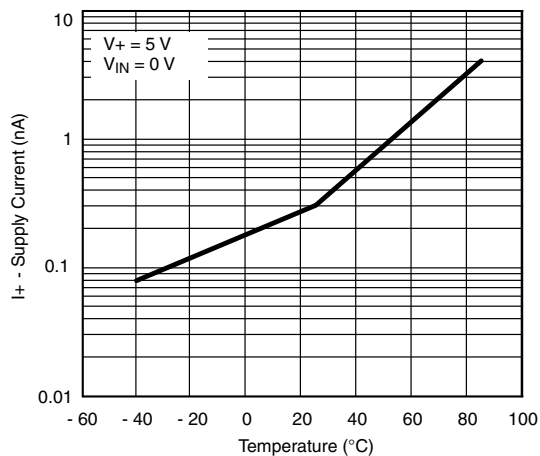
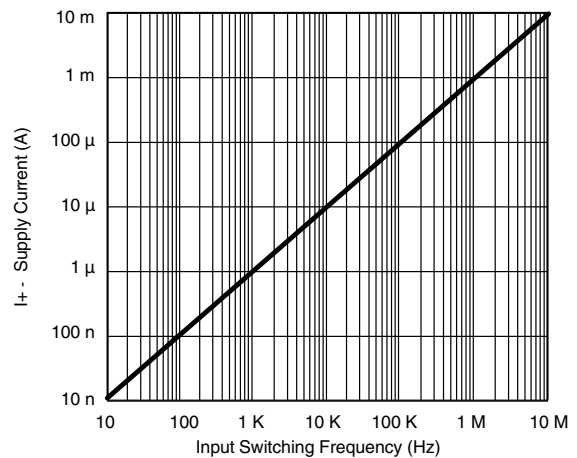
SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V _{IN} = 0.4 V or 2 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} V _{COM}		Full	0		V+	V
On-Resistance ^d	R _{ON}	V+ = 2.7 V, V _{COM} = 1.5 V, I _{NO} , I _{NC} = 10 mA	Room Full		3.3 3.4	4.1 4.2	Ω
R _{ON} Flatness ^d	R _{ON} Flatness	V+ = 2.7 V, V _{COM} = 0 to V+, I _{NO} , I _{NC} = 10 mA	Room		1.3		
Switch Off Leakage Current ^f	I _{NO(off)} I _{NC(off)}	V+ = 3.3 V V _{NO} , V _{NC} = 1 V/3 V, V _{COM} = 3 V/1 V	Room Full	- 800 - 13		800 13	pA nA
	I _{COM(off)}		Room Full	- 800 - 13		800 13	pA nA
Channel-On Leakage Current ^f	I _{COM(on)}	V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 1 V/3 V	Room Full	- 800 - 13		800 13	pA nA
Digital Control							
Input High Voltage	V _{INH}		Full	2			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Capacitance ^d	C _{in}		Full		5		pF
Input Current ^d	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	t _{ON}	V _{NO} or V _{NC} = 2 V, R _L = 300 Ω, C _L = 35 pF Figures 1 and 2	Room Full		34	49 52	ns
Turn-Off Time ^d	t _{OFF}		Room Full		12	30 33	
Break-Before-Make Time ^d	t _d		Room	1	23		
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 3	Room		4		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		- 61		dB
Crosstalk ^d	X _{TALK}		Room		- 67		
NO, NC Off Capacitance ^d	C _{NO(off)} C _{NC(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		31		pF
Channel-On Capacitance ^d	C _{ON}		Room		47		
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current ^d	I+	V _{IN} = 0 or V+			0.1	1	μA
Power Consumption	P _C					3.3	μW

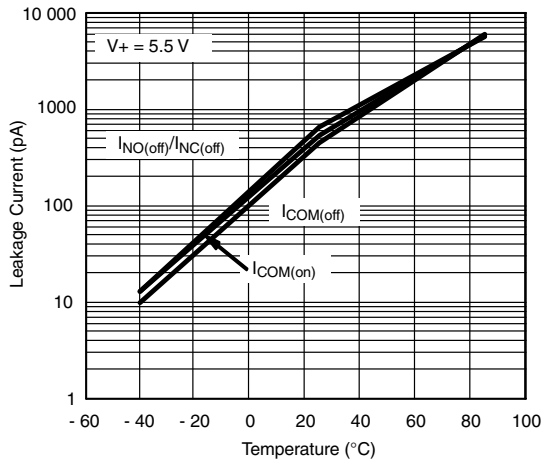
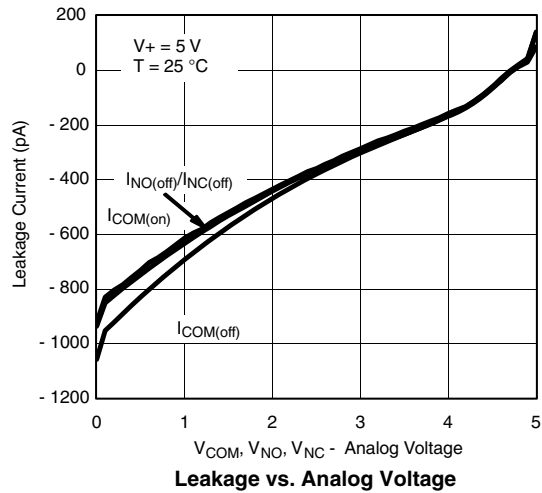
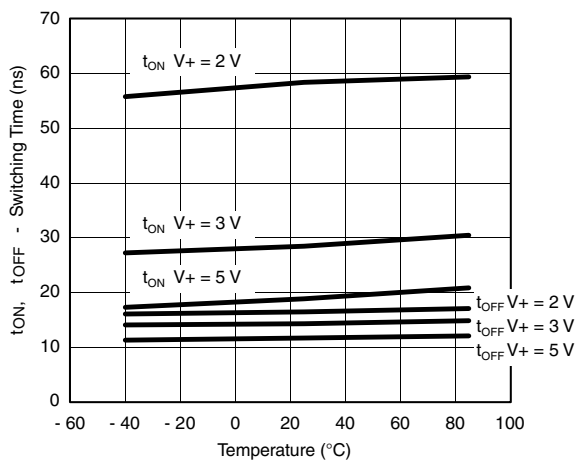
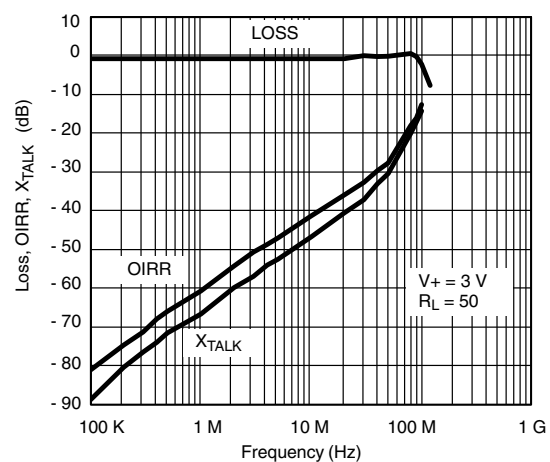
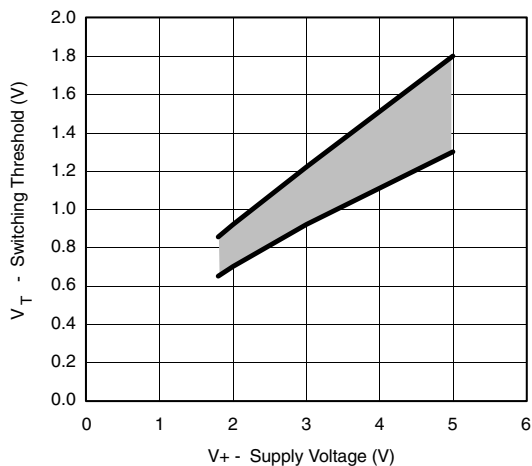
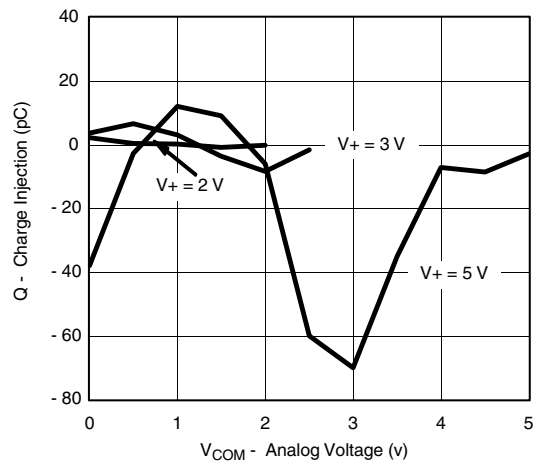
SPECIFICATIONS (V+ = 5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10 %, VIN = 0.8 V or 2.4 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Analog Switch							
Analog Signal Range ^d	VNO, VNC VCOM		Full	0		V+	V
On- Resistance	RON	V+ = 4.5 V, VCOM = 3 V, INO, INC = 10 mA	Room Full		1.4 1.6	2.3 2.8	Ω
RON Flatness ^d	RON Flatness	V+ = 4.5 V, VCOM = 0 to V+, INO, INC = 10 mA	Room		0.5		
Switch Off Leakage Current	INO(off) INC(off)	V+ = 5.5 V VNO, VNC = 1 V/4.5 V, VCOM = 4.5 V/1 V	Room Full	- 1.2 - 21		1.2 21	nA
	ICOM(off)		Room Full	- 1.2 - 21		1.2 21	
Channel-On Leakage Current	ICOM(on)	V+ = 5.5 V, V+ = 5.5 V VNO, VNC = VCOM = 1 V/4.5 V	Room Full	- 1.2 - 21		1.2 21	
Digital Control							
Input High Voltage	VINH		Full	2.4			V
Input Low Voltage	VINL		Full			0.8	
Input Capacitance	Cin		Full		5		pF
Input Current	IINL or IINH	VIN = 0 or V+	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	tON	VNO or VNC = 3 V, RL = 300 Ω, CL = 35 pF Figures 1 and 2	Room Full		24	36 39	ns
Turn-Off Time ^d	tOFF		Room Full		9	22 25	
Break-Before-Make Time ^d	td		Room	1	15		
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω, Figure 3	Room		38		pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		- 61		dB
Crosstalk ^d	XTALK		Room		- 67		
Source-Off Capacitance ^d	CNO(off) CNC(off)	VIN = 0 or V+, f = 1 MHz	Room		30		pF
Channel-On Capacitance ^d	CON		Room		96		
Power Supply							
Power Supply Range	V+			4.5		5.5	V
Power Supply Current	I+	VIN = 0 or V+			0.1	1	μA
Power Consumption	PC						5.5

Notes:

- Room = 25 °C, full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by 5 V leakage testing, not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted) **R_{ON} vs. V_{COM} and Supply Voltage** **R_{ON} vs. Analog Voltage and Temperature** **R_{ON} vs. Analog Voltage and Temperature****Supply Current vs. Temperature****Supply Current vs. Input Switching Frequency**

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Leakage Current vs. Temperature****Leakage vs. Analog Voltage****Switching Time vs. Temperature and Supply Voltage****Insertion Loss, Off-Isolation, Crosstalk vs. Frequency****Switching Threshold vs. Supply Voltage****Charge Injection vs. Analog Voltage**



TEST CIRCUITS

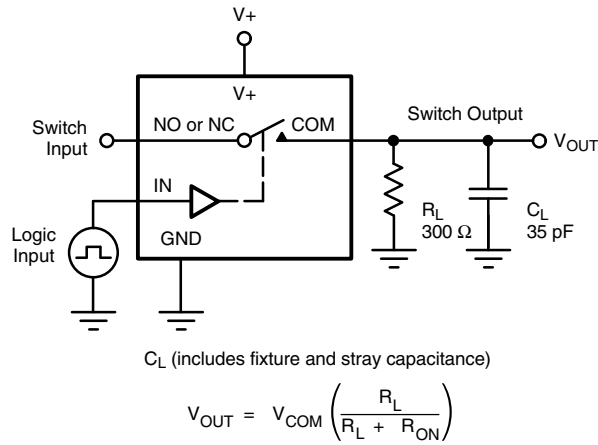
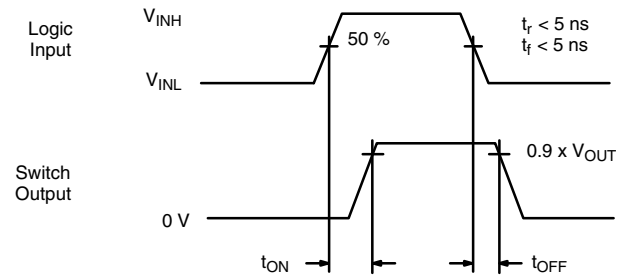


Figure 1. Switching Time



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

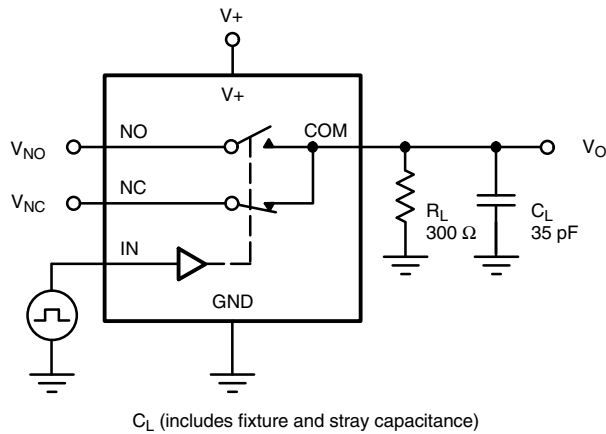


Figure 2. Break-Before-Make Interval

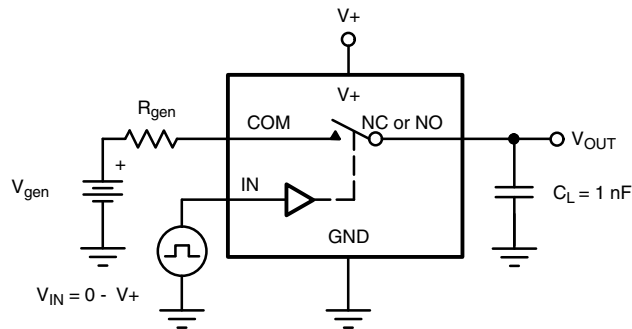
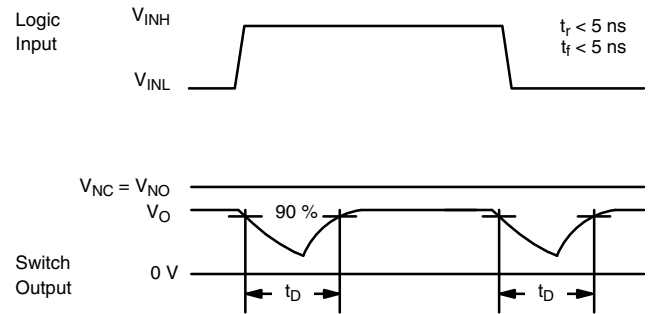
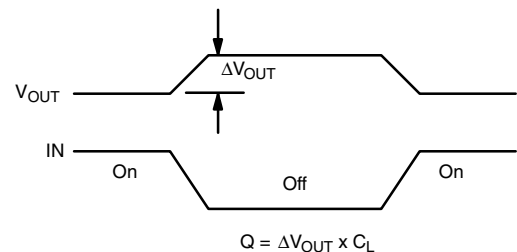


Figure 3. Charge Injection



IN depends on switch configuration: input polarity determined by sense of switch.

TEST CIRCUITS

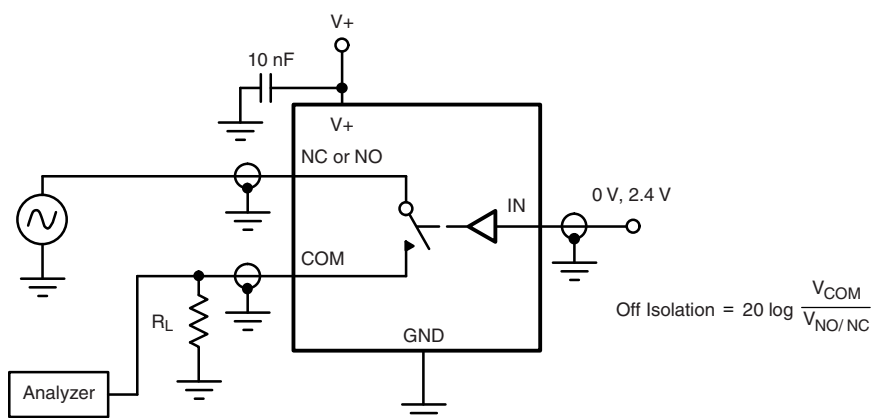


Figure 4. Off-Isolation

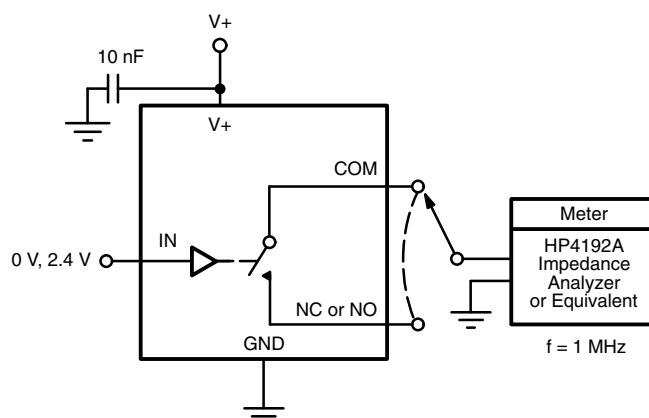
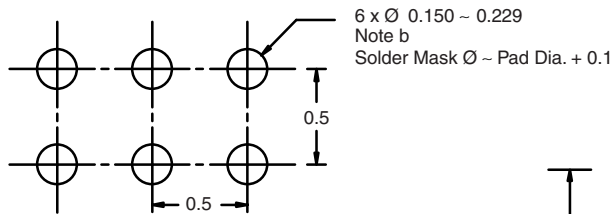


Figure 5. Channel Off/On Capacitance

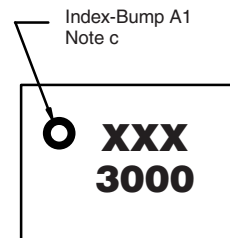


PACKAGE OUTLINE

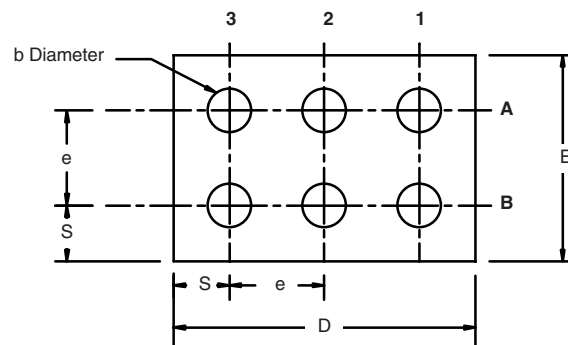
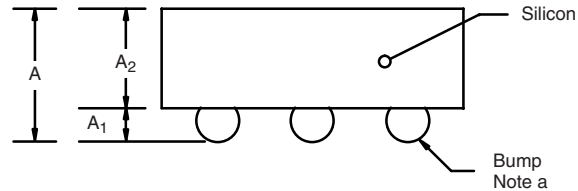
MICRO FOOT: 6-BUMP (3 x 2, 0.5 mm PITCH)



Recommended Land Pattern



Top Side (Die Back)



Notes (Unless Otherwise Specified):

- a. Bump is Eutectic 63/57 Sn/Pb or Lead (Pb)-free Sn/Ag/Cu.
- b. Non-solder mask defined copper landing pad.
- c. Laser Mark on silicon die back; no coating. Shown is not actual marking; sample only.

EUTECTIC (Sn/Pb)				
Dim.	Millimeters ^a		Inches	
	Min.	Max.	Min.	Max.
A	0.615	0.715	0.0242	0.0281
A ₁	0.140	0.190	0.0055	0.0075
A ₂	0.470	0.495	0.0185	0.0195
b	0.180	0.250	0.0071	0.0098
D	1.555	1.585	0.0612	0.0624
E	1.055	1.085	0.0415	0.0427
e	0.5 BASIC		0.0197 BASIC	
S	0.278	0.293	0.0109	0.0115

Notes:

- a. Use millimeters as the primary measurement.

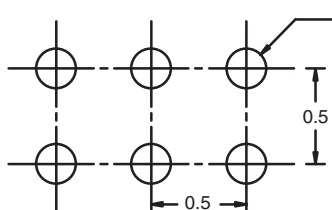
LEAD (Pb)-FREE (Sn/Ag/Cu)				
Dim.	Millimeters ^a		Inches	
	Min.	Max.	Min.	Max.
A	0.688	0.753	0.0271	0.0296
A ₁	0.218	0.258	0.0086	0.0102
A ₂	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.555	1.585	0.0612	0.0624
E	1.055	1.085	0.0415	0.0427
e	0.5 BASIC		0.0197 BASIC	
S	0.278	0.293	0.0109	0.0115

Notes:

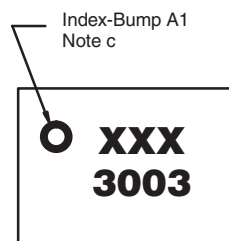
- a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71742.

MICRO FOOT: 6-BUMP (3 mm x 2 mm, 0.5 mm PITCH, 165 µm BUMP HEIGHT)

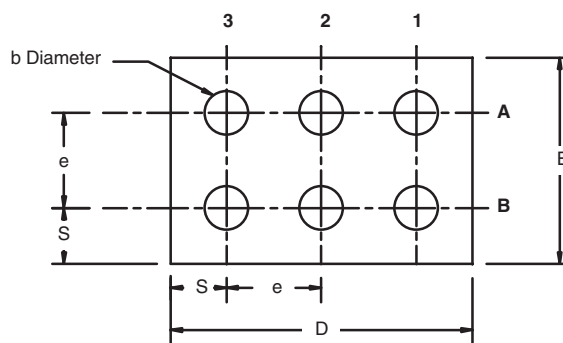
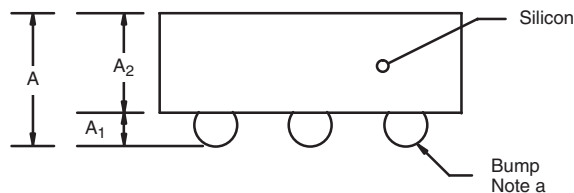


Recommended Land Pattern



Top Side (Die Back)

6 x $\varnothing$ 0.150 $\square$ 0.229
Note b
Solder Mask $\varnothing$ $\square$ Pad Dia. + 0.1



Notes

(unless otherwise specified)

- Bump is Eutectic 63/57 Sn/Pb or lead (Pb)-free Sn/Ag/Cu.
- Non-solder mask defined copper landing pad.
- Laser mark on silicon die back; no coating. Shown is not actual marking; sample only.

EUTECTIC (Sn/Pb)				
DIM.	MILLIMETERS ^a		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.610	0.685	0.0240	0.0270
A ₁	0.140	0.190	0.0055	0.0075
A ₂	0.470	0.495	0.0185	0.0195
b	0.180	0.250	0.0071	0.0098
D	1.490	1.515	0.0587	0.0596
E	0.990	1.015	0.0390	0.0400
e	0.5 BASIC		0.0197 BASIC	
S	0.245	0.258	0.0096	0.0101

Note

- Use millimeters as the primary measurement.

LEAD (Pb)-FREE (Sn/Ag/Cu)				
DIM.	MILLIMETERS ^a		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.688	0.753	0.0271	0.0296
A ₁	0.218	0.258	0.0086	0.0102
A ₂	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.490	1.515	0.0587	0.0596
E	0.990	1.015	0.0390	0.0400
e	0.5 BASIC		0.0197 BASIC	
S	0.245	0.258	0.0096	0.0101

Note

- Use millimeters as the primary measurement.

ECN: S11-1065-Rev. A, 13-Jun-11
DWG: 6003

PCB Design and Assembly Guidelines For MICRO FOOT® Products

Johnson Zhao

INTRODUCTION

Vishay Siliconix's MICRO FOOT product family is based on a wafer-level chip-scale packaging (WL-CSP) technology that implements a solder bump process to eliminate the need for an outer package to encase the silicon die. MICRO FOOT products include power MOSFETs, analog switches, and power ICs.

For battery powered compact devices, this new packaging technology reduces board space requirements, improves thermal performance, and mitigates the parasitic effect typical of leaded packaged products. For example, the 6-bump MICRO FOOT Si8902EDB common drain power MOSFET, which measures just 1.6 mm x 2.4 mm, achieves the same performance as TSSOP-8 devices in a footprint that is 80% smaller and with a 50% lower height profile (Figure 1). A MICRO FOOT analog switch, the 6-bump DG3000DB, offers low charge injection and 1.4 W on-resistance in a footprint measuring just 1.08 mm x 1.58 mm (Figure 2).

Vishay Siliconix MICRO FOOT products can be handled with the same process techniques used for high-volume assembly of packaged surface-mount devices. With proper attention to PCB and stencil design, the device will achieve reliable performance without underfill. The advantage of the device's small footprint and short thermal path make it an ideal option for space-constrained applications in portable devices such as battery packs, PDAs, cellular phones, and notebook computers.

This application note discusses the mechanical design and reliability of MICRO FOOT, and then provides guidelines for board layout, the assembly process, and the PCB rework process.

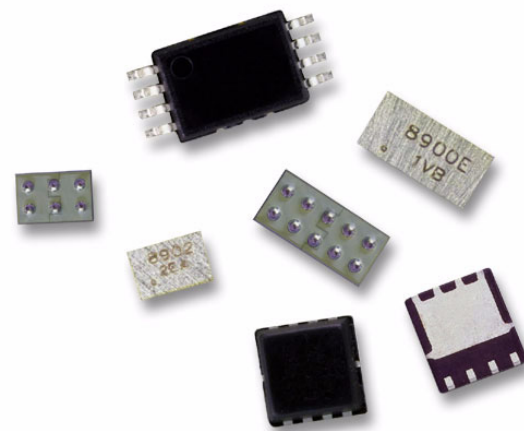


FIGURE 1. 3D View of MICRO FOOT Products Si8902EDB and Si8900EDB

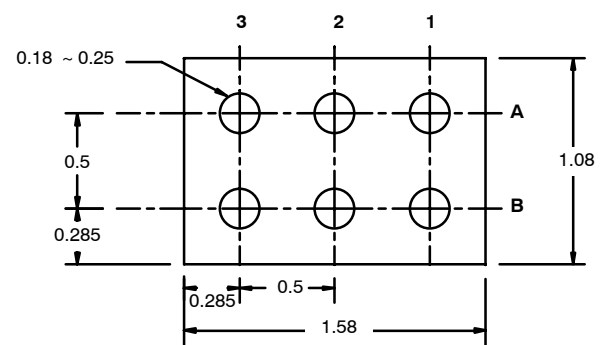


FIGURE 2. Outline of MICRO FOOT CSP & Analog Switch DG3000DB

TABLE 1
Main Parameters of Solder Bumps in MICRO FOOT Designs

MICRO FOOT CSP	Bump Material	Bump Pitch*	Bump Diameter*	Bump Height*
MICRO FOOT CSP MOSFET	Eutectic Solder: 63Sn/37Pb	0.8	0.37-0.41	0.26-0.29
MICRO FOOT CSP Analog Switch		0.5	0.18-0.25	0.14-0.19
MICRO FOOT UCSP Analog Switch		0.5	0.32-0.34	0.21-0.24

* All measurements in millimeters

MICRO FOOT'S DESIGN AND RELIABILITY

As a mechanical, electrical, and thermal connection between the device and PCB, the solder bumps of MICRO FOOT products are mounted on the top active surface of the die. Table 1 shows the main parameters for solder bumps used in MICRO FOOT products. A silicon nitride passivation layer is applied to the active area as the last masking process in fabrication, ensuring that the device passes the pressure pot test. A green laser is used to mark the backside of the die without damaging it. Reliability results for MICRO FOOT products mounted on a FR-4 board without underfill are shown in Table 2.

TABLE 2
MICRO FOOT Reliability Results

Test Condition C: -65° to 150°C	>500 Cycles
Test condition B: -40° to 125°C	>1000 Cycles
121°C @ 15PSI 100% Humidity Test	96 Hours

The main failure mechanism associated with wafer-level chip-scale packaging is fatigue of the solder joint. The results shown in Table 2 demonstrate that a high level of reliability can be achieved with proper board design and assembly techniques.

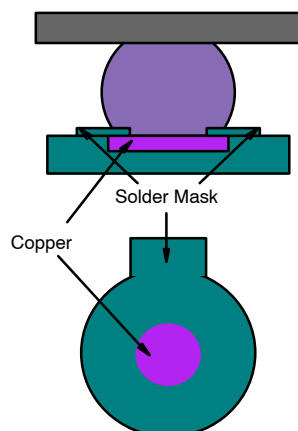


FIGURE 3. SMD

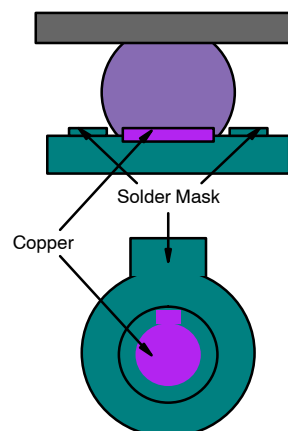


FIGURE 4. NSMD

BOARD LAYOUT GUIDELINES

Board materials. Vishay Siliconix MICRO FOOT products are designed to be reliable on most board types, including organic boards such as FR-4 or polyamide boards. The package qualification information is based on the test on 0.5-oz. FR-4 and polyamide boards with NSMD pad design.

Land patterns. Two types of land patterns are used for surface-mount packages. Solder mask defined (SMD) pads have a solder mask opening smaller than the metal pad (Figure 3), whereas on-solder mask defined (NSMD) pads have a metal pad smaller than the solder-mask opening (Figure 4).

NSMD is recommended for copper etch processes, since it provides a higher level of control compared to SMD etch processes. A small-size NSMD pad definition provides more area (both lateral and vertical) for soldering and more room for escape routing on the PCB. By contrast, SMD pad definition introduces a stress-concentration point near the solder mask on the PCB side that may result in solder joint cracking under extreme fatigue conditions.

Copper pads should be finished with an organic solderability preservative (OSP) coating. For electroplated nickel-immersion gold finish pads, the gold thickness must be less than 0.5 μm to avoid solder joint embrittlement.

Board pad design. The landing-pad size for MICRO FOOT products is determined by the bump pitch as shown in Table 3. The pad pattern is circular to ensure a symmetric, barrel-shaped solder bump.

TABLE 3 Dimensions of Copper Pad and Solder Mask Opening in PCB and Stencil Aperture			
Pitch	Copper Pad	Solder Mask Opening	Stencil Aperture
0.80 mm	0.30 ± 0.01 mm	0.41 ± 0.01 mm	0.33 ± 0.01 mm in circle aperture
0.50 mm	0.17 ± 0.01 mm	0.27 ± 0.01 mm	0.30 ± 0.01 mm in square aperture

ASSEMBLY PROCESS

MICRO FOOT products' surface-mount-assembly operations include solder paste printing, component placement, and solder reflow as shown in the process flow chart (Figure 5).

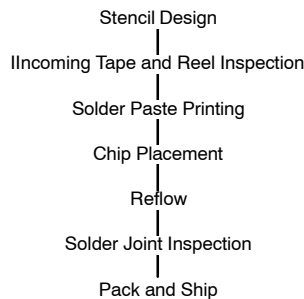


FIGURE 5. SMT Assembly Process Flow

Stencil design. Stencil design is the key to ensuring maximum solder paste deposition without compromising the assembly yield from solder joint defects (such as bridging and extraneous solder spheres). The stencil aperture is dependent on the copper pad size, the solder mask opening, and the quantity of solder paste.

In MICRO FOOT products, the stencil is 0.125-mm (5-mils) thick. The recommended apertures are shown in Table 3 and are fabricated by laser cut.

Solder-paste printing. The solder-paste printing process involves transferring solder paste through pre-defined apertures via application of pressure.

In MICRO FOOT products, the solder paste used is UP78 No-clean eutectic 63 Sn/37Pb type3 or finer solder paste.

Chip pick-and-placement. MICRO FOOT products can be picked and placed with standard pick-and-place equipment. The recommended pick-and-place force is 150 g. Though the part will self-center during solder reflow, the maximum placement offset is 0.02 mm.

Reflow Process. MICRO FOOT products can be assembled using standard SMT reflow processes. Similar to any other package, the thermal profile at specific board locations must be determined. Nitrogen purge is recommended during reflow operation. Figure 6 shows a typical reflow profile.

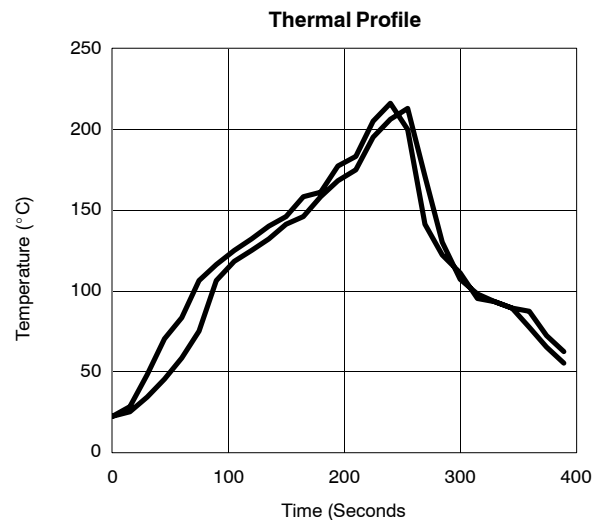


FIGURE 6. Reflow Profile

PCB REWORK

To replace MICRO FOOT products on PCB, the rework procedure is much like the rework process for a standard BGA or CSP, as long as the rework process duplicates the original reflow profile. The key steps are as follows:

1. Remove the MICRO FOOT device using a convection nozzle to create localized heating similar to the original reflow profile. Preheat from the bottom.
2. Once the nozzle temperature is +190°C, use tweezers to remove the part to be replaced.
3. Resurface the pads using a temperature-controlled soldering iron.
4. Apply gel flux to the pad.
5. Use a vacuum needle pick-up tip to pick up the replacement part, and use a placement jig to place it accurately.
6. Reflow the part using the same convection nozzle, and preheat from the bottom, matching the original reflow profile.



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