3 GHz Variable Gain LNA with Integrated ½ W Driver Amplifier

Data Sheet

ADL5246

FEATURES

RF output frequency range: 0.6 GHz to 3 GHz
Output IP3: 37 dBm at 2.2 GHz
Output P1dB: 28 dBm at 2.2 GHz
Noise figure of input amplifier: 1 dB at 2.2 GHz
Maximum gain: 31.5 dB at 2.2 GHz
Voltage variable attenuation range: 45 dB
0 V to 3.3 V attenuation control range
Integrated bypass switch for low noise VGA
Matched 50 Ω input stage
3.3 V to 5 V single supply
32-lead, 5 mm × 5 mm LFCSP package

APPLICATIONS

Multistandard radio receivers
Point to point Rx and Tx
Instrumentation
Military and aerospace

GENERAL DESCRIPTION

The ADL5246 is a high performance, low noise variable gain amplifier (VGA) optimized for multistandard base station receivers and point to point receive (Rx) and transmit (Tx) applications. The low noise figure and excellent linearity performance allow the device to be used in a variety of applications.

The device consists of a low noise amplifier, a high linearity VGA, and a ½ W output driver stage. The variable attenuator networks are optimized to provide high linearity performance over the 45 dB gain control range. Gain is set using a unipolar control voltage from 0 V to 3.3 V. The output stage of the ADL5246 is an externally tuned ½ W driver amplifier, which allows the device to be optimized anywhere between the 0.6 GHz to 3 GHz range, with an average tuning bandwidth of 200 MHz wide. An external filter can be used between the VGA and the final driver amplifier. The ADL5246 can be biased between 3.3 V and 5 V to trade off between performance and power consumption.

The ADL5246 is fabricated on an advanced GaAs process. The device is available in a 32-lead, RoHS compliant, 5 mm × 5 mm LFCSP and thermally rated to operate over the −40°C to +105°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

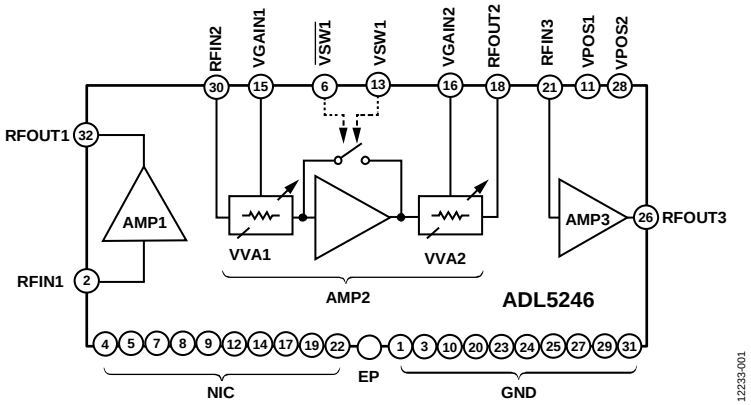

Figure 1.

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REVISION HISTORY

9/15—Rev. 0 to Rev. A

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Added Figure 21 to Figure 26; Renumbered Sequentially ... 13
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Changes to Figure 57, Figure 58, Figure 59 ... 19
Changes to Full Chain Operation Considerations Section ... 28

4/14—Revision 0: Initial Version

SPECIFICATIONS

V_{POS} = 5 V, T_A = 25°C, unless otherwise noted. Amplifier 1 = AMP1, Amplifier 2 = AMP2, and Amplifier 3 = AMP3.

Table 1.

		3.3 V			5 V			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
OVERALL FUNCTION								
Frequency Range		0.6		3	0.6		3	GHz
AMP1 FREQUENCY = 0.75 GHz	RFIN1 and RFOUT1 pins							
Gain			19.5			20		dB
vs. Frequency	±50 MHz		±0.3			±0.3		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		±0.6			±0.5		dB
vs. Supply	3.135 V to 3.465 V, 4.75 V to 5.25 V		±0.1			±0.05		dB
Input Return Loss	S11		−21			−22		dB
Output Return Loss	S22		−9			−9		dB
Output 1 dB Compression Point			18.5			21.5		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 0 dBm/tone		31			34.5		dBm
Noise Figure			1.4			1.5		dB
AMP1 FREQUENCY = 0.9 GHz	RFIN1 and RFOUT1 pins							
Gain			19			18.5		dB
vs. Frequency	±50 MHz		±0.4			±0.4		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		±0.5			±0.5		dB
vs. Supply	3.135 V to 3.465 V, 4.75 V to 5.25 V		±0.1			±0.05		dB
Input Return Loss	S11		−21			−24		dB
Output Return Loss	S22		−11			−10		dB
Output 1 dB Compression Point			19			22		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 0 dBm/tone		32			35		dBm
Noise Figure			0.9			1.2		dB
AMP1 FREQUENCY = 1.5 GHz	RFIN1 and RFOUT1 pins							
Gain			15			14.5		dB
vs. Frequency	±100 MHz		±0.7			±0.4		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		±0.4			±0.5		dB
vs. Supply	3.135 V to 3.465 V, 4.75 V to 5.25 V		±0.1			±0.1		dB
Input Return Loss	S11		−14.5			−16		dB
Output Return Loss	S22		−14			−12		dB
Output 1 dB Compression Point			19			22.5		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 0 dBm/tone		33			37		dBm
Noise Figure			0.8			0.85		dB
AMP1 FREQUENCY = 1.9 GHz	RFIN1 and RFOUT1 pins							
Gain			12.5			13		dB
vs. Frequency	±100 MHz		±0.5			±0.5		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		±0.5			±0.5		dB
vs. Supply	3.135 V to 3.465 V, 4.75 V to 5.25 V		±0.1			±0.05		dB
Input Return Loss	S11		−13			−14		dB
Output Return Loss	S22		−14			−12		dB
Output 1 dB Compression Point			19			22.5		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 0 dBm/tone		34			37.5		dBm
Noise Figure			0.9			0.9		dB

Parameter	Test Conditions/Comments	3.3 V Min	3.3 V Typ	3.3 V Max	5 V Min	5 V Typ	5 V Max	Unit
AMP1 FREQUENCY = 2.2 GHz	RFIN1 and RFOUT1 pins							
Gain			11			11.5		dB
vs. Frequency	±100 MHz		±0.5			±0.5		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		±0.5			±0.5		dB
vs. Supply	3.135 V to 3.465 V, 4.75 V to 5.25 V		±0.05			±0.05		dB
Input Return Loss	S11		−11			−12		dB
Output Return Loss	S22		−15			−12		dB
Output 1 dB Compression Point			19			22.3		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 0 dBm/tone		34			37.5		dBm
Noise Figure			1			1		dB
AMP1 FREQUENCY = 2.6 GHz	RFIN1 and RFOUT1 pins							
Gain			10			10		dB
vs. Frequency	±100 MHz		±0.4			±0.5		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		±0.4			±0.5		dB
vs. Supply	3.135 V to 3.465 V, 4.75 V to 5.25 V		±0.05			±0.05		dB
Input Return Loss	S11		−10			−11		dB
Output Return Loss	S22		−17			−13		dB
Output 1 dB Compression Point			19.5			22.5		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 0 dBm/tone		34			37.4		dBm
Noise Figure			1.2			1.2		dB
AMP2 FREQUENCY = 0.75 GHz	RFIN2 to RFOUT2 at maximum gain							
Gain			12.5			16		dB
vs. Frequency	±50 MHz		±0.4			±0.4		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		+3 to −4			+0.5 to −2		dB
Gain Range	HG mode		15			60		dB
Input Return Loss			−10			−9		dB
Output Return Loss			−29			−16		dB
Input 1 dB Compression Point			2			4.5		dBm
Input Third Order Intercept	Δf = 1 MHz, P_{IN} = −5 dBm/tone		13			15		dBm
Noise Figure			4.5			3.5		dB
AMP2 FREQUENCY = 0.9 GHz	RFIN2 to RFOUT2 at maximum gain							
Gain			11.5			14.5		dB
vs. Frequency	±50 MHz		±0.5			±0.5		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		+2.5 to −4			+0.5 to −2		dB
Gain Range	HG mode		15			60		dB
Input Return Loss			−9.5			−9		dB
Output Return Loss			−21			−15		dB
Input 1 dB Compression Point			3.5			5.5		dBm
Input Third Order Intercept	Δf = 1 MHz, P_{IN} = −5 dBm/tone		14			15.5		dBm
Noise Figure			4.2			3.2		dB

Parameter	Test Conditions/Comments	3.3 V Min	3.3 V Typ	3.3 V Max	5 V Min	5 V Typ	5 V Max	Unit
AMP2 FREQUENCY = 1.5 GHz	RFIN2 to RFOUT2 at maximum gain							
Gain			7.5			10		dB
vs. Frequency	±100 MHz		±0.6			±0.7		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		+2.5 to −4			+0.5 to −2		dB
Gain Range	HG mode		14.5			50		dB
Input Return Loss			−9			−10		dB
Output Return Loss			−12			−10		dB
Input 1 dB Compression Point			7			8		dBm
Input Third Order Intercept	Δf = 1 MHz, P_{IN} = −5 dBm/tone		18.5			19.5		dBm
Noise Figure			4.2			3.2		dB
AMP2 FREQUENCY = 1.9 GHz	RFIN2 to RFOUT2 at maximum gain							
Gain			5			7.5		dB
vs. Frequency	±100 MHz		±0.6			±0.6		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		+2.5 to −4			+0.5 to −2		dB
Gain Range	HG mode		14			48		dB
Input Return Loss			−9			−10		dB
Output Return Loss			−10			−8		dB
Input 1 dB Compression Point			9			10		dBm
Input Third Order Intercept	Δf = 1 MHz, P_{IN} = −5 dBm/tone		20.5			21.5		dBm
Noise Figure			4.6			3.6		dB
AMP2 FREQUENCY = 2.2 GHz	RFIN2 to RFOUT2 at maximum gain							
Gain			3.5			5.5		dB
vs. Frequency	±100 MHz		±0.5			±0.5		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		+2 to −3			+0.5 to −2		dB
Gain Range	HG mode		13.5			45		dB
Input Return Loss			−9			−10		dB
Output Return Loss			−8			−7		dB
Input 1 dB Compression Point			11			11		dBm
Input Third Order Intercept	Δf = 1 MHz, P_{IN} = −5 dBm/tone		22.5			23		dBm
Noise Figure			5.1			4.2		dB
AMP2 FREQUENCY = 2.6 GHz	RFIN2 to RFOUT2 at maximum gain							
Gain			1.5			3.7		dB
vs. Frequency	±100 MHz		±0.5			±0.5		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		+2 to −3			+0.3 to −3		dB
Gain Range	HG mode		13			42		dB
Input Return Loss			−9			−10		dB
Output Return Loss			−7.5			−6.5		dB
Input 1 dB Compression Point			14			13.5		dBm
Input Third Order Intercept	Δf = 1 MHz, P_{IN} = −5 dBm/tone		24			24.5		dBm
Noise Figure			5.3			4.3		dB
AMP2 GAIN SETTLING, 0.9 GHz	RFIN2 to RFOUT2							
Full Range Step, VGAIN1 or VGAIN2	1 dB settling, HG mode							
0 to 3.3 V			2			1		µs
3.3 to 0 V			4			3		µs
0.5 V_{GAIN} Step	HG mode, V_{GAIN1} = 2.0 to 1.5 V, 1 dB settling		4			3		µs
HG to LG Transition	V_{GAIN1} = V_{GAIN2} = 0 V, 1 dB settling		0.3			0.2		µs
LG to HG Transition	V_{GAIN1} = V_{GAIN2} = 0 V, 1 dB settling		0.2			0.1		µs

Parameter	Test Conditions/Comments	3.3 V Min	3.3 V Typ	3.3 V Max	5 V Min	5 V Typ	5 V Max	Unit
AMP3 FREQUENCY = 0.75GHz	RFIN3 to RFOUT3 pins							
Gain								dB
vs. Frequency	±50 MHz		+0 to −1			+0 to −1.25		dB
vs. Temperature	−40°C ≤ TA ≤ +105°C		+0.5 to −1			+0.6 to −0.9		dB
vs. Supply	3.135 V to 3.465 V		+0.3 to −0.3					dB
	4.75 V to 5.25 V					+0.05 to −0.1		dB
Input Return Loss	S11		−10.5			−14		dB
Output Return Loss	S22		−10			−12.4		dB
Output 1 dB Compression Point			26			28.8		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 0 dBm/tone		31.8			41		dBm
Noise Figure			3.5			4.5		dB
AMP3 FREQUENCY = 0.9 GHz	RFIN3 to RFOUT3 pins							
Gain			16.3			16.3		dB
vs. Frequency	±50 MHz		+0 to −0.7			+0 to −1		dB
vs. Temperature	−40°C ≤ TA ≤ +105°C		+0.6 to −0.8			+0.6 to −0.9		dB
vs. Supply	3.135 V to 3.465 V		+0.3 to −0.3					dB
	4.75 V to 5.25 V					+0.05 to −0.15		dB
Input Return Loss	S11		−11.5			−13.5		dB
Output Return Loss	S22		−12.5			−13.5		dB
Output 1 dB Compression Point			25.5			29		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 0 dBm/tone		33.8			41.4		dBm
Noise Figure			3.3			4.3		dB
AMP3 FREQUENCY = 1.9 GHz	RFIN3 to RFOUT3 pins							
Gain			12.8			13.8		dB
vs. Frequency	±100 MHz		0 to −2			0 to −1.5		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		+0.7 to −1			+0.7 to −1		dB
vs. Supply	3.135 V to 3.465 V, 4.75 V to 5.25 V		+0.3 to −0.2			0 to −0.2		dB
Input Return Loss	S11		−14			−14		dB
Output Return Loss	S22		−16			−18		dB
Output 1 dB Compression Point			24.5			28.5		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 0 dBm/tone		30.5			37.8		dBm
Noise Figure			5.8			6.1		dB
AMP3 FREQUENCY = 2.2 GHz	RFIN3 to RFOUT3 pins							
Gain			12			12.8		dB
vs. Frequency	±100 MHz		0 to −1.75			0 to −1.8		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		+1 to −1			+1 to −1		dB
vs. Supply	3.135 V to 3.465 V, 4.75 V to 5.25 V		+0.4 to −0.2			0 to −0.3		dB
Input Return Loss	S11		−14			−15.5		dB
Output Return Loss	S22		−16			−18		dB
Output 1 dB Compression Point			25			28.8		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 0 dBm/tone		28			37		dBm
Noise Figure			5.4			5.9		dB

Parameter	Test Conditions/Comments	3.3 V			5 V			Unit
		Min	Typ	Max	Min	Typ	Max	
AMP3 FREQUENCY = 2.6 GHz	RFIN3 to RFOUT3 pins							
Gain			10.3			11.1		dB
vs. Frequency	±100 MHz		0 to −1.8			0 to −1.4		dB
vs. Temperature	−40°C ≤ T_A ≤ +105°C		+1 to −1.2			+1 to −1.2		dB
vs. Supply	3.135 V to 3.465 V, 4.75 V to 5.25 V		+0.4 to −0.1			0 to −0.3		dB
Input Return Loss	S11		−10			−10		dB
Output Return Loss	S22		−17			−17		dB
Output 1 dB Compression Point			22.5			27		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 0 dBm/tone		30			38		dBm
Noise Figure			7.5			7.8		dB
FULL CHAIN FREQUENCY = 2.2 GHz	AMP1→AMP2→AMP3, AMP2 at maximum gain							
Gain			27.5			31.5		dB
vs. Frequency	±100 MHz		0 to −1.4			0 to −1.6		dB
Gain Range	HG mode		13			44		dB
Input Return Loss	S11		−6			−9		dB
Output Return Loss	S22		−13			−16		dB
Output 1 dB Compression Point			24			28		dBm
Output Third Order Intercept	Δf = 1 MHz, P_{OUT} = 5 dBm/tone		29			37		dBm
Noise Figure			1.8			1.5		dB
LOGIC INPUTS	Pin VSW1 and Pin $\overline{VSW1}$							
Logic Level Low	Maximum voltage for a logic low			0.8			0.8	V
Logic Level High	Minimum voltage for a logic high	1.8			1.8			V
Bias Current, $\overline{VSW1}$	$V_{\overline{VSW1}}$ = 0 V		<1			<1		µA
	$V_{\overline{VSW1}}$ = 3.3 V		290			290		µA
Bias Current, VSW1	V_{VSW1} = 0 V		<1			<1		µA
	V_{VSW1} = 3.3 V		<1			<1		µA
GAIN CONTROL INTERFACE	Pin VGAIN1 and Pin VGAIN2							
VGAIN Minimum	Minimum gain control voltage	0			0			V
VGAIN Maximum	Maximum gain control voltage			3.3			3.3	V
Bias Current	V_{GAIN1}, V_{GAIN2} = 0 V		−120			−120		µA
	V_{GAIN1}, V_{GAIN2} = 3.3 V		190			190		µA
Input Resistance			10.6			10.6		kΩ
POWER SUPPLIES								
Voltage		3.135	3.3	3.465	4.75	5	5.25	V
Total Supply Current	All three amplifiers active, maximum gain		141			270		mA
	LG mode, V_{GAIN1} = V_{GAIN2} = 0 V		105			211		mA
Individual Supply Currents	AMP1		37			59		mA
	AMP2 (VPOS1 only, HG mode)[1]		37			59		mA
	AMP2 (VPOS1 only, LG mode)[1]		<1			<1		mA
	VPOS2, V_{GAIN1} = V_{GAIN2} = 0 V[1]		6			13		mA
	VPOS2, V_{GAIN1} = V_{GAIN2} = 3.3 V[1]		9.5			17		mA
	AMP3 (output bias only)[2]		61			139		mA

[1] VPOS1 and VPOS2 are both required for AMP2 functionality.
[2] VPOS2 and AMP3 output bias are both required for AMP3 functionality.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
Maximum RF Input Level (AMP1)	20 dBm
Internal Power Dissipation	3 W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 30 sec)	250°C
Human Body Model (HBM) ESD Rating (ESDA/JEDEC JS-001-2011)	±1.0 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a ADL5246 soldered to the evaluation board, a 4-layer circuit board with a 5 × 5 thermal via array under the exposed paddle. θ_{JA} measured at the top of the package. θ_{JC} derived using a JEDEC test board.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	16.5	1.15	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

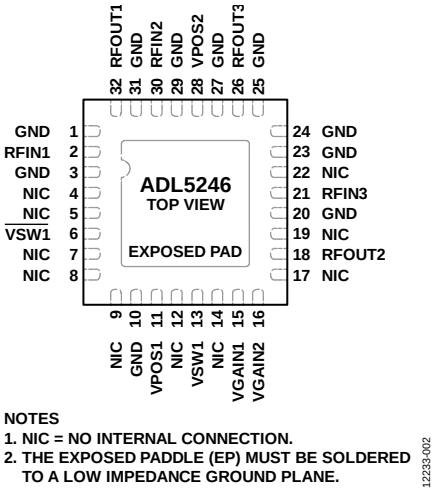

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 10, 20, 23, 24, 25, 27, 29, 31, EP	GND	Ground. The exposed paddle (EP) and ground pins must be soldered to a low impedance ground plane.
2	RFIN1	RF Input. This pin requires a dc blocking capacitor. Use a 100 pF capacitor for normal operation.
4, 5, 7, 8, 9, 12, 14, 17, 19, 22	NIC	No Internal Connection. These pins are not connected to internal circuitry. The user may optionally solder to a low impedance ground plane for grounding, shielding, and printed circuit board (PCB) trace impedance continuity.
6	$\overline{\text{VSW1}}$	Bypass Switch Control. Logic low = 0 V, and logic high = 3.3 V. Switch logic is shown in Table 5.
11	VPOS1	Bias for the AMP2 LNA. Connect this pin to the dc supply voltage through an RF choke.
13	VSW1	Bypass Switch Control. Logic low = 0 V, and logic high = 3.3 V. Switch logic is shown in Table 5.
15	VGAIN1	Gain Control for VVA1. The gain control range is 0 V to 3.3 V.
16	VGAIN2	Gain Control VVA2. The gain control range is 0 V to 3.3 V.
18	RFOUT2	RF Output of the Voltage Variable Attenuator (VVA) Block.
21	RFIN3	Driver Amplifier Input. This pin requires a dc blocking capacitor. Use a 100 pF capacitor for normal operation.
26	RFOUT3	Driver Amplifier Output. Connect this pin to a dc supply through an RF choke.
28	VPOS2	Bias for VVA1, VVA2, and the AMP3 Bias Circuit. Connect this pin to the dc supply voltage through an RF choke.
30	RFIN2	RF Input to the VGA Block.
32	RFOUT1	Low Noise Amplifier Output. Connect this pin to a dc supply through an RF choke.

TYPICAL PERFORMANCE CHARACTERISTICS

All supply pins at 5 V, T_A = 25°C, unless otherwise noted.

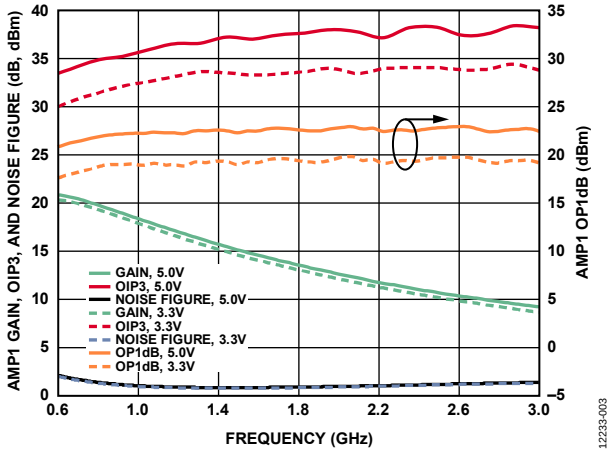

Figure 3. AMP1 Gain, OIP3 at P_{OUT} = 0 dBm/Tone, Noise Figure, and OP1dB vs. Frequency

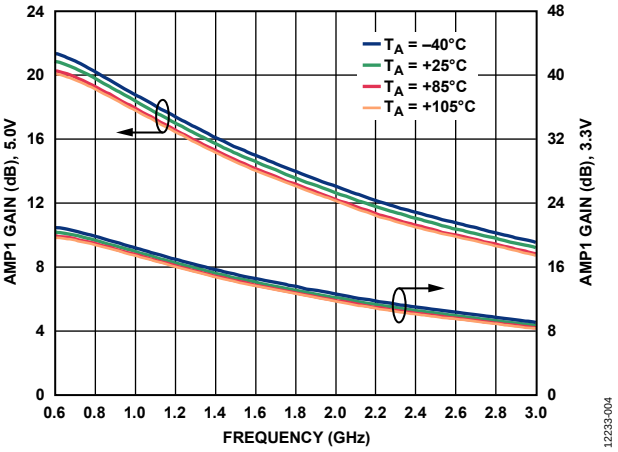

Figure 4. AMP1 Gain vs. Frequency by Temperature

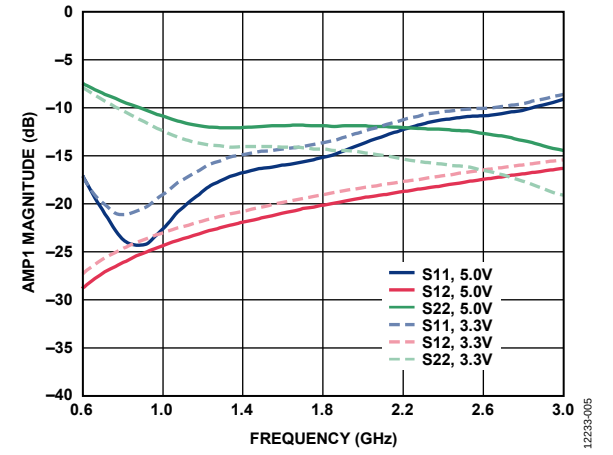

Figure 5. AMP1 Magnitude of Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

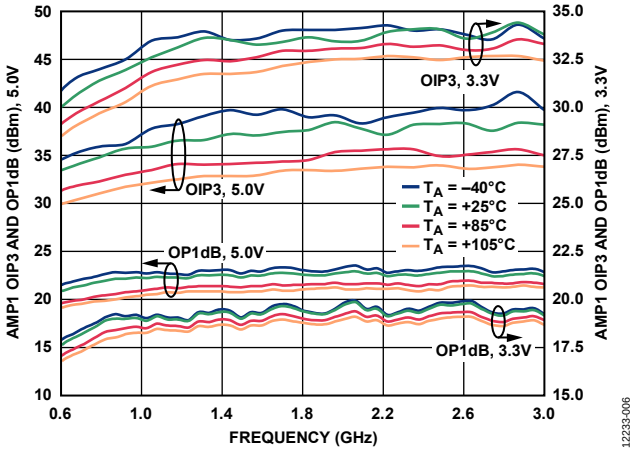

Figure 6. AMP1 OIP3 at P_{OUT} = 0 dBm/Tone and OP1dB vs. Frequency by Temperature

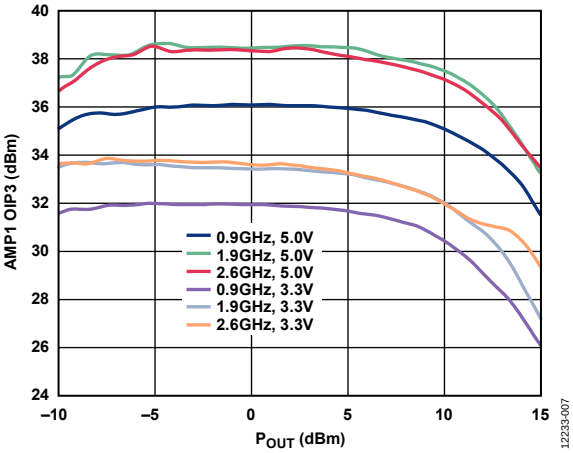

Figure 7. AMP1 OIP3 vs. P_{OUT} by Frequency

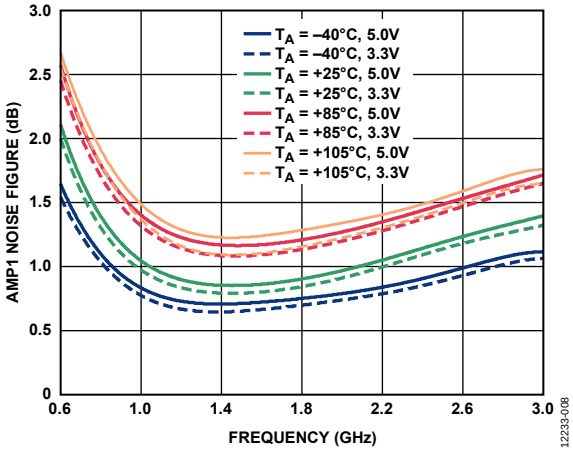

Figure 8. AMP1 Noise Figure vs. Frequency by Temperature

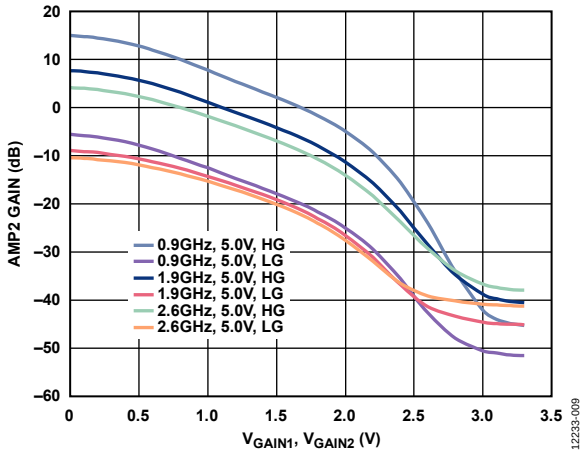

Figure 9. AMP2 Gain vs. V_{GAIN1}, V_{GAIN2} at Three Frequencies, 5 V Supply, Both Gain Controls Varied, $V_{GAIN1} = V_{GAIN2}$

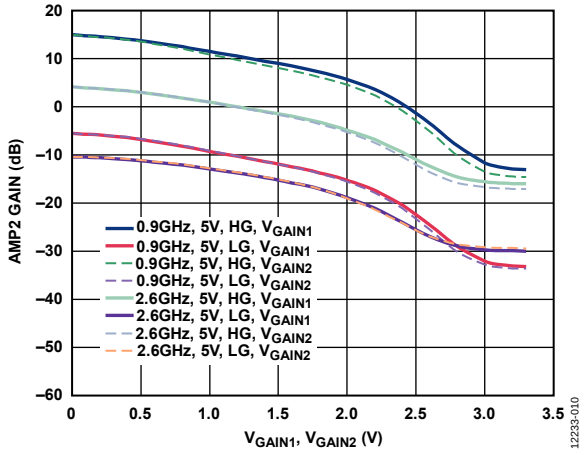

Figure 10. AMP2 Gain vs. V_{GAIN1}, V_{GAIN2} at Two Frequencies, 5 V Supply, Only One Gain Control Varied

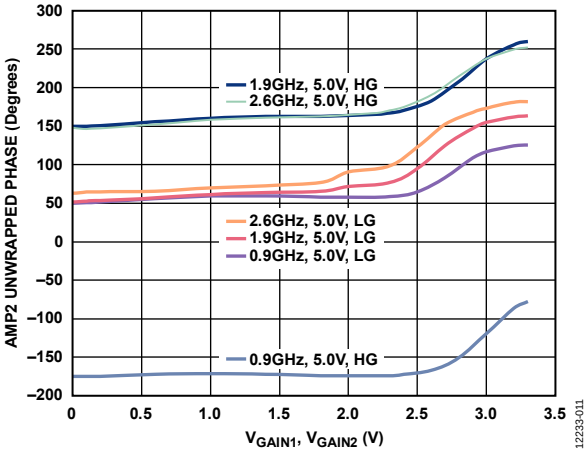

Figure 11. AMP2 Unwrapped Phase vs. V_{GAIN1}, V_{GAIN2} at Three Frequencies, 5 V Supply, Both Gain Controls Varied, $V_{GAIN1} = V_{GAIN2}$

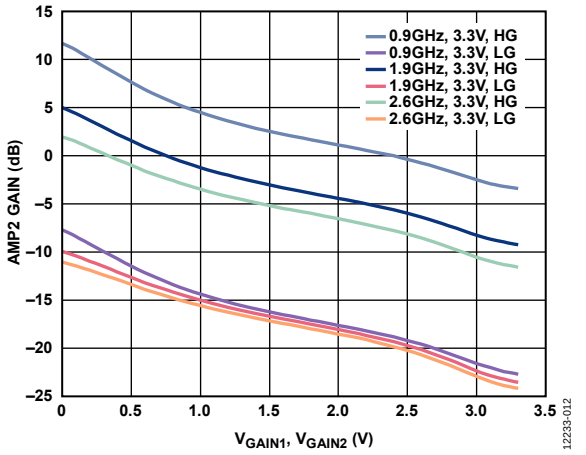

Figure 12. AMP2 Gain vs. V_{GAIN1}, V_{GAIN2} at Three Frequencies, 3.3 V Supply, Both Gain Controls Varied, $V_{GAIN1} = V_{GAIN2}$

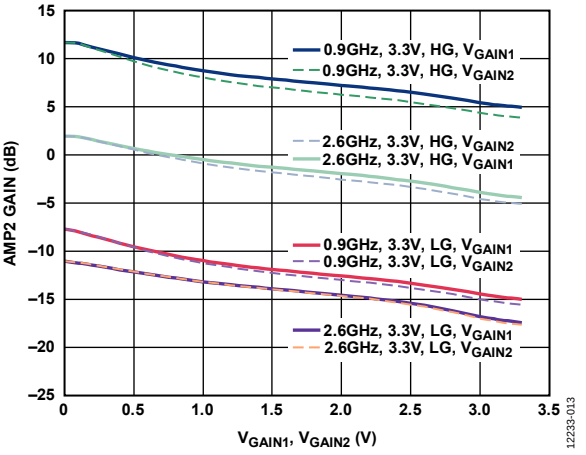

Figure 13. AMP2 Gain vs. V_{GAIN1}, V_{GAIN2} at Two Frequencies, 3.3 V Supply, Only One Gain Control Varied

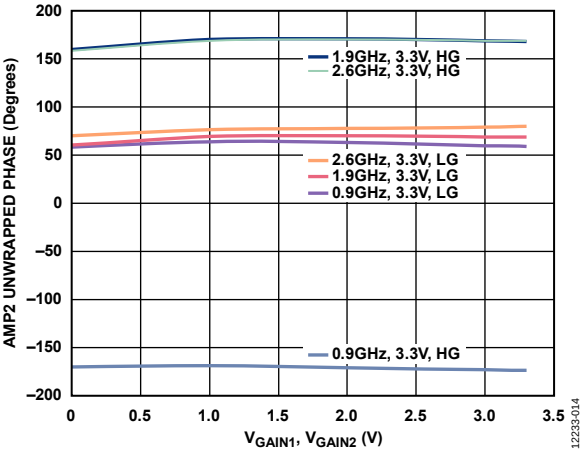

Figure 14. AMP2 Unwrapped Phase vs. V_{GAIN1}, V_{GAIN2} at Three Frequencies, 3.3 V Supply, Both Gain Controls Varied, $V_{GAIN1} = V_{GAIN2}$

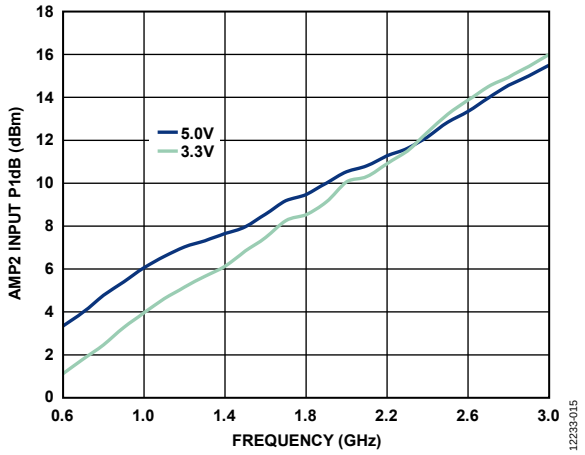

Figure 15. AMP2 Input P1dB vs. Frequency at Maximum Gain, HG Only

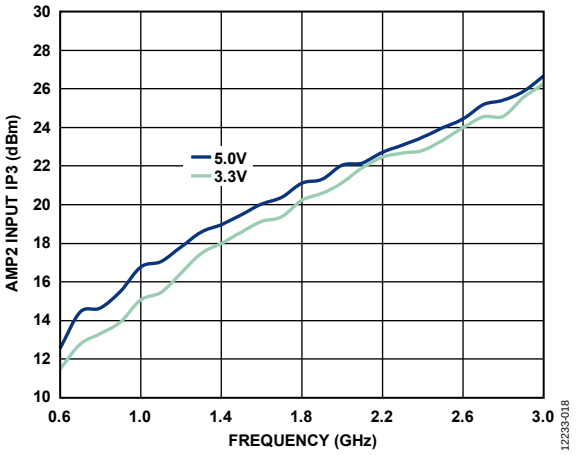

Figure 18. AMP2 Input IP3 vs. Frequency at Maximum Gain, HG Only

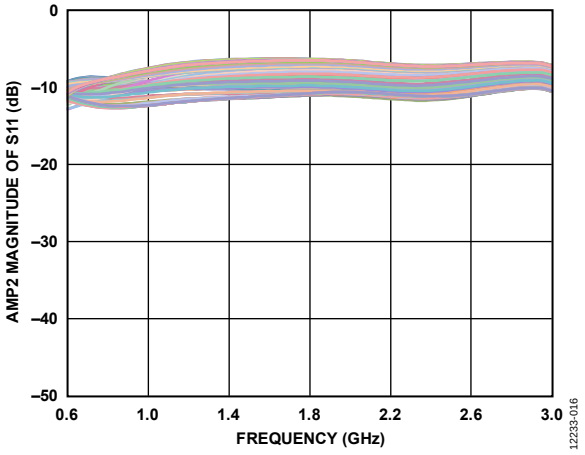

Figure 16. AMP2 Magnitude of Input Return Loss (S11) vs. Frequency, 5 V Supply, Gain Stepped Across Full Range

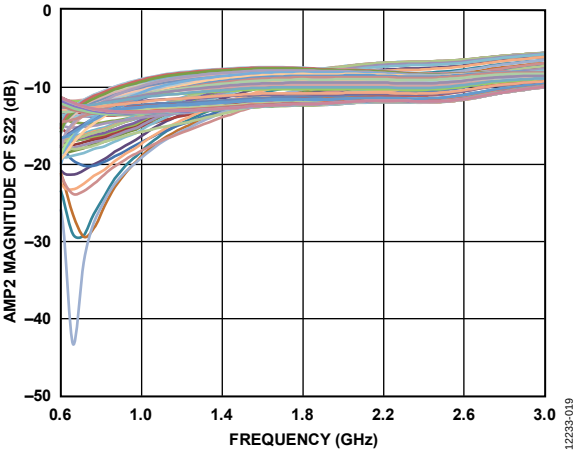

Figure 19. AMP2 Magnitude of Output Return Loss (S22) vs. Frequency, 5 V Supply, Gain Stepped Across Full Range

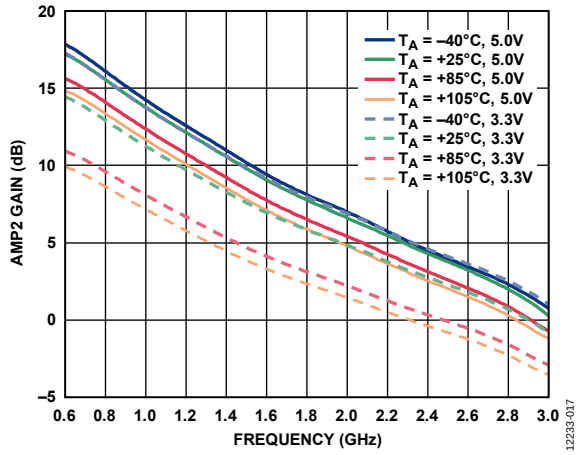

Figure 17. AMP2 Gain vs. Frequency by Temperatures at Maximum Gain

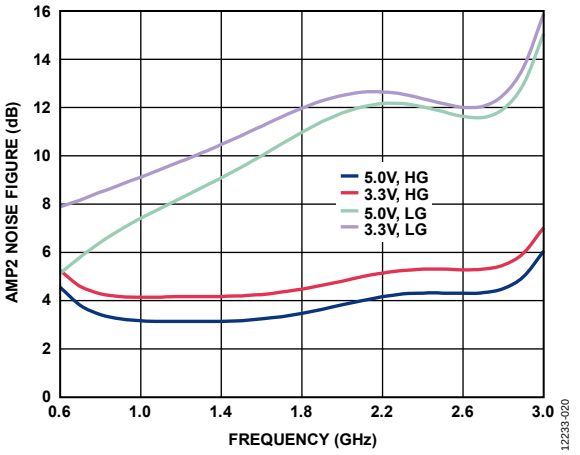

Figure 20. AMP2 Noise Figure vs. Frequency at $V_{GAIN1} = V_{GAIN2} = 0$ V

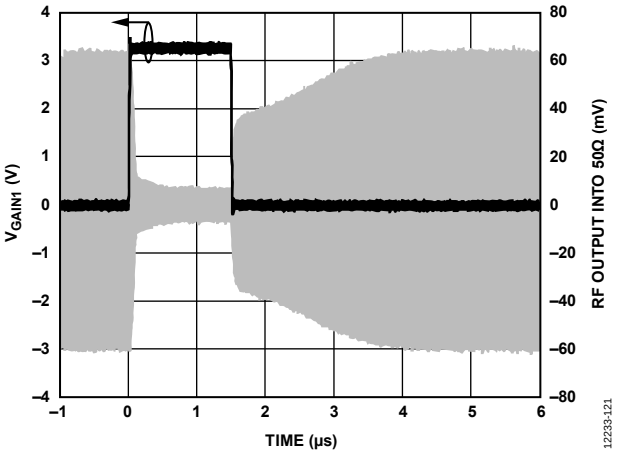

Figure 21. AMP2 Typical Output Response with 3.3 V Step on V_{GAIN1}, V_{GAIN2} = 0 V, HG Mode, 0.9 GHz

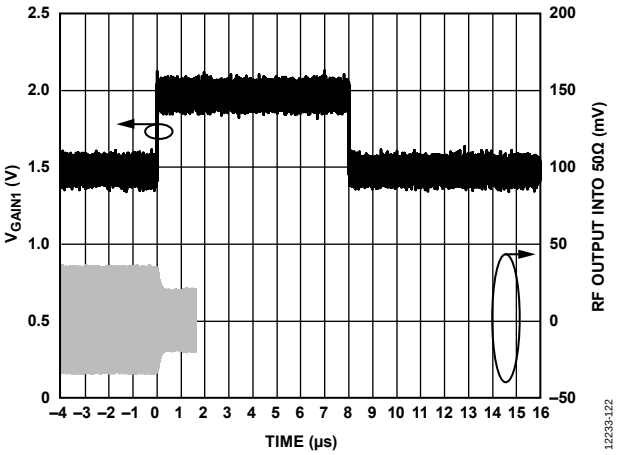

Figure 22. AMP2 Typical Output Response with 0.5 V Step on V_{GAIN1}, V_{GAIN2} = 0 V, HG Mode, 0.9 GHz

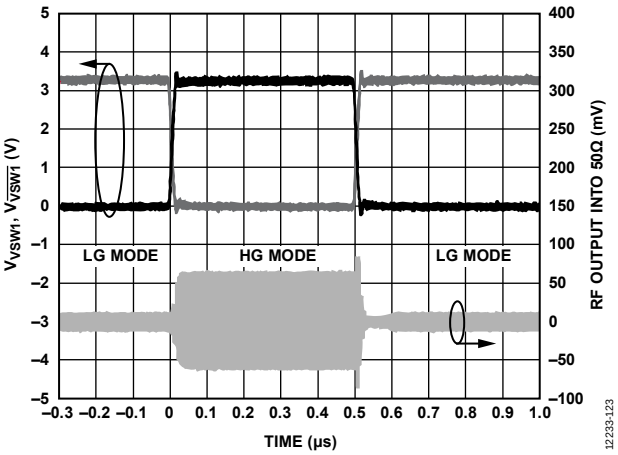

Figure 23. AMP2 Typical Output Response During Gain Mode Switching, V_{GAIN1} = V_{GAIN2} = 0 V, 0.9 GHz

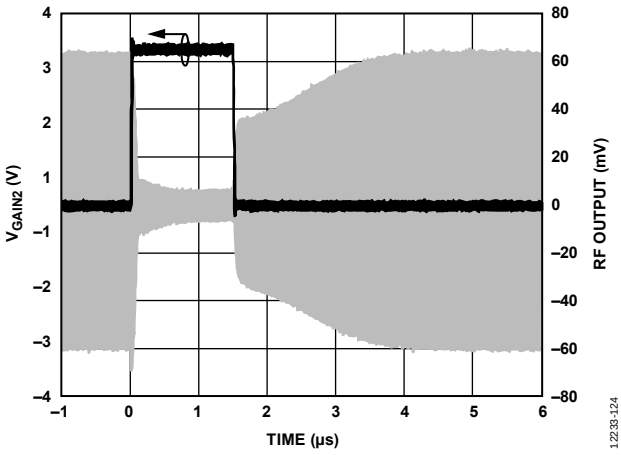

Figure 24. AMP2 Typical Output Response with 3.3 V Step on V_{GAIN2}, V_{GAIN1} = 0 V, HG Mode, 0.9 GHz

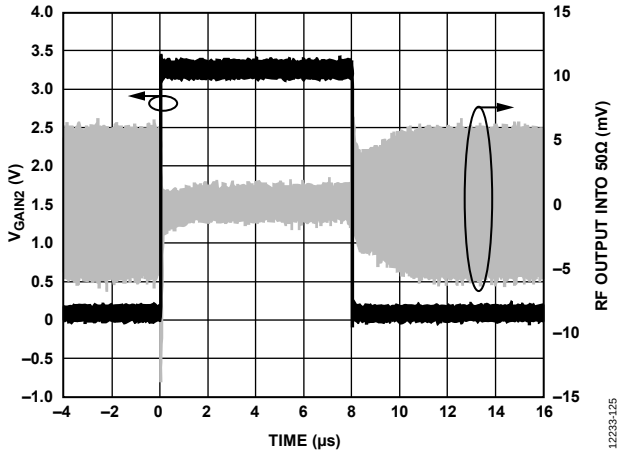

Figure 25. AMP2 Typical Output Response with 3.3 V Step on V_{GAIN2}, V_{GAIN1} = 3.3 V, HG Mode, 0.9 GHz

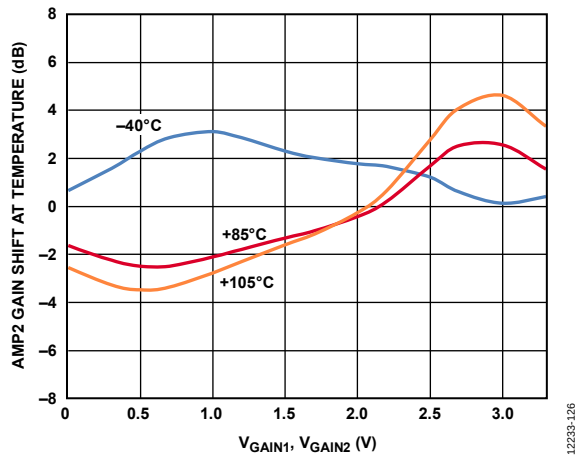

Figure 26. AMP2 Typical Gain Shift at Temperature With Respect to 25 °C vs. V_{GAIN1} = V_{GAIN2}, Both Gain Controls Varied, 1.75 GHz

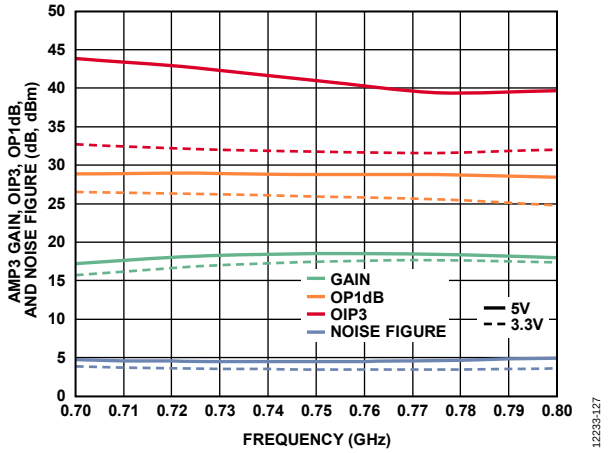

Figure 27. AMP3 0.75 GHz Gain, OIP3 at P_{OUT} = 0 dBm/Tone, OP1dB and Noise Figure vs. Frequency

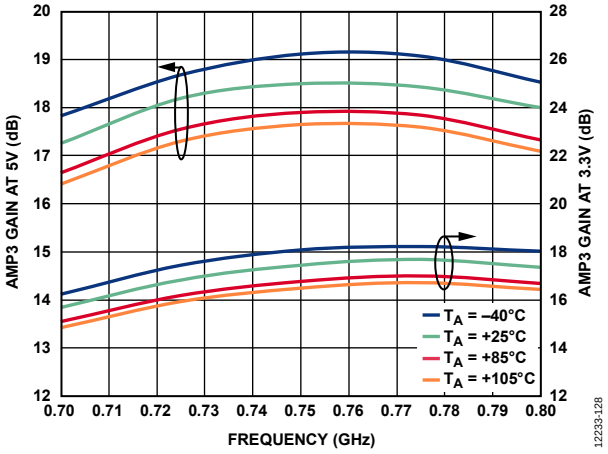

Figure 28. AMP3 0.75 GHz Gain vs. Frequency by Temperature

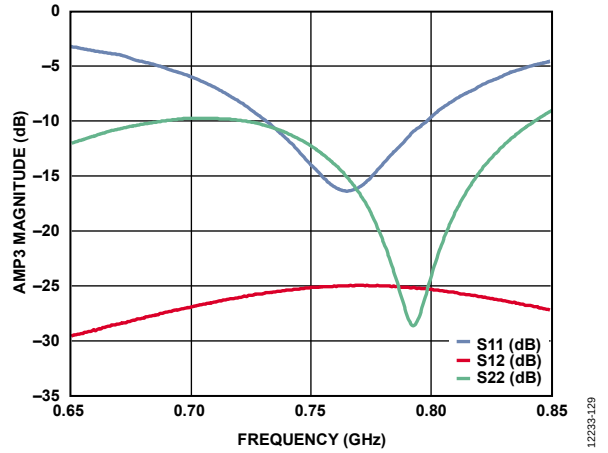

Figure 29. AMP3 0.75 GHz Magnitude of Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

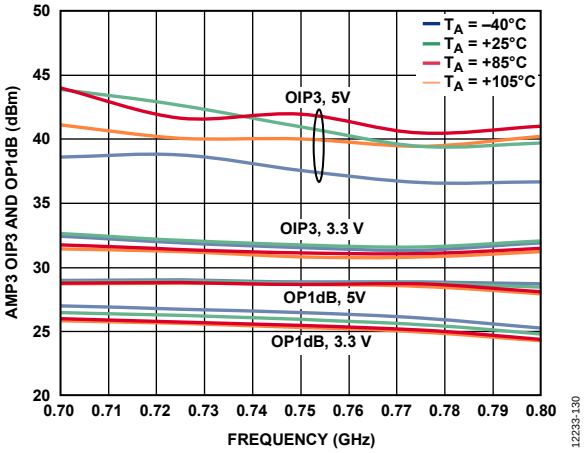

Figure 30. AMP3 0.75 GHz OIP3 at P_{OUT} = 0 dBm/Tone and OP1dB vs. Frequency by Temperature

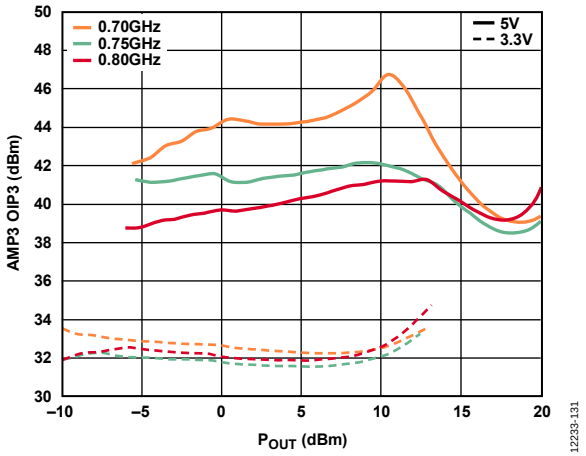

Figure 31. AMP3 0.75 GHz OIP3 vs. P_{OUT} by Frequency

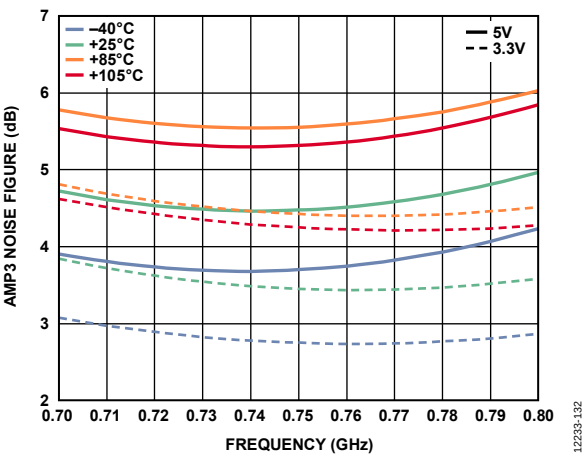

Figure 32. AMP3 0.75 GHz Noise Figure vs. Frequency by Temperature

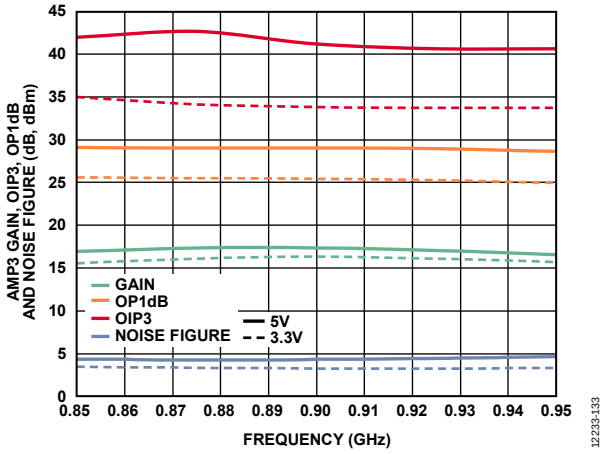

Figure 33. AMP3 0.9 GHz Gain, OIP3 at P_{OUT} = 0 dBm/Tone, OP1dB, and Noise Figure vs. Frequency

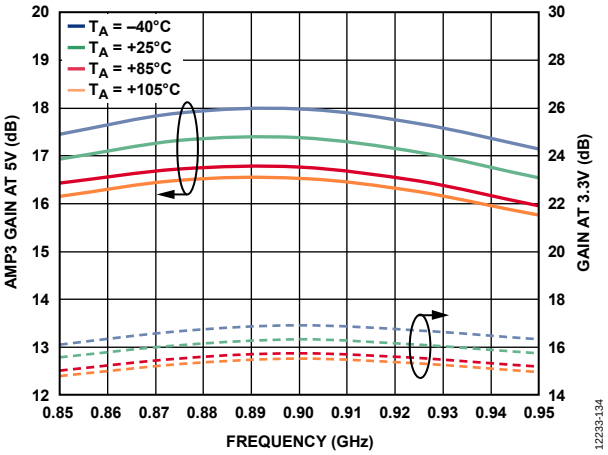

Figure 34. AMP3 0.9 GHz Gain vs. Frequency by Temperature

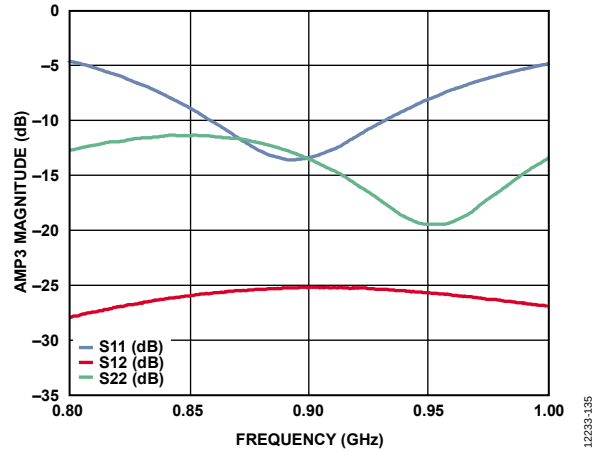

Figure 35. AMP3 0.9 GHz Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

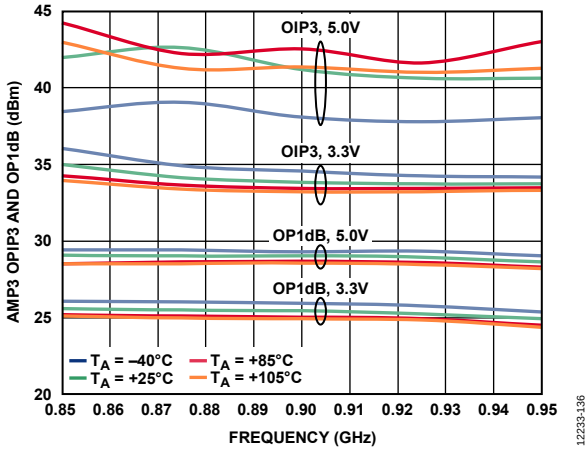

Figure 36. AMP3 0.9 GHz OIP3 at P_{OUT} = 0 dBm/Tone and OP1dB vs. Frequency by Temperature

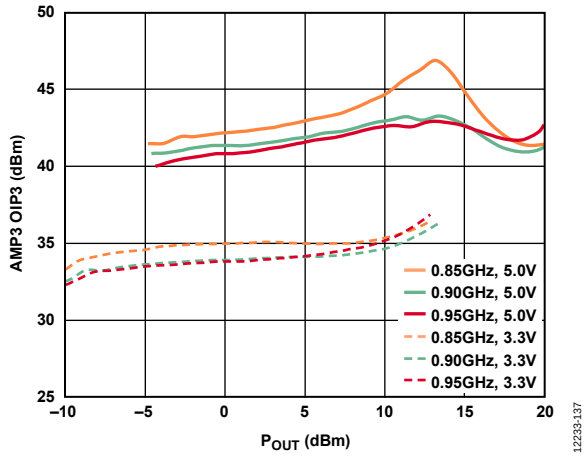

Figure 37. AMP3 0.9 GHz OIP3 vs. P_{OUT} by Frequency

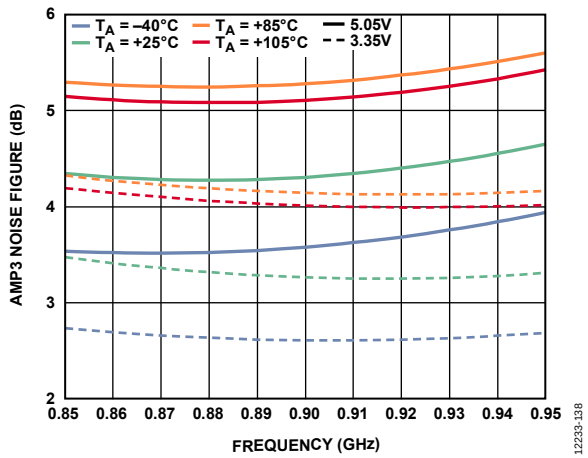

Figure 38. AMP3 0.9 GHz Noise Figure vs. Frequency by Temperature

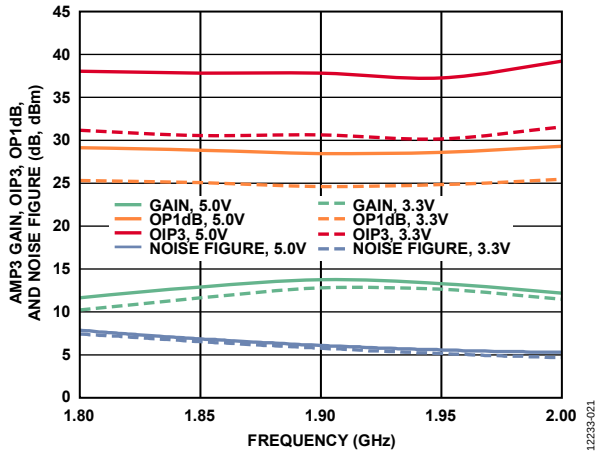

Figure 39. AMP3 1.9 GHz Gain, OIP3 at P_{OUT} = 0 dBm/Tone, OP1dB, and Noise Figure vs. Frequency

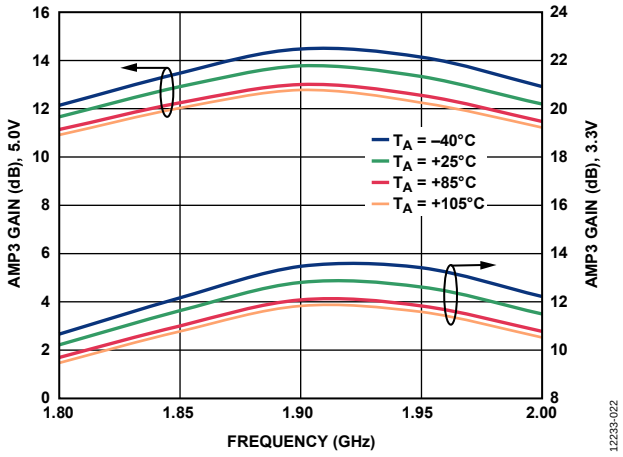

Figure 40. AMP3 1.9 GHz Gain vs. Frequency by Temperature

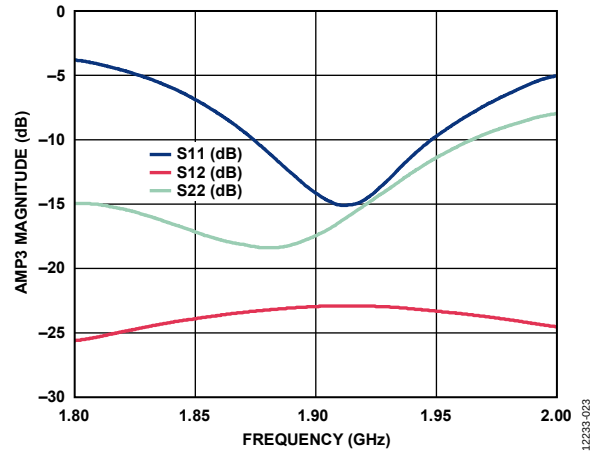

Figure 41. AMP3 1.9 GHz Magnitude of Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

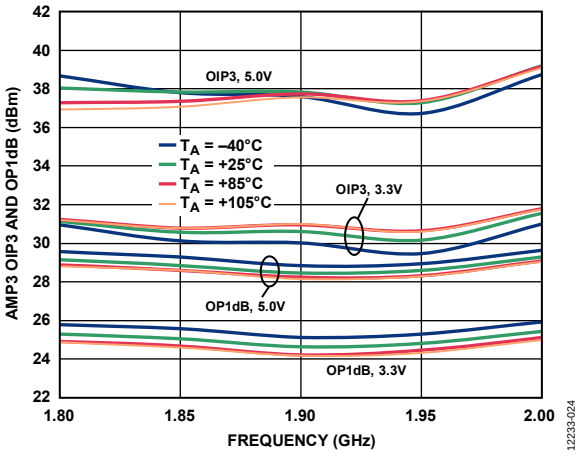

Figure 42. AMP3 1.9 GHz OIP3 at P_{OUT} = 0 dBm/Tone and OP1dB vs. Frequency by Temperature

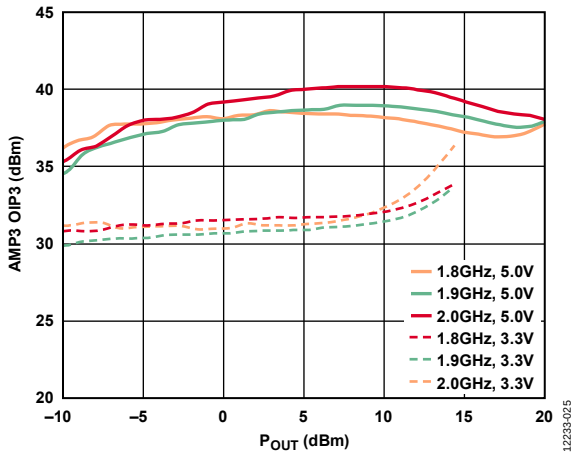

Figure 43. AMP3 1.9 GHz OIP3 vs. P_{OUT} by Frequency

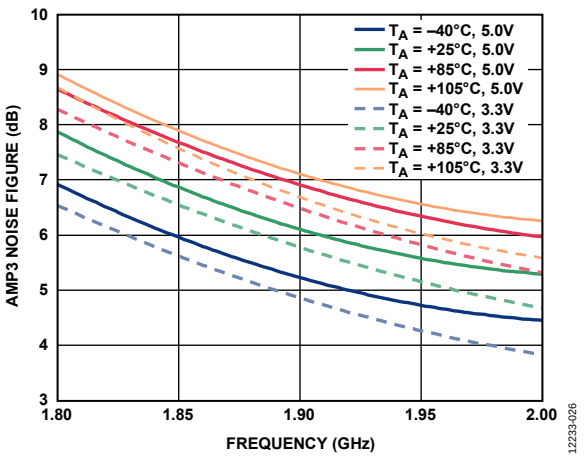

Figure 44. AMP3 1.9 GHz Noise Figure vs. Frequency by Temperature

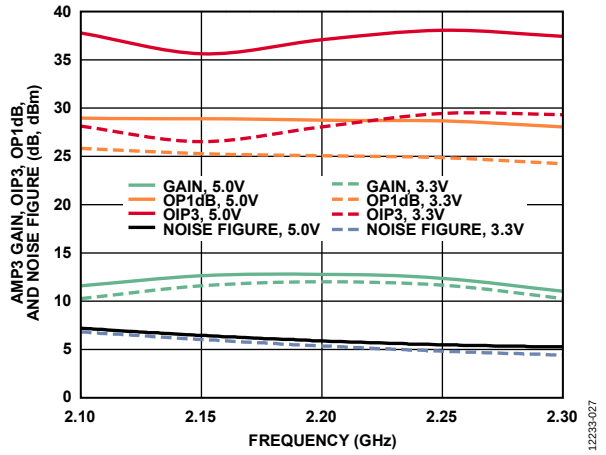

Figure 45. AMP3 2.2 GHz Gain, OIP3 at P_{OUT} = 0 dBm/Tone, OP1dB, and Noise Figure vs. Frequency

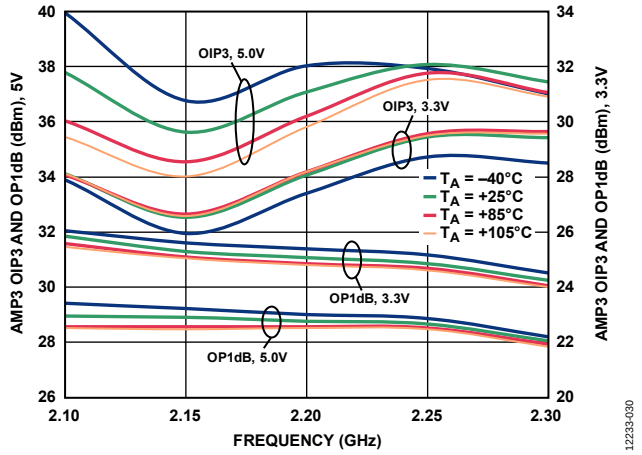

Figure 48. AMP3 2.2 GHz OIP3 at P_{OUT} = 0 dBm/Tone and OP1dB vs. Frequency by Temperature

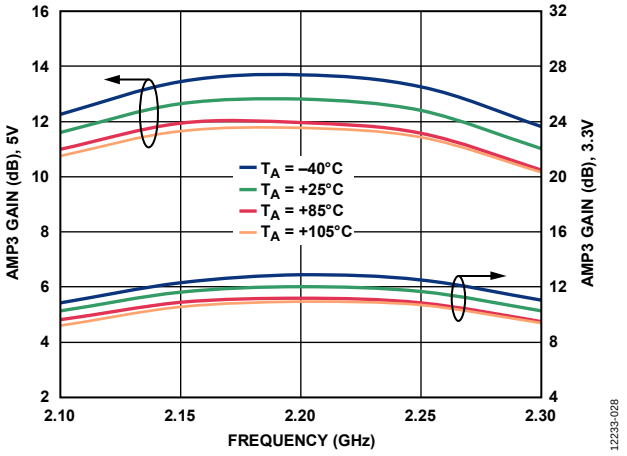

Figure 46. AMP3 2.2 GHz Gain vs. Frequency by Temperature

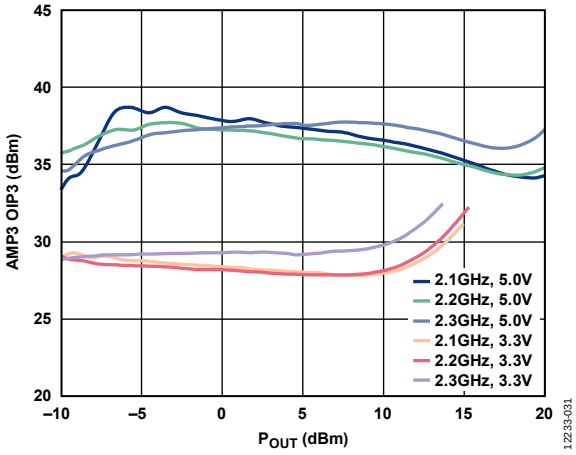

Figure 49. AMP3 2.2 GHz OIP3 vs. P_{OUT} by Frequency

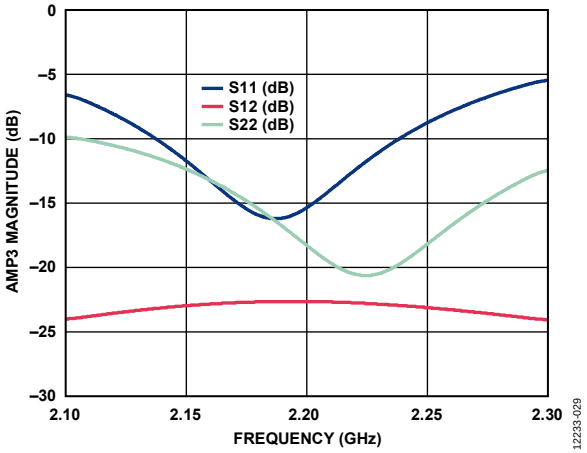

Figure 47. AMP3 2.2 GHz Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

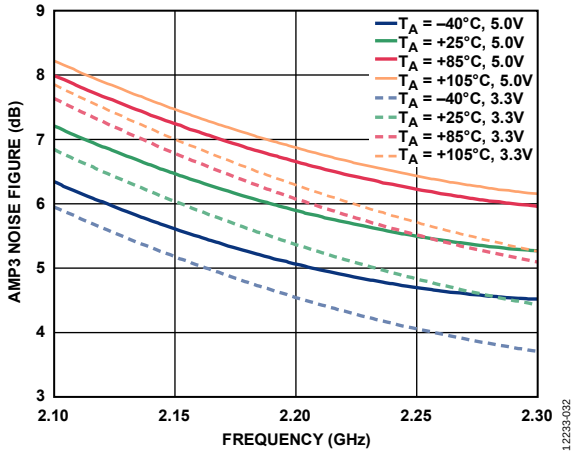

Figure 50. AMP3 2.2 GHz Noise Figure vs. Frequency by Temperature

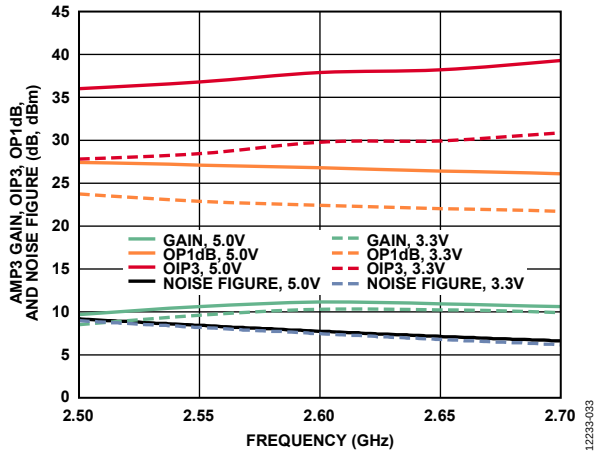

Figure 51. AMP3 2.6 GHz Gain, OIP3 at P_{OUT} = 0 dBm/Tone, OP1dB, and Noise Figure vs. Frequency

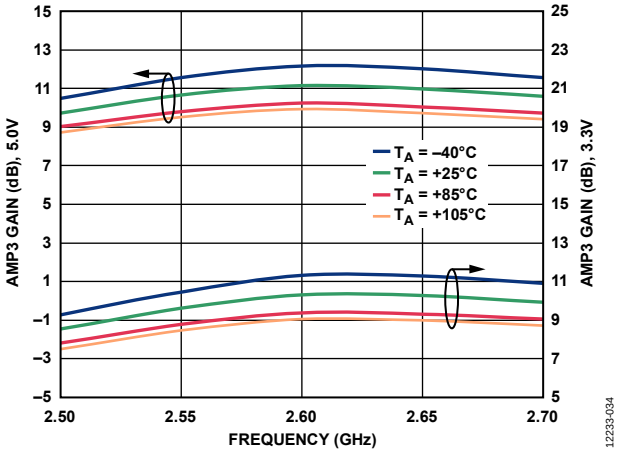

Figure 52. AMP3 2.6 GHz Gain vs. Frequency by Temperature

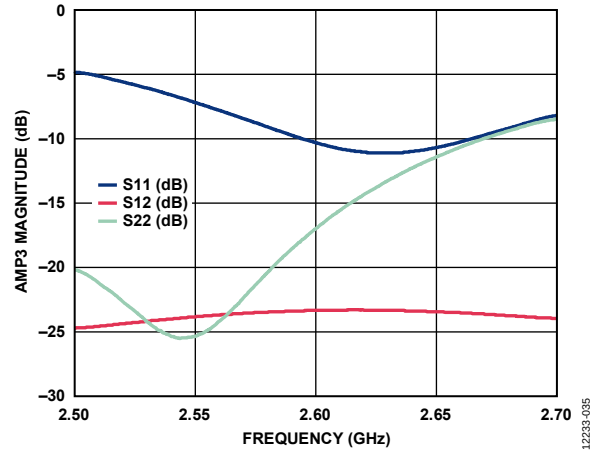

Figure 53. AMP3 2.6 GHz Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

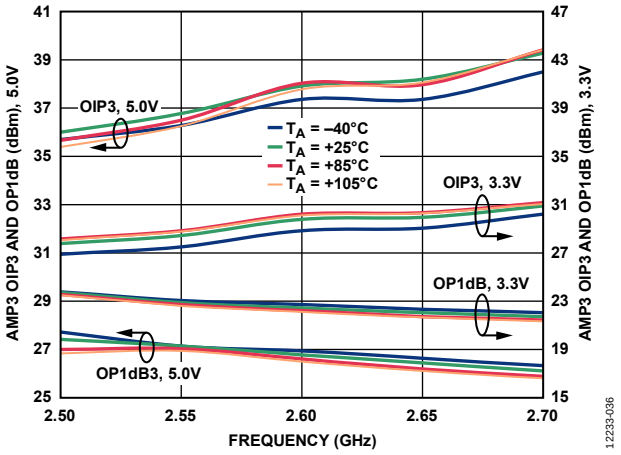

Figure 54. AMP3 2.6 GHz OIP3 at P_{OUT} = 0dBm/Tone and OP1dB vs. Frequency and Temperature

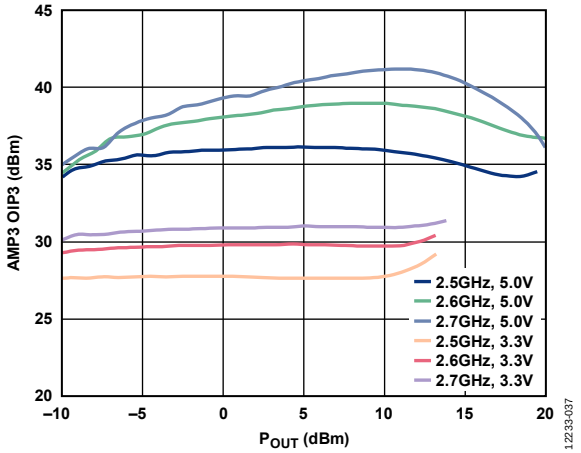

Figure 55. AMP3 2.6 GHz OIP3 vs. P_{OUT} by Frequency

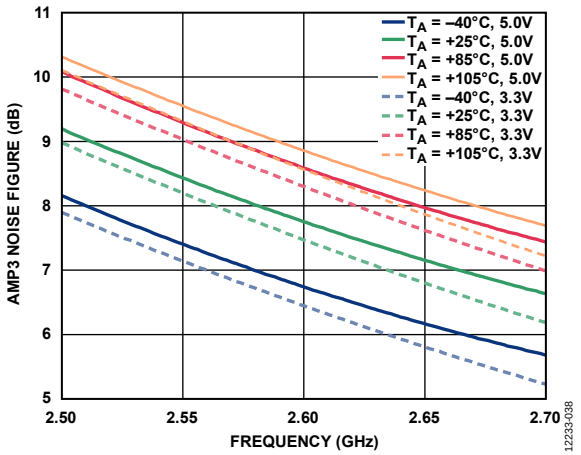

Figure 56. AMP3 2.6 GHz Noise Figure vs. Frequency by Temperature

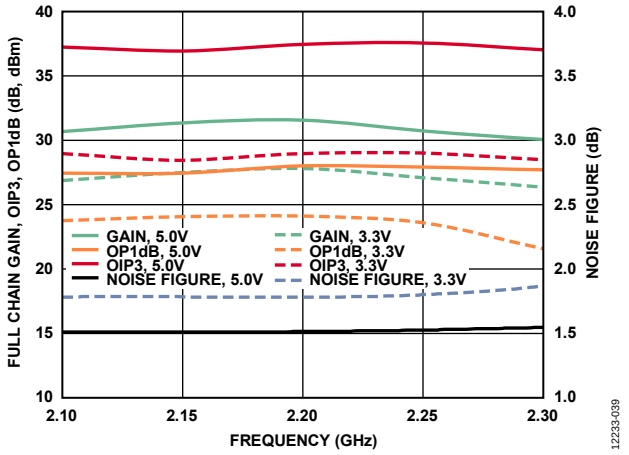

Figure 57. Full Chain 2.2 GHz Gain, OIP3 at P_{OUT} = 5 dBm/Tone, OP1dB, and Noise Figure vs. Frequency at Maximum Gain

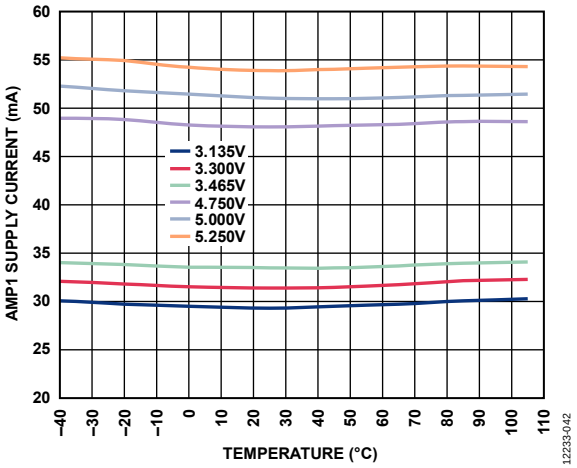

Figure 60. AMP1 Supply Current vs. Temperature by Voltage

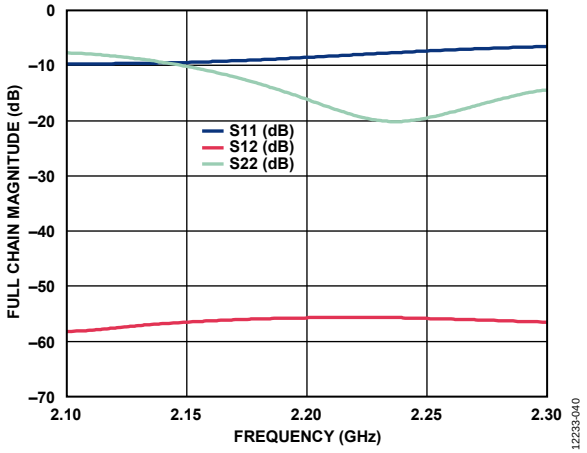

Figure 58. Full Chain 2.2 GHz Magnitude of Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency at Maximum Gain

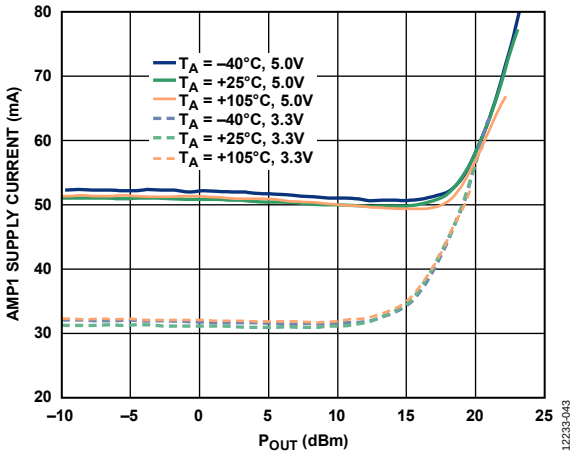

Figure 61. AMP1 Supply Current vs. P_{OUT} by Temperature

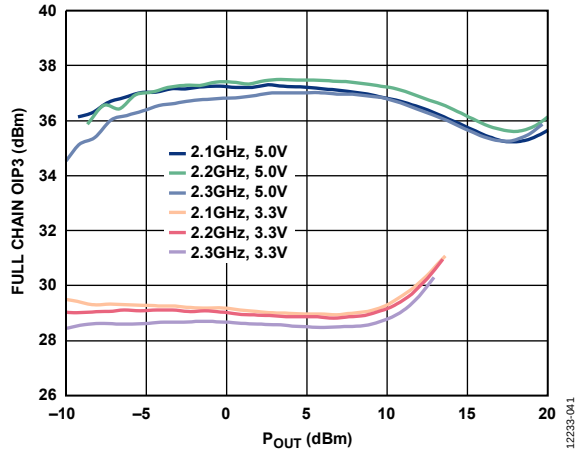

Figure 59. Full Chain 2.2 GHz OIP3 vs. P_{OUT} by Frequency at Maximum Gain

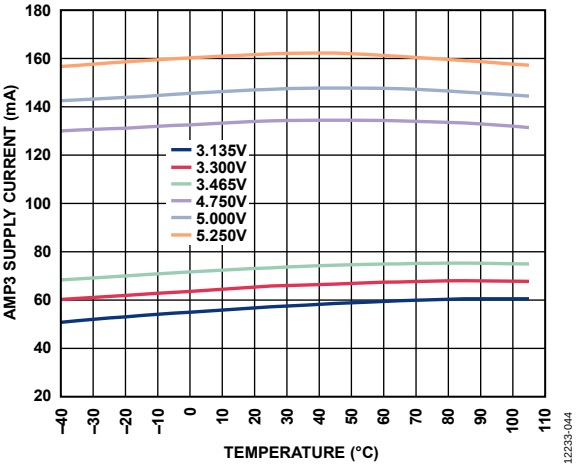

Figure 62. AMP3 Supply Current vs. Temperature by Voltage

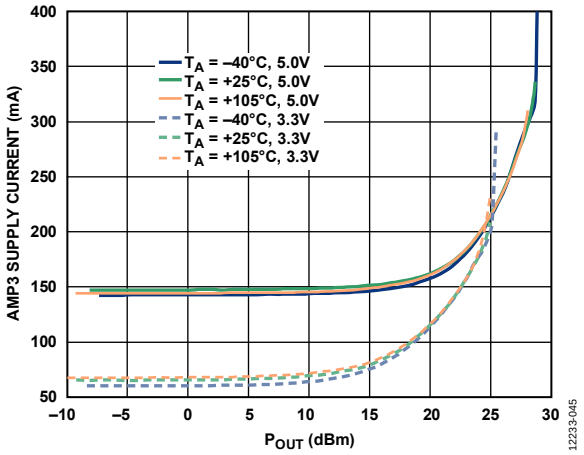

Figure 63. AMP3 Supply Current vs. P_{OUT} by Temperature

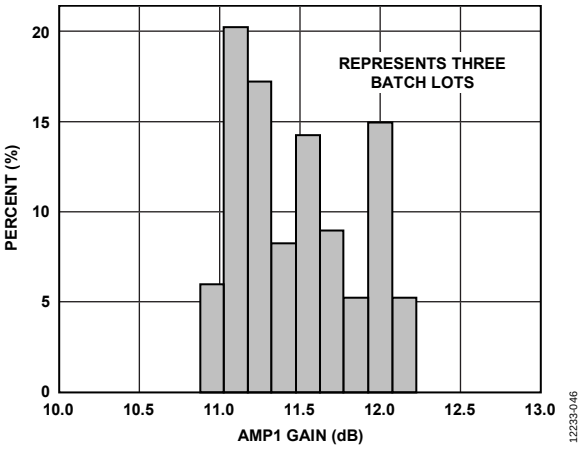

Figure 64. AMP1 Gain Distribution at 2.2 GHz

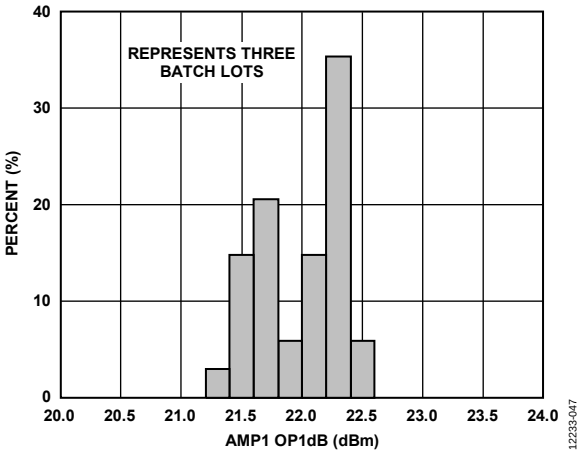

Figure 65. AMP1 OP1dB Distribution at 2.2 GHz

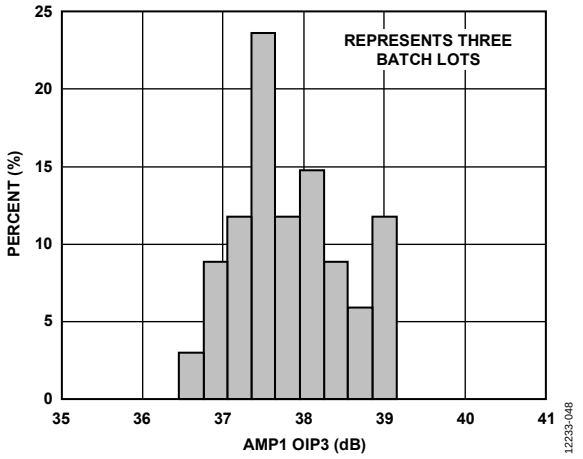

Figure 66. AMP1 OIP3 Distribution at 2.2 GHz, P_{OUT} = 0 dBm/Tone

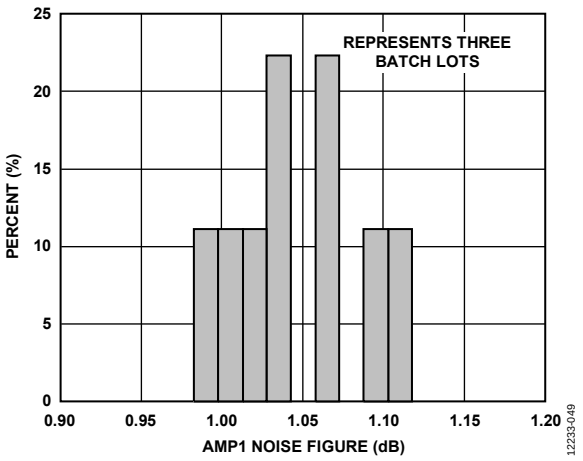

Figure 67. AMP1 Noise Figure Distribution at 2.2 GHz

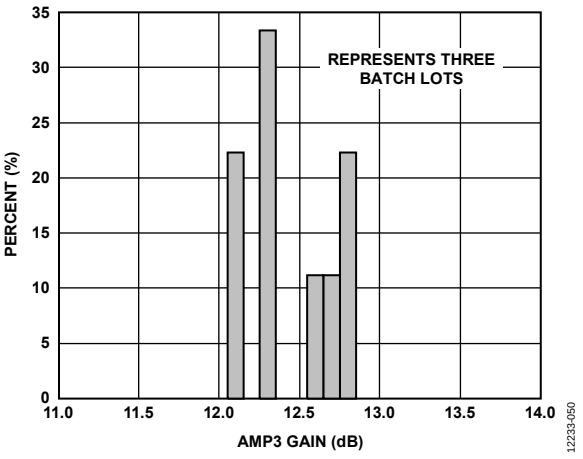

Figure 68. AMP3 Gain Distribution at 2.2 GHz

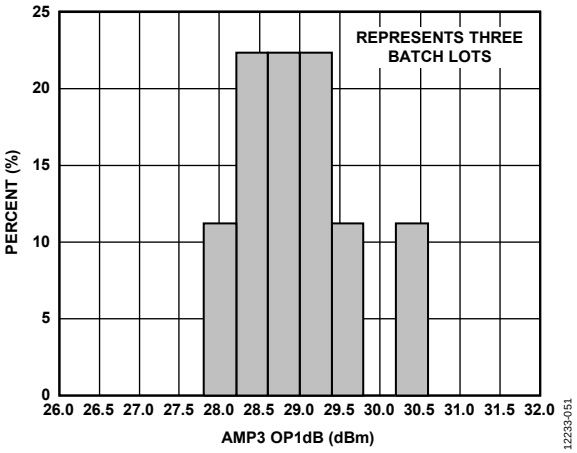

Figure 69. AMP3 OP1dB Distribution, 2.2 GHz

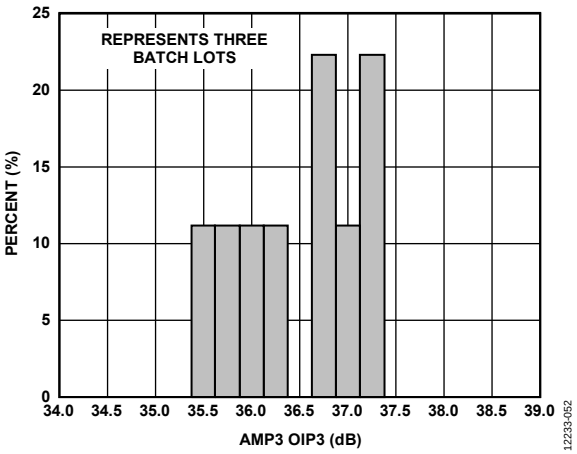

Figure 70. AMP3 OIP3 Distribution at 0 dBm/Tone, 2.2 GHz

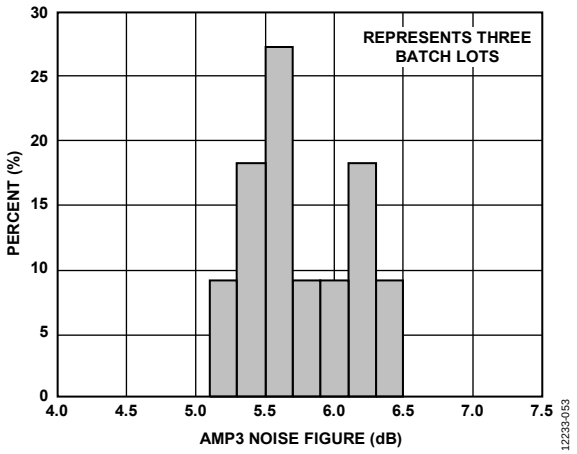

Figure 71. AMP3 Noise Figure Distribution, 2.2 GHz

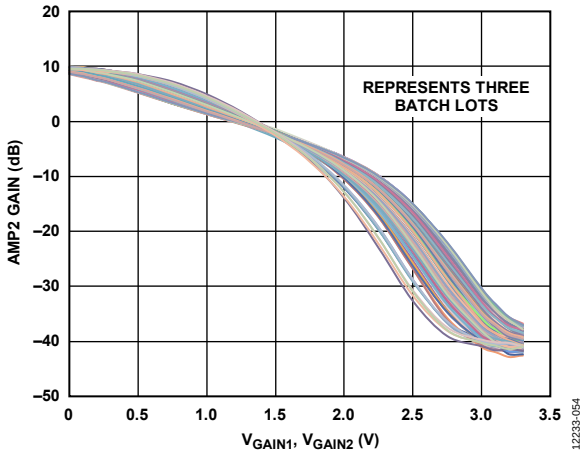

Figure 72. Distribution of AMP2 Gain vs. V_{GAIN1}, V_{GAIN2} at 1.5 GHz, 5 V Supply, HG, Both Gain Controls Varied, $V_{GAIN1} = V_{GAIN2}$

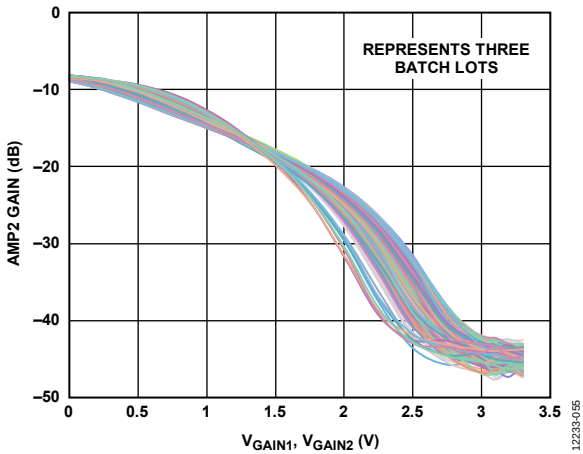

Figure 73. Distribution of AMP2 Gain vs. V_{GAIN1}, V_{GAIN2} at 1.5 GHz, 5 V Supply, LG, Both Gain Controls Varied, $V_{GAIN1} = V_{GAIN2}$

TERMINOLOGY

Full Chain Configuration
The full chain configuration is a serial connection of Amplifier 1 (AMP1), Amplifier 2 (AMP2), and Amplifier 3 (AMP3), in that order. The performance data shown in Table 1 and Figure 57 through Figure 59 are measured without any filters or attenuators between amplifiers.

High Gain (HG) Mode
The amplifier within AMP2 is active and not bypassed. In addition, the input and output attenuators are active.

Low Gain (LG) Mode
The amplifier within AMP2 is bypassed and inactive. However, the input and output attenuators remain active.

Maximum Gain
When AMP2is in HG mode, $V_{GAIN1} = V_{GAIN2} = 0$ V.

THEORY OF OPERATION

BASIC CONNECTIONS

The basic connections for operating the ADL5246 are shown in Figure 74. The schematic of AMP3 is configured for operation at 2.2 GHz.

Amplifier 1 (AMP1)

AMP1 in the ADL5246 is a broadband low noise amplifier. The radio frequency (RF) input is internally matched to 50 Ω and optimally matched for the minimum noise figure and is unconditionally stable. The RF output is internally matched for 50 Ω. The RF inputs and outputs require dc blocking capacitors (C8 and C9) for operation. DC bias is supplied through Inductor L1 and is connected to the RFOUT1 pin. Three decoupling capacitors (C40, C41, and C5) prevent RF signals from propagating on the dc supply lines. The value of L1 must be high enough to isolate the bias from RF; however, the exact value is not critical for operation. The self resonance of L1 has little effect upon the operation of AMP1, within reasonable limits. AMP1 is completely independent from the rest of the ADL5246 and may be left unpowered if not needed. When AMP1 is not in use, terminate the RFIN1 and RFOUT1 pins to ground via a 100 pF capacitor and a 50 Ω resistor in series on each pin.

Amplifier 2 (AMP2)

AMP2 is a 50 Ω internally matched RF VGA consisting of two VVAs with an LNA in between them. RFIN2 and RFOUT2 are internally ac-coupled with a 20 pF on-chip capacitor. The LNA has an integral bypass switch that allows the user to choose between a low gain range and a high gain range. When the LNA is bypassed, it is also not powered, reducing the supply current by approximately 59 mA.

Each VVA may be controlled independently or in tandem via VGAIN1 and VGAIN2. Bias is supplied to AMP2 via VPOS1 and VPOS2. VPOS1 provides the bias to the amplifier circuit, and VPOS2 provides bias to the VVAs. Therefore, both VPOS1 and VPOS2 must be connected to bias to operate AMP2.

Inductors L2 and L3 with capacitors C2, C4, C7, C16, C17, and C20 prevent RF signals from propagating on the dc supply lines. The L2 value has some bearing on the gain of AMP2, with the 10 nH value giving an unhindered frequency response as low as approximately 0.6 GHz.

AMP2 is sensitive to capacitance on the VPOS2 bias line. Place all bypass capacitors as shown in Figure 74. Excessive capacitance between L3 and Pin 28 (VPOS2) can cause undesirable gain loss. When AMP2 is not in use, terminate the RFIN2 and RFOUT2 pins to ground via a 100 pF capacitor and a 50 Ω resistor in series on each pin.

Table 5. Bypass Switch Logic

Mode	$\overline{VSW1}$	VSW1
Undefined	0	0
High Gain Mode	0	1
Low Gain Mode	1	0
Undefined	1	1

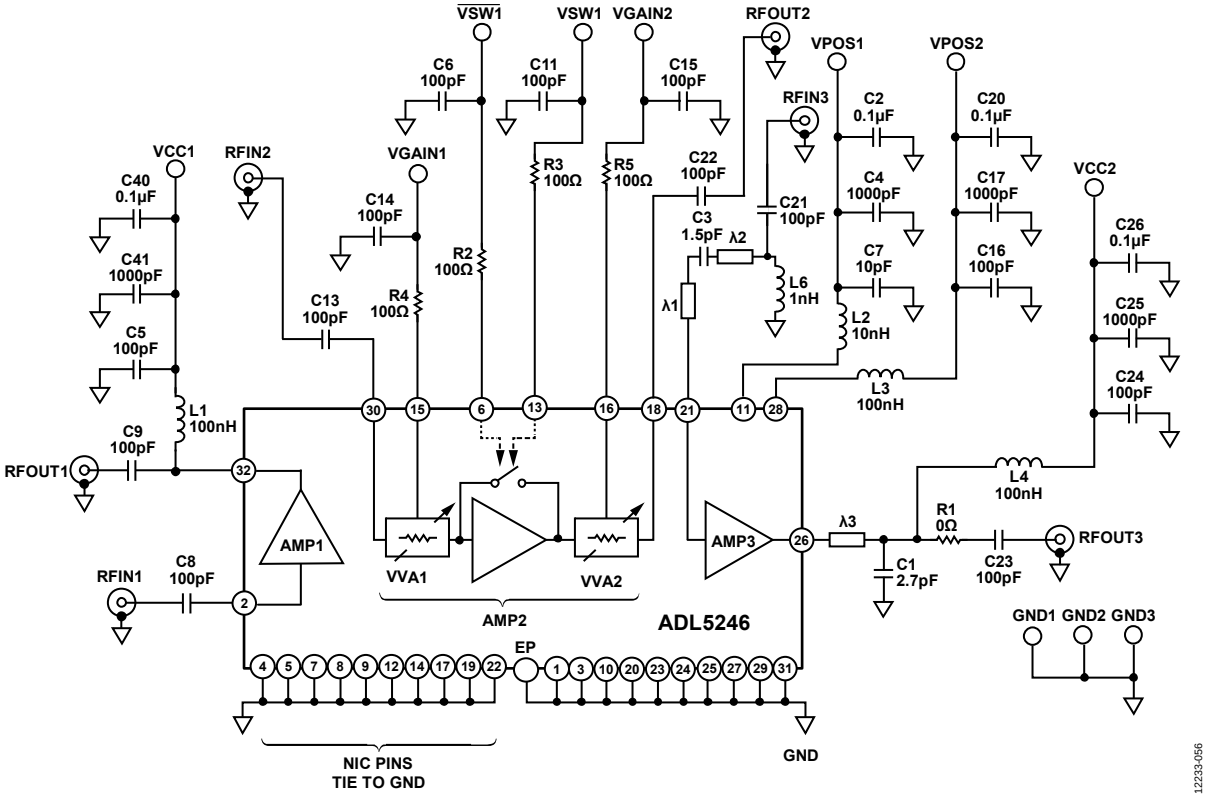

Figure 74. Basic Connections

Amplifier 3 (AMP3)

AMP3 is a broadband 1⁄2 watt driver requiring band specific matching to achieve the specified performance. The input and output are easily matched using a combination of series and shunt capacitors and a microstrip line serving as an inductor.

VPOS2 provides dc bias to the internal bias circuit. Bias for the output stage is supplied to the amplifier via the L4 inductor that is connected to RFOUT3. Therefore, both VPOS2 and VCC2 must be connected to bias to operate AMP3. Capacitors C24, C25, and C26 provide the power supply decoupling. When AMP3 is not in use, terminate the RFIN3 and RFOUT3 pins to ground via a 100 pF capacitor and a 50 Ω resistor in series on each pin. Figure 78 shows the matching components for operation at 2.2 GHz.

Gain Control

The integrated VVAs are controlled by VGAIN1 and VGAIN2. The attenuators maybe controlled independently, if desired. The gain control voltage range is 0 V to 3.3 V. R4 and R5 isolate the gain control circuit from external capacitance. Capacitors C14 and C15 provide decoupling.

VSW1 and $\overline{\text{VSW1}}$ are complementary 3 V logic that is used to control the bypass switch operation and are detailed in Table 5.

R2 and R3 isolate the logic control circuitry from external capacitance. The C6 and C11 capacitors provide decoupling. Figure 9 through Figure 14 show that operating AMP2 at 5 V gives greater gain range; however, operating at 3.3 V gives better phase linearity. Operating at 5 V gives better temperature stability, as shown in Figure 17. It is possible to operate the gain control section at 5 V while operating the remainder of the ADL5246 at 3.3 V for reduced power consumption.

Amplifier 3 Matching

The input and output of the driver amplifier, AMP3, can be matched to 50 Ω using two to three external components. The microstrip transmission line is used as an inductor. The matching component values are listed in Table 6. All capacitors are Murata GRM15 series (0402 size), L4 is a Coilcraft® 0603CS series (0603 size). The 0603 size is preferred over the 0402 size for additional current handling capability. The self resonance of L4 has little bearing on the performance of AMP3, within reasonable limits. For all frequency bands, the placement of C1, C3, and L6 are critical. Table 7 lists the component spacing for C1, C3, and L6. The placement of C3 and R1 are fixed for the matching network on the evaluation board. The spacing is 69 mils and 301 mils, respectively. In the case of 0.75 GHz and 0.9 GHz, a 2 Ω resistor is used in place of the capacitor in the C21 location.

Table 6. Matching Component Values on the ADL5246 Evaluation Board

Frequency (GHz)	C21	C3 (pF)	L6 (nH)	C1 (pF)	C23 (pF)	R1 (Ω)
0.75	2 Ω	9	3.3	8.2	100	0
0.9	2 Ω	6	3.3	6	100	0
1.9	100 pF	2	1	2.7	100	0
2.2	100 pF	1.5	1	2.7	100	0
2.6	100 pF	1.0	1	2.2 F	100	0

Table 7. Matching Component Spacing on the ADL5246 Evaluation Board

Frequency (GHz)	C3: λ1 (mils)	L6: λ2 (mils)	R1 (mils)	C1: λ3 (mils)
0.75	69	24	301	528.4
0.9	69	24	301	422.4
1.9	69	24	301	184.2
2.2	69	24	301	75.4
2.6	69	24	301	75.4

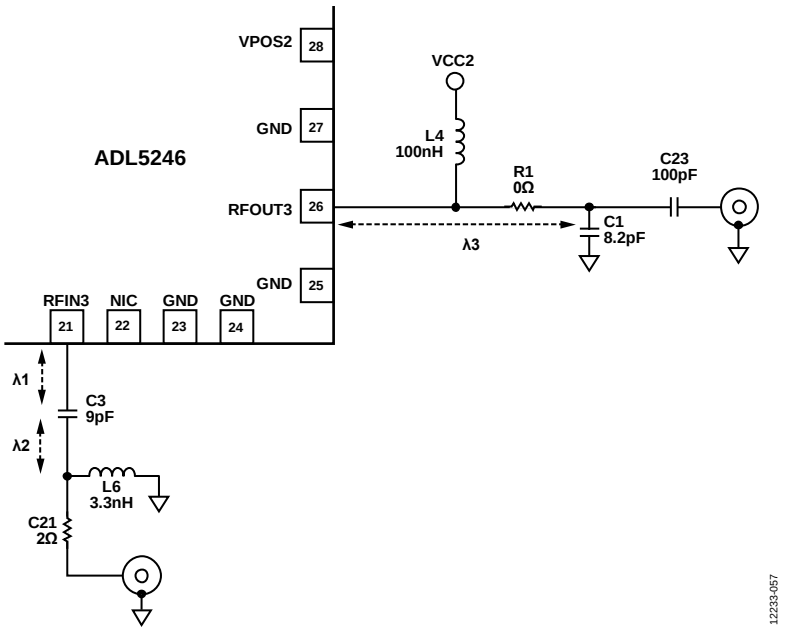

Figure 75. AMP3 Matching Circuit at 0.75 GHz

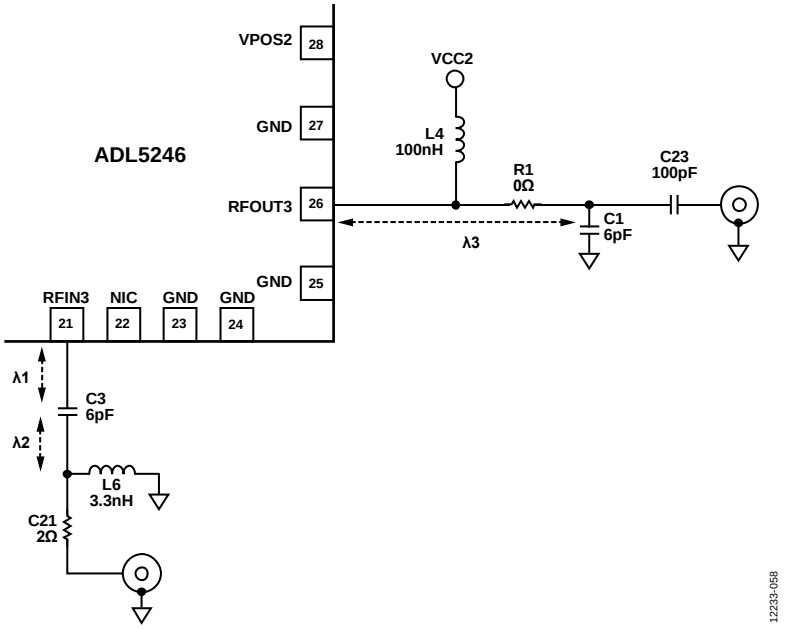

Figure 76. AMP3 Matching Circuit at 0.9 GHz

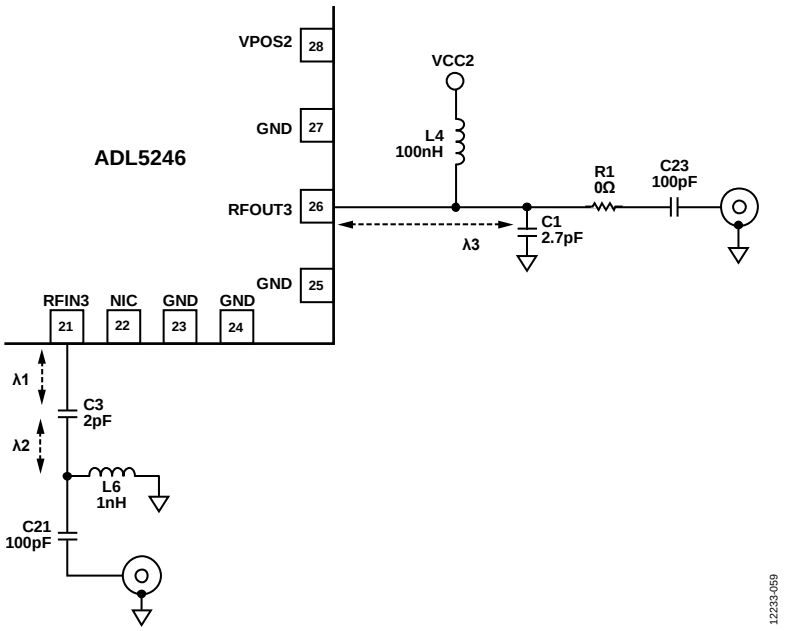

Figure 77. AMP3 Matching Circuit at 1.9 GHz

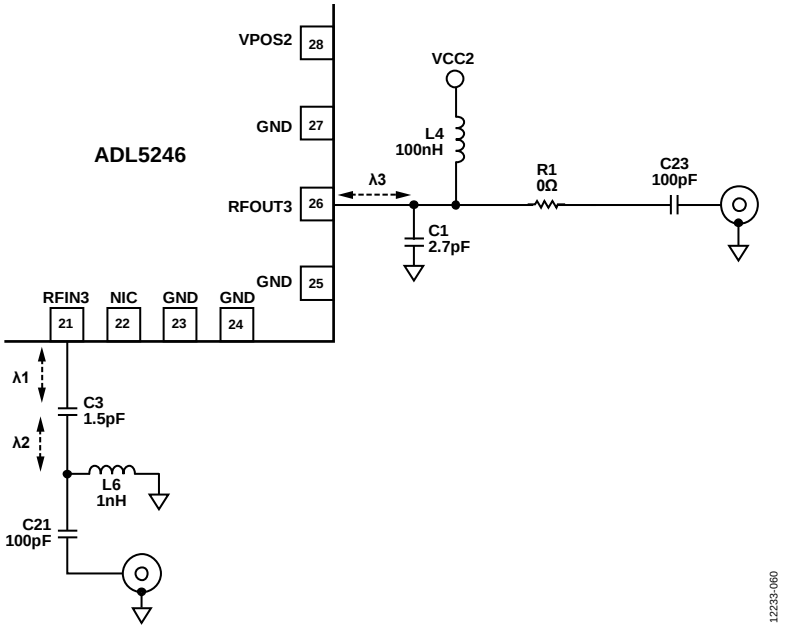

Figure 78. AMP3 Matching Circuit at 2.2 GHz

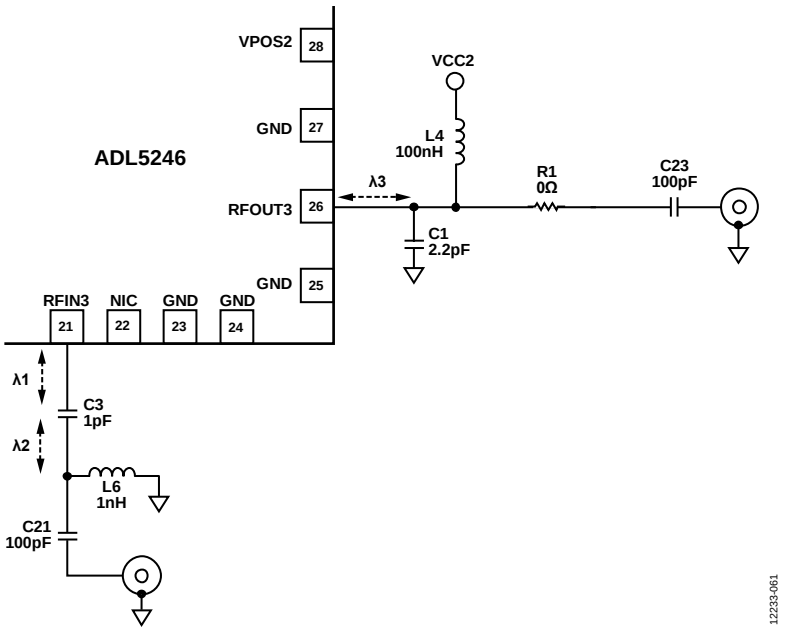

Figure 79. AMP3 Matching Circuit at 2.6 GHz

ERROR VECTOR MAGNITUDE (EVM) PERFORMANCE

EVM is a measure used to quantify the performance of a digital radio transmitter or receiver. A signal received by a receiver has all constellation points at their ideal locations; however, various imperfections in the implementation (such as magnitude imbalance, noise floor, and phase imbalance) cause the actual constellation points to deviate from their ideal locations.

Figure 80 shows the EVM vs. the mean output power for a full chain connection (AMP1 driving AMP2 driving AMP3) operating at 2.2 GHz.

In general, a receiver exhibits three distinct EVM limitations vs. received input signal power.

- At strong signal levels, the distortion components falling in band due to nonlinearities in the device components cause strong degradation to EVM as signal levels increase.
- At medium signal levels, where the signal chain behaves in a linear manner and the signal is well above any notable noise contributions, EVM has a tendency to reach an optimum level determined dominantly by the quadrature accuracy and the precision of the test equipment. As signal levels decrease such that noise is a major contribution, the EVM performance vs. the signal level exhibits a decibel for decibel degradation with decreasing signal level.
- At lower signal levels, where noise proves to be the dominant limitation, the decibel EVM proves to be directly proportional to the SNR.

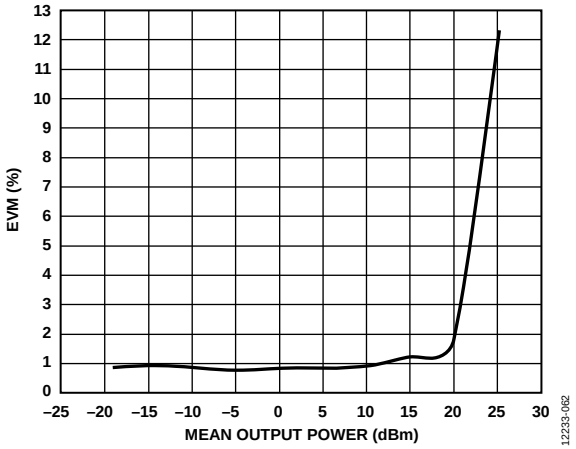

Figure 80. EVM vs. Mean Output Power (P_{OUT}) of Full Chain Connection at 2.2 GHz, 64 QAM, 5 MSPS, α = 0.2 Root Raised Cosine Filter, P_{IN} = −3.7 dBm

THERMAL INFORMATION AND RECOMMENDED PCB LAND PATTERN

The majority of the heat generated during operation is removed via the exposed paddle on the bottom of the package. Figure 81 shows the recommended land pattern for the ADL5246. To minimize thermal impedance, the exposed paddle on the 5 mm × 5 mm LFCSP package is soldered down to a ground plane. To improve thermal dissipation, 25 thermal vias are arranged in a 5 × 5 array under the exposed paddle. The land pattern on the ADL5246 evaluation board provides a thermal resistance (θ_{JA}) of 16.5°C/W.

For the best thermal performance, add as many thermal vias as possible under the exposed pad of the LFCSP. If multiple ground layers exist, tie them together using vias. For more information on land pattern design and layout, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

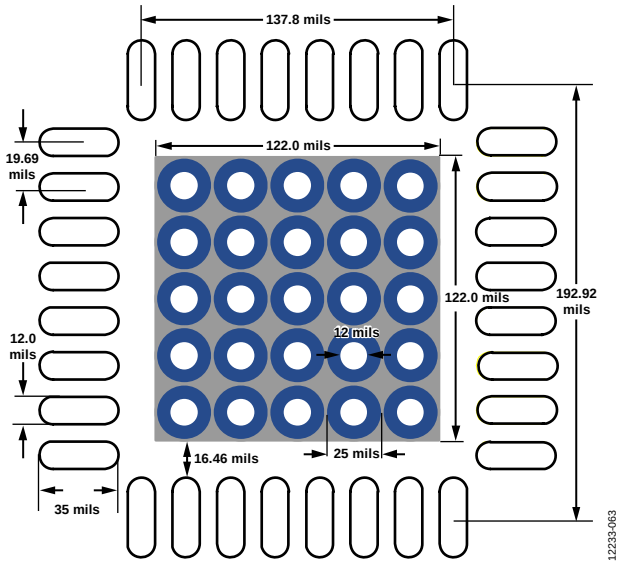

Figure 81. Recommended Land Pattern Under ADL5246

FULL CHAIN OPERATION CONSIDERATIONS

The gain of a cascaded series of amplifiers may differ from a simple summation of the gain of each amplifier in the chain due to impedance matching considerations.

Take the following precautions in the PCB layout of a full chain connection of AMP1 driving AMP2 driving AMP3:

- The VPOS2 pin may couple RF from the three amplifiers into AMP2 and lead to instability. Therefore, it is recommended that the VPOS2 trace be well shielded from the other amplifiers. To accomplish this with the ADL5246 evaluation board, the VPOS2 trace passes through a via to the bottom side of the PCB close to Pin 28.
- At frequencies below 1.5 GHz, there can be more than 40 dB of gain from the full chain connection. With so much gain available, take care to maintain stable operation. Coupling from trace to trace on the PCB can be a significant factor leading to instability. Minimizing coupling between the amplifiers through good PCB layout is important. It can be helpful to reduce the overall gain with resistance before AMP3 (such as R10 on the evaluation board) or to include filters or attenuators between the amplifiers.

EVALUATION BOARD

The schematic of the ADL5246 evaluation board is shown in Figure 82. All RF traces on the evaluation board have a characteristic impedance of 50 Ω and are fabricated from FR408 material. The traces are grounded coplanar waveguide (GCPWG) with a width of 25 mils, spacing to ground of 20 mils, and dielectric thickness of 13 mils. To ensure broadband performance, the inputs and outputs of AMP1, AMP2, and AMP3 are ac-coupled with 100 pF capacitors.

The bias to AMP1 is provided through the L1 inductor. VPOS1 and VPOS2 provide bias to AMP2. The L2 and L3 inductors provide a high impedance to the RF signals that might be present on these pins. The AMP3 bias circuit receives bias from VPOS2. The AMP3 output receives bias through the L1 inductor. Bypassing capacitors are recommended on all supply lines to minimize RF coupling. AMP3 on the ADL5246 evaluation board is configured for 2.2 GHz operation.

The evaluation board is designed so that the gain control pins of AMP2 can be controlled individually or in tandem using VGAIN1 and VGAIN2. The gain range is switched by providing the appropriate logic level to the internal bypass switch via VSW1 and $\overline{\text{VSW1}}$. See Table 5 for switch control logic information.

By default, the ADL5246 evaluation board is configured to evaluate each of the amplifiers individually. To configure the evaluation board to cascade AMP1, AMP2, and AMP3, remove the C9, C13, C21, and C22 blocking capacitors and install the C10, C12, C18, and C19 capacitors. The C33, C34, C31, C32, L8, and L7 components are place holders that allow for adding filters between the gain stages, if required. If a filter is not being used, install a 0 Ω resistor as a jumper in place of L7 and L8. Inductor L5 is provided for optional interstage tuning between RFOUT2 and RFIN3.

Table 8. Evaluation Board Configurations Options

Component	Function	Default Value
VCC1, VCC2 VPOS1, VPOS2, GND1, GND2, GND3	Power supply and ground test loops.	Installed
R6, R7	Jumpers to connect VPOS1 and VPOS2 to the internal power plane.	R6, R7 = 0 Ω
U1	ADL5246ACPZN the device under test.	Installed
RFIN1, RFOUT1, RFIN2, RFOUT2, RFIN3, RFOUT3	RF input and output SMA connecters.	Installed
R8, R9, R10, R11	Jumpers to facilitate the modification of the RF connections between the amplifier blocks.	R8, R9, R10, R11 = 0 Ω
C8, C9	AC coupling capacitors for AMP1.	C8, C9 = 100 pF
C5, C40, C41	Power supply decoupling capacitors for AMP1. Of these three capacitors, C5 must be located closest to the device.	C5 = 100 pF, C40 = 0.1 µF, C41 = 1000 pF
L1	The bias for AMP1 comes through L1 when connected to a 5 V supply. L1 must be high impedance for the frequency of operation, while providing low resistance for the dc current.	L1 = 100 nH
VSW1, $\overline{\text{VSW1}}$	Logic control test loops for the AMP2 integrated bypass switch.	Installed
R2, R3, C6, C11	R2 and R3 isolate the switch control pins from the external capacitance. C6 and C11 provide the decoupling.	R2, R3 = 100 Ω, C6, C11 = 100 pF
VGAIN1, VGAIN2	VGAIN1 and VGAIN2 are test loops to apply the control voltage to the integrated VVAs.	Installed
R4, R5, C14, C15	R4 and R5 isolate the gain control pins from external capacitance. C14 and C15 provide the decoupling.	R4, R5 = 100 Ω, C14, C15 = 100 pF
C13, C22	AC coupling capacitors for AMP2.	C13, C22 = 100 pF
C2, C4, C7, C16, C17, C20	Power supply decoupling capacitors for AMP2. Of these six capacitors, C7 and C16 must be located closest to the device.	C7, C16 = 100 pF, C2, C20 = 0.1 µF, C4, C17 = 1000 pF
L2, L3	The bias for AMP2 comes through L2 and L3 when connected to a 5 V supply. L2 and L3 must be high impedance for the frequency of operation, while providing low resistance for the dc current.	L2 = 10 nH, L3 = 100 nH
L5	L5 is an optional tuning element, which can aid gain, bandwidth, and OP1dB in some circumstances.	L5 = do not install (DNI)
C21, C23	AC coupling capacitors for AMP3.	C21, C23 = 100 pF

Component	Function	Default Value
L6, C3	AMP3 input matching elements.	L6 = 1 nH, C3 = 1.5 pF
C24, C25, C26	Power supply decoupling capacitors for AMP1. Of these three capacitors, C24 must be located closest to the device.	C24 = 100 pF, C25 = 1000 pF, C26 = 0.1 µF
L4	The bias for AMP3 comes through L4 when connected to a 5 V supply. L4 must be high impedance for the frequency of operation, while providing low resistance for the dc current.	L4 = 100 nH
C1, R1	C1 is the output matching element for AMP3. R1 is a placeholder for the optional tuning configurations.	C1 = 2.7 pF, R1 = 0 Ω
C10, C12, C18, C19, C27 to C34, L7, L8	Optional components for loop integration.	C10, C12, C18, C19, C27 to C34, L7, and L8 = DNI

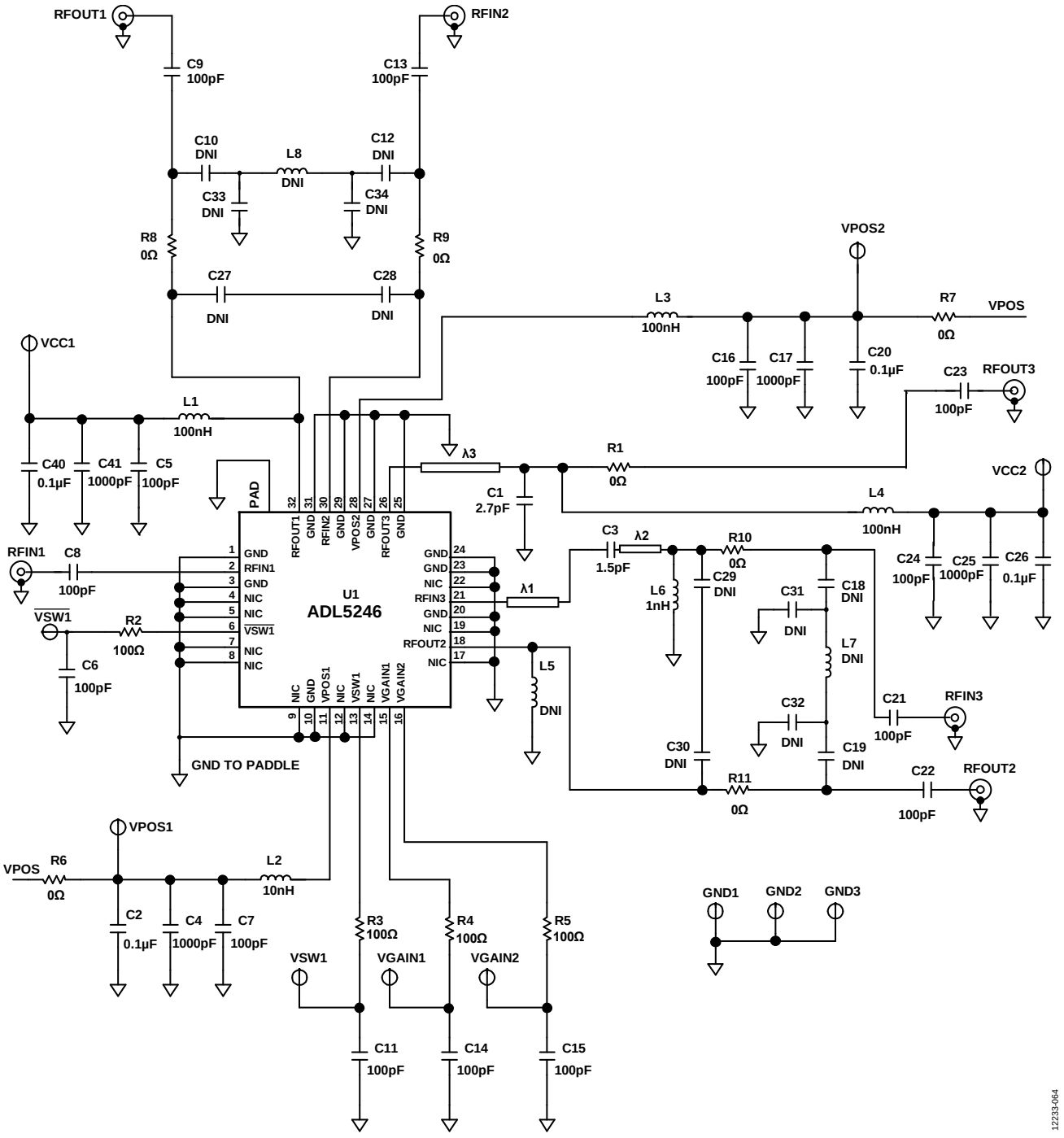

Figure 82. Evaluation Board Schematic

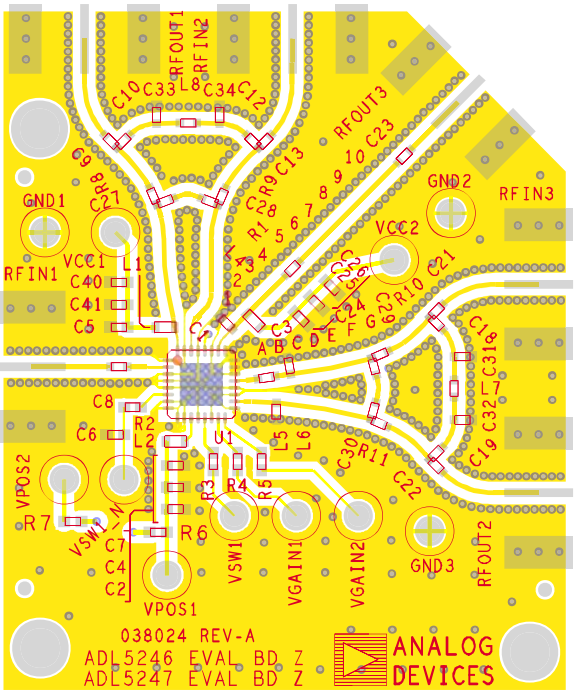

Figure 83. Evaluation Board Layout Top

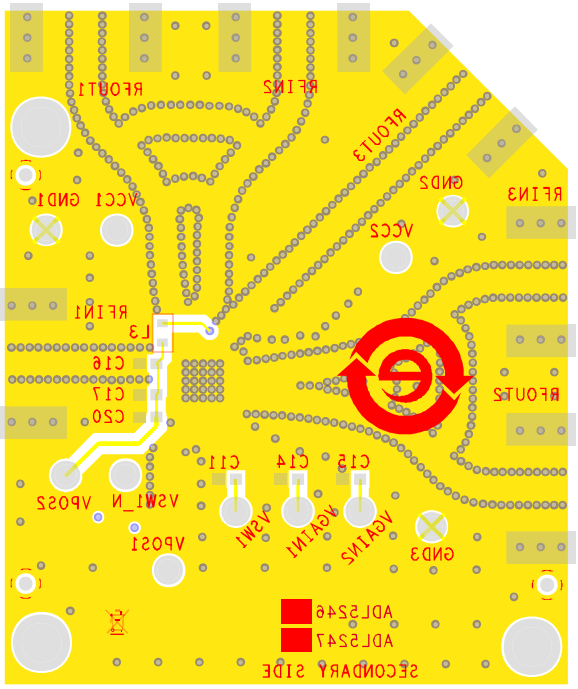

Figure 84. Evaluation Board Layout Bottom

CHARACTERIZATION INFORMATION

The ADL5246 was characterized with multiple samples obtained from three batch lots. Each ADL5246 was attached to its own circuit board that was dedicated and tuned to one of the AMP3 frequency bands. This created a body of boards dedicated to each band. AMP1 and AMP2 operate over a broad frequency range and do not require tuning. Aggregating boards with their AMP3 tuned to the various bands increased the sample size for the characterization of AMP1 and AMP2.

Characterization measurements employed an Agilent Technologies PNA-X vector network analyzer, scalar rack and stack equipment, a noise figure analyzer, and temperature forcing equipment, all under software control.

The typical performance figures represent one typical ADL5246 with performance near the median of a body of available samples. A typical example ADL5246 was selected to represent AMP1 and a different ADL5246 was selected to represent AMP2. Separate examples are used for each of the AMP3 bands; therefore, the AMP3 plots do not show the same ADL5246 board retuned to each band.

The plots show the performance obtained by the typical ADL5246 chosen to demonstrate each amplifier, rather than showing the numerical median of all the samples measured for any one parameter.

The circuit boards used for device characterization are fabricated with Isola FR408, which offers a low coefficient of thermal expansion (CTE) and lower attenuation than standard FR4 without the fragility of Rogers materials.

All three amplifiers are powered on even when not directly in use and this made heat a concern when testing in a high temperature environment. Two 10 mm × 10 mm heat sinks are attached to the back of the circuit board with Arctic Silver thermal adhesive. This lowered the θJA at the top of the package from 16.5°C/W without the heat sink to 12.5°C/W with one, making operating AMP3 at P1dB output power levels in a 105°C ambient temperature possible without reaching the maximum junction temperature of the ADL5246.

OUTLINE DIMENSIONS

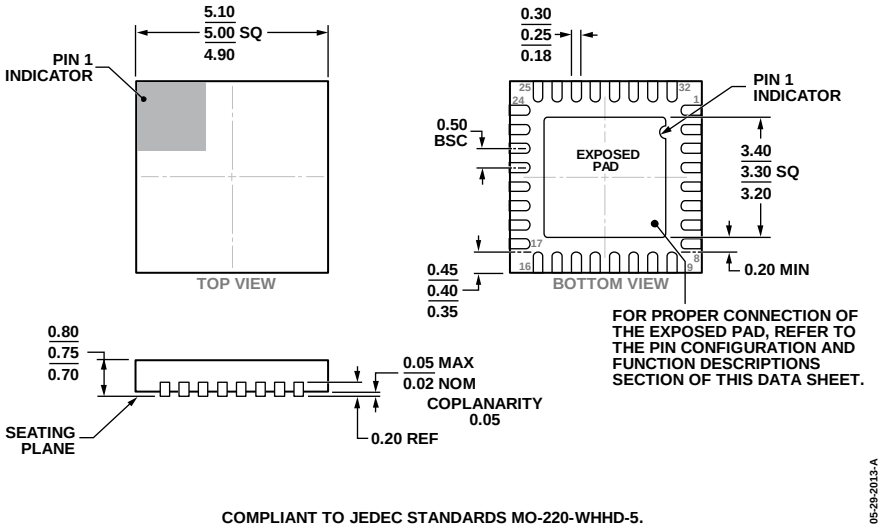

Figure 85. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5mm Body, Very Very Thin Quad
(CP-32-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL5246ACPZN-R7	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-20
ADL5246-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D12233-0-9/15(A)

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Analog Devices Inc.:

ADL5246ACPZN-R7 ADL5246-EVALZ