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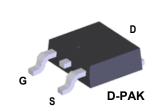
FQD5P10 P-Channel QFET[®] MOSFET -100 V, -3.6 A, 1.05Ω

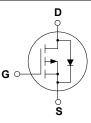
Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor[®]'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.



FQD5P10 P-Channel QFET[®] MOSFET





• Low Gate Charge (Typ. 6.3 nC)

• Low Crss (Typ. 18 pF)

100% avalanche tested

-3.6 A, -100 V, R_{DS(on)} = 1.05 Ω (Max.) @ V_{GS} = -10 V,

Features

I_D = 1.8 A

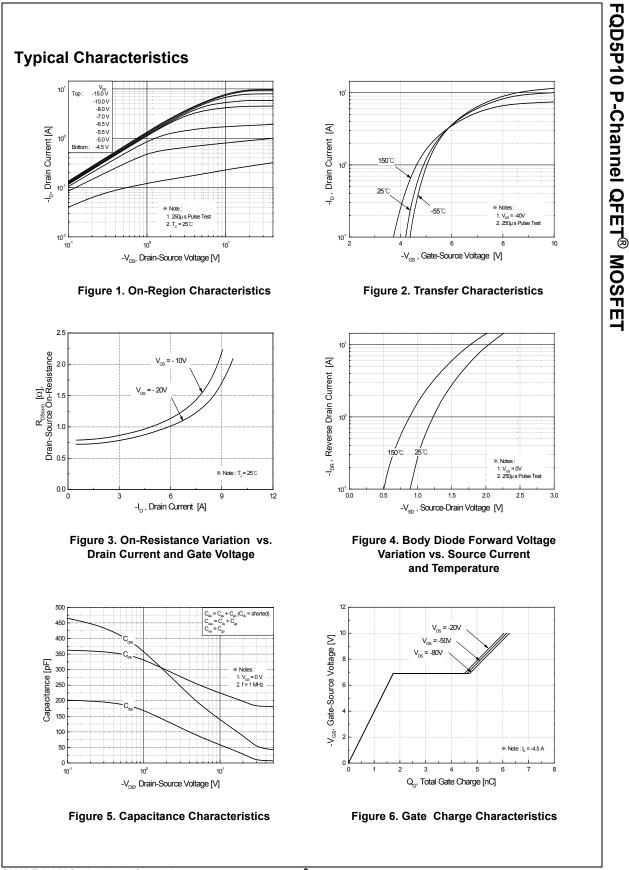
Absolute Maximum Ratings T_c = 25°C unless otherwise noted

Symbol	Parameter			FQD5P10	Unit
V _{DSS}	Drain-Source V	/oltage		-100	V
I _D	Drain Current - Continuous ($T_C = 25^{\circ}C$)		°C)	-3.6	A
		- Continuous (T _C = 10	0°C)	-2.28	A
I _{DM}	Drain Current	- Pulsed	(Note 1)	-14.4	A
V _{GSS}	Gate-Source Voltage			± 30	V
E _{AS}	Single Pulsed Avalanche Energy		(Note 2)	55	mJ
I _{AR}	Avalanche Current		(Note 1)	-3.6	А
E _{AR}	Repetitive Avalanche Energy		(Note 1)	2.5	mJ
dv/dt	Peak Diode Re	covery dv/dt	(Note 3)	-6.0	V/ns
P _D	Power Dissipation (T _A = 25°C) *			2.5	W
	Power Dissipation (T _C = 25°C)			25	W
	- Derate above 25°C			0.2	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +150	°C
TL	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C

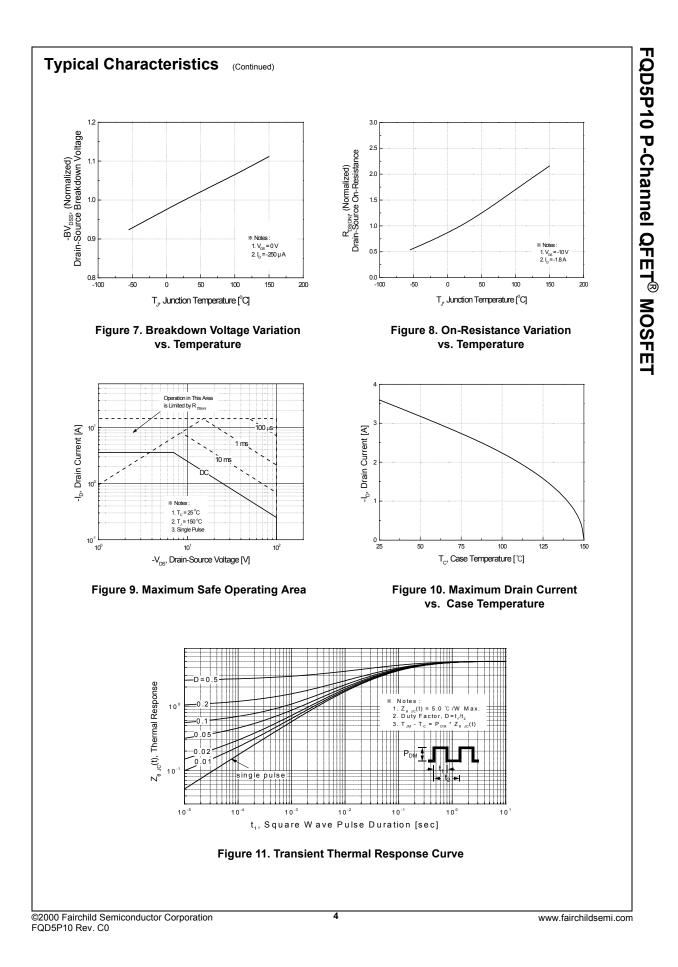
Thermal Characteristics

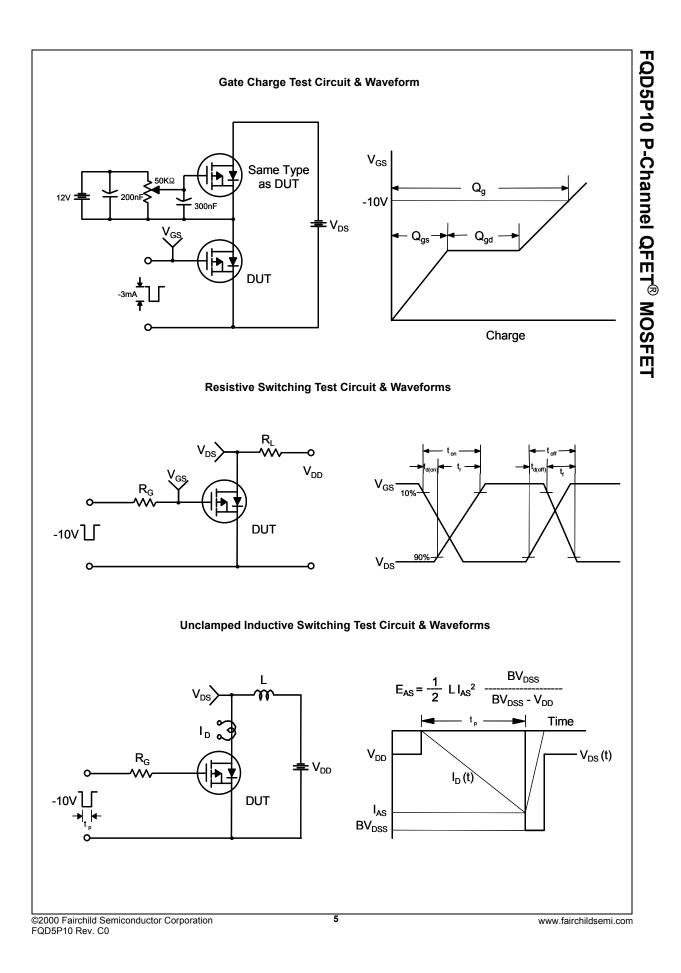
Symbol	Parameter	FQD5P10	Unit
$R_{ ext{ heta}JC}$	Thermal Resistance, Junction-to-Case, Max.	5.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	110	°C/W

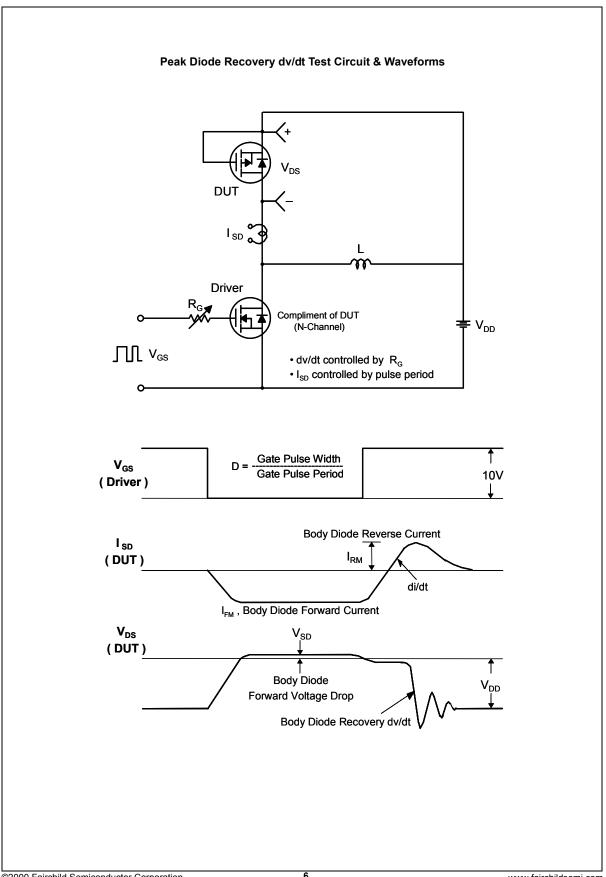
	Parameter	Test Conditions	Min	Тур	Мах	Unit
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-100			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = -250 \ \mu$ A, Referenced to 25°	C	-0.1		V/°C
IDSS		V _{DS} = -100 V, V _{GS} = 0 V			-1	μA
	Zero Gate Voltage Drain Current	$V_{DS} = -80 \text{ V}, \text{ T}_{C} = 125^{\circ}\text{C}$			-10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = -30 V, V _{DS} = 0 V			-100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
On Cha	racteristics		i			
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-2.0		-4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	$V_{\rm GS}$ = -10 V, I _D = -1.8 A		0.82	1.05	Ω
9 _{FS}	Forward Transconductance	V _{DS} = -40 V, I _D = -1.8 A		2.3		S
C _{iss}	ic Characteristics Input Capacitance	V _{DS} = -25 V, V _{GS} = 0 V,		190	250	pF
		V_{DS} = -25 V, V_{GS} = 0 V,				•
C _{oss} C _{rss}	Output Capacitance Reverse Transfer Capacitance	f = 1.0 MHz		70 18	90 25	pF pF
	ing Characteristics	1		1	1	1
t _{d(on)}	Turn-On Delay Time	V _{DD} = -50 V, I _D = -4.5 A,		9	30	ns
t _r	Turn-On Rise Time	R _G = 25 Ω		70	150	ns
t _{d(off)}	Turn-Off Delay Time	(Note	4)	12	35	ns
t _f	Turn-Off Fall Time			30	70	ns
Q _g	Total Gate Charge	V _{DS} = -80 V, I _D = -4.5 A,		6.3	8.2	nC
()	Gate-Source Charge	V _{GS} = -10 V		1.7		nC
Q _{gs}	Gate-Drain Charge	(Note	4)	3.0		nC
Q _{gd}						
Q _{gd}	ource Diode Characteristics a	nd Maximum Ratings				
Q _{gd} Drain-S	ource Diode Characteristics an Maximum Continuous Drain-Source Dio				-3.6	A
Q _{gd} Drain-S		ode Forward Current			-3.6 -14.4	A A
Q _{gd} Drain-S	Maximum Continuous Drain-Source Dic	ode Forward Current				
Q _{gd} Drain-S	Maximum Continuous Drain-Source Dio Maximum Pulsed Drain-Source Diode F	ode Forward Current	 		-14.4	Α

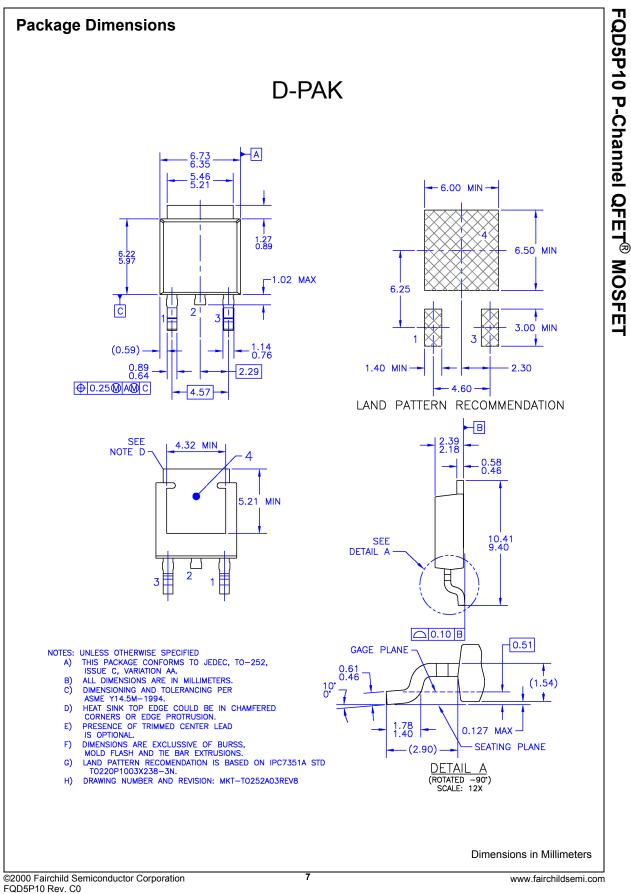


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