

Kinetis KL16 Sub-Family

48 MHz Cortex-M0+ Based Microcontroller

Designed with efficiency in mind. Compatible with all other Kinetis L families as well as Kinetis K1x family. General purpose MCU featuring market leading ultra low-power to provide developers an appropriate entry-level 32-bit solution.

This product offers:

- Run power consumption down to 50 μ A/MHz in very low power run mode
- Static power consumption down to 2 μ A with full state retention and 4.5 μ s wakeup
- Ultra-efficient Cortex-M0+ processor running up to 48 MHz with industry leading throughput
- Memory option is up to 256 KB flash and 32 KB RAM
- Energy-saving architecture is optimized for low power with 90nm TFS technology, clock and power gating techniques, and zero wait state flash memory controller

MKL16Z256VLH4
MKL16Z256VMP4



64-pin LQFP (LH) 10 x 10 x 1.4 Pitch 0.5 mm
64-pin MAPBGA (MP) 5 x 5 x 1.23 Pitch 0.5 mm

Performance

- 48 MHz ARM[®] Cortex[®]-M0+ core

Memories and memory interfaces

- Up to 256 KB program flash memory
- Up to 32 KB SRAM

System peripherals

- Nine low-power modes to provide power optimization based on application requirements
- COP Software watchdog
- 4-channel DMA controller, supporting up to 63 request sources
- Low-leakage wakeup unit
- SWD debug interface and Micro Trace Buffer
- Bit Manipulation Engine

Clocks

- 32 kHz to 40 kHz or 3 MHz to 32 MHz crystal oscillator
- Multi-purpose clock source

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

Human-machine interface

- Low-power hardware touch sensor interface (TSI)
- Up to 54 general-purpose input/output (GPIO)

Communication interfaces

- Two 16-bit SPI modules
- I2S (SAI) module
- One low power UART module
- Two UART modules
- Two I2C module

Analog Modules

- 16-bit SAR ADC
- 12-bit DAC
- Analog comparator (CMP) containing a 6-bit DAC and programmable reference input

Timers

- Six channel Timer/PWM (TPM)
- Two 2-channel Timer/PWM modules
- Periodic interrupt timers
- 16-bit low-power timer (LPTMR)
- Real time clock

Security and integrity modules

- 80-bit unique identification number per chip

Ordering Information ¹

| Part Number | Memory | | Maximum number of I/O's |
|---------------|------------|-----------|-------------------------|
| | Flash (KB) | SRAM (KB) | |
| MKL16Z256VLH4 | 256 | 32 | 54 |
| MKL16Z256VMP4 | 256 | 32 | 54 |

1. To confirm current availability of orderable part numbers, go to <http://www.freescale.com> and perform a part number search.

Related Resources

| Type | Description | Resource |
|------------------|--|--|
| Selector Guide | The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. | Solution Advisor |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | KL16P64M48SF4RM ¹ |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | KL16P64M48SF4 ¹ |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. | KINETIS_L_xN40H ² |
| Package drawing | Package dimensions are provided in package drawings. | LQFP 64-pin: 98ASS23234W ¹ MAPBGA 64-pin: 98ASA00420D ¹ |

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.
2. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term with the "x" replaced by the revision of the device you are using.

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1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T _{STG} | Storage temperature | -55 | 150 | °C | 1 |
| T _{SDR} | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Table 3. ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|-------|-------|------|-------|
| V _{HBM} | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| V _{CDM} | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| I _{LAT} | Latch-up current at ambient temperature of 105 °C | -100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|-----------|---|----------------|----------------|------|
| V_{DD} | Digital supply voltage | -0.3 | 3.8 | V |
| I_{DD} | Digital supply current | — | 120 | mA |
| V_{IO} | IO pin input voltage | -0.3 | $V_{DD} + 0.3$ | V |
| I_D | Instantaneous maximum current single pin limit (applies to all port pins) | -25 | 25 | mA |
| V_{DDA} | Analog supply voltage | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V |

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

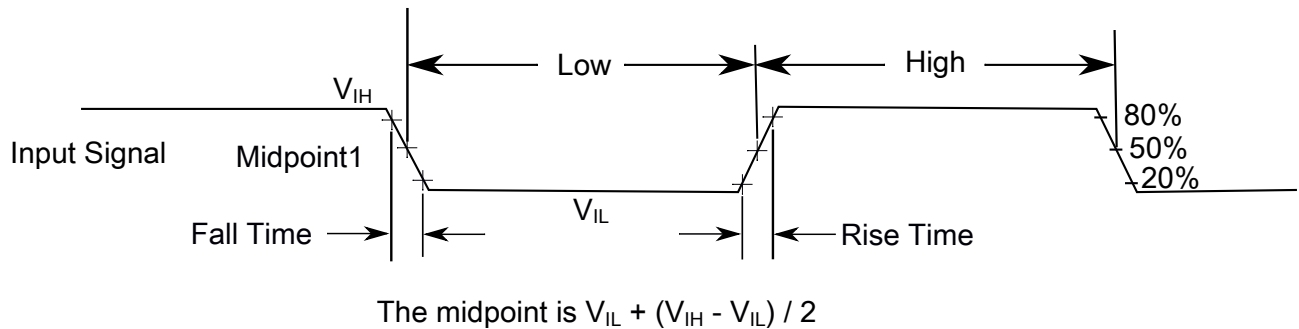


Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- $C_L=30$ pF loads
- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------------------|---|---|---|--------|-------|
| V_{DD} | Supply voltage | 1.71 | 3.6 | V | |
| V_{DDA} | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} - V_{DDA}$ | V_{DD} -to- V_{DDA} differential voltage | -0.1 | 0.1 | V | |
| $V_{SS} - V_{SSA}$ | V_{SS} -to- V_{SSA} differential voltage | -0.1 | 0.1 | V | |
| V_{IH} | Input high voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | $0.7 \times V_{DD}$ $0.75 \times V_{DD}$ | — — | V V | |
| V_{IL} | Input low voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | — — | $0.35 \times V_{DD}$ $0.3 \times V_{DD}$ | V V | |
| V_{HYS} | Input hysteresis | $0.06 \times V_{DD}$ | — | V | |
| I_{ICIO} | IO pin negative DC injection current — single pin <ul style="list-style-type: none"> $V_{IN} < V_{SS}-0.3\text{V}$ | -3 | — | mA | 1 |
| I_{ICcont} | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins <ul style="list-style-type: none"> Negative current injection | -25 | — | mA | |
| V_{ODPU} | Open drain pullup voltage level | V_{DD} | V_{DD} | V | 2 |
| V_{RAM} | V_{DD} voltage required to retain RAM | 1.2 | — | V | |

- All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} ($= V_{SS}-0.3\text{ V}$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|$.
- Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements

Table 6. V_{DD} supply LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------|---|------|------|------|------|-------|
| V_{POR} | Falling V_{DD} POR detect voltage | 0.8 | 1.1 | 1.5 | V | — |
| V_{LVDH} | Falling low-voltage detect threshold — high range (LVDV = 01) | 2.48 | 2.56 | 2.64 | V | — |
| | Low-voltage warning thresholds — high range | | | | | 1 |

Table continues on the next page...

Table 6. V_{DD} supply LVD and POR operating requirements (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------|---|------|------|------|------|-------|
| V _{LVW1H} | <ul style="list-style-type: none"> Level 1 falling (LVWV = 00) | 2.62 | 2.70 | 2.78 | V | |
| V _{LVW2H} | <ul style="list-style-type: none"> Level 2 falling (LVWV = 01) | 2.72 | 2.80 | 2.88 | V | |
| V _{LVW3H} | <ul style="list-style-type: none"> Level 3 falling (LVWV = 10) | 2.82 | 2.90 | 2.98 | V | |
| V _{LVW4H} | <ul style="list-style-type: none"> Level 4 falling (LVWV = 11) | 2.92 | 3.00 | 3.08 | V | |
| V _{HYSH} | Low-voltage inhibit reset/recover hysteresis — high range | — | ±60 | — | mV | — |
| V _{LVDL} | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | — |
| V _{LVW1L} | Low-voltage warning thresholds — low range <ul style="list-style-type: none"> Level 1 falling (LVWV = 00) | 1.74 | 1.80 | 1.86 | V | 1 |
| V _{LVW2L} | <ul style="list-style-type: none"> Level 2 falling (LVWV = 01) | 1.84 | 1.90 | 1.96 | V | |
| V _{LVW3L} | <ul style="list-style-type: none"> Level 3 falling (LVWV = 10) | 1.94 | 2.00 | 2.06 | V | |
| V _{LVW4L} | <ul style="list-style-type: none"> Level 4 falling (LVWV = 11) | 2.04 | 2.10 | 2.16 | V | |
| V _{HYSL} | Low-voltage inhibit reset/recover hysteresis — low range | — | ±40 | — | mV | — |
| V _{BG} | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | — |
| t _{LPO} | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | — |

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|--|--|------------|--------|-------|
| V _{OH} | Output high voltage — Normal drive pad (except RESET_b) <ul style="list-style-type: none"> 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -5 mA 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -2.5 mA | V _{DD} - 0.5 V _{DD} - 0.5 | — — | V V | 1, 2 |
| V _{OH} | Output high voltage — High drive pad (except RESET_b) <ul style="list-style-type: none"> 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20 mA 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10 mA | V _{DD} - 0.5 V _{DD} - 0.5 | — — | V V | 1, 2 |
| I _{OHT} | Output high current total for all ports | — | 100 | mA | |
| V _{OL} | Output low voltage — Normal drive pad <ul style="list-style-type: none"> 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA | — — | 0.5 0.5 | V V | 1 |

Table continues on the next page...

Table 7. Voltage and current operating behaviors (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|------|-------|------|-------|
| V _{OL} | Output low voltage — High drive pad <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA | — | 0.5 | V | 1 |
| | | — | 0.5 | V | |
| I _{OLT} | Output low current total for all ports | — | 100 | mA | |
| I _{IN} | Input leakage current (per pin) for full temperature range | — | 1 | μA | 3 |
| I _{IN} | Input leakage current (per pin) at 25 °C | — | 0.025 | μA | 3 |
| I _{IN} | Input leakage current (total all pins) for full temperature range | — | | μA | 3 |
| I _{OZ} | Hi-Z (off-state) leakage current (per pin) | — | 1 | μA | |
| R _{PU} | Internal pullup resistors | 20 | 50 | kΩ | 4 |

1. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at V_{DD} = 3.6 V
4. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx→RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Table 8. Power mode transition operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|--|------|------|------|------|-------|
| t _{POR} | After a POR event, amount of time from the point V _{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip. <ul style="list-style-type: none"> • VLLS0 → RUN | — | — | 300 | μs | 1 |
| | | — | 113 | 124 | μs | |

Table continues on the next page...

Table 8. Power mode transition operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|---------------|------|------|------|------|-------|
| | • VLLS1 → RUN | — | 112 | 124 | μs | |
| | • VLLS3 → RUN | — | 53 | 60 | μs | |
| | • LLS → RUN | — | 4.5 | 5.0 | μs | |
| | • VLPS → RUN | — | 4.5 | 5.0 | μs | |
| | • STOP → RUN | — | 4.5 | 5.0 | μs | |

1. Normal boot (FTFA_FOPT[LPBOOT]=11).

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 9. Power consumption operating behaviors

| Symbol | Description | Typ. | Max | Unit | Note | |
|--------------------------|--|-----------|----------|------|------|------|
| I _{DDA} | Analog supply current | — | See note | mA | 1 | |
| I _{DD_RUNCO_CM} | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus disabled, LPTMR running using 4 MHz internal reference clock, CoreMark® benchmark code executing from flash, at 3.0 V | — | 6.7 | mA | 2 | |
| I _{DD_RUNCO} | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash, at 3.0 V | — | 4.5 | 5.1 | mA | 3 |
| I _{DD_RUN} | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code executing from flash | at 1.8 V | 5.6 | 6.3 | mA | 3 |
| | | at 3.0 V | 5.4 | 6.0 | mA | |
| I _{DD_RUN} | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 1.8 V | — | 6.9 | 7.3 | mA | 3, 4 |
| | | at 25 °C | 6.9 | 7.1 | mA | |
| | | at 125 °C | 7.3 | 7.6 | mA | |

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

| Symbol | Description | | Typ. | Max | Unit | Note |
|---------------------------|---|-----------|-------|--------|------|------|
| I _{DD_WAIT} | Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled, at 3.0 V | — | 2.9 | 3.5 | mA | 3 |
| I _{DD_WAIT} | Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled | — | 2.2 | 2.8 | mA | 3 |
| I _{DD_PSTOP2} | Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus, at 3.0 V | — | 1.6 | 2.1 | mA | 3 |
| I _{DD_VLPRCO_CM} | Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, LPTMR running with 4 MHz internal reference clock, CoreMark benchmark code executing from flash, at 3.0 V | — | 798 | — | μA | 5 |
| I _{DD_VLPRCO} | Very low power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code executing from flash, at 3.0 V | — | 167 | 336 | μA | 6 |
| I _{DD_VLPR} | Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code executing from flash, at 3.0 V | — | 192 | 354 | μA | 6 |
| I _{DD_VLPR} | Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 3.0 V | — | 257 | 431 | μA | 4, 6 |
| I _{DD_VLPW} | Very low power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled, at 3.0 V | — | 112 | 286 | μA | 6 |
| I _{DD_STOP} | Stop mode current at 3.0 V | at 25 °C | 306 | 328 | μA | — |
| | | at 50 °C | 322 | 349 | μA | |
| | | at 70 °C | 348 | 382 | μA | |
| | | at 85 °C | 384 | 433 | μA | |
| | | at 105 °C | 481 | 578 | μA | |
| I _{DD_VLPS} | Very-low-power stop mode current at 3.0 V | at 25 °C | 2.71 | 5.03 | μA | — |
| | | at 50 °C | 7.05 | 11.94 | μA | |
| | | at 70 °C | 15.80 | 26.87 | μA | |
| | | at 85 °C | 29.60 | 47.30 | μA | |
| | | at 105 °C | 69.13 | 106.04 | μA | |

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

| Symbol | Description | | Typ. | Max | Unit | Note |
|-----------------------|---|-----------|-------|-------|------|------|
| I _{DD_ULLS} | Low leakage stop mode current at 3.0 V | at 25 °C | 2.00 | 2.7 | μA | — |
| | | at 50 °C | 3.96 | 5.14 | μA | |
| | | at 70 °C | 7.77 | 10.71 | μA | |
| | | at 85 °C | 14.15 | 18.79 | μA | |
| | | at 105 °C | 33.20 | 43.67 | μA | |
| I _{DD_VLLS3} | Very low-leakage stop mode 3 current at 3.0 V | at 25 °C | 1.5 | 2.2 | μA | — |
| | | at 50 °C | 2.83 | 3.55 | μA | |
| | | at 70 °C | 5.53 | 7.26 | μA | |
| | | at 85 °C | 9.92 | 12.71 | μA | |
| | | at 105 °C | 22.90 | 29.23 | μA | |
| I _{DD_VLLS1} | Very low-leakage stop mode 1 current at 3.0V | at 25 °C | 0.71 | 1.2 | μA | — |
| | | at 50 °C | 1.27 | 1.9 | μA | |
| | | at 70 °C | 2.48 | 3.51 | μA | |
| | | at 85 °C | 4.65 | 6.29 | μA | |
| | | at 105 °C | 11.55 | 14.34 | μA | |
| I _{DD_VLLS0} | Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V | at 25 °C | 0.41 | 0.9 | μA | — |
| | | at 50 °C | 0.96 | 1.56 | μA | |
| | | at 70 °C | 2.17 | 3.1 | μA | |
| | | at 85 °C | 4.35 | 5.32 | μA | |
| | | at 105 °C | 11.24 | 14.00 | μA | |
| I _{DD_VLLS0} | Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V | at 25 °C | 0.23 | 0.69 | μA | 7 |
| | | at 50 °C | 0.77 | 1.35 | μA | |
| | | at 70 °C | 1.98 | 2.52 | μA | |
| | | at 85 °C | 4.16 | 5.14 | μA | |
| | | at 105 °C | 11.05 | 13.80 | μA | |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for PEE mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
6. MCG configured for BLPI mode.
7. No brownout.

Table 10. Low power mode peripheral adders — typical value

| Symbol | Description | Temperature (°C) | | | | | | Unit | |
|----------------------------|--|---|-----|-----|-----|-----|-----|------|----|
| | | -40 | 25 | 50 | 70 | 85 | 105 | | |
| I _{IREFSTEN4MHz} | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled. | 56 | 56 | 56 | 56 | 56 | 56 | μA | |
| I _{IREFSTEN32KHz} | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled. | 52 | 52 | 52 | 52 | 52 | 52 | μA | |
| I _{EREFSTEN4MHz} | External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled. | 206 | 228 | 237 | 245 | 251 | 258 | μA | |
| I _{EREFSTEN32KHz} | External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. | VLLS1 | 440 | 490 | 540 | 560 | 570 | 580 | nA |
| | | VLLS3 | 440 | 490 | 540 | 560 | 570 | 580 | |
| | | LLS | 490 | 490 | 540 | 560 | 570 | 680 | |
| | | VLPS | 510 | 560 | 560 | 560 | 610 | 680 | |
| | | STOP | 510 | 560 | 560 | 560 | 610 | 680 | |
| I _{CMP} | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 22 | 22 | 22 | 22 | 22 | 22 | μA | |
| I _{RTC} | RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption. | 432 | 357 | 388 | 475 | 532 | 810 | nA | |
| I _{UART} | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. | MCGIRCLK (4 MHz internal reference clock) | 66 | 66 | 66 | 66 | 66 | 66 | μA |
| | | OSCERCLK (4 MHz external crystal) | 214 | 237 | 246 | 254 | 260 | 268 | |
| I _{TPM} | TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. | MCGIRCLK (4 MHz internal reference clock) | 86 | 86 | 86 | 86 | 86 | 86 | μA |
| | | OSCERCLK (4 MHz external crystal) | 235 | 256 | 265 | 274 | 280 | 287 | |

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value (continued)

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|------------------|--|------------------|-----|-----|-----|-----|-----|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| I _{BG} | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode. | 45 | 45 | 45 | 45 | 45 | 45 | μA |
| I _{ADC} | ADC peripheral adder combining the measured values at V _{DD} and V _{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 366 | 366 | 366 | 366 | 366 | 366 | μA |

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

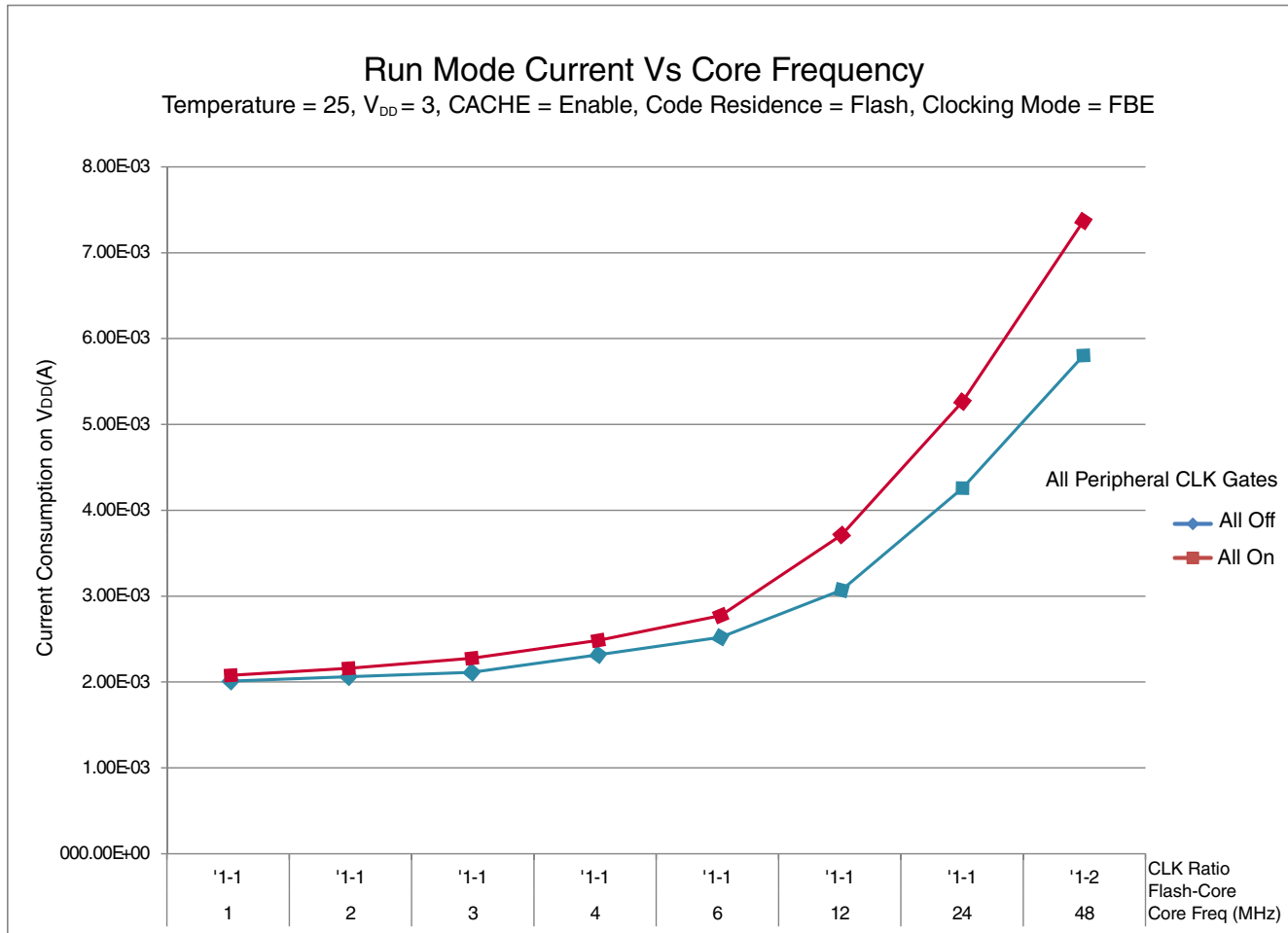


Figure 3. Run mode supply current vs. core frequency

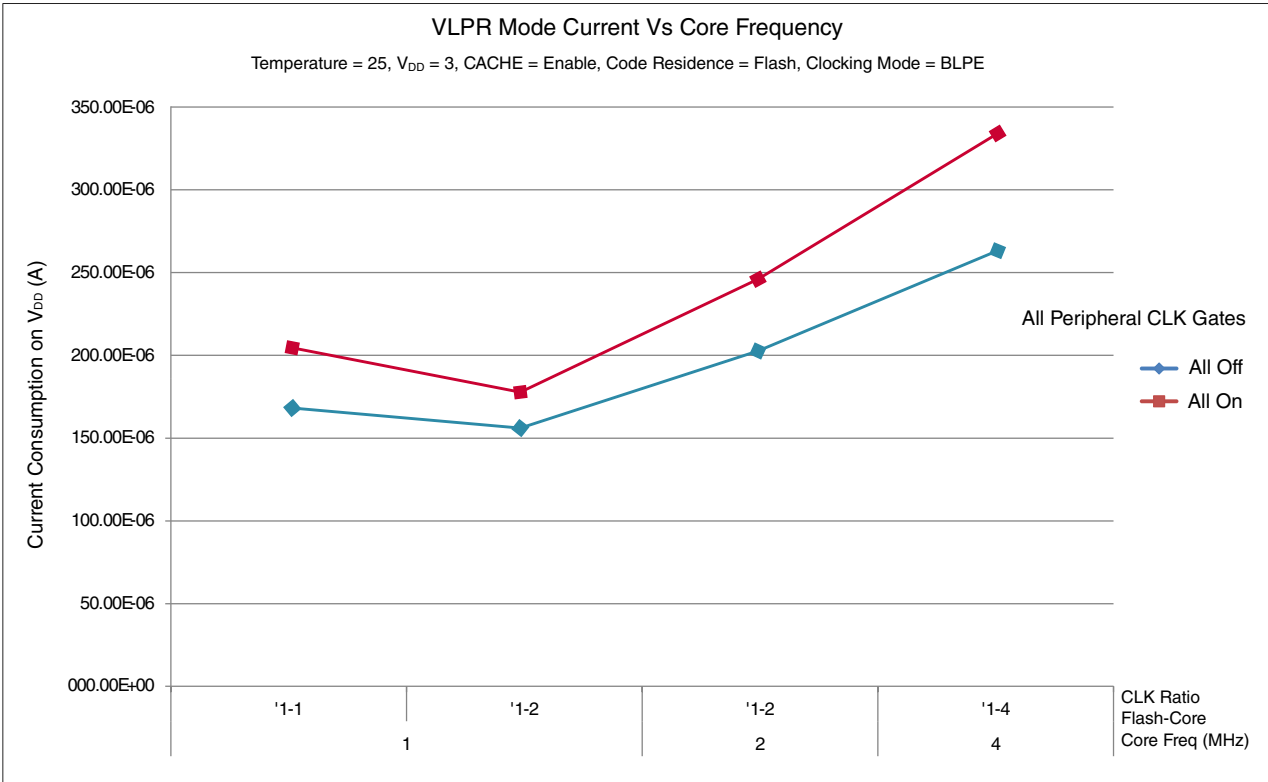


Figure 4. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 11. EMC radiated emissions operating behaviors

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|---------------------|------------------------------------|----------------------|------|------|-------|
| V _{RE1} | Radiated emissions voltage, band 1 | 0.15–50 | 12 | dBμV | 1,2 |
| V _{RE2} | Radiated emissions voltage, band 2 | 50–150 | 8 | dBμV | |
| V _{RE3} | Radiated emissions voltage, band 3 | 150–500 | 7 | dBμV | |
| V _{RE4} | Radiated emissions voltage, band 4 | 500–1000 | 4 | dBμV | |
| V _{RE_IEC} | IEC level | 0.15–1000 | M | — | 2,3 |

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 8 MHz (crystal), f_{SYS} = 48 MHz, f_{BUS} = 24 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 12. Capacitance attributes

| Symbol | Description | Min. | Max. | Unit |
|----------|-------------------|------|------|------|
| C_{IN} | Input capacitance | — | 7 | pF |

2.3 Switching specifications

2.3.1 Device clock specifications

Table 13. Device clock specifications

| Symbol | Description | Min. | Max. | Unit |
|----------------------------------|---|------|------|------|
| Normal run mode | | | | |
| f_{SYS} | System and core clock | — | 48 | MHz |
| f_{BUS} | Bus clock | — | 24 | MHz |
| f_{FLASH} | Flash clock | — | 24 | MHz |
| f_{LPTMR} | LPTMR clock | — | 24 | MHz |
| VLPR and VLPS modes ¹ | | | | |
| f_{SYS} | System and core clock | — | 4 | MHz |
| f_{BUS} | Bus clock | — | 1 | MHz |
| f_{FLASH} | Flash clock | — | 1 | MHz |
| f_{LPTMR} | LPTMR clock ² | — | 24 | MHz |
| f_{ERCLK} | External reference clock | — | 16 | MHz |
| f_{LPTMR_ERCLK} | LPTMR external reference clock | — | 16 | MHz |
| $f_{osc_hi_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | — | 16 | MHz |
| f_{TPM} | TPM asynchronous clock | — | 8 | MHz |
| f_{UART0} | UART0 asynchronous clock | — | 8 | MHz |

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 14. General switching specifications

| Description | Min. | Max. | Unit | Notes |
|---|------|------|------------------|-------|
| GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1 |
| External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 2 |
| GPIO pin interrupt pulse width — Asynchronous path | 16 | — | ns | 2 |
| Port rise and fall time | — | 36 | ns | 3 |

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 15. Thermal operating requirements

| Symbol | Description | Min. | Max. | Unit |
|----------------|--------------------------|------|------|------|
| T _J | Die junction temperature | −40 | 125 | °C |
| T _A | Ambient temperature | −40 | 105 | °C |

2.4.2 Thermal attributes

Table 16. Thermal attributes

| Board type | Symbol | Description | 64 LQFP | 64 MAPBGA | Unit | Notes |
|-------------------|------------------|---|---------|-----------|------|-------|
| Single-layer (1S) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 69 | 49.8 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 51 | 42.3 | °C/W | |
| Single-layer (1S) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 58 | 40.9 | °C/W | |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 44 | 37.7 | °C/W | |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 33 | 39.2 | °C/W | 2 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 19 | 50.3 | °C/W | 3 |
| — | Ψ_{JT} | Thermal characterization parameter, junction to package top outside center (natural convection) | 4 | 2.2 | °C/W | 4 |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

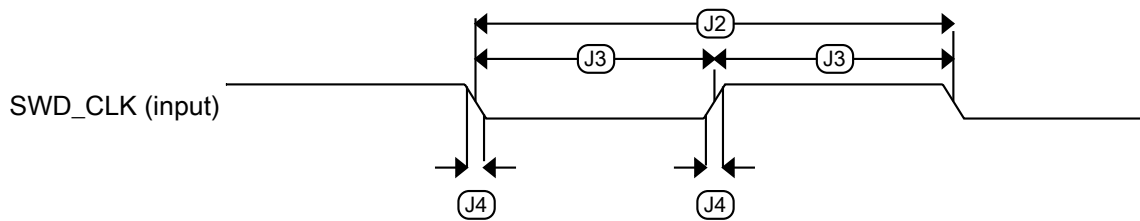
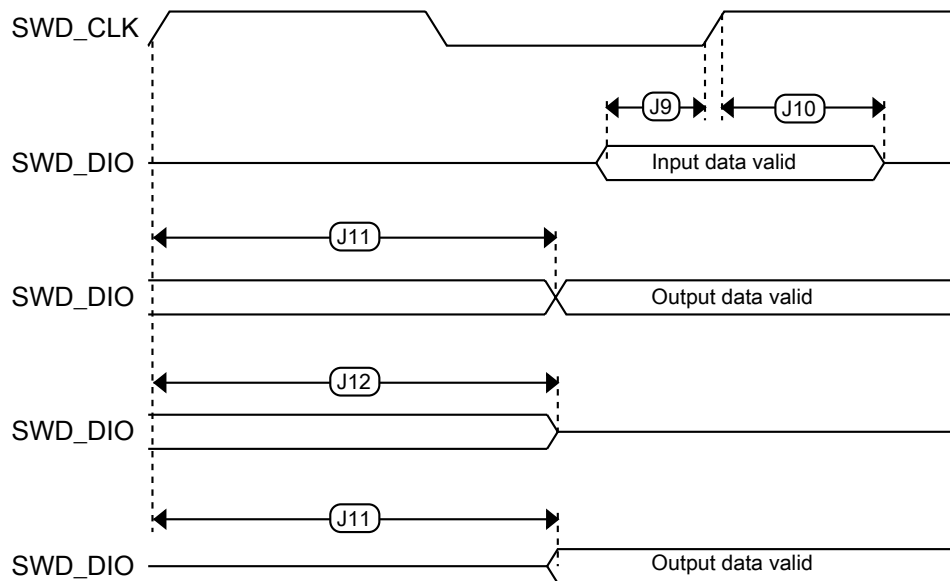
Table 17. SWD full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|--------------------------------|------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | SWD_CLK frequency of operation | | | |

Table continues on the next page...

Table 17. SWD full voltage range electricals (continued)

| Symbol | Description | Min. | Max. | Unit |
|--------|--|------|------|------|
| | • Serial wire debug | 0 | 25 | MHz |
| J2 | SWD_CLK cycle period | 1/J1 | — | ns |
| J3 | SWD_CLK clock pulse width • Serial wire debug | 20 | — | ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 0 | — | ns |
| J11 | SWD_CLK high to SWD_DIO data valid | — | 32 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |


Figure 5. Serial wire clock input timing

Figure 6. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 18. MCG specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes | |
|--------------------------|---|--|-----------|-----------|------------------|-------|------|
| f_{ints_ft} | Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C | — | 32.768 | — | kHz | | |
| f_{ints_t} | Internal reference frequency (slow clock) — user trimmed | 31.25 | — | 39.0625 | kHz | | |
| $\Delta f_{dco_res_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTTRIM] and C4[SCFTRIM] | — | ± 0.3 | ± 0.6 | % f_{dco} | 1 | |
| Δf_{dco_t} | Total deviation of trimmed average DCO output frequency over voltage and temperature | — | +0.5/-0.7 | ± 3 | % f_{dco} | 1, 2 | |
| Δf_{dco_t} | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C | — | ± 0.4 | ± 1.5 | % f_{dco} | 1, 2 | |
| f_{intf_ft} | Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C | — | 4 | — | MHz | | |
| Δf_{intf_ft} | Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C | — | +1/-2 | ± 3 | % f_{intf_ft} | 2 | |
| f_{intf_t} | Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C | 3 | — | 5 | MHz | | |
| f_{loc_low} | Loss of external clock minimum frequency — RANGE = 00 | $(3/5) \times f_{ints_t}$ | — | — | kHz | | |
| f_{loc_high} | Loss of external clock minimum frequency — | $(16/5) \times f_{ints_t}$ | — | — | kHz | | |
| FLL | | | | | | | |
| f_{fil_ref} | FLL reference frequency range | 31.25 | — | 39.0625 | kHz | | |
| f_{dco} | DCO output frequency range | Low range (DRS = 00) $640 \times f_{fil_ref}$ | 20 | 20.97 | 25 | MHz | 3, 4 |
| | | Mid range (DRS = 01) $1280 \times f_{fil_ref}$ | 40 | 41.94 | 48 | MHz | |
| $f_{dco_t_DMX3_2}$ | DCO output frequency | Low range (DRS = 00) | — | 23.99 | — | MHz | 5, 6 |

Table continues on the next page...

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------|---|------|------|------|------|-------|
| V _{DD} | Supply voltage | 1.71 | — | 3.6 | V | |
| I _{DDOSC} | Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz | — | 500 | — | nA | 1 |
| | | — | 200 | — | μA | |
| | | — | 300 | — | μA | |
| | | — | 950 | — | μA | |
| | | — | 1.2 | — | mA | |
| | | — | 1.5 | — | mA | |
| I _{DDOSC} | Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz | — | 25 | — | μA | 1 |
| | | — | 400 | — | μA | |
| | | — | 500 | — | μA | |
| | | — | 2.5 | — | mA | |
| | | — | 3 | — | mA | |
| | | — | 4 | — | mA | |
| C _x | EXTAL load capacitance | — | — | — | | 2, 3 |
| C _y | XTAL load capacitance | — | — | — | | 2, 3 |
| R _F | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| R _S | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | | | | | |

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------|--|------|----------|------|------------|-------|
| | | — | 0 | — | k Ω | |
| V_{pp}^5 | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | V_{DD} | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | V_{DD} | — | V | |

1. $V_{DD}=3.3$ V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x, C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 20. Oscillator frequency specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|------|------|------|-------|
| f_{osc_lo} | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc_hi_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc_hi_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| f_{ec_extal} | Input clock frequency (external clock mode) | — | — | 48 | MHz | 1, 2 |
| t_{dc_extal} | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| t_{cst} | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

Peripheral operating requirements and behaviors

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------|--|------|------|------|---------|-------|
| t_{hvpgm4} | Longword Program high-voltage time | — | 7.5 | 18 | μ s | — |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversblk128k}$ | Erase Block high-voltage time for 128 KB | — | 52 | 452 | ms | 1 |
| $t_{hversall}$ | Erase All high-voltage time | — | 52 | 452 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|--|------|------|------|---------|-------|
| $t_{rd1blk128k}$ | Read 1s Block execution time • 128 KB program flash | — | — | 1.7 | ms | — |
| $t_{rd1sec1k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | μ s | 1 |
| t_{pgmchk} | Program Check execution time | — | — | 45 | μ s | 1 |
| t_{rdsrc} | Read Resource execution time | — | — | 30 | μ s | 1 |
| t_{pgm4} | Program Longword execution time | — | 65 | 145 | μ s | — |
| $t_{ersblk128k}$ | Erase Flash Block execution time • 128 KB program flash | — | 88 | 600 | ms | 2 |

Table continues on the next page...

Table 22. Flash command timing specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---------------|---|------|------|------|---------|-------|
| t_{ersscr} | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| t_{rd1all} | Read 1s All Blocks execution time | — | — | 1.8 | ms | — |
| t_{rdonce} | Read Once execution time | — | — | 25 | μ s | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 65 | — | μ s | — |
| t_{ersall} | Erase All Blocks execution time | — | 175 | 1300 | ms | 2 |
| t_{vfykey} | Verify Backdoor Access Key execution time | — | — | 30 | μ s | 1 |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 23. Flash high voltage current behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---------------|---|------|------|------|------|
| I_{DD_PGM} | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| I_{DD_ERS} | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

3.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------------|--|------|-------------------|------|--------|-------|
| Program Flash | | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | — |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | — |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 25](#) and [Table 26](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.6.1.1 16-bit ADC operating conditions

Table 25. 16-bit ADC operating conditions

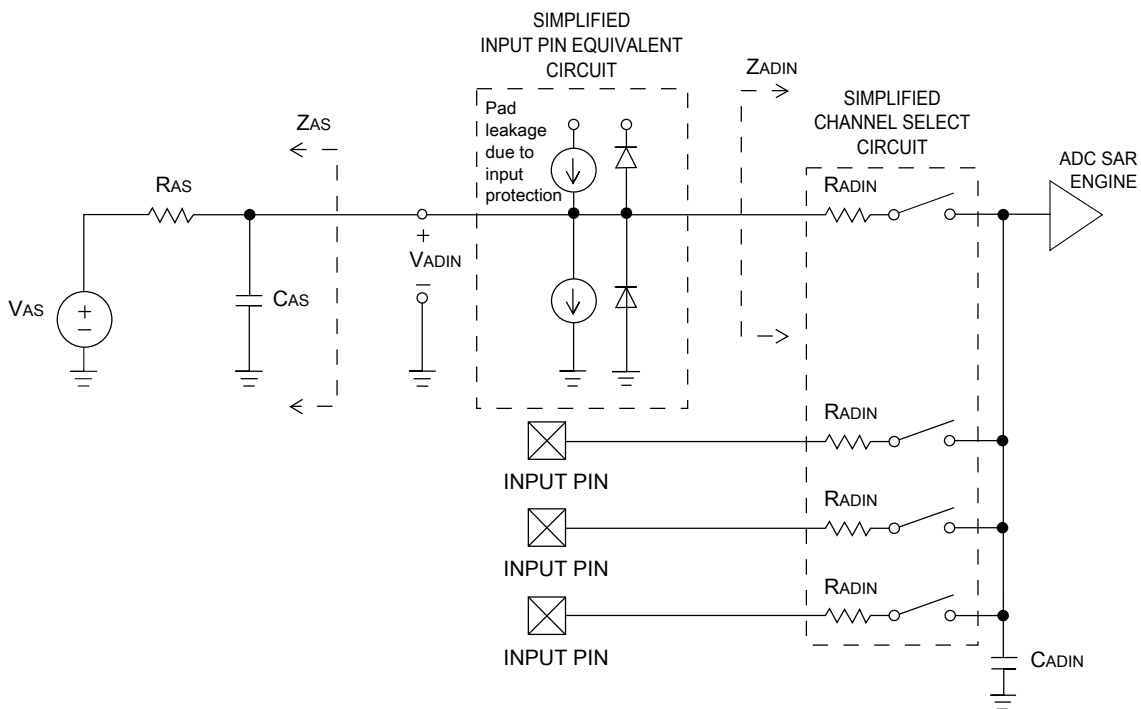
| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|-------------------|-------------------------------------|---|--|-------------------|---|------|-------------------|
| V _{DDA} | Supply voltage | Absolute | 1.71 | — | 3.6 | V | — |
| ΔV _{DDA} | Supply voltage | Delta to V _{DD} (V _{DD} – V _{DDA}) | -100 | 0 | +100 | mV | 2 |
| ΔV _{SSA} | Ground voltage | Delta to V _{SS} (V _{SS} – V _{SSA}) | -100 | 0 | +100 | mV | 2 |
| V _{REFH} | ADC reference voltage high | | 1.13 | V _{DDA} | V _{DDA} | V | |
| V _{REFL} | ADC reference voltage low | | V _{SSA} | V _{SSA} | V _{SSA} | V | |
| V _{ADIN} | Input voltage | <ul style="list-style-type: none"> 16-bit differential mode All other modes | V _{REFL} V _{REFL} | — — | 31/32 * V _{REFH} V _{REFH} | V | — |
| C _{ADIN} | Input capacitance | <ul style="list-style-type: none"> 16-bit mode 8-bit / 10-bit / 12-bit modes | — — | 8 4 | 10 5 | pF | — |
| R _{ADIN} | Input series resistance | | — | 2 | 5 | kΩ | — |
| R _{AS} | Analog source resistance (external) | 13-bit / 12-bit modes f _{ADCK} < 4 MHz | — | — | 5 | kΩ | 3 |
| f _{ADCK} | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 18.0 | MHz | 4 |
| f _{ADCK} | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |
| C _{rate} | ADC conversion rate | ≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | Ksps | 5 |

Table continues on the next page...

Table 25. 16-bit ADC operating conditions (continued)

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------|---------------------|--|--------|-------------------|---------|------|-------|
| C_{rate} | ADC conversion rate | 16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 37.037 | — | 461.467 | Ksps | 5 |

1. Typical values assume $V_{DDA} = 3.0\text{ V}$, $Temp = 25\text{ }^{\circ}\text{C}$, $f_{ADCK} = 1.0\text{ MHz}$, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had $< 8\ \Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to $< 1\text{ ns}$.
4. To use the maximum ADC conversion clock frequency, $CFG2[ADHSC]$ must be set and $CFG1[ADLPC]$ must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).


Figure 7. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|----------------|-------------------------------|---|----------------------------------|------------------------|------------------------------|------------------|-----------------------------------|
| I_{DDA_ADC} | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| f_{ADACK} | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0 | 1.2 | 2.4 | 3.9 | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | | • ADLPC = 1, ADHSC = 1 | 2.4 | 4.0 | 6.1 | MHz | |
| | | • ADLPC = 0, ADHSC = 0 | 3.0 | 5.2 | 7.3 | MHz | |
| | | • ADLPC = 0, ADHSC = 1 | 4.4 | 6.2 | 9.5 | MHz | |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12-bit modes • <12-bit modes | — — | ± 4 ± 1.4 | ± 6.8 ± 2.1 | LSB ⁴ | 5 |
| DNL | Differential non-linearity | • 12-bit modes • <12-bit modes | — — | ± 0.7 ± 0.2 | -1.1 to +1.9 -0.3 to 0.5 | LSB ⁴ | 5 |
| INL | Integral non-linearity | • 12-bit modes • <12-bit modes | — — | ± 1.0 ± 0.5 | -2.7 to +1.9 -0.7 to +0.5 | LSB ⁴ | 5 |
| E_{FS} | Full-scale error | • 12-bit modes • <12-bit modes | — — | -4 -1.4 | -5.4 -1.8 | LSB ⁴ | $V_{ADIN} = V_{DDA}$ ⁵ |
| E_Q | Quantization error | • 16-bit modes • ≤ 13 -bit modes | — — | -1 to 0 — | — ± 0.5 | LSB ⁴ | |
| ENOB | Effective number of bits | 16-bit differential mode | 12.8 | 14.5 | — | bits | 6 |
| | | • Avg = 32 | 11.9 | 13.8 | — | bits | |
| | | • Avg = 4 | 12.2 | 13.9 | — | bits | |
| | | 16-bit single-ended mode | 11.4 | 13.1 | — | bits | |
| | | See ENOB | $6.02 \times \text{ENOB} + 1.76$ | | | dB | |
| THD | Total harmonic distortion | 16-bit differential mode | — | -94 | — | dB | 7 |
| | | • Avg = 32 | — | -85 | — | dB | |
| | | 16-bit single-ended mode | | | | | |
| | | • Avg = 32 | | | | | |
| SFDR | Spurious free dynamic range | 16-bit differential mode | 82 | 95 | — | dB | 7 |

Table continues on the next page...

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|--------------|---------------------|---|------------------------|-------------------|------|-------|---|
| | | <ul style="list-style-type: none"> Avg = 32 16-bit single-ended mode <ul style="list-style-type: none"> Avg = 32 | 78 | 90 | — | dB | |
| E_{IL} | Input leakage error | | $I_{in} \times R_{AS}$ | | | mV | I_{in} = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | 1.55 | 1.62 | 1.69 | mV/°C | 8 |
| V_{TEMP25} | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 8 |

- All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
- Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
- ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- ADC conversion clock < 3 MHz

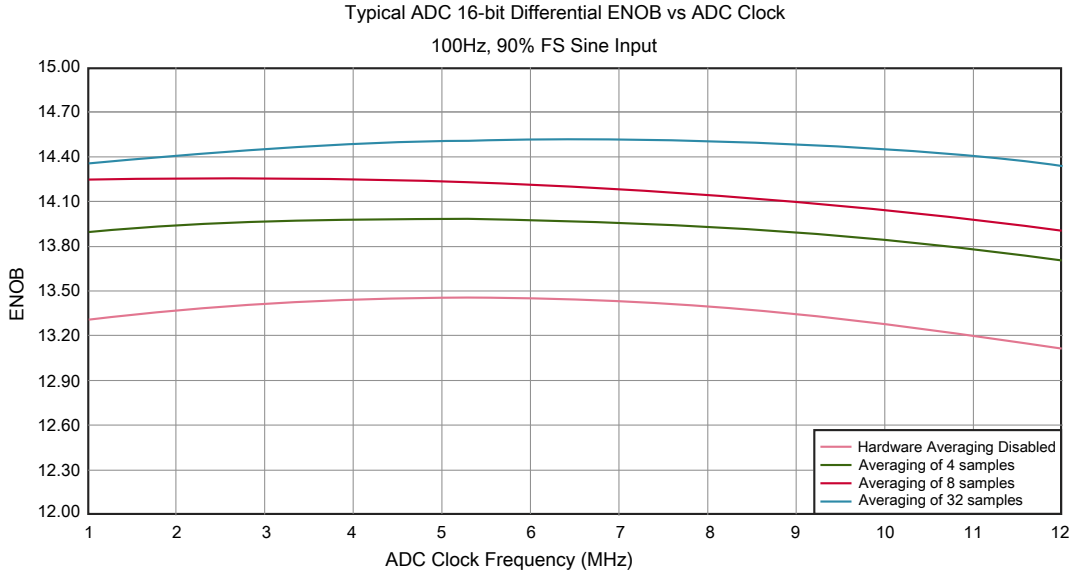


Figure 8. Typical ENOB vs. ADC_CLK for 16-bit differential mode

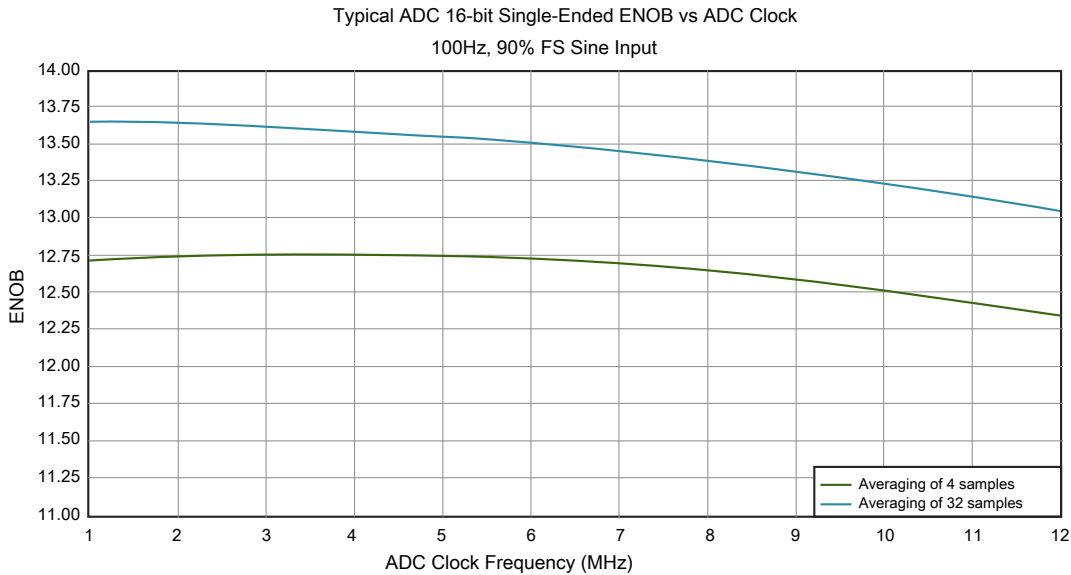


Figure 9. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 27. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------------|----------------|------|------|------|------|
| V _{DD} | Supply voltage | 1.71 | — | 3.6 | V |

Table continues on the next page...

Table 27. Comparator and 6-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-------------|--|----------------|------|----------|------------------|
| I_{DDHS} | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | μA |
| $I_{DDL S}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | μA |
| V_{AIN} | Analog input voltage | $V_{SS} - 0.3$ | — | V_{DD} | V |
| V_{AIO} | Analog input offset voltage | — | — | 20 | mV |
| V_H | Analog comparator hysteresis ¹ <ul style="list-style-type: none"> • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11 | — | 5 | — | mV |
| | | — | 10 | — | mV |
| | | — | 20 | — | mV |
| | | — | 30 | — | mV |
| V_{CMPOH} | Output high | $V_{DD} - 0.5$ | — | — | V |
| V_{CMPOI} | Output low | — | — | 0.5 | V |
| t_{DHS} | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| t_{DLS} | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay ² | — | — | 40 | μs |
| I_{DAC6b} | 6-bit DAC current adder (enabled) | — | 7 | — | μA |
| INL | 6-bit DAC integral non-linearity | -0.5 | — | 0.5 | LSB ³ |
| DNL | 6-bit DAC differential non-linearity | -0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{\text{reference}}/64$

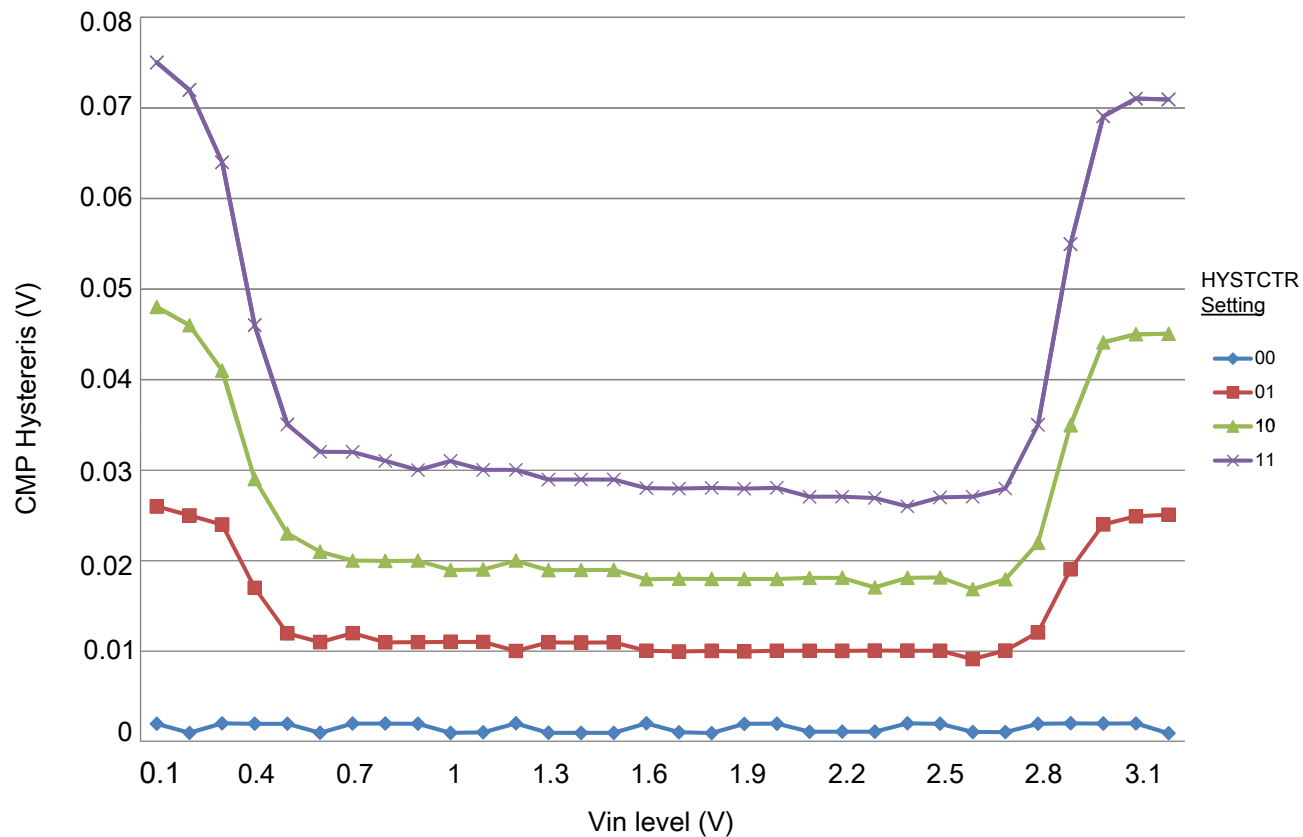


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

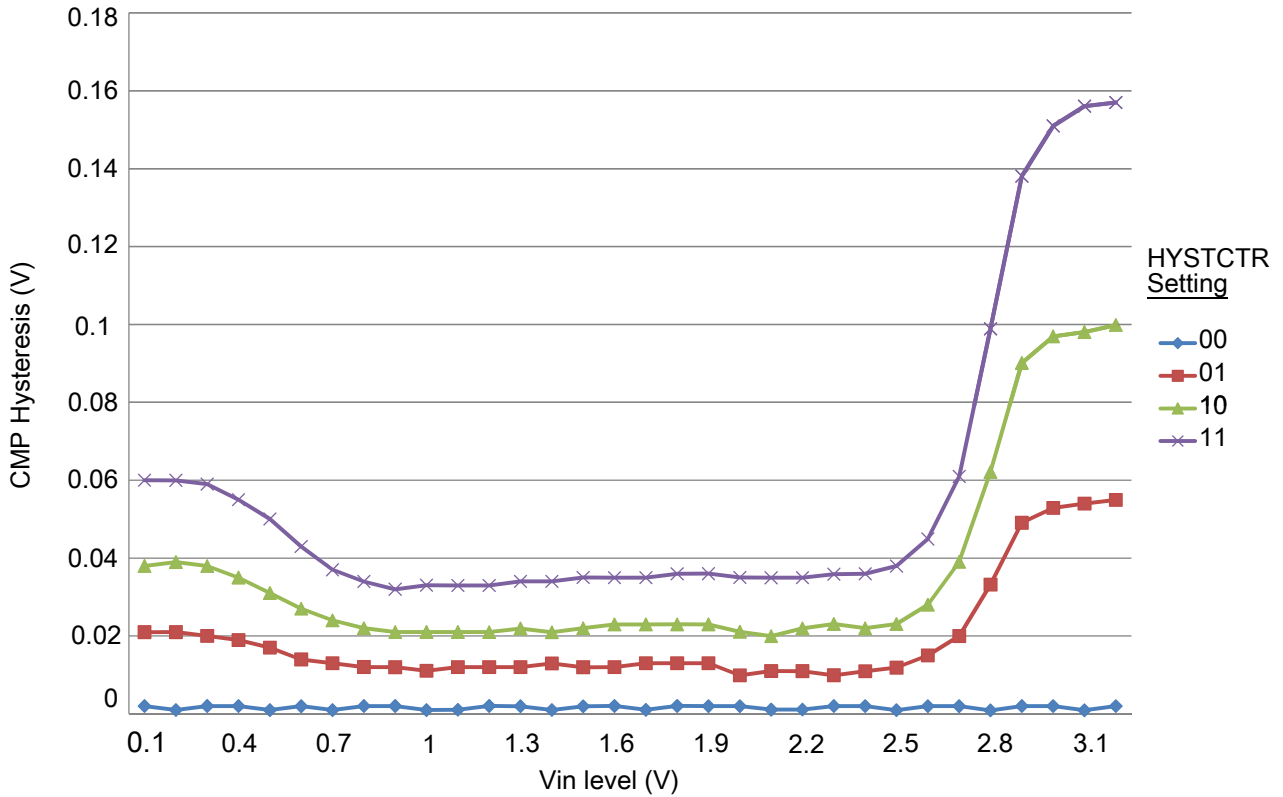


Figure 11. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 28. 12-bit DAC operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------|-------------------------|------|------|------|-------|
| V_{DDA} | Supply voltage | 1.71 | 3.6 | V | |
| V_{DACR} | Reference voltage | 1.13 | 3.6 | V | 1 |
| C_L | Output load capacitance | — | 100 | pF | 2 |
| I_L | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be V_{DDA} or V_{REFH} .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.6.3.2 12-bit DAC operating behaviors

Table 29. 12-bit DAC operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------------------|-------------|------------|------------------------|-------|
| I_{DDA_DACLP} | Supply current — low-power mode | — | — | 250 | μA | |
| I_{DDA_DACHP} | Supply current — high-speed mode | — | — | 900 | μA | |
| t_{DACLP} | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | μs | 1 |
| t_{DACHP} | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | μs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | μs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | $V_{DACR} - 100$ | — | V_{DACR} | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ± 8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR} > 2\text{ V}$ | — | — | ± 1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$ | — | — | ± 1 | LSB | 4 |
| V_{OFFSET} | Offset error | — | ± 0.4 | ± 0.8 | %FSR | 5 |
| E_G | Gain error | — | ± 0.1 | ± 0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$ | 60 | — | 90 | dB | |
| T_{CO} | Temperature coefficient offset voltage | — | 3.7 | — | $\mu\text{V}/\text{C}$ | 6 |
| T_{GE} | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| R_{op} | Output resistance (load = 3 k Ω) | — | — | 250 | Ω | |
| SR | Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> • High power (SP_{HP}) • Low power (SP_{LP}) | 1.2 0.05 | 1.7 0.12 | — — | V/ μs | |
| BW | 3dB bandwidth <ul style="list-style-type: none"> • High power (SP_{HP}) • Low power (SP_{LP}) | 550 40 | — — | — — | kHz | |

1. Settling within ± 1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4\text{ V}$
5. Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV
6. $V_{DDA} = 3.0\text{ V}$, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

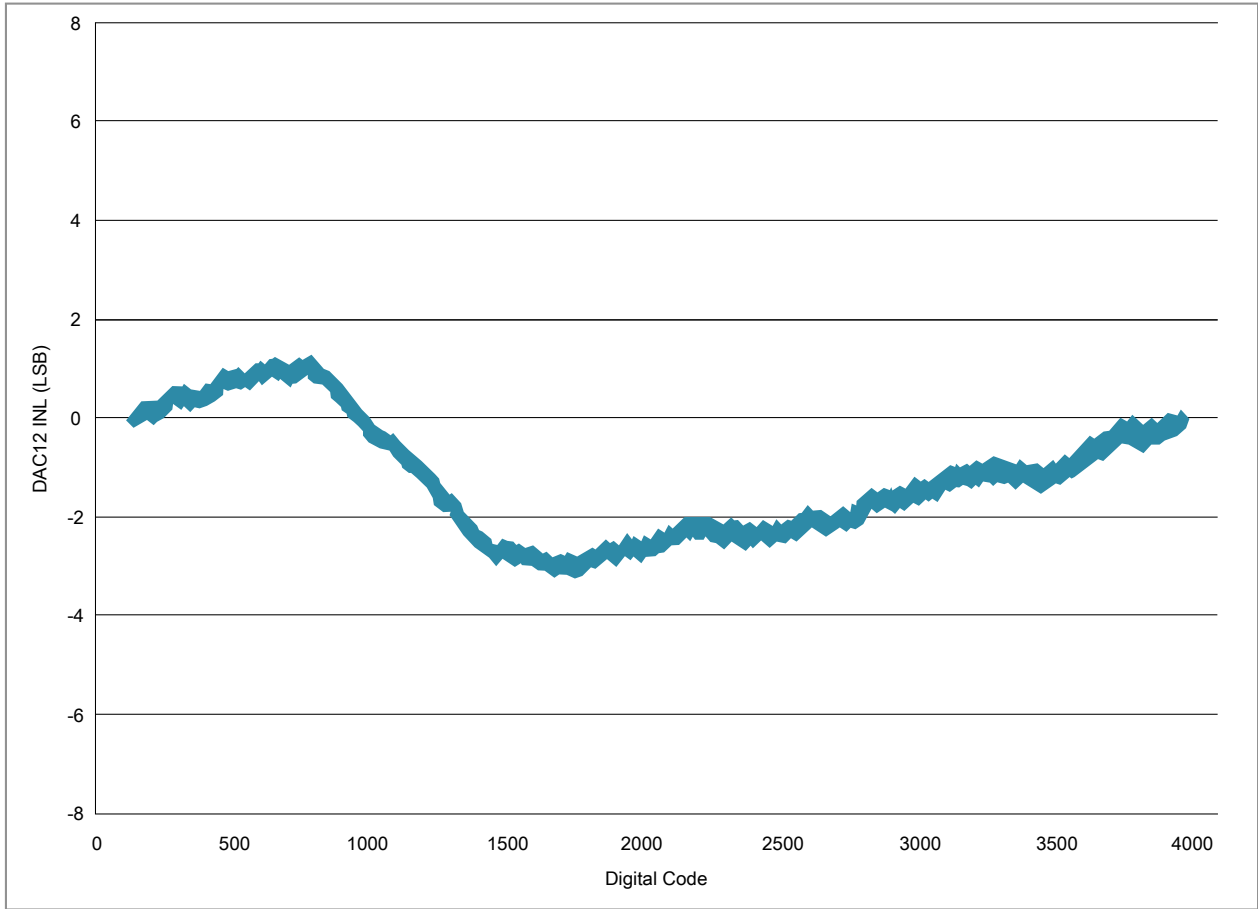


Figure 12. Typical INL error vs. digital code

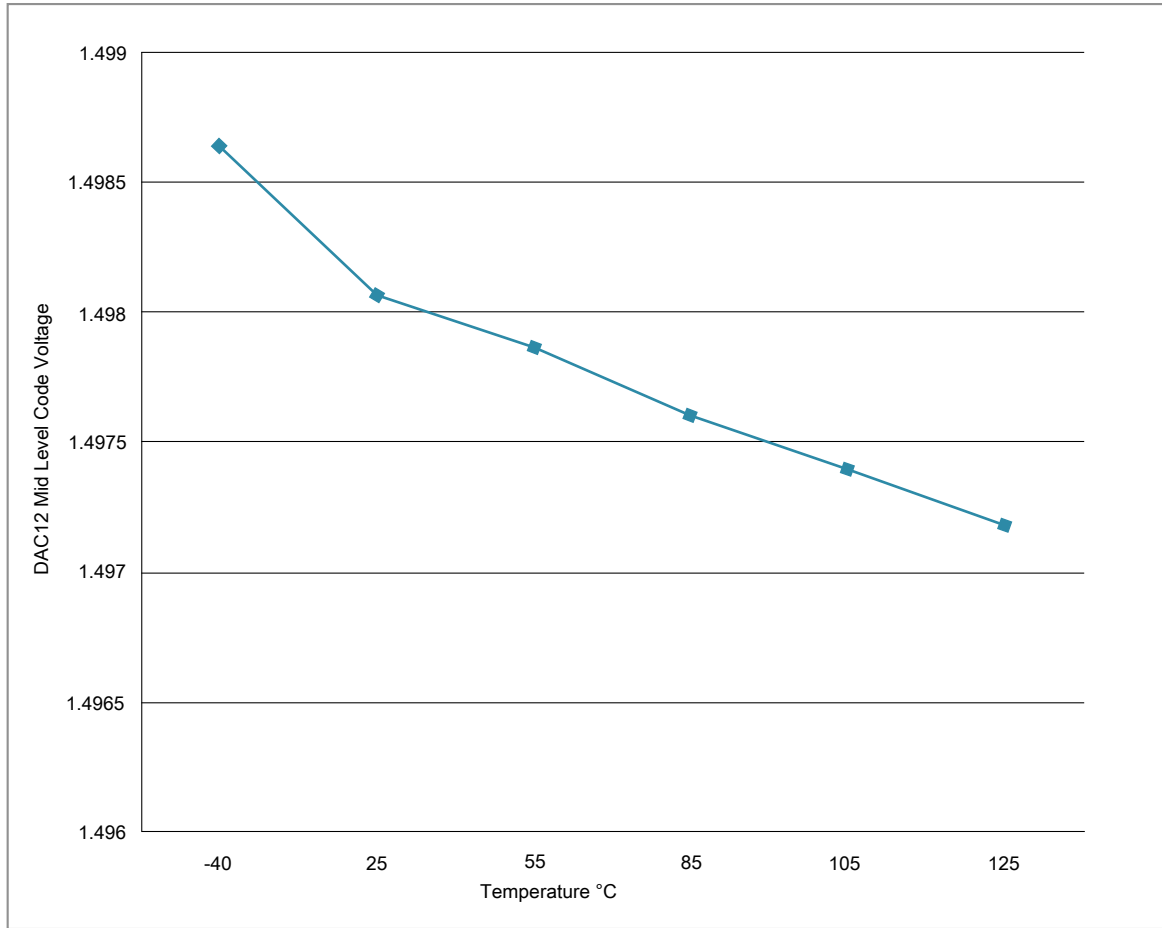


Figure 13. Offset at half scale vs. temperature

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces

3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 30. SPI master mode timing on slew rate disabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-----------------------|--------------------------|-------------|------|
| 1 | f_{op} | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1/2 | — | t_{SPSCK} | — |
| 4 | t_{Lag} | Enable lag time | 1/2 | — | t_{SPSCK} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | $1024 \times t_{periph}$ | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 18 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 0 | — | ns | — |
| 8 | t_v | Data valid (after SPSCK edge) | — | 15 | ns | — |
| 9 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 10 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 11 | t_{RO} | Rise time output | — | 25 | ns | — |
| | t_{FO} | Fall time output | | | | |

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$

Table 31. SPI master mode timing on slew rate enabled pads

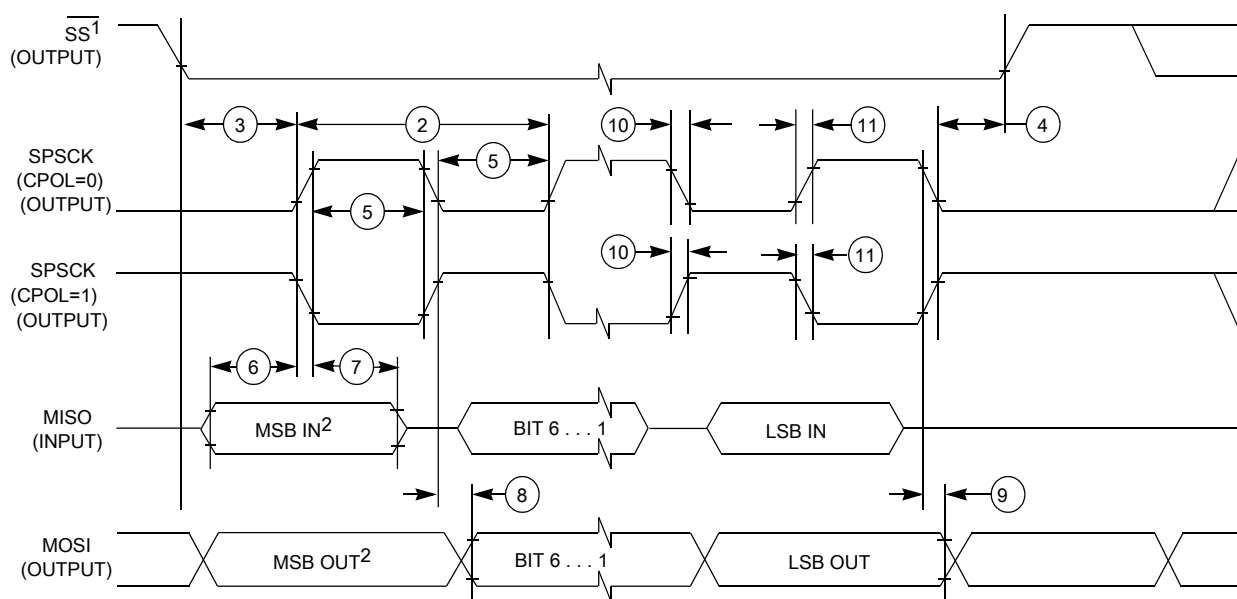
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-----------------------|--------------------------|-------------|------|
| 1 | f_{op} | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1/2 | — | t_{SPSCK} | — |
| 4 | t_{Lag} | Enable lag time | 1/2 | — | t_{SPSCK} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | $1024 \times t_{periph}$ | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 96 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 0 | — | ns | — |

Table continues on the next page...

Table 31. SPI master mode timing on slew rate enabled pads (continued)

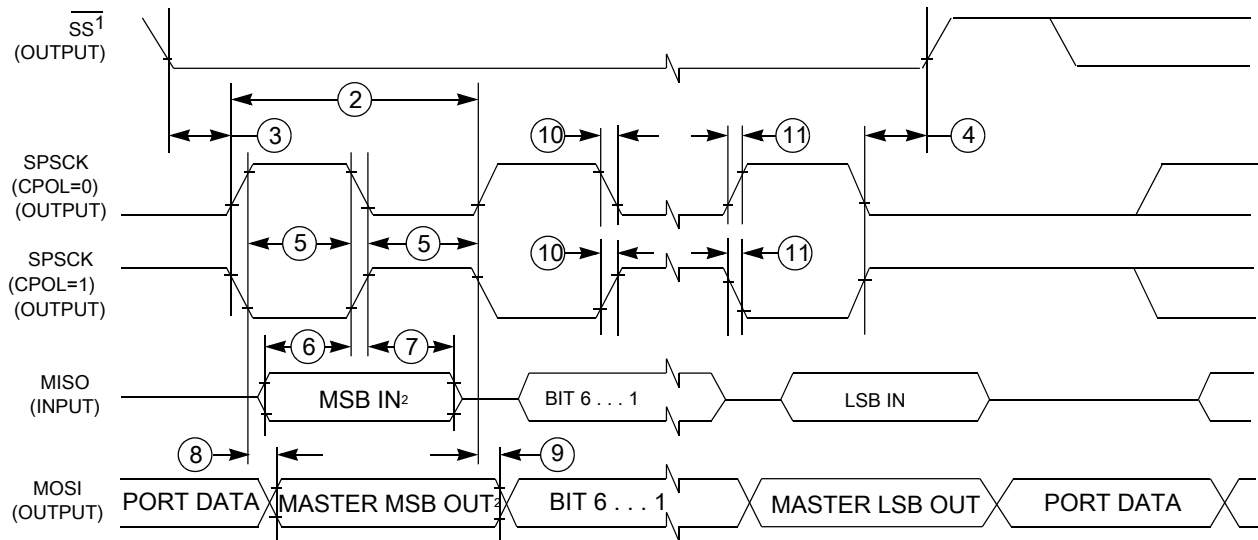
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|----------|--------------------------------|------|-------------------|------|------|
| 8 | t_v | Data valid (after SPSCCK edge) | — | 52 | ns | — |
| 9 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 10 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 11 | t_{RO} | Rise time output | — | 36 | ns | — |
| | t_{FO} | Fall time output | | | | |

- For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
- $t_{periph} = 1/f_{periph}$



- If configured as an output.
- LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI master mode timing (CPHA = 0)



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI master mode timing (CPHA = 1)
Table 32. SPI slave mode timing on slew rate disabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|---------------|---------------------------------|-----------------------|-------------------|--------------|------|
| 1 | f_{op} | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | t_{SPSCCK} | SPSCCK period | $4 \times t_{periph}$ | — | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1 | — | t_{periph} | — |
| 4 | t_{Lag} | Enable lag time | 1 | — | t_{periph} | — |
| 5 | $t_{WSPSCCK}$ | Clock (SPSCCK) high or low time | $t_{periph} - 30$ | — | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 2.5 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 3.5 | — | ns | — |
| 8 | t_a | Slave access time | — | t_{periph} | ns | 3 |
| 9 | t_{dis} | Slave MISO disable time | — | t_{periph} | ns | 4 |
| 10 | t_v | Data valid (after SPSCCK edge) | — | 31 | ns | — |
| 11 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 12 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 13 | t_{RO} | Rise time output | — | 25 | ns | — |
| | t_{FO} | Fall time output | | | | |

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

Table 33. SPI slave mode timing on slew rate enabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-----------------------|-------------------|--------------|------|
| 1 | f_{op} | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $4 \times t_{periph}$ | — | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1 | — | t_{periph} | — |
| 4 | t_{Lag} | Enable lag time | 1 | — | t_{periph} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | — | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 2 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 7 | — | ns | — |
| 8 | t_a | Slave access time | — | t_{periph} | ns | 3 |
| 9 | t_{dis} | Slave MISO disable time | — | t_{periph} | ns | 4 |
| 10 | t_v | Data valid (after SPSCK edge) | — | 122 | ns | — |
| 11 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 12 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 13 | t_{RO} | Rise time output | — | 36 | ns | — |
| | t_{FO} | Fall time output | | | | |

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

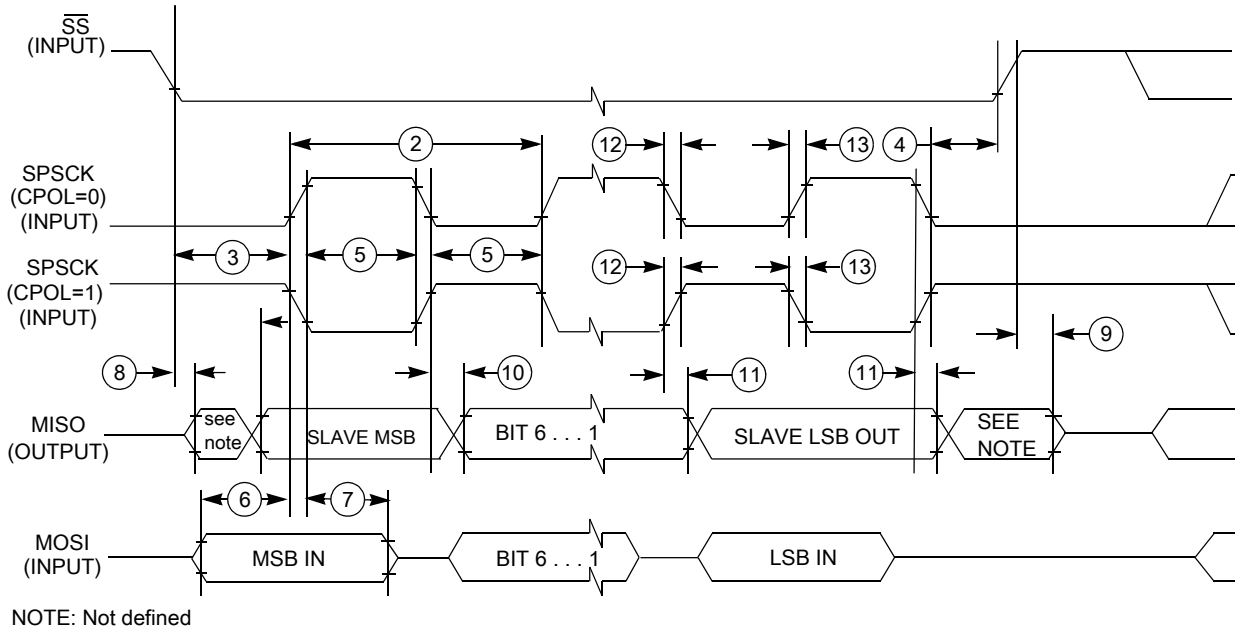
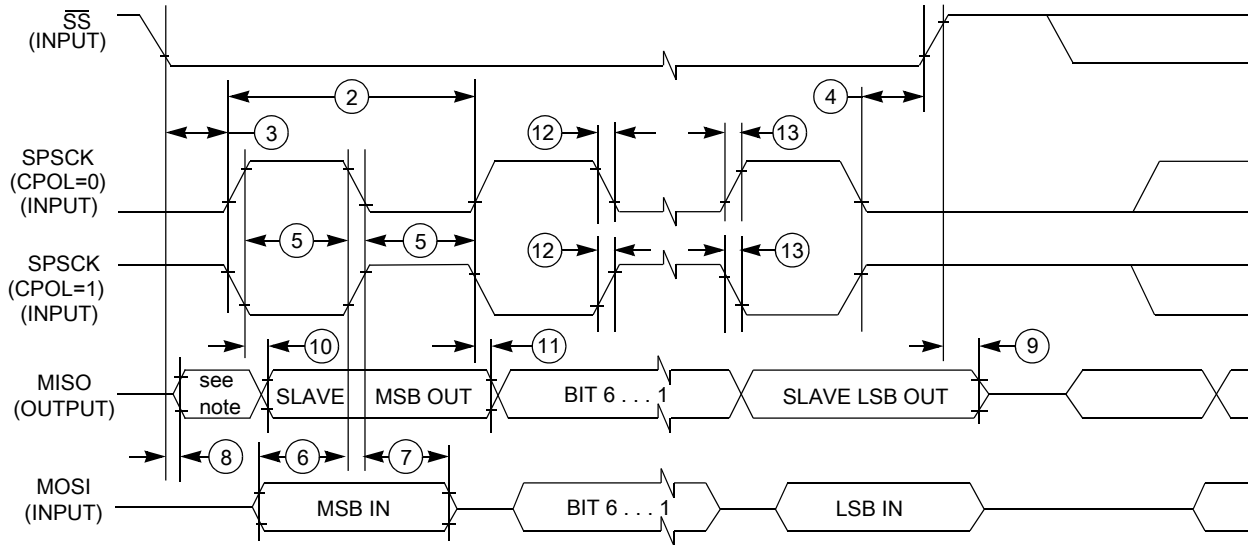


Figure 16. SPI slave mode timing (CPHA = 0)



NOTE: Not defined

Figure 17. SPI slave mode timing (CPHA = 1)

3.8.2 Inter-Integrated Circuit Interface (I2C) timing

Table 34. I2C timing

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|--|---------------|------------------|-------------------|----------------------------|------------------|---------|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | f_{SCL} | 0 | 100 | 0 | 400 ¹ | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD}; STA$ | 4 | — | 0.6 | — | μs |
| LOW period of the SCL clock | t_{LOW} | 4.7 | — | 1.3 | — | μs |
| HIGH period of the SCL clock | t_{HIGH} | 4 | — | 0.6 | — | μs |
| Set-up time for a repeated START condition | $t_{SU}; STA$ | 4.7 | — | 0.6 | — | μs |
| Data hold time for I ² C bus devices | $t_{HD}; DAT$ | 0 ² | 3.45 ³ | 0 ⁴ | 0.9 ² | μs |
| Data set-up time | $t_{SU}; DAT$ | 250 ⁵ | — | 100 ^{3, 6} | — | ns |
| Rise time of SDA and SCL signals | t_r | — | 1000 | $20 + 0.1C_b$ ⁷ | 300 | ns |
| Fall time of SDA and SCL signals | t_f | — | 300 | $20 + 0.1C_b$ ⁶ | 300 | ns |
| Set-up time for STOP condition | $t_{SU}; STO$ | 4 | — | 0.6 | — | μs |
| Bus free time between STOP and START condition | t_{BUF} | 4.7 | — | 1.3 | — | μs |
| Pulse width of spikes that must be suppressed by the input filter | t_{SP} | N/A | N/A | 0 | 50 | ns |

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins (see [Voltage and current operating behaviors](#)) or when using the Normal drive pins and $VDD \geq 2.7 V$

Peripheral operating requirements and behaviors

2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t_{HD; DAT} must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU; DAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

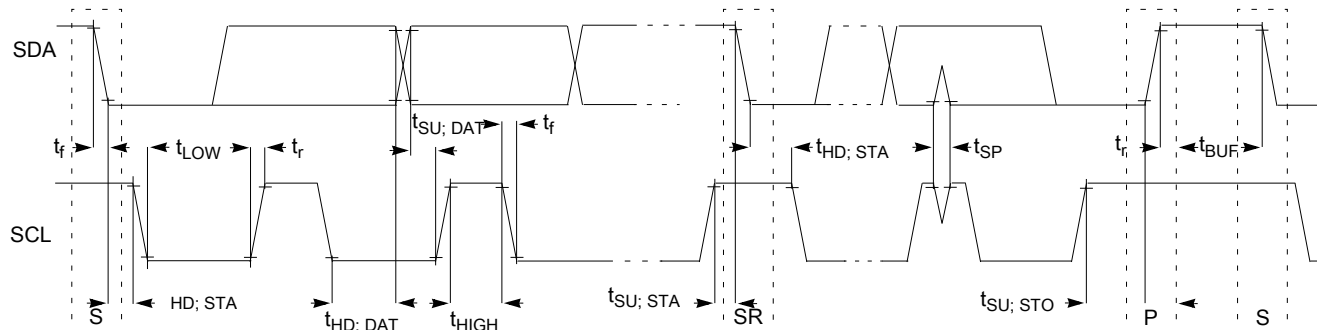


Figure 18. Timing definition for fast and standard mode devices on the I²C bus

3.8.3 UART

See [General switching specifications](#).

3.8.4 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

3.8.4.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 35. I2S/SAI master mode timing

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 40 | — | ns |
| S2 | I2S_MCLK (as an input) pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 80 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 15.5 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 19 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 26 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

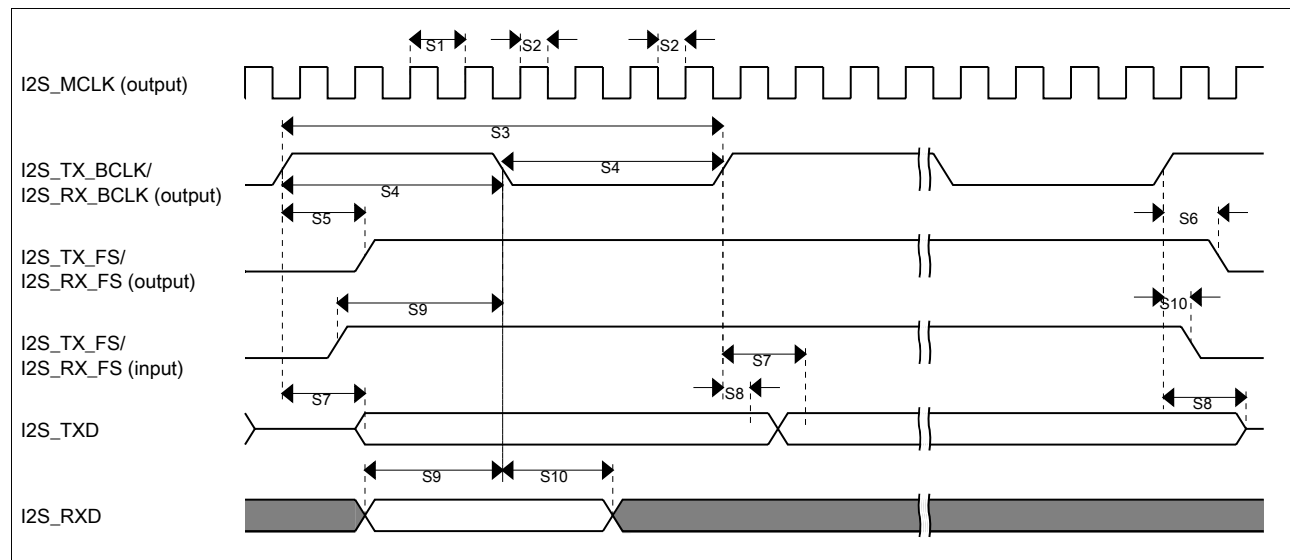


Figure 19. I2S/SAI timing — master modes

Table 36. I2S/SAI slave mode timing

| Num. | Characteristic | Min. | Max. | Unit |
|------|--|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 10 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 33 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 10 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid ¹ | — | 28 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

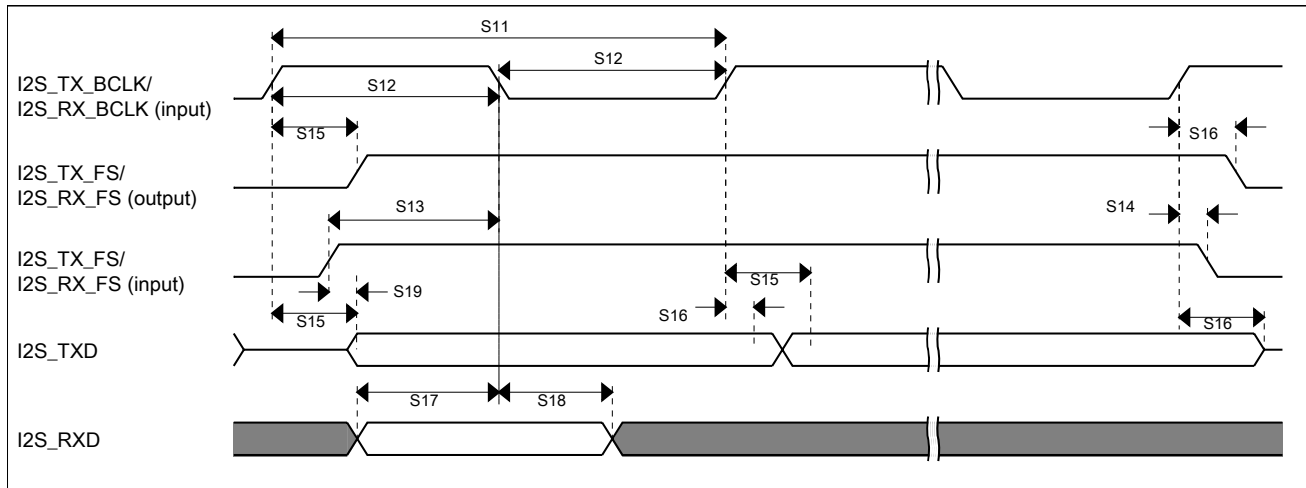


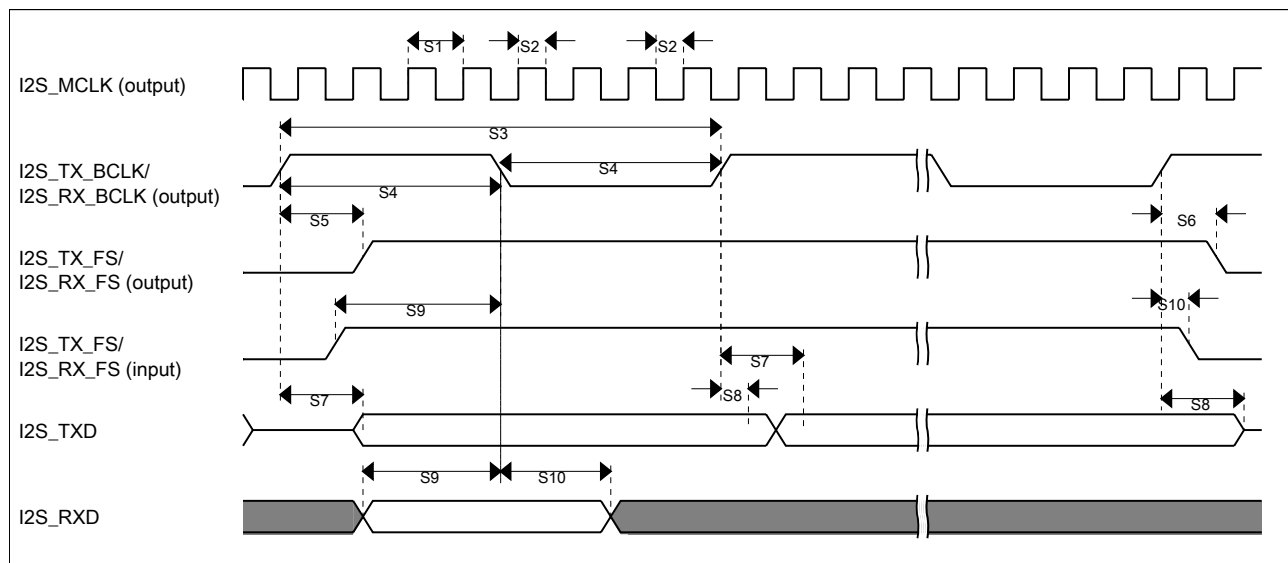
Figure 20. I2S/SAI timing — slave modes

3.8.4.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 37. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 62.5 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 250 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 45 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 45 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 75 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |


Figure 21. I2S/SAI timing — master modes
Table 38. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|------|--|------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 250 | — | ns |

Table continues on the next page...

Table 38. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

| Num. | Characteristic | Min. | Max. | Unit |
|------|--|------|------|-------------|
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 30 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 87 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 30 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid ¹ | — | 72 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

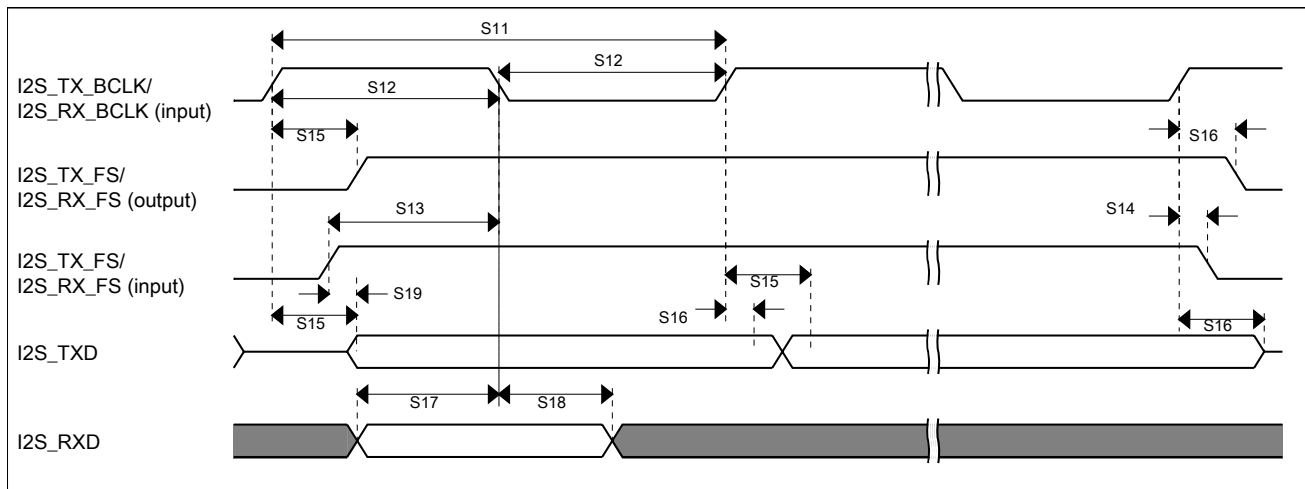


Figure 22. I2S/SAI timing — slave modes

3.9 Human-machine interfaces (HMI)

3.9.1 TSI electrical specifications

Table 39. TSI electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|----------|-------------------------------------|------|------|------|------|
| TSI_RUNF | Fixed power consumption in run mode | — | 100 | — | μA |

Table continues on the next page...

Table 39. TSI electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------|--|------|------|------|------|
| TSI_RUNV | Variable power consumption in run mode (depends on oscillator's current selection) | 1.0 | — | 128 | μA |
| TSI_EN | Power consumption in enable mode | — | 100 | — | μA |
| TSI_DIS | Power consumption in disable mode | — | 1.2 | — | μA |
| TSI_TEN | TSI analog enable time | — | 66 | — | μs |
| TSI_CREF | TSI reference capacitor | — | 1.0 | — | pF |
| TSI_DVOLT | Voltage variation of VP & VM around nominal values | 0.19 | — | 1.03 | V |

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 64-pin LQFP | 98ASS23234W |
| 64-pin MAPBGA | 98ASA00420D |

5 Pinout

5.1 KL16 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 64 BGA | 64 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|--------|---------|----------|----------|------|------|-----------|----------|------------|-----------|----------|------|
| A1 | 1 | PTE0 | DISABLED | | PTE0 | SPI1_MISO | UART1_TX | RTC_CLKOUT | CMP0_OUT | I2C1_SDA | |
| B1 | 2 | PTE1 | DISABLED | | PTE1 | SPI1_MOSI | UART1_RX | | SPI1_MISO | I2C1_SCL | |

Pinout

| 64 BGA | 64 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|--------|---------|----------|-------------------------------------|-------------------------------------|-------|-----------|----------|------------|-----------|------------------|---------|
| — | 3 | VDD | VDD | VDD | | | | | | | |
| C4 | 4 | VSS | VSS | VSS | | | | | | | |
| E1 | 5 | PTE16 | ADC0_DP1/ ADC0_SE1 | ADC0_DP1/ ADC0_SE1 | PTE16 | SPI0_PCS0 | UART2_TX | TPM_CLKIN0 | | | |
| D1 | 6 | PTE17 | ADC0_DM1/ ADC0_SE5a | ADC0_DM1/ ADC0_SE5a | PTE17 | SPI0_SCK | UART2_RX | TPM_CLKIN1 | | LPTMR0_ ALT3 | |
| E2 | 7 | PTE18 | ADC0_DP2/ ADC0_SE2 | ADC0_DP2/ ADC0_SE2 | PTE18 | SPI0_MOSI | | I2C0_SDA | SPI0_MISO | | |
| D2 | 8 | PTE19 | ADC0_DM2/ ADC0_SE6a | ADC0_DM2/ ADC0_SE6a | PTE19 | SPI0_MISO | | I2C0_SCL | SPI0_MOSI | | |
| G1 | 9 | PTE20 | ADC0_DP0/ ADC0_SE0 | ADC0_DP0/ ADC0_SE0 | PTE20 | | TPM1_CH0 | UART0_TX | | | |
| F1 | 10 | PTE21 | ADC0_DM0/ ADC0_SE4a | ADC0_DM0/ ADC0_SE4a | PTE21 | | TPM1_CH1 | UART0_RX | | | |
| G2 | 11 | PTE22 | ADC0_DP3/ ADC0_SE3 | ADC0_DP3/ ADC0_SE3 | PTE22 | | TPM2_CH0 | UART2_TX | | | |
| F2 | 12 | PTE23 | ADC0_DM3/ ADC0_SE7a | ADC0_DM3/ ADC0_SE7a | PTE23 | | TPM2_CH1 | UART2_RX | | | |
| F4 | 13 | VDDA | VDDA | VDDA | | | | | | | |
| G4 | 14 | VREFH | VREFH | VREFH | | | | | | | |
| G3 | 15 | VREFL | VREFL | VREFL | | | | | | | |
| F3 | 16 | VSSA | VSSA | VSSA | | | | | | | |
| H1 | 17 | PTE29 | CMP0_IN5/ ADC0_SE4b | CMP0_IN5/ ADC0_SE4b | PTE29 | | TPM0_CH2 | TPM_CLKIN0 | | | |
| H2 | 18 | PTE30 | DAC0_OUT/ ADC0_SE23/ CMP0_IN4 | DAC0_OUT/ ADC0_SE23/ CMP0_IN4 | PTE30 | | TPM0_CH3 | TPM_CLKIN1 | | | |
| H3 | 19 | PTE31 | DISABLED | | PTE31 | | TPM0_CH4 | | | | |
| H4 | 20 | PTE24 | DISABLED | | PTE24 | | TPM0_CH0 | | I2C0_SCL | | |
| H5 | 21 | PTE25 | DISABLED | | PTE25 | | TPM0_CH1 | | I2C0_SDA | | |
| D3 | 22 | PTA0 | SWD_CLK | TSIO_CH1 | PTA0 | | TPM0_CH5 | | | | SWD_CLK |
| D4 | 23 | PTA1 | DISABLED | TSIO_CH2 | PTA1 | UART0_RX | TPM2_CH0 | | | | |
| E5 | 24 | PTA2 | DISABLED | TSIO_CH3 | PTA2 | UART0_TX | TPM2_CH1 | | | | |
| D5 | 25 | PTA3 | SWD_DIO | TSIO_CH4 | PTA3 | I2C1_SCL | TPM0_CH0 | | | | SWD_DIO |
| G5 | 26 | PTA4 | NMI_b | TSIO_CH5 | PTA4 | I2C1_SDA | TPM0_CH1 | | | | NMI_b |
| F5 | 27 | PTA5 | DISABLED | | PTA5 | | TPM0_CH2 | | | I2S0_TX_ BCLK | |
| H6 | 28 | PTA12 | DISABLED | | PTA12 | | TPM1_CH0 | | | I2S0_TXD0 | |
| G6 | 29 | PTA13 | DISABLED | | PTA13 | | TPM1_CH1 | | | I2S0_TX_FS | |
| G7 | 30 | VDD | VDD | VDD | | | | | | | |
| H7 | 31 | VSS | VSS | VSS | | | | | | | |
| H8 | 32 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | UART1_RX | TPM_CLKIN0 | | | |

| 64 BGA | 64 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|--------|---------|------------------------|---------------------|---------------------|------------------------|-----------|-------------|--------------|-----------|--------------|---------|
| G8 | 33 | PTA19 | XTAL0 | XTAL0 | PTA19 | | UART1_TX | TPM_CLKIN1 | | LPTMR0_ALT1 | |
| F8 | 34 | PTA20 | RESET_b | | PTA20 | | | | | | RESET_b |
| F7 | 35 | PTB0/LLWU_P5 | ADC0_SE8/TSIO_CH0 | ADC0_SE8/TSIO_CH0 | PTB0/LLWU_P5 | I2C0_SCL | TPM1_CH0 | | | | |
| F6 | 36 | PTB1 | ADC0_SE9/TSIO_CH6 | ADC0_SE9/TSIO_CH6 | PTB1 | I2C0_SDA | TPM1_CH1 | | | | |
| E7 | 37 | PTB2 | ADC0_SE12/TSIO_CH7 | ADC0_SE12/TSIO_CH7 | PTB2 | I2C0_SCL | TPM2_CH0 | | | | |
| E8 | 38 | PTB3 | ADC0_SE13/TSIO_CH8 | ADC0_SE13/TSIO_CH8 | PTB3 | I2C0_SDA | TPM2_CH1 | | | | |
| E6 | 39 | PTB16 | TSIO_CH9 | TSIO_CH9 | PTB16 | SPI1_MOSI | UART0_RX | TPM_CLKIN0 | SPI1_MISO | | |
| D7 | 40 | PTB17 | TSIO_CH10 | TSIO_CH10 | PTB17 | SPI1_MISO | UART0_TX | TPM_CLKIN1 | SPI1_MOSI | | |
| D6 | 41 | PTB18 | TSIO_CH11 | TSIO_CH11 | PTB18 | | TPM2_CH0 | I2S0_TX_BCLK | | | |
| C7 | 42 | PTB19 | TSIO_CH12 | TSIO_CH12 | PTB19 | | TPM2_CH1 | I2S0_TX_FS | | | |
| D8 | 43 | PTC0 | ADC0_SE14/TSIO_CH13 | ADC0_SE14/TSIO_CH13 | PTC0 | | EXTRG_IN | | CMP0_OUT | I2S0_TXD0 | |
| C6 | 44 | PTC1/LLWU_P6/RTC_CLKIN | ADC0_SE15/TSIO_CH14 | ADC0_SE15/TSIO_CH14 | PTC1/LLWU_P6/RTC_CLKIN | I2C1_SCL | | TPM0_CH0 | | I2S0_TXD0 | |
| B7 | 45 | PTC2 | ADC0_SE11/TSIO_CH15 | ADC0_SE11/TSIO_CH15 | PTC2 | I2C1_SDA | | TPM0_CH1 | | I2S0_TX_FS | |
| C8 | 46 | PTC3/LLWU_P7 | DISABLED | | PTC3/LLWU_P7 | | UART1_RX | TPM0_CH2 | CLKOUT | I2S0_TX_BCLK | |
| E3 | 47 | VSS | VSS | VSS | | | | | | | |
| E4 | 48 | VDD | VDD | VDD | | | | | | | |
| B8 | 49 | PTC4/LLWU_P8 | DISABLED | | PTC4/LLWU_P8 | SPI0_PCS0 | UART1_TX | TPM0_CH3 | I2S0_MCLK | | |
| A8 | 50 | PTC5/LLWU_P9 | DISABLED | | PTC5/LLWU_P9 | SPI0_SCK | LPTMR0_ALT2 | I2S0_RXD0 | | CMP0_OUT | |
| A7 | 51 | PTC6/LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/LLWU_P10 | SPI0_MOSI | EXTRG_IN | I2S0_RX_BCLK | SPI0_MISO | I2S0_MCLK | |
| B6 | 52 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_MISO | | I2S0_RX_FS | SPI0_MOSI | | |
| A6 | 53 | PTC8 | CMP0_IN2 | CMP0_IN2 | PTC8 | I2C0_SCL | TPM0_CH4 | I2S0_MCLK | | | |
| B5 | 54 | PTC9 | CMP0_IN3 | CMP0_IN3 | PTC9 | I2C0_SDA | TPM0_CH5 | I2S0_RX_BCLK | | | |
| B4 | 55 | PTC10 | DISABLED | | PTC10 | I2C1_SCL | | I2S0_RX_FS | | | |
| A5 | 56 | PTC11 | DISABLED | | PTC11 | I2C1_SDA | | I2S0_RXD0 | | | |
| C3 | 57 | PTD0 | DISABLED | | PTD0 | SPI0_PCS0 | | TPM0_CH0 | | | |
| A4 | 58 | PTD1 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | | TPM0_CH1 | | | |
| C2 | 59 | PTD2 | DISABLED | | PTD2 | SPI0_MOSI | UART2_RX | TPM0_CH2 | SPI0_MISO | | |
| B3 | 60 | PTD3 | DISABLED | | PTD3 | SPI0_MISO | UART2_TX | TPM0_CH3 | SPI0_MOSI | | |

Pinout

| 64 BGA | 64 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|--------|---------|-------------------|-----------|-----------|-------------------|-----------|----------|----------|-----------|------|------|
| A3 | 61 | PTD4/ LLWU_P14 | DISABLED | | PTD4/ LLWU_P14 | SPI1_PCS0 | UART2_RX | TPM0_CH4 | | | |
| C1 | 62 | PTD5 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI1_SCK | UART2_TX | TPM0_CH5 | | | |
| B2 | 63 | PTD6/ LLWU_P15 | ADC0_SE7b | ADC0_SE7b | PTD6/ LLWU_P15 | SPI1_MOSI | UART0_RX | | SPI1_MISO | | |
| A2 | 64 | PTD7 | DISABLED | | PTD7 | SPI1_MISO | UART0_TX | | SPI1_MOSI | | |
| C5 | — | NC | NC | NC | | | | | | | |

5.2 KL16 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see [KL16 Signal Multiplexing and Pin Assignments](#).

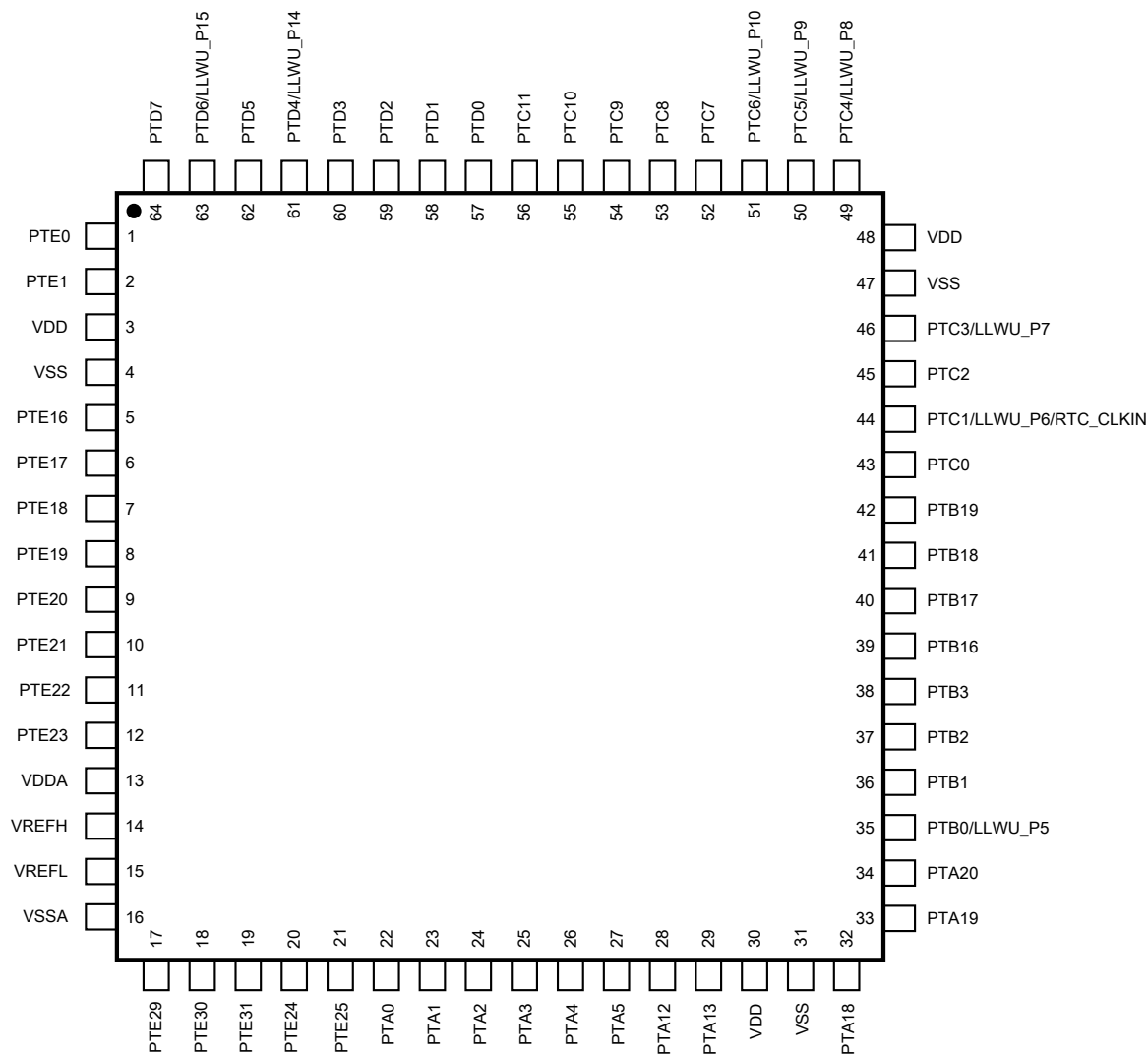


Figure 23. KL16 64-pin LQFP pinout diagram

| | | | | | | | | | |
|---|-------|-------------------|-------------------|-------|-------|--------------------------------|-------------------|------------------|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
| A | PTE0 | PTD7 | PTD4/ LLWU_P14 | PTD1 | PTC11 | PTC8 | PTC6/ LLWU_P10 | PTC5/ LLWU_P9 | A |
| B | PTE1 | PTD6/ LLWU_P15 | PTD3 | PTC10 | PTC9 | PTC7 | PTC2 | PTC4/ LLWU_P8 | B |
| C | PTD5 | PTD2 | PTD0 | VSS | NC | PTC1/ LLWU_P6/ RTC_CLKIN | PTB19 | PTC3/ LLWU_P7 | C |
| D | PTE17 | PTE19 | PTA0 | PTA1 | PTA3 | PTB18 | PTB17 | PTC0 | D |
| E | PTE16 | PTE18 | VSS | VDD | PTA2 | PTB16 | PTB2 | PTB3 | E |
| F | PTE21 | PTE23 | VSSA | VDDA | PTA5 | PTB1 | PTB0/ LLWU_P5 | PTA20 | F |
| G | PTE20 | PTE22 | VREFL | VREFH | PTA4 | PTA13 | VDD | PTA19 | G |
| H | PTE29 | PTE30 | PTE31 | PTE24 | PTE25 | PTA12 | VSS | PTA18 | H |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |

Figure 24. KL16 64-pin BGA pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PKL16 and MKL16

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 40. Part number fields descriptions

| Field | Description | Values |
|-------|-----------------------------|--|
| Q | Qualification status | <ul style="list-style-type: none"> M = Fully qualified, general market flow P = Prequalification |
| KL## | Kinetis family | <ul style="list-style-type: none"> KL16 |
| A | Key attribute | <ul style="list-style-type: none"> Z = Cortex-M0+ |
| FFF | Program flash memory size | <ul style="list-style-type: none"> 256 = 256 KB |
| R | Silicon revision | <ul style="list-style-type: none"> (Blank) = Main A = Revision after main |
| T | Temperature range (°C) | <ul style="list-style-type: none"> V = -40 to 105 |
| PP | Package identifier | <ul style="list-style-type: none"> LH = 64 LQFP (10 mm x 10 mm) MP = 64 MAPBGA (5 mm x 5 mm) |
| CC | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> 4 = 48 MHz |
| N | Packaging type | <ul style="list-style-type: none"> R = Tape and reel |

7.4 Example

This is an example part number:

MKL16Z256VLH4

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | 0.9 | 1.1 | V |

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|--------|---------------------------------|------|------|------|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

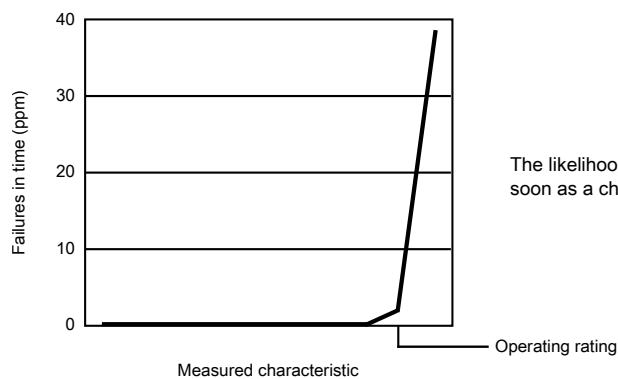
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

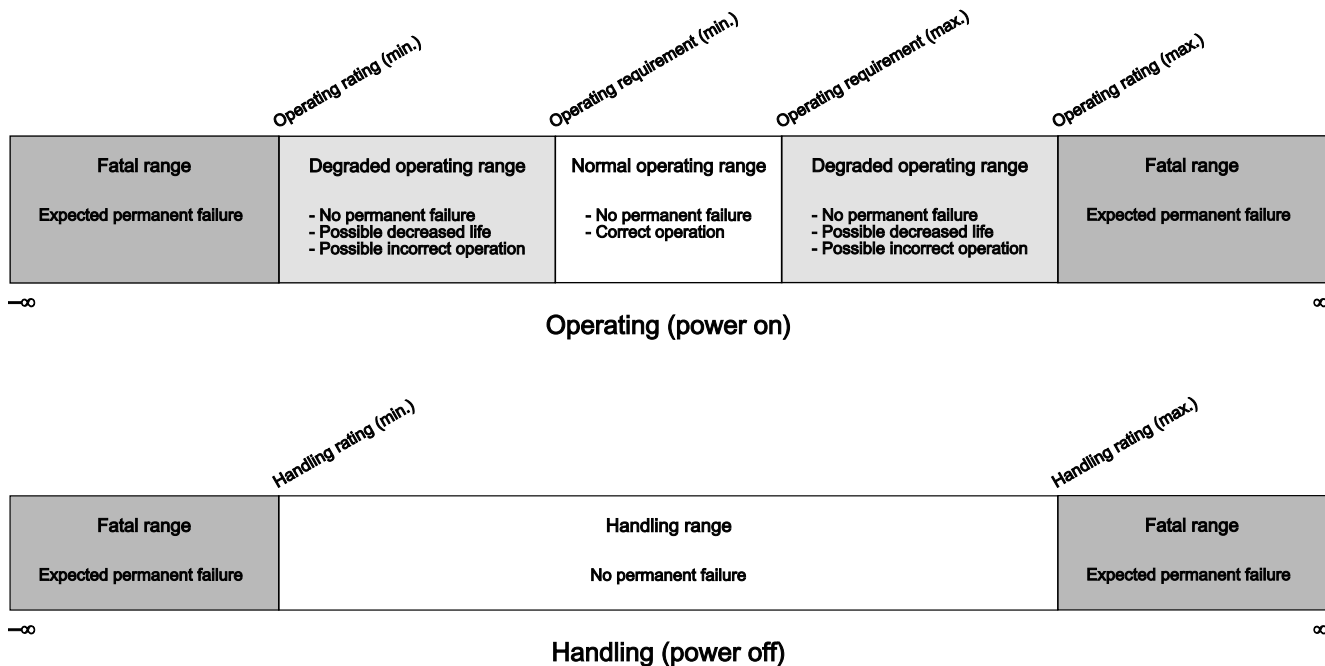
| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | -0.3 | 1.2 | V |

8.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

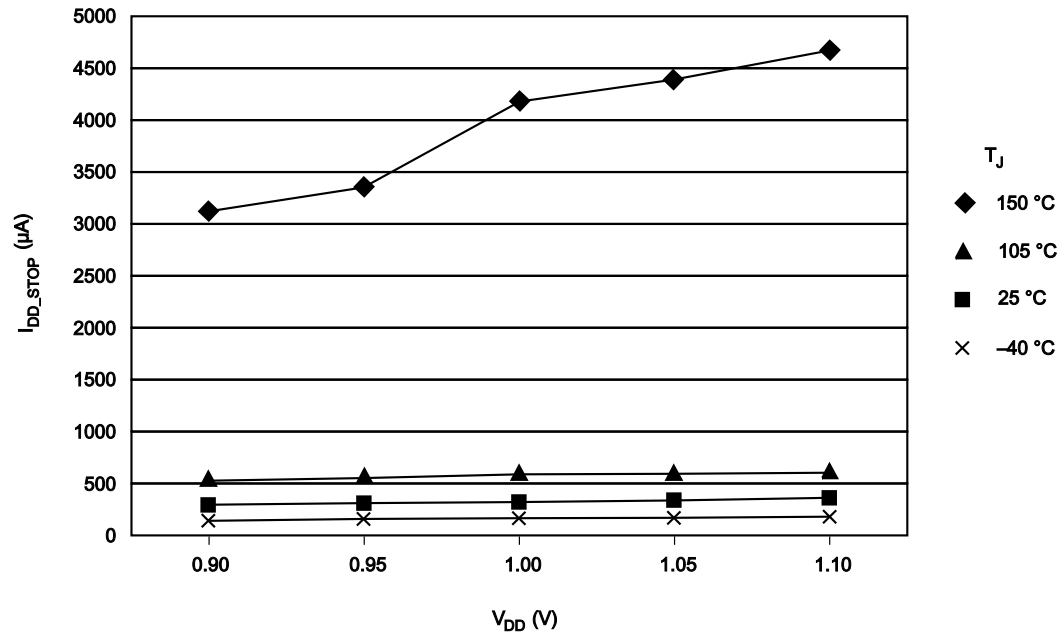
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|----------|--|------|------|------|---------------|
| I_{WP} | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | μA |

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 41. Typical value conditions

| Symbol | Description | Value | Unit |
|-----------------|----------------------|-------|------|
| T _A | Ambient temperature | 25 | °C |
| V _{DD} | 3.3 V supply voltage | 3.3 | V |

9 Revision history

The following table provides a revision history for this document.

Table 42. Revision history

| Rev. No. | Date | Substantial Changes |
|----------|---------|---|
| 3 | 3/2014 | <ul style="list-style-type: none"> Updated the front page and restructured the chapters Updated Voltage and current operating behaviors Updated EMC radiated emissions operating behaviors Updated Power mode transition operating behaviors Updated Capacitance attributes Updated footnote in the Device clock specifications Added V_{REFH} and V_{REFL} in the 16-bit ADC electrical characteristics Updated footnote to the V_{DACR} in the 12-bit DAC operating requirements Added Inter-Integrated Circuit Interface (I2C) timing |
| 4 | 5/2014 | <ul style="list-style-type: none"> Updated Power consumption operating behaviors Updated Definition: Operating behavior |
| 5 | 08/2014 | <ul style="list-style-type: none"> Updated related source in the front page Updated Power consumption operating behaviors |

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