RENESAS

DATASHEET

EL8176

Micropower Single Supply Rail-to-Rail Input/Output Precision Op Amp

FN7436 Rev 9.00 January 6, 2015

The EL8176 is a precision low power, operational amplifier. The device is optimized for single supply operation between 2.4V to 5.5V.

The EL8176 draws minimal supply current while meeting excellent DC-accuracy noise and output drive specifications. Competing devices seriously degrade these parameters to achieve micropower supply current.

The EL8176 can be operated from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail. The output swings to both rails.

Features

- 55µA supply current
- 100µV max offset voltage (8 Ld SO)
- 2nA input bias current
- 400kHz gain-bandwidth product
- Single supply operation down to 2.4V
- Rail-to-rail input and output
- Output sources 31mA and sinks 26mA load current
- Pb-free (RoHS compliant)

Applications

- · Battery- or solar-powered systems
- 4mA to 20mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre amps
- pH probe amplifiers

Pin Configurations











Pin Descriptions

SO PIN NUMBER	SOT-23 PIN NUMBER	PIN NAME	Equivalent Circuit	DESCRIPTION
1, 5		NC		No internal connection
2	4	IN-	Circuit 1	Amplifier's inverting input
3	3	IN+	Circuit 1	Amplifier's non-inverting input
4	2	V-	Circuit 4	Negative power supply
6	1	OUT	Circuit 3 Amplifier's output	
7	6	V+	Circuit 4	Positive power supply
8	5	EN	Circuit 2	Amplifier's enable pin with internal pull-down; Logic "1" selects the disabled state; Logic "0" selects the enabled state.







CIRCUIT 3



CIRCUIT 4

Ordering Information

PART NUMBER (<u>Notes 2</u> , <u>3</u>)	PART MARKING	PACKAGE (RoHS Compliant)	PKG. DWG. #
EL8176FSZ	8176FSZ	8 Ld SO	M8.15E
EL8176FSZ-T7 (<u>Note 1</u>)	8176FSZ	8 Ld SO	M8.15E
EL8176FWZ-T7 (<u>Note 1, 4</u>) BBVA		6 Ld SOT-23	P6.064A
EL8176FWZ-T7A (<u>Note 1</u> , <u>4</u>)	BBVA	6 Ld SOT-23	P6.064A

NOTES:

1. Please refer to $\underline{\text{TB347}}$ for details on reel specifications.

 These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

3. For Moisture Sensitivity Level (MSL), please see product information page for EL8176. For more information on MSL, please see tech brief TB363.

4. The part marking is located on the bottom of the parts.



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V _S) and Power-up Ramp Rate	5.75V, 1V/μs
Differential Input Voltage	0.5V
Current into IN+, IN-, and EN	5mA
Input Voltage V	/0.5V to V+ + 0.5V
ESD Tolerance	
Human Body Model	3kV
Machine Model	

Thermal Information

Thermal Resistance (Typical, <u>Note 5</u>)	θ j (°C/W)
6 Ld SOT-23 Package	230
8 Ld SO Package	125
Ambient Operating Temperature Range	°C to +125°C
Storage Temperature Range65	°C to +150°C
Operating Junction Temperature	+125°C
Pb-Free Reflow Profile	see <u>TB493</u>

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief <u>TB379</u> for details.

Electrical Specifications $V_{+} = 5V$, $V_{-} = 0V$, $V_{CM} = 2.5V$, $R_{L} = 0$ pen, $V_{EN} = 0V$, $T_{A} = +25$ °C, unless otherwise specified. Boldface limits apply across the operating temperature range, -40 °C to +125 °C. Temperature data established by characterization.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (<u>Note 6</u>)	ТҮР	MAX (<u>Note 6</u>)	UNITS
DC SPECIFICATIO	NS					
V _{OS}	Input Offset Voltage	8 Ld SO	-100	±25	100	μV
			-220		220	μV
		6 Ld SOT-23	-350	±80	350	μV
			-350		350	μV
∆V _{OS} ∆Time	Long Term Input Offset Voltage Stability			2.4		µV/Mo
$\frac{\Delta \mathbf{v}_{OS}}{\Delta \mathbf{T}}$	Input Offset Drift vs Temperature			0.7		µV∕°C
	In much Office of Ourseast		-1	±0.4	1	nA
los	Input Offset Current		-4		4	nA
	Janut Bing Oursent		-2	±0.5	2	nA
IB	Input Blas Current		-5		5	nA
CMIR	Input Voltage Range	Guaranteed by CMRR test	0		5	v
OMEE	Common-mode Rejection Ratio	V _{CM} = 0V to 5V	90	110		dB
CMRR			90			dB
DCDD	Deven Sumply Dejection Detic		90	110		dB
PSKK	Power Supply Rejection Ratio	$v_{\rm S} = 2.4v$ to 5.5v	90			dB
	Large Signal Voltage Gain	$V_0 = 0.5V$ to 4.5V, R _L = 100k Ω	200	500		V/mV
A _{VOL}			200			V/mV
		$V_0 = 0.5V$ to 4.5V, $R_L = 1k\Omega$		25		V/mV
		VOL; Output low, $R_L = 100k\Omega$		3	8	mV
	Maximum Output Voltage Swing				10	mV
		VOL; Output low, $R_L = 1k\Omega$		130	200	mV
N.					300	mV
VOUT		VOH; Output high, R _L = 100kΩ	4.994	4.997		v
			4.992			v
		VOH; Output high, R _L = 1kΩ	4.750	4.867		v
			4.7			v
	Supply Current Enabled	V _{EN} = 5V	35	55	75	μA
'S, ON	Supply Current, Enabled		30		90	μΑ
I	Supply Current Disabled	V		3	10	μA
'S, OFF		VEN = OV			10	μA



PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (<u>Note 6</u>)	ТҮР	MAX (<u>Note 6</u>)	UNITS
Lat Short Circuit Output Sourcing Current		B = 100	18	31		mA
10+	Short Circuit Output Sourcing Current		18			mA
I _O -	Short Circuit Output Sinking Current	R = 100	17	26		mA
		$R_{L} = 10\Omega$	15			mA
N.	Supply Veltere	Cuerenteed by BSBD test	2.4		5.5	v
۷S	Supply voltage	Guaranteed by FSRR test	2.4		5.5	v
V _{INH}	Enable Pin High Level		2			v
V _{INL}	Enable Pin Low Level				0.8	v
	Enable Bin Input Current	V – 5V	0.25	0.7	2.0	μA
'ENH	Enable Pin Input Current	$v_{\rm EN} = 5v$			2.5	μA
	Frankla Din Innut Ormant		-0.5	0	+0.5	μA
'ENL		VEN - OV	-1		+1	μA
AC SPECIFICATIO	NS					
GBW	Gain Bandwidth Product			400		kHz
Unity Gain Bandwidth	-3dB Bandwidth	$A_V = 1$, $R_f = 0\Omega$, $R_L = 100k\Omega$ to V_{CM} , $V_{OUT} = 10mV_{P-P}$		1		MHz
	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz, R_L = 10k Ω to V _{CM}		1.5		μV _{P-P}
e _N	Input Noise Voltage Density	f ₀ = 1kHz		28		nV/√Hz
i _N	Input Noise Current Density	f ₀ = 1kHz		0.16		pA∕√Hz
ISO	Off-State Input to Output Isolation	$V_{EN} = 5V, f_0 = 1kHz, A_V = +1, V_{IN} = 1V_{P-P}$		-73		dB
CMRR	Input Common Mode Rejection Ratio	f ₀ = 120Hz; V _{CM} = 1V _{P-P}		-70		dB
PSRR+	Power Supply Rejection Ratio (V+)	$f_0 = 120Hz; V_+, V = \pm 2.5V, V_{SOURCE} = 1V_{P-P}$		-90		dB
PSRR-	Power Supply Rejection Ratio (V_)	$f_0 = 120Hz; V_+, V = \pm 2.5V, V_{SOURCE} = 1V_{P-P}$		-70		dB
TRANSIENT RESP	ONSE					
SR	Slew Rate		±0.065	±0.13	±0.3	V/µs
t _r , t _f , Large Signal	Rise Time, 10% to 90%, V _{OUT}	$A_V = +2$, $V_{OUT} = 2V_{P-P}$, $R_g = R_f = R_L = 10k\Omega$ to V_{CM}		18		μs
	Fall Time, 90% to 10%, V _{OUT}	$A_V = +2$, $V_{OUT} = 2V_{P-P}$, $R_g = R_f = R_L = 10k\Omega$ to V_{CM}		19		μs
t _r , t _f , Small Signal	Rise Time, 10% to 90%, V _{OUT}			2.4		μs
	Fall Time, 90% to 10%, V _{OUT}	$A_V = +2, V_{OUT} = 10mV_{P-P}$ $R_g = R_f = R_L = 10k\Omega \text{ to } V_{CM}$		2.4		μs
	Enable to Output Turn-on Delay Time, 10% EN to 10% V _{OUT}	$V_{\overline{EN}} = 5V$ to 0V, A _V = +2, R _g = R _f = R _L = 10k\Omega to V _{CM}		4		μs
tEN	Enable to Output Turn-off Delay Time, 10% EN to 10% V _{OUT}	$V_{\overline{EN}} = 0V$ to 5V, $A_V = +2$, $R_g = R_f = R_L = 10k\Omega$ to V_{CM}		0.1		μs

Electrical Specifications $V_{+} = 5V$, $V_{-} = 0V$, $V_{CM} = 2.5V$, $R_{L} = 0$ pen, $V_{EN} = 0V$, $T_{A} = +25$ °C, unless otherwise specified. Boldface limits apply across the operating temperature range, -40 °C to +125 °C. Temperature data established by characterization. (Continued)

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25 °C, unless otherwise specified. Temperature limits established by characterization and are not production tested.



Typical Performance Curves

FIGURE 1. A_{VOL} vs FREQUENCY AT $1k\Omega$ LOAD



FIGURE 3. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES ${\rm R_{f}}/{\rm R_{g}}$





FIGURE 2. A_{VOL} vs FREQUENCY AT 100k Ω LOAD



FIGURE 4. GAIN vs FREQUENCY vs V_{OUT}, R_L = 1k









FIGURE 8. FREQUENCY RESPONSE vs CLOSED LOOP GAIN





FIGURE 11. GAIN vs FREQUENCY vs CL

















FIGURE 17. INPUT VOLTAGE NOISE 0.1Hz TO 10Hz







FIGURE 16. INPUT CURRENT NOISE DENSITY vs FREQUENCY



FIGURE 18. LARGE SIGNAL STEP RESPONSE





FIGURE 19. SMALL SIGNAL STEP RESPONSE



FIGURE 20. ENABLE TO OUTPUT RESPONSE



FIGURE 21. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE



FIGURE 23. INPUT OFFSET VOLTAGE vs OUTPUT VOLTAGE



FIGURE 22. INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

















FIGURE 29. I_{BIAS} (-) vs TEMPERATURE V_S = ±2.5V







































FIGURE 37. CMRR vs TEMPERATURE VCM = +2.5V TO -2.5V









FIGURE 38. PSRR vs TEMPERATURE V_S = ±1.2V TO ±2.5V



FIGURE 40. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 1k $V_S = \pm 2.5V$



V_S = ±2.5V







Applications Information

Introduction

The EL8176 is a rail-to-rail input and output micro-power precision single supply operational amplifier with an enable feature. The device achieves rail-to-rail input and output operation and eliminates the concerns introduced by a conventional rail-to-rail I/O operational amplifier as discussed below.

Rail-to-Rail Input

The input common-mode voltage range of the EL8176 goes from negative supply to positive supply without introducing offset errors or degrading performance associated with a conventional rail-to-rail input operational amplifier. Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The EL8176 achieves input rail-to-rail without sacrificing important precision specifications and without degrading distortion performance. The EL8176's input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range for the EL8176 gives us an undistorted behavior from typically 10mV above the negative rail all the way up to the positive rail.



Input Bias Current Compensation

The input bias currents as low as 500pA are achieved while maintaining an excellent bandwidth for a micro-power operational amplifier. Inside the EL8176 is an input bias canceling circuit. The input stage transistors are still biased with an adequate current for speed but the canceling circuit sinks most of the base current, leaving a small fraction as input bias current. The input bias current compensation/cancellation is stable from -40°C to +125°C and operates from typically 10mV to the positive supply rail.

Rail-to-Rail Output

A pair of complementary MOSFET devices achieves rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. The EL8176 with a 100k Ω load will swing to within 3mV of the supply rails.

Enable/Disable Feature

The EL8176 offers an \overline{EN} pin. The active low \overline{EN} pin disables the device when pulled up to at least 2.0V. When disabled, the output is in a high impedance state and the part consumes typically $3\mu A$. When disabled, the high impedance output allows multiple parts to be MUXed together. When configured as a MUX, the outputs are tied together in parallel and a channel can be selected by pulling the \overline{EN} pin to 0.8V or lower. The \overline{EN} pin has an internal pull-down. If left open or floating, the \overline{EN} pin will internally be pulled low, enabling the part by default.

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage of the EL8176, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 46 shows how the guard ring should be configured and Figure 47 shows the top view of how a surface mount layout can be arranged. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.





FIGURE 47.

Typical Applications



FIGURE 48. THERMOCOUPLE AMPLIFIER

Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability and ability to measure a wide range of temperatures. The EL8176 is used to convert the differential thermocouple voltage into single-ended signal with 10x gain. The EL8176's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the converter to run from a single 5V supply.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
January 6, 2015	FN7436.9	 Updated entire datasheet to Intersil new standard. Removed WLCSP throughout the document. Ordering information table on page 2: Added MSL note. Added revision history and about Intersil verbiage Updated 8 Ld SO POD from "MDP0027" to "M8.15E".

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Package Outline Drawing

M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE Rev 0, 08/09





SIDE VIEW "B"



- 1. Dimensions are in millimeters. Dimensions in () for Reference Only.
- 2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
- 3. Unless otherwise specified, tolerance : Decimal ± 0.05
- Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
- 5. The pin #1 identifier may be either a mold or mark feature.
- 6. Reference to JEDEC MS-012.

TYPICAL RECOMMENDED LAND PATTERN



Package Outline Drawing

P6.064A

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE Rev 0, 2/10



<u>/</u>5

SIDE VIEW

2.90

☐ 0.15 C A-B

0.05-0.15

1.14 ±0.15

2x



END VIEW





 NOTES:

- 1. Dimensions are in millimeters. Dimensions in () for Reference Only.
- 2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
- 3. Dimension is exclusive of mold flash, protrusions or gate burrs.
- A. Foot length is measured at reference to guage plane.
- 5. This dimension is measured at Datum "H".
- 6. Package conforms to JEDEC MO-178AA.

