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FAIRCHILD SEMICONDUCTOR®

August 2009

FXL4TD245

Low-Voltage Dual-Supply 4-Bit Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-STATE Outputs and Independent Direction Controls

Features

- Bi-directional interface between any 2 levels from 1.1V to 3.6V
- Fully configurable: inputs track V_{CC} level
- Non-preferential power-up sequencing; either V_{CC} may be powered-up first
- Outputs remain in 3-STATE until active V_{CC} level is reached
- Outputs switch to 3-STATE if either V_{CC} is at GND
- Power-off protection
- Control inputs ($T/\overline{R}_n$, $\overline{OE}$) levels are referenced to V_{CCA} voltage
- Packaged in 16-terminal DQFN (2.5mm x 3.5mm) and 16-terminal MicroMLP (1.8mm x 2.6mm)
- ESD protections exceeds:
  - 4kV HBM ESD (per JESD22-A114 & Mil Std 883e 3015.7)
  - 8kV HBM I/O to GND ESD (per JESD22-A114 & Mil Std 883e 3015.7)
  - 1kV CDM ESD (per ESD STM 5.3)
  - 200V MM ESD (per JESD22-A115 & ESD STM5.2)

General Description

The FXL4TD245 is a configurable 4-bit dual-voltage-supply translator designed for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6V to as low as 1.1V. The A port tracks the V_{CCA} level, and the B port tracks the V_{CCB} level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.

The device remains in 3-STATE until both V_{CC}s reach active levels allowing either V_{CC} to be powered-up first. Internal power down control circuits place the device in 3-STATE if either V_{CC} is removed.

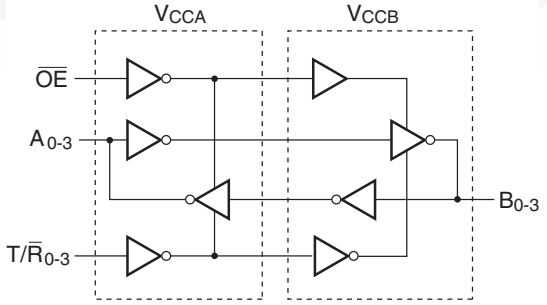
The Transmit/Receive ($T/\overline{R}$) inputs independently determine the direction of data through each of the four bits. The $\overline{OE}$ input, when HIGH, disables both the A and B Ports by placing them in a 3-STATE condition. The FXL4TD245 is designed so that the control pins ($T/\overline{R}$ and $\overline{OE}$) are supplied by V_{CCA}.

Ordering Information

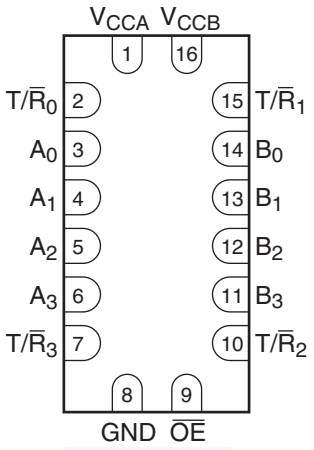
Order Number	Package Number	Eco Status	Package Description
FXL4TD245BQX	MLP016E	Green	16-Terminal Depopulated Quad Very-Thin Flat Pack, No Leads (DQFN), JEDEC MO-241, 2.5mm x 3.5mm
FXL4TD245UMX	UMLP16A	Green	16-Terminal Quad, Ultrathin, Molded Leadless Package (UMLP), 1.8mm x 2.6mm, 0.4mm Pitch

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

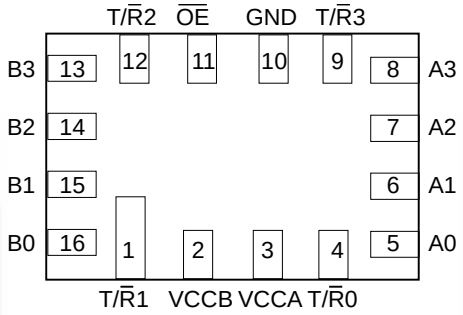
Functional Diagram



Connection Diagrams

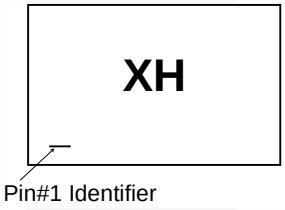


DQFN Pad Assignments (Top Through View)



MicroMLP Pad Assignments (Top Through View)

Top Mark



MicroMLP Top Mark (Top View)

Pin Assignment

DQFN Pin #	µMLP Pin #	Terminal Name	Description
1	3	V_{CCA}	Side A Power Supply
2	4	$T/\overline{R}_0$	Transmit/Receive Input
3–6	5–8	A_0–A_3	Side A Inputs or 3-STATE Outputs
7	9	$T/\overline{R}_3$	Transmit/Receive Input
8	10	GND	Ground
9	11	$\overline{OE}$	Output Enable Input
10	12	$T/\overline{R}_2$	Transmit/Receive Input
11–14	13–16	B_3–B_0	Side B Inputs or 3-STATE Outputs
15	1	$T/\overline{R}_1$	Transmit/Receive Input
16	2	V_{CCB}	Side B Power Supply

Truth Table

Inputs					Outputs
$\overline{OE}$	$T/\overline{R}_0$	$T/\overline{R}_1$	$T/\overline{R}_2$	$T/\overline{R}_3$	
L	L	X	X	X	B0 Data to A0 Output
L	H	X	X	X	A0 Data to B0 Output
L	X	L	X	X	B1 Data to A1 Output
L	X	H	X	X	A1 Data to B1 Output
L	X	X	L	X	B2 Data to A2 Output
L	X	X	H	X	A2 Data to B2 Output
L	X	X	X	L	B3 Data to A3 Output
L	X	X	X	H	A3 Data to B3 Output
H	X	X	X	X	3-State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Power-Up/Power-Down Sequencing

FXL translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 volts, outputs are in a HIGH-Impedance state. The control inputs ($T/\overline{R}_n$ and $\overline{OE}$) are designed to track the V_{CCA} supply. A pull-up resistor tying $\overline{OE}$ to V_{CCA} should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-up resistor is based upon the current-sinking capability of the $\overline{OE}$ driver.

The recommended power-up sequence is the following:

1. Apply power to either V_{CC}.
2. Apply power to the $T/\overline{R}_n$ inputs (Logic HIGH for A-to-B operation; Logic LOW for B-to-A operation) and to the respective data inputs (A Port or B Port). This may occur at the same time as Step 1.
3. Apply power to other V_{CC}.
4. Drive the $\overline{OE}$ input LOW to enable the device.

The recommended power-down sequence is the following:

1. Drive $\overline{OE}$ input HIGH to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Symbol	Parameter	Rating
V_{CCA}, V_{CCB}	Supply Voltage	−0.5V to +4.6V
V_I	DC Input Voltage	
	I/O Port A	−0.5V to +4.6V
	I/O Port B	−0.5V to +4.6V
	Control Inputs ($T/\overline{R}_n$, $\overline{OE}$)	−0.5V to +4.6V
V_O	Output Voltage[1]	
	Outputs 3-STATE	−0.5V to +4.6V
	Outputs Active (A_n)	−0.5V to V_{CCA} + 0.5V
	Outputs Active (B_n)	−0.5V to V_{CCB} + 0.5V
I_{IK}	DC Input Diode Current @ V_I < 0V	−50mA
I_{OK}	DC Output Diode Current @	
	V_O < 0V	−50mA
	V_O > V_{CC}	+50mA
I_{OH} / I_{OL}	DC Output Source/Sink Current	−50mA / +50mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin	±100mA
T_{STG}	Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions[2]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Rating
V_{CCA} or V_{CCB}	Power Supply Operating	1.1V to 3.6V
	Input Voltage	
	Port A	0.0V to 3.6V
	Port B	0.0V to 3.6V
	Control Inputs ($T/\overline{R}_n$, $\overline{OE}$)	0.0V to V_{CCA}
	Output Current in I_{OH}/I_{OL} with V_{CC} @	
	3.0V to 3.6V	±24mA
	2.3V to 2.7V	±18mA
	1.65V to 1.95V	±6mA
	1.4V to 1.65V	±2mA
	1.1V to 1.4V	±0.5mA
T_A	Free Air Operating Temperature	−40°C to +85°C
$\Delta t / \Delta V$	Maximum Input Edge Rate $V_{CCA/B}$ = 1.1V to 3.6V	10ns/V

Notes:

1. I_O Absolute Maximum Rating must be observed.
2. All unused inputs and I/O pins must be held at V_{CCI} or GND.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CCI} (V)	V_{CCO} (V)	Min.	Max.	Units
V_{IH}	High Level Input Voltage[3]	Data Inputs A_n, B_n	2.7–3.6	1.1–3.6	2.0		V
			2.3–2.7		1.6		
			1.65–2.3		0.65 x V_{CCI}		
			1.4–1.65		0.65 x V_{CCI}		
			1.1–1.4		0.9 x V_{CCI}		
		Control Pins $\overline{OE}$, T/$\overline{R}_n$ (Referenced to V_{CCA})	2.7–3.6	1.1–3.6	2.0		
			2.3–2.7		1.6		
			1.65–2.3		0.65 x V_{CCA}		
			1.4–1.65		0.65 x V_{CCA}		
			1.1–1.4		0.9 x V_{CCA}		
V_{IL}	Low Level Input Voltage[3]	Data Inputs A_n, B_n	2.7–3.6	1.1–3.6		0.8	V
			2.3–2.7			0.7	
			1.65–2.3			0.35 x V_{CCI}	
			1.4–1.65			0.35 x V_{CCI}	
			1.1–1.4			0.1 x V_{CCI}	
		Control Pins $\overline{OE}$, T/$\overline{R}_n$ (Referenced to V_{CCA})	2.7–3.6	1.1–3.6		0.8	
			2.3–2.7			0.7	
			1.65–2.3			0.35 x V_{CCA}	
			1.4–1.65			0.35 x V_{CCA}	
			1.1–1.4			0.1 x V_{CCA}	
V_{OH}	High Level Output Voltage[4]	I_{OH} = –100μA	1.1–3.6	1.1–3.6	V_{CC0}–0.2		V
		I_{OH} = –12mA	2.7	2.7	2.2		
		I_{OH} = –18mA	3.0	3.0	2.4		
		I_{OH} = –24mA	3.0	3.0	2.2		
		I_{OH} = –6mA	2.3	2.3	2.0		
		I_{OH} = –12mA	2.3	2.3	1.8		
		I_{OH} = –18mA	2.3	2.3	1.7		
		I_{OH} = –6mA	1.65	1.65	1.25		
		I_{OH} = –2mA	1.4	1.4	1.05		
		I_{OH} = –0.5mA	1.1	1.1	0.75 x V_{CC0}		
V_{OL}	Low Level Output Voltage[4]	I_{OL} = 100μA	1.1–3.6	1.1- 3.6		0.2	V
		I_{OL} = 12mA	2.7	2.7		0.4	
		I_{OL} = 18mA	3.0	3.0		0.4	
		I_{OL} = 24mA	3.0	3.0		0.55	
		I_{OL} =12mA	2.3	2.3		0.4	
		I_{OL} = 18mA	2.3	2.3		0.6	
		I_{OL} = 6mA	1.65	1.65		0.3	
		I_{OL} = 2mA	1.4	1.4		0.35	
		I_{OL} = 0.5mA	1.1	1.1		0.3 x V_{CC0}	

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CCI} (V)	V_{CCO} (V)	Min.	Max.	Units
I_I	Input Leakage Current. Control Pins	$V_I = V_{CCA}$ or GND	1.1–3.6	3.6		±1.0	µA
I_{OFF}	Power Off Leakage Current	A_n, V_I or V_O = 0V to 3.6V	0	3.6		±10.0	µA
		B_n, V_I or V_O = 0V to 3.6V	3.6	0		±10.0	
I_{OZ}	3-STATE Output Leakage[5] $0 \le V_O \le 3.6V$ $V_I = V_{IH}$ or V_{IL}	A_n, B_n $\overline{OE} = V_{IH}$	3.6	3.6		±10.0	µA
		B_n, $\overline{OE}$ = Don't Care	0	3.6		+10.0	
		A_n, $\overline{OE}$ = Don't Care	3.6	0		+10.0	
$I_{CCA/B}$	Quiescent Supply Current[6]	$V_I = V_{CCI}$ or GND; $I_O = 0$	1.1–3.6	1.1–3.6		20.0	µA
I_{CCZ}	Quiescent Supply Current[6]	$V_I = V_{CCI}$ or GND; $I_O = 0$	1.1–3.6	1.1–3.6		20.0	µA
I_{CCA}	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$	0	1.1–3.6		−10.0	µA
		$V_I = V_{CCA}$ or GND; $I_O = 0$	1.1–3.6	0		10.0	µA
I_{CCB}	Quiescent Supply Current	$V_I = V_{CCB}$ or GND; $I_O = 0$	1.1–3.6	0		−10.0	µA
		$V_I = V_{CCB}$ or GND; $I_O = 0$	0	1.1–3.6		10.0	µA
$\Delta I_{CCA/B}$	Increase in I_{CC} per Input; Other Inputs at V_{CC} or GND	V_{IH} = 3.0	3.6	3.6		500	µA

Notes:

3. V_{CCI} = the V_{CC} associated with the data input under test.
4. V_{CCO} = the V_{CC} associated with the output under test.
5. Don't Care = Any valid logic level.
6. Reflects current per supply, V_{CCA} or V_{CCB}.

AC Electrical Characteristics

V_{CCA} = 3.0V to 3.6V

Symbol	Parameter	$T_A = -40°C$ to $+85°C$										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	1.4	22.0	ns
	Propagation Delay B to A	0.2	3.5	0.2	3.8	0.3	4.0	0.5	4.3	0.8	13.0	
t_{PZH}, t_{PZL}	Output Enable $\overline{OE}$ to B	0.5	4.0	0.7	4.4	1.0	5.9	1.0	6.4	1.5	17.0	ns
	Output Enable $\overline{OE}$ to A	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{OE}$ to B	0.2	3.8	0.2	4.0	0.7	4.8	1.5	6.2	2.0	17.0	ns
	Output Disable $\overline{OE}$ to A	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	

V_{CCA} = 2.3V to 2.7V

Symbol	Parameter	$T_A = -40°C$ to $+85°C$										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	1.4	22.0	ns
	Propagation Delay B to A	0.3	3.9	0.4	4.2	0.5	4.5	0.5	4.8	1.0	7.0	
t_{PZH}, t_{PZL}	Output Enable $\overline{OE}$ to B	0.6	4.2	0.8	4.6	1.0	6.0	1.0	6.8	1.5	17.0	ns
	Output Enable $\overline{OE}$ to A	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{OE}$ to B	0.2	4.1	0.2	4.3	0.7	4.8	1.5	6.7	2.0	17.0	ns
	Output Disable $\overline{OE}$ to A	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	

V_{CCA} = 1.65V to 1.95V

Symbol	Parameter	$T_A = -40°C$ to $+85°C$										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.3	4.0	0.5	4.5	0.8	5.7	0.9	7.1	1.5	22.0	ns
	Propagation Delay B to A	0.5	5.4	0.5	5.6	0.8	5.7	1.0	6.0	1.2	8.0	
t_{PZH}, t_{PZL}	Output Enable $\overline{OE}$ to B	0.6	5.2	0.8	5.4	1.2	6.9	1.2	7.2	1.5	18.0	ns
	Output Enable $\overline{OE}$ to A	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{OE}$ to B	0.2	5.1	0.2	5.2	0.8	5.2	1.5	7.0	2.0	17.0	ns
	Output Disable $\overline{OE}$ to A	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	

AC Electrical Characteristics (Continued)

V_{CCA} = 1.4V to 1.6V

Symbol	Parameter	$T_A = -40°C$ to $+85°C$										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.5	4.3	0.5	4.8	1.0	6.0	1.0	7.3	1.5	22.0	ns
	Propagation Delay B to A	0.6	6.8	0.8	6.9	0.9	7.1	1.0	7.3	1.3	9.5	
t_{PZH}, t_{PZL}	Output Enable $\overline{OE}$ to B	1.1	7.5	1.1	7.6	1.3	7.7	1.4	7.9	2.0	20.0	ns
	Output Enable $\overline{OE}$ to A	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{OE}$ to B	0.4	6.1	0.4	6.2	0.9	6.2	1.5	7.5	2.0	18.0	ns
	Output Disable $\overline{OE}$ to A	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	

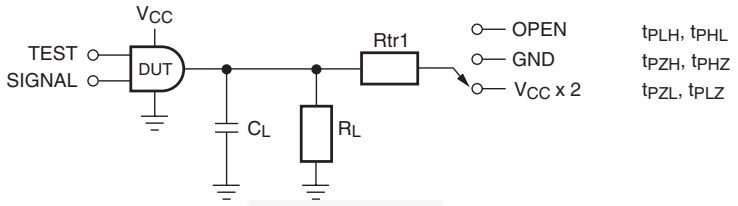
V_{CCA} = 1.1V to 1.3V

Symbol	Parameter	$T_A = -40°C$ to $+85°C$										Units
		V_{CCB} = 3.0V to 3.6V		V_{CCB} = 2.3V to 2.7V		V_{CCB} = 1.65V to 1.95V		V_{CCB} = 1.4V to 1.6V		V_{CCB} = 1.1V to 1.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.8	13.0	1.0	7.0	1.2	8.0	1.3	9.5	2.0	24.0	ns
	Propagation Delay B to A	1.4	22.0	1.4	22.0	1.5	22.0	1.5	22.0	2.0	24.0	
t_{PZH}, t_{PZL}	Output Enable $\overline{OE}$ to B	1.0	12.0	1.0	9.0	2.0	10.0	2.0	11.0	2.0	24.0	ns
	Output Enable $\overline{OE}$ to A	2.0	22.0	2.0	22.0	2.0	22.0	2.0	22.0	2.0	22.0	
t_{PHZ}, t_{PLZ}	Output Disable $\overline{OE}$ to B	1.0	15.0	0.7	7.0	1.0	8.0	2.0	10.0	2.0	20.0	ns
	Output Disable $\overline{OE}$ to A	2.0	15.0	2.0	12.0	2.0	12.0	2.0	12.0	2.0	12.0	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$	Units
			Typical	
C_{IN}	Input Capacitance Control Pins ($\overline{OE}$, T/$\overline{R}$)	$V_{CCA} = V_{CCB} = 3.3V$, $V_I = 0V$ or $V_{CCA/B}$	4.0	pF
$C_{I/O}$	Input/Output Capacitance A_n, B_n Ports	$V_{CCA} = V_{CCB} = 3.3V$, $V_I = 0V$ or $V_{CCA/B}$	5.0	pF
C_{PD}	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3V$, $V_I = 0V$ or V_{CC}, F = 10MHz	20.0	pF

AC Loading and Waveforms

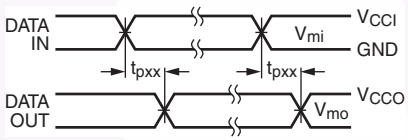


Test	Switch
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	V_{CCO} x 2 at V_{CCO} = 3.3 ± 0.3V, 2.5V ± 0.2V, 1.8V ± 0.15V, 1.5V ± 0.1V, 1.2V ± 0.1V
t_{PHZ}, t_{PZH}	GND

Figure 1. AC Test Circuit

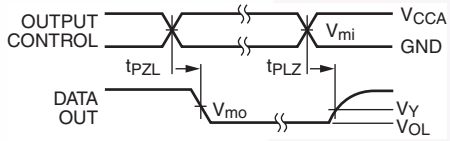
AC Load Table

V_{CCO}	C_L	R_L	Rtr1
1.2V ± 0.1V	15pF	2kΩ	2kΩ
1.5V ± 0.1V	15pF	2kΩ	2kΩ
1.8V ± 0.15V	15pF	2kΩ	2kΩ
2.5V ± 0.2V	15pF	2kΩ	2kΩ
3.3V ± 0.3V	15pF	2kΩ	2kΩ



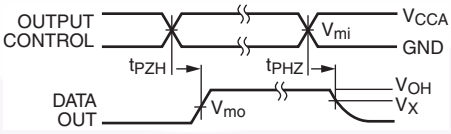
Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ V_I = 3.0V to 3.6V only

Figure 2. Waveform for Inverting and Non-Inverting Functions



Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ V_I = 3.0V to 3.6V only

Figure 3. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic



Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ V_I = 3.0V to 3.6V only

Figure 4. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}				
	3.3V ± 0.3V	**2.5V ± 0.2V**	**1.8V ± 0.15V**	**1.5V ± 0.1V**	**1.2V ± 0.1V**
V_{mi}	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$	$V_{CCI}/2$
V_{mo}	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$	$V_{CCO}/2$
V_X	$V_{OH}-0.3V$	$V_{OH}-0.15V$	$V_{OH}-0.15V$	$V_{OH}-0.1V$	$V_{OH}-0.1V$
V_Y	$V_{OL}+0.3V$	$V_{OL}+0.15V$	$V_{OL}+0.15V$	$V_{OL}+0.1V$	$V_{OL}+0.1V$

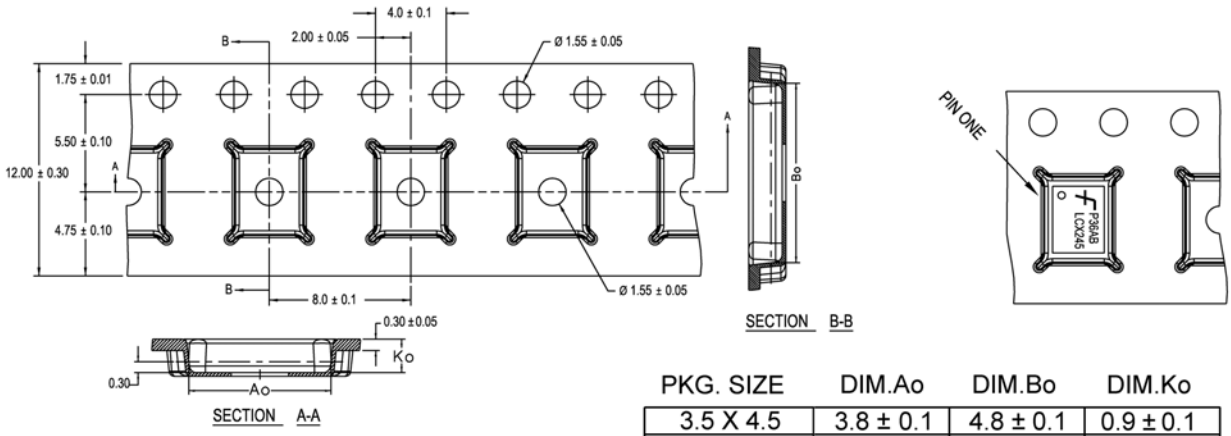
For V_{mi}: $V_{CCI} = V_{CCA}$ for Control Pins T/$\overline{R}$ and $\overline{OE}$, or $V_{CCA}/2$

Tape and Reel Specification

Tape Format for DQFN 10

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

Tape Dimensions millimeters



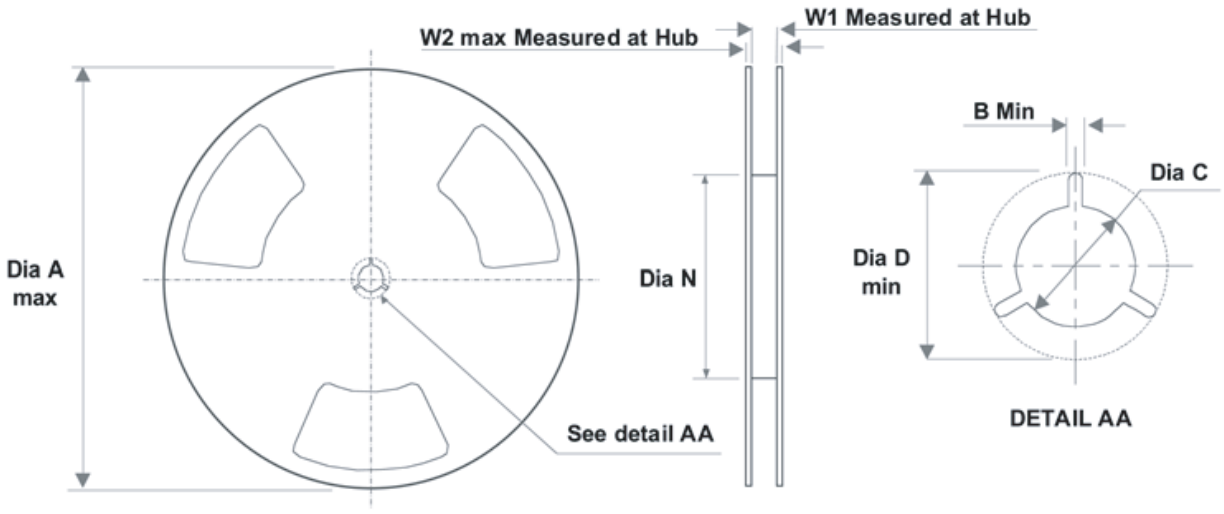
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

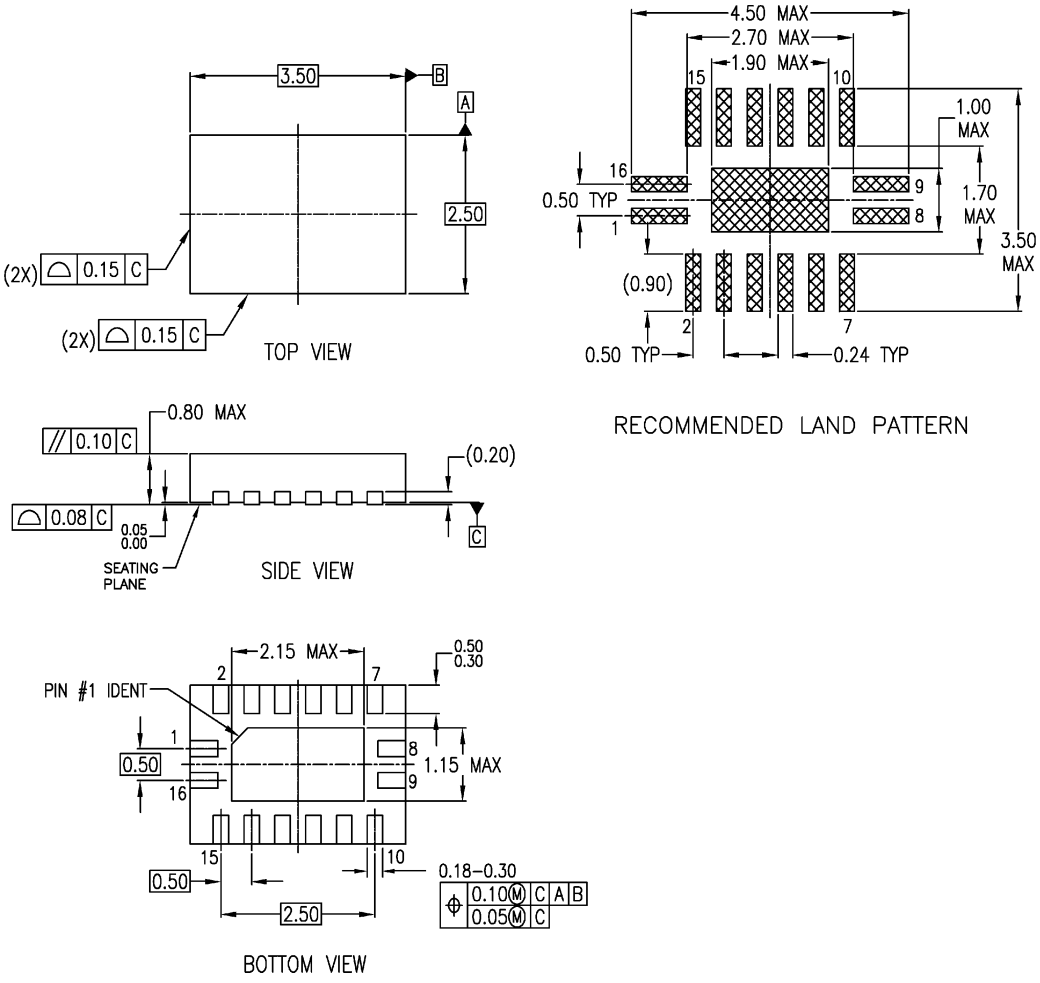
1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−241, VARIATION AB
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP016ErevA

Figure 5. 16-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241 2.5 x 3.5mm

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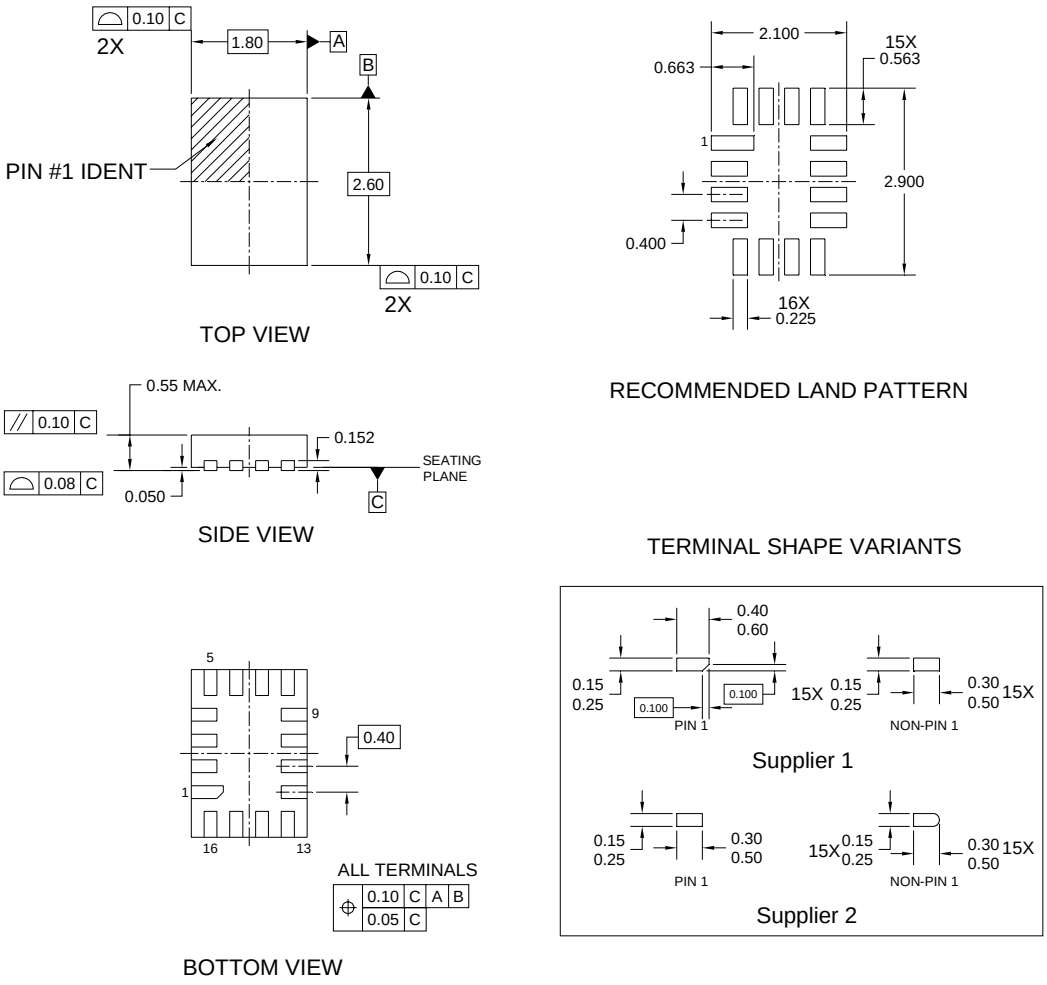
Physical Dimensions



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E. LAND PATTERN IS A MINIMAL TOE DESIGN
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Figure 5. 16-Terminal Quad, Ultrathin, Molded Leadless Package (UMLP), 1.8mm x 2.6mm

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