

LV55D Series 3.3 V LVDS Clock Oscillators

November 2018

Lead Free 

- Pletronics' LV55D Series is a quartz crystal controlled precision square wave generator with an LVDS output.
- The package is designed for high density surface mount designs.
- Low cost mass produced oscillator.
- Tape and Reel or cut tape packaging is available.
- 3.2 x 5 mm LCC Ceramic Package
- Enable/Disable Function on pad 1
- Disable function includes low standby power mode
- Low Jitter

**Pletronics Inc. certifies this device is in accordance with the
RoHS 6/6 (2011/65/EC) and WEEE (2002/96/EC) directives.**

Pletronics Inc. guarantees the device does not contain the following:

Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's

Weight of the Device: 0.09 grams

Moisture Sensitivity Level: 1 As defined in J-STD-020C

Second Level Interconnect code: e4

Absolute Maximum Ratings:

Parameter	Unit
V _{CC} Supply Voltage	-0.5V to +5.0V
V _i Input Voltage	-0.5V to V _{CC} + 0.5V
V _o Output Voltage	-0.5V to V _{CC} + 0.5V

Thermal Characteristics

The maximum die or junction temperature is 155°C

The thermal resistance junction to board is 45 to 65°C/Watt depending on the solder pads, ground plane and construction of the PCB.

Part Number:

LV55	45	D	E	V	-125.0M	-XX	
							Packaging code or blank T250 = 250 per Tape and Reel T500 = 500 per Tape and Reel T1K = 1000 per Tape and Reel
							Frequency in MHz
							Supply Voltage V_{CC} V = 3.3V \pm 10%
							Optional Enhanced OTR Blank = Temp. range -10 to +70°C C = Temp. range -20 to +70°C E = Temp. range -40 to +85°C
							Series Model
							Frequency Stability 45 = \pm 50 ppm 44 = \pm 25 ppm 20 = \pm 20 ppm
							Series Model

Part Marking:

PFFF.FL
• **YMDXX**

Marking Legend:

P = Pletronics
 FFF.F = Frequency in MHz
 L = LVDS
 YMD = Date of Manufacture (year and week, or year-month-day)
 All other marking is internal factory codes

Specifications such as frequency stability, supply voltage and operating temperature range, etc. are not identified from the marking. External packaging labels and packing list will correctly identify the ordered Pletronics part number.

Codes for Date Code YMD

Code	6	7	8	9	0	Code	A	B	C	D	E	F	G	H	J	K	L	M
Year	2016	2017	2018	2019	2020	Month	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC

Code	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	G
Day	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Code	H	J	K	L	M	N	P	R	T	U	V	W	X	Y	Z	
Day	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Electrical Specification for 3.30V $\pm 10\%$ over the specified temperature range and the frequency range of 80 to 325 MHz

Item	Min	Max	Unit	Condition	
Frequency Accuracy “45”	-50	+50	ppm	For all supply voltages, load changes, aging for 1 year, shock, vibration and temperatures	
“44”	-25	+25			
“20”	-20	+20			
Output Waveform	LVDS				
Output High Level	--	1.60	Volts	-	See load circuit R1 = 50 ohms
Output Low Level	0.90	--	Volts	-	
Differential Output (V _{OD})	250	450	mVolts	-	
Output Offset Voltage (V _{OS})	1.125	1.375	Volts	≥ 80 MHz	
	1.125	1.500	Volts	< 80 MHz	
Differential Output Error (dV _{OS})	--	50	mVolts	-	
Output Symmetry	45	55	%	Referenced to 50% of amplitude or crossing point	
Output T _{RISE} and T _{FALL}	-	700	pS	≥ 80 MHz	Vth is 20% and 80% of waveform
	-	900	pS	< 80 MHz	
Jitter	-	0.6	pS RMS	Measured from 12KHz to 20MHz from Fnominal	
	-	2.8		Measured from 10Hz to 1MHz from Fnominal	
Vcc Supply Current	-	66	mA	≥ 80 MHz	Includes current of properly terminated device
	-	45	mA	< 80 MHz	
Enable/Disable Internal Pull-up	50	-	Kohm	To Vcc (equivalent resistance)	
V disable	-	0.8	Volts	Referenced to Ground	
V enable	2.0	-	Volts	Referenced to Ground	
Output leakage V _{OUT} = V _{CC}	-10	+10	uA	Pad 1 low, device disabled	
V _{OUT} = 0V	-10	+10	uA		
Enable	-	2	mS	Time for output to reach a logic state	
Disable time	-	200	nS	Time for output to reach a high Z state	
Start up time	-	5	mS	≥ 80 MHz	Measured from the time Vcc = 3.0V
	-	3	mS	< 80 MHz	
Operating Temperature Range	-10	+70	°C	Standard Temperature Range	
	-20	+70	°C	Extended Temperature Range “C” Option	
	-40	+85	°C	Extended Temperature Range “E” Option	
Storage Temperature Range	-55	+125	°C		
Standby Current I _{CC}	-	30	uA	≥ 80 MHz	Pad 1 low, device disabled
	-	1.5	mA	< 80 MHz	

Specifications with Pad 1 E/D open circuit

The diagram shows a Unit Under Test (UUT) with the following connections:

- Pin 1 (E/D):** Connected to $V_{E/D}$.
- Pin 2 (Vcc):** Connected to V_{cc} . A $0.01 \mu F$ capacitor is connected from V_{cc} to ground. A $2.2 \mu F$ SMD Tantalum capacitor is connected from V_{cc} to V_{cc} (likely a typo for a different supply or ground).
- Pin 3 (GND):** Connected to ground.
- Pins 4 (Out) and 5 (Out*):** Connected to a load network consisting of two resistors $R1$ in series. The voltage across the load is V_{dd} and $V_{bss, dV_{bss}}$.

Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002, Condition B
Vibration	MIL-STD-883 Method 2007, Condition A
Solderability	MIL-STD-883 Method 2003
Thermal Shock	MIL-STD-883 Method 1011, Condition A

ESD Rating

Model	Minimum Voltage	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

Package Labeling

Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Courier New
Bar code is 39-Full ASCII

Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Arial

P/N:  LV5545DV-100.0M	
Customer P/N:  12345678	
Qty:  1000 D/C  6MC	

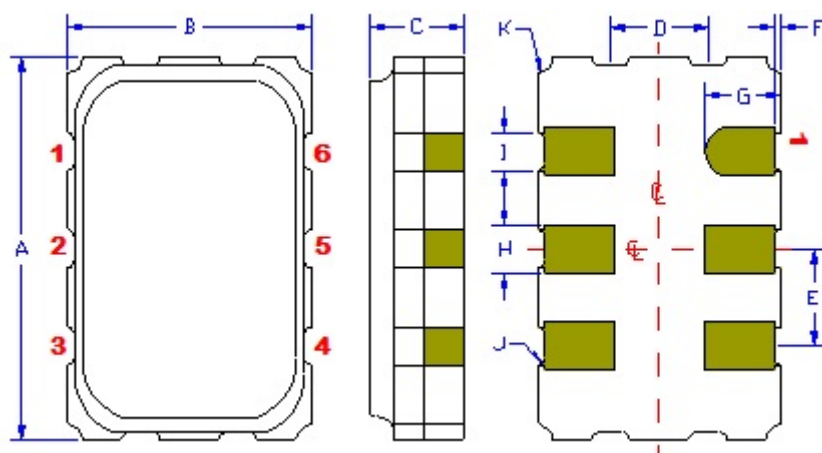
RoHS Compliant

2nd LVL Interconnect

Category=e4

Max Safe Temp=260C for 10s 2X Max

Mechanical:



Contacts:

Gold 11.8 to 39.4 μ m (0.3 to 1.0 μ m)
over
Nickel 50 to 350 μ m (1.27 to 8.89 μ m)

¹ Typical dimensions

Not to Scale

	Inches	mm
A	0.197 \pm 0.006	5.00 \pm 0.15
B	0.125 \pm 0.006	3.20 \pm 0.15
C	0.053 max	1.35 max
D ¹	0.050	1.27
E ¹	0.050	1.27
F ¹	0.004	0.10
G ¹	0.039	1.00
H ¹	0.025	0.63
I ¹	0.020	0.50
J ¹	0.004R	0.10R
K ¹	0.008R	0.20R

Pad	Function	Note
1	Output Enable/Disable	When this pad is not connected the oscillator shall operate. When this pad is <0.30 volts, the output will be inhibited (high impedance state.) Recommend connecting this pad to V _{CC} if the oscillator is to be always on.
2	No connect	There is no internal connection to this pad
3	Ground (GND)	
4	Output	The outputs must be terminated, 100 ohms between the outputs is the ideal termination.
5	Output*	
6	Supply Voltage (V _{CC})	Recommend connecting appropriate power supply bypass capacitors as close as possible.



Layout and application information

Recommend connecting Pad 1 and Pad 2 together to permit the design to accept Enable/Disable on both input pads

For Optimum Jitter Performance, Pletronics recommends:

- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply
- do not place near piezoelectric buzzers or mechanical fans.

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