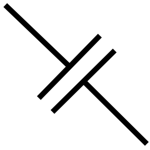
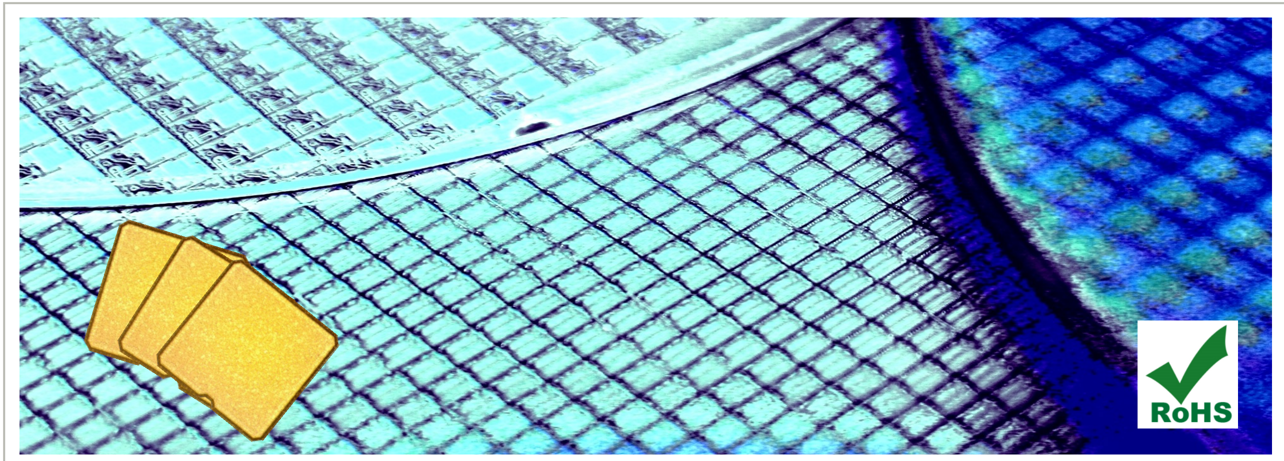


WBSC
Wire Bonding vertical Silicon Capacitor

Rev 4.0



Key Features

- **Wire bondable vertical capacitors**
- **Physical parameters:**
  - Various sizes: from **0101 to 0805** format
  - Substrate: **Silicon** with gold backing
  - Dielectric: Silicon dioxide / Silicon nitride
- **Electrical parameters:**
  - Capacitance range: **few pF to several 10's nF**
  - Low ESR < 10 mΩ and low ESL < 10 pH
  - Excellent **reliability**
  - No memory effect, ultra low dielectric abs. (< 0.05%)
  - Ultra high stability of capacitance value:
  Temp. 0 ± 24 ppm/°C (-55 °C to +150 °C),
  DC voltage < 0.02 %/V, negligible **ageing**
  - Low leakage current down to 100 pA

Key Applications

- **Any demanding applications** such as radar, wireless infrastructure communication, data broadcasting…
- **Standard wire bonding approach** (top & bottom gold metallization)
- **Decoupling / DC noise and harmonic filtering / Matching networks** (ex: GaN power amplifier, LDMOS)
- **High reliability applications**
- **Downsizing. Low profile applications** (250 µm)
- Fully compatible with **single layer ceramic capacitors** and **Metal Oxide Semiconductor**

The WBSC Capacitor targets **RF High Power applications** for wireless communication, radar and data broadcasting systems. The WBSC is suitable for **DC decoupling, matching network, and harmonic / noise filtering functions**.
The unique technology of integrated passive devices in silicon developed by IPDiA, can **solve most of the problems encountered** in demanding applications. These Si capacitors in **ultra–deep trenches** have been developed with a semiconductor process which enables the integration of **high capacitance density** from 1.3nF/mm² to 250nF/mm² (with a breakdown voltage of respectively **450 V** to 11 V).

Our SiCap technology features **high reliability** - up to 10 times better than alternative capacitors technologies - thanks to a full control of the production process with **high temperature curing** (above 900°C) generating a highly pure oxide.
This technology provides **industry-leading performance** particularly in terms of capacitor stability over the full operating DC voltage & temperature range. In addition, intrinsic properties of the silicon show a low dielectric absorption and a low to zero piezo electric effect resulting **in no memory effect.** This Silicon based technology is ROHS compliant.

Electrical Specifications

Unit	10	15	22	33	47	68	82
	Capacitance value						
1pF	10pF: 935.142.522.210 935.142.528.210	15pF: 935.142.528.215	22pF: 935.142.528.222	33pF: 935.142.528.233	47pF: 935.142.528.247	68pF: 935.142.528.268	Contact IPDIA Sales
10pF	100pF: 935.142.522.310 935.142.521.310	150pF: 935.142.522.315 935.142.528.315	220pF: 935.142.528.322	330pF: 935.142.528.333	Contact IPDIA Sales	680pF: 935.142.521.368	820pF: 935.142.521.382
0.1nF	1nF: 935.142.622.410 935.142.521.410 935.142.822.410	Contact IPDIA Sales	Contact IPDIA Sales	Contact IPDIA Sales	Contact IPDIA Sales	Contact IPDIA Sales	Contact IPDIA Sales
1nF	10nF: 935.142.821.510 935.142.620.510	Contact IPDIA Sales	22nF: 935.142.827.522 935.142.624.522	Contact IPDIA Sales	Contact IPDIA Sales	Contact IPDIA Sales	Contact IPDIA Sales
10nF	Contact IPDIA Sales	Contact IPDIA Sales	Contact IPDIA Sales	Contact IPDIA Sales	Contact IPDIA Sales:	Contact IPDIA Sales	Contact IPDIA Sales

Parameters	Value
Capacitance range	10 pF to 22 nF
Capacitance tolerance	±15%*
Operating temperature range	-55 to 150 °C**
Storage temperature	- 70 to 165 °C
Temperature coefficient	0 ± 24 ppm/°C from -55 to +150°C
Breakdown Voltage (BV)	450, 150, 50, 30, 11 V
Capacitance variation versus RVDC	0.02 % /V from 0 V to RVDC
Equivalent Serial Inductor (ESL)	10 pH typ.
Equivalent Serial Resistor (ESR)	10 mΩ typ.
Insulation resistance	100 GΩ @ 16 V from -55 to 150°C
Aging	Negligible, < 0.001% / 1000h
Reliability	FIT<0.017 parts / billions hours, RVDC, from -55 to +150°C
Capacitor height	Max 250 µm ***

* other tolerances on request
** for temperatures up to 200°C or 250°C, see our WTSC and WXSC ranges
*** for low profile @ 100 µm, see our WLSC range

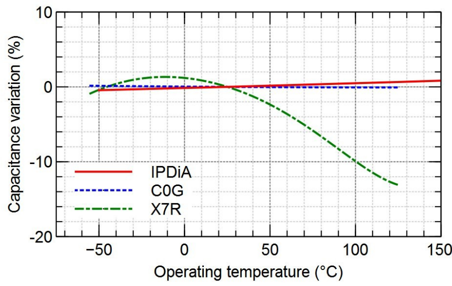


Fig.1: Capacitance variation vs temperature (for WBSC and MLCC technologies)

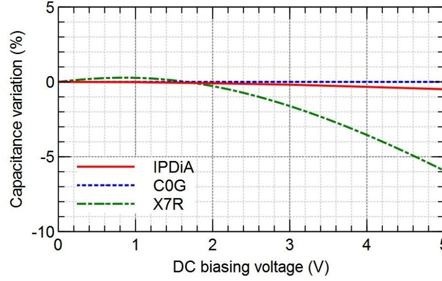
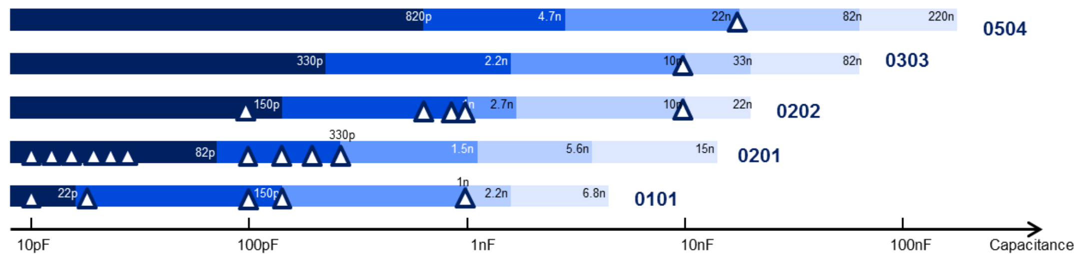


Fig.2: Capacitance variation vs DC biasing voltage (for WBSC and MLCC technologies)

WBSC Capacitance Range



Δ Available parts – see table above
For other values, contact your IPDiA sales representative

BV 450V
BV 50V
BV 11V
BV 150V
BV 30V

Termination and Outline

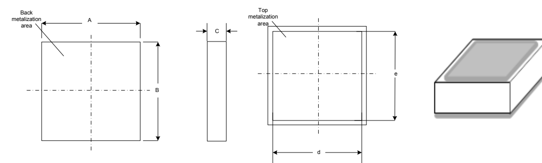
Termination

Top electrode metallization: Ti (0.2µm) / Cu (3.4µm) / Ni (3µm) / Au (1.5µm).
Bottom electrode metallization: Ti (0.1 µm) / Ni (0.3µm) / Au (0.2µm)
Other finishings are available on request.
Ex: Aluminum (3µm Al/Si/Cu: 98.96%/1%/0.04%) or Copper (5µm Cu).
Applicable for standard wire bonding approach (ball and wedge).

Package Outline (typical dimensions, all dimensions in mm)

Typ.		0101*	0201	0202	0302	0303	0402	0404	0504	0805
Comp. size	A	0.25 ±0.01	0.50 ±0.01	0.50 ±0.01	0.80 ±0.01	0.80 ±0.01	1.02 ±0.01	1.01 ±0.05	1.37 ±0.01	2.00 ±0.01
	B	0.25 ±0.01	0.25 ±0.01	0.50 ±0.01	0.50 ±0.01	0.80 ±0.01	0.50 ±0.01	1.02 ±0.01	1.02 ±0.01	1.25 ±0.01

* excepted for 1nF/BV 50 ⇒ 0.294 x 0.294 mm



Packaging

Tape and reel, waffle pack or wafer delivery.

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For more information, please visit: http://www.ipdia.com
To contact us, email to: sales@ipdia.com

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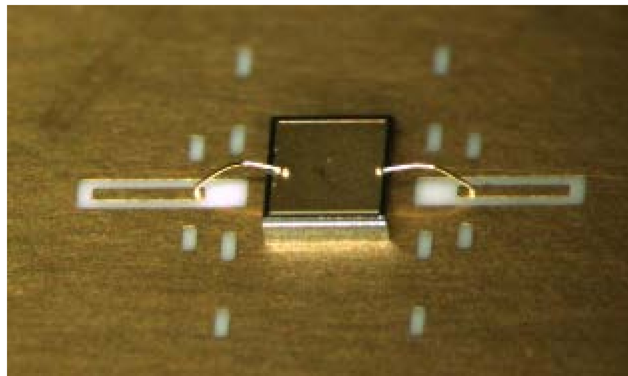
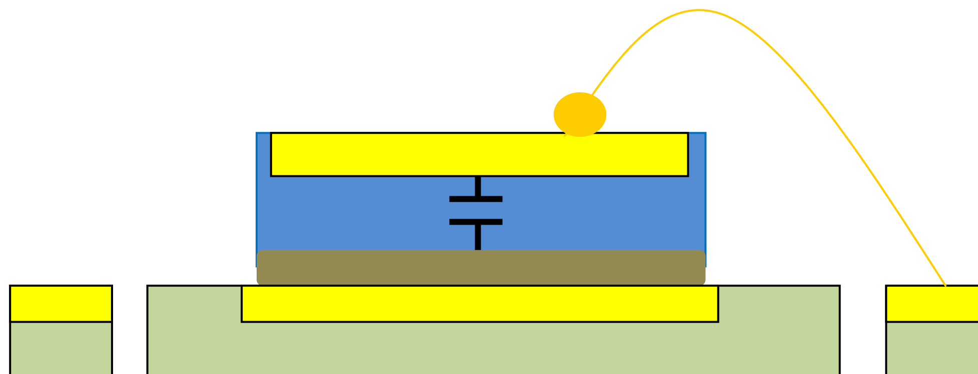


IPDiA Silicon capacitor W type



Introduction

This document describes the attachment techniques recommended by IPDiA for their vertical capacitors on the customer substrates. This document is non-exhaustive. Customers with specific attachment requirements or attachment scenarios that are not covered by this document should contact IPDiA.

Handling Precautions and Storage

Silicon dies must always be handled in a clean room environment (usually class 1000 (ISO 6)) but the assembled devices do not need to be handled in this type of environment since the product is already well packed. The remaining quantities must be repacked immediately after any process step, under the same conditions as before opening (ESD bag + N2).

Store the capacitors in the manufacturer's package under the following conditions, with no rapid temperature change in an indoor room:

- Temperature: -10 to 40 °C
- Humidity: 30 to 70 % RH

Avoid storing the capacitors under the following conditions:

(a) Ambient air containing corrosive gas: (chlorine, hydrogen sulfide, ammonia, sulfuric acid, nitric oxide, etc.)
(b) Ambient air containing volatile or combustible gas
(c) In environments with a high concentration of airborne particles
(d) In liquid (water, oil, chemical solution, organic solvents, etc.)
(e) In direct sunlight
(f) In freezing environments

To avoid contamination and damage such as scratches and cracks, we recommend the following:

- Never handle the die with the bare hands
- Avoid touching the active face
- Do not store or transport die outside protective bags, tubes, boxes, sawing tape
- Work only in ESD environments
- Use plastic tweezers or a soft vacuum tool to remove the silicon die from the packing.

Standard packing is tape & reel for die size larger than 0201 but silicon capacitors can be provided in waffle pack, gelpak or sawing frame. Please contact the IPDiA sales contact for drawing and references (sales@ipdia.com).

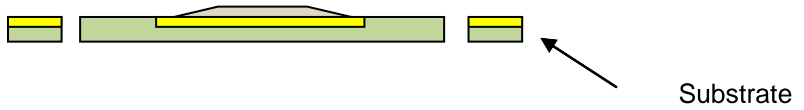
Pad Finishing

The finishing could be:

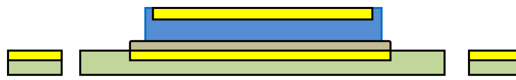
- For top electrode(s):
  - TiCuNiAu electroplating: Ti(0.2 µm)/Cu(3.4 µm)/Ni(3 µm)/Au(1.5 µm), recommended for gold wiring.
  - 3 µm aluminium (Al/Si/Cu: 98.96 %/1 %/0.04 %) (finishing recommended for aluminium wire bonding)
  - Other finishes are available upon request
- Bottom electrode: Ti(0.1 µm)/Ni(0.3 µm)/Au(0.2 µm)

Process Flow with Glue

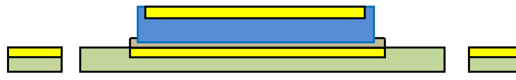
Step A - Glue application:



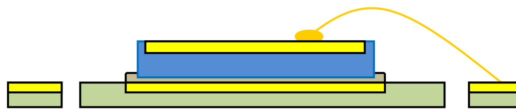
Step B - Pick and place/bonding:



Step C - Curing the glue:

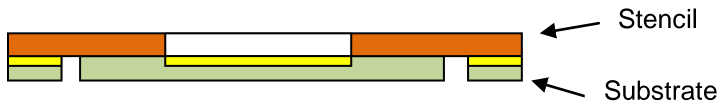


Step D - Wire bonding:

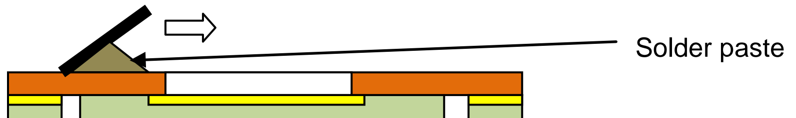


Process Flow with Solder Paste

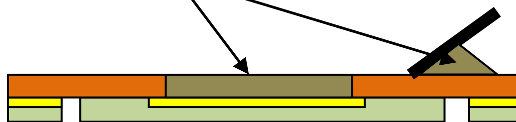
Step A - Stencil:



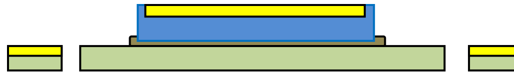
Step B - Solder printing:



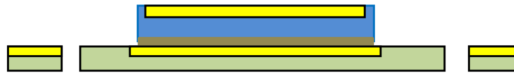
Solder paste



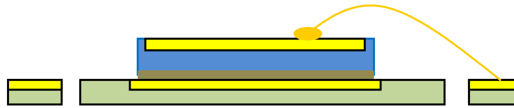
Step C - Die bonding:



Step D - Reflow soldering:



Step E - Wire bonding:



Recommendations concerning the Glue for Die Attachment

An electrical conductive glue must be used. IPDiA often uses the following type of glue:

TYPICAL PROPERTIES OF UNCURED MATERIAL

Thixotropic Index (0.5/5 rpm)	4.0
Viscosity, Brookfield CP51, 25 °C, mPa·s (cP):	
Speed 5 rpm	30,000
Work Life @ 25°C, weeks	2
Shelf Life (from date of manufacture):	
@ 5ºC, months	3
@ -10ºC, months	6
@ -40ºC, year	1

TYPICAL CURING PERFORMANCE

Cure Schedule

1 hour @ 150°C

Alternative Cure Schedule

2 hours @ 125°C

TYPICAL PERFORMANCE OF CURED MATERIAL

Die Shear Strength:

2 X 2 mm Si die, kg-f,

Substrate	@25°C
Ag/Cu leadframe	19

Lap Shear Strength @ 25ºC:

Substrate	MPa	psi
Al to Al	12	1500

Landing Pad Opening

IPDiA recommends that the length and width of the landing pad should be 400 µm greater than those of the die pad.

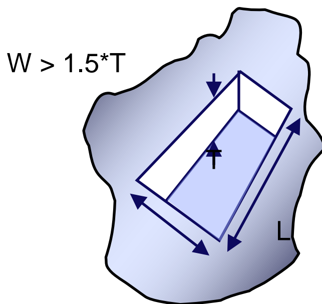
Solder Print Material and Stencil Printing Recommendations

Solder pastes SnPb63/37 and SAC305 are generally used by IPDiA. AuSn 80/20 and SnPb 95/5 can be also used, although they are more expensive. The powder size can be adjusted depending on the die back side size.

ALLOY	COMPOSITION	SOLIDUS	LIQUIDUS	COMMENTS
Sn63	63Sn, 37Pb	183 °C	183 °C	Eutectic
SAC305	96.5Sn, 3Ag, 0.5Cu	217 °C	217 °C	Eutectic
AuSn	80Au20Sn	280 °C	280 °C	Eutectic
SnPb	95Sn5Pb	308 °C	312 °C	Eutectic

Water soluble flux or no-clean flux can be used. If water soluble flux is used, cleaning must be carried out immediately after reflow.

Stencil design rules depending on the quality:



STAINLESS STEEL LASER: [(L*W)/(2*(L+W)*T)] > 0.66 & W > 1.5*T

NICKEL LASER: [(L*W)/(2*(L+W)*T)] > 0.53 & W > 1.2*T

Die Picking

The most common approach is with automatic equipment using vision inspection to correct die placement after picking and before placement. Manual picking can also be carried out. Use of a rubber or Torlon® tip is strongly recommended for the die picking. A metal tip could damage the capacitor. A minimum picking force (about 100 grams) is recommended.

Die Bonding

If automatic equipment is used, it is best to use the same tool as for picking. The placement force will depend on the die size. A minimum placement force is required in order to cover all the die back side with glue. Too much force can damage the die. In case of die bonding with stencil printing application, IPDiA recommends using the minimum of force, around 50-100 g.

Recommended forces with recommended glue:

Silicon Capacitor Type	Capacitor size (µm²)	Capacitor thickness	Placement force (grams)
W0101	250x250	100 µm minimum	100
W0202	500x500		200
W0303	800x800		300
W0402	1000x700		350
W0504	1400x1000		450

Reflow Soldering

IPDiA recommends convection reflow but vapor phase reflow and infrared reflow can be also used. Reflow must be carried out in accordance with the JEDEC standard.

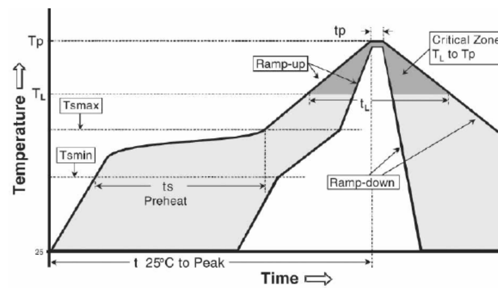
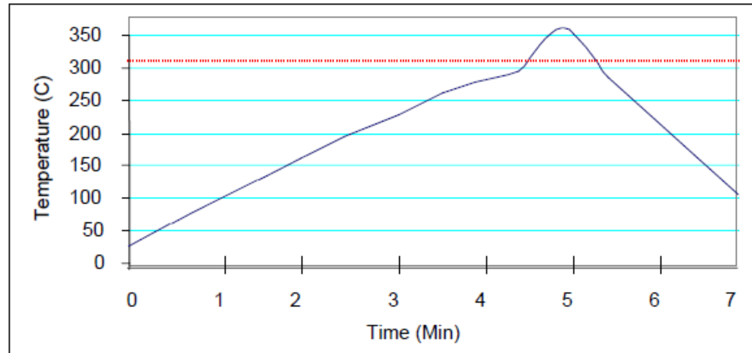


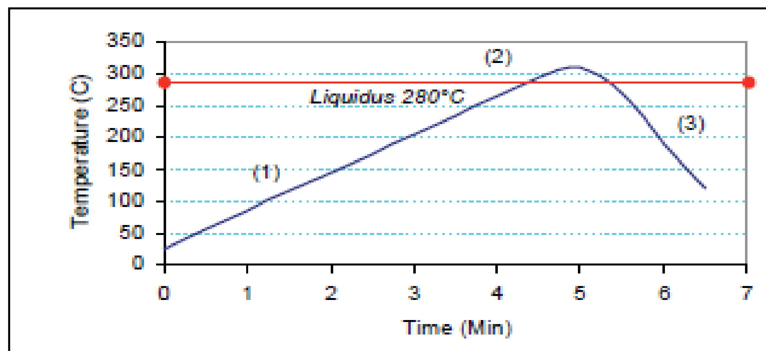
Figure 2: Generic reflow profile according to JEDEC J-STD-020-C

PROFILE FEATURE	SnPb 63/37	SAC305 (Lead-Free Assembly)
Preheat/soak		
Min. temperature (Ts min)	100 °C	150 °C
Max. temperature (Ts max)	150 °C	200 °C
Time (ts) from (Ts min to Ts max)	60 to 120 s	60 to 120 s
Ramp-up		
Ramp-up rate (tL to tp)	maximum 3 °C/s	maximum 3 °C/s
Liquidus temperature (TL)	183 °C	217 °C
Time (tL) maintained above TL	60 to 150 s	60 to 150 s
Peak temperature (Tp)	220 °C	260 °C
Time from 25 °C to peak temperature	maximum 6 minutes	maximum 8 minutes
Ramp-down		
Ramp-down rate (Tp to TL)	maximum 6 °C/s	maximum 6 °C/s

SnPb profile: (IPDiA uses Indalloy Sn95Pb5 from Indium – Indalloy ref. #171)



AuSn profile: (IPDiA uses Indalloy Au80Sn20 from Indium – Indalloy ref. #182)



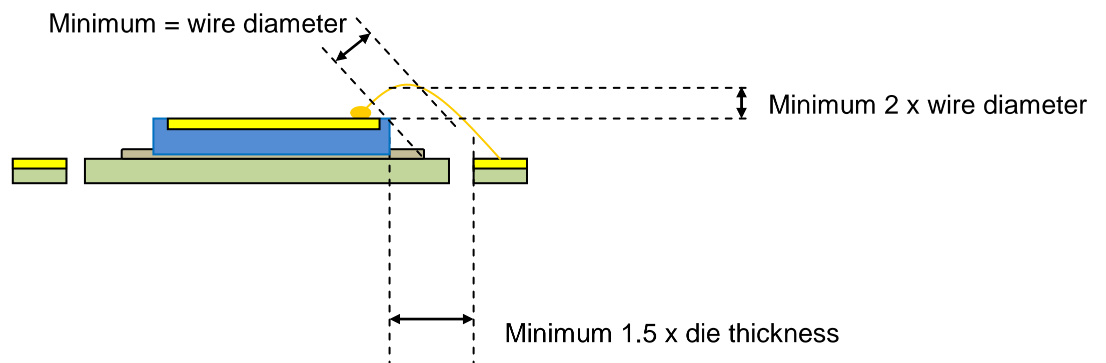
Flux removes tarnish films, maintains surface cleanliness and facilitates solder spreading during the attachment operations. The flux must be compatible with the soldering temperature and soldering times. Please refer to the solder paste supplier for the cleaning and flux removal. Flux residues could be responsible for current leakage or short circuits. For optimum results, clean the circuits immediately after reflow.

Wire Bonding

Materials used and bonding conditions

- Wire lead: diameter 20 to 25 microns, Au/Al wire
- Wire bonding temperature for gold wire bonding: 150 to 200 °C
- Wire bonding methods: Ball bonding or wedge bonding

Wire bonding specifications:

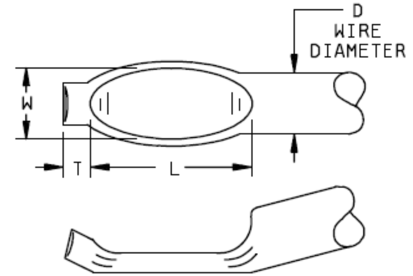


Ball bonding specifications

- The gold ball diameter must be between 2 and 5 times the wire diameter.
- The wire exit must be completely within the periphery of the ball.
- 100 % of the ball must be on the die pad metallization.

Wedge bonding specifications

- The wedge bond on die pad must between 1.2 and 3 times the gold wire diameter in width.
- The wedge bond must be between 1.5 and 6 times the gold wire diameter in length.
- The bond width must be between 1 and 3 times the aluminium wire diameter.
- The tool impression on wedge bond must cover the entire width of the wire.
- 100 % of the wedge (tail not included) must be on the die pad metallization.



Revision

Version	Author	Date	Description
1	Samuel YON	07/11/2014	Creation of the document
1.4	Samuel YON	07/05/2015	Update
1.5	Samuel YON	18/06/2015	Update

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