NVD5890N

Power MOSFET
40 V, 123 A, Single N−Channel DPAK

Features
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- MSL 1/260°C
- AEC Q101 Qualified and PPAP Capable
- 100% Avalanche Tested
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications
- Motor Drivers
- Pump Drivers for Automotive Braking, Steering and Other High Current Systems

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current ($R_{\theta JC}$)	Steady State	T_C = 25°C	I_D	123	A
		T_C = 85°C		95	
Power Dissipation ($R_{\theta JC}$)		T_C = 25°C	P_D	107	W
Continuous Drain Current ($R_{\theta JA}$) (Note 1)		T_A = 25°C	I_D	24	A
		T_A = 85°C		18.5	
Power Dissipation ($R_{\theta JA}$) (Note 1)		T_A = 25°C	P_D	4.0	W
Pulsed Drain Current	t_p=10μs	T_A = 25°C	I_{DM}	400	A
Current Limited by Package		T_A = 25°C	$I_{DmaxPkg}$	100	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	100	A
Drain to Source dV/dt			dV/dt	6.0	V/ns
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 32 V, V_{GS} = 10 V, L = 0.3 mH, $I_{L(pk)}$ = 40 A, R_G = 25 Ω)			E_{AS}	240	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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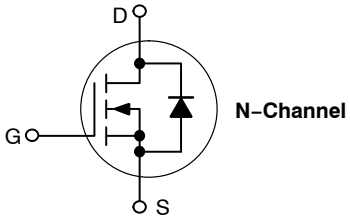
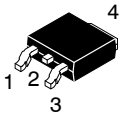
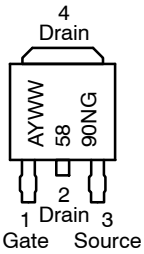
$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
40 V	3.7 mΩ @ 10 V	123 A





CASE 369C
DPAK
(Bent Lead)
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location*
Y = Year
WW = Work Week
5890N = Device Code
G = Pb−Free Package

* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejecter pin), the front side assembly code may be blank.

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	1.4	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	37	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	76	

1. Surface−mounted on FR4 board using 650 mm^2 pad size, 2 oz Cu.
2. Surface−mounted on FR4 board using 36 mm^2 pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				40		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			1.0	μA
			T_J = 150°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		3.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				7.4		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 50 A			2.9	3.7	mΩ
Forward Transconductance	gFS	V_{DS} = 15 V, I_D = 15 A			16.8		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 12 V			4975		pF
Output Capacitance	C_{oss}				785		
Reverse Transfer Capacitance	C_{rss}				490		
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			4760		pF
Output Capacitance	C_{oss}				580		
Reverse Transfer Capacitance	C_{rss}				385		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 50 A			74	100	nC
Threshold Gate Charge	$Q_{G(TH)}$				5.0		
Gate−to−Source Charge	Q_{GS}				17		
Gate−to−Drain Charge	Q_{GD}				16		
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 20 V, I_D = 50 A, R_G = 2.0 Ω			14		ns
Rise Time	t_r				55		
Turn−Off Delay Time	$t_{d(off)}$				35		
Fall Time	t_f				7.0		

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.9	1.2	V
		V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.8	1.0	
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 50 A			35		ns
Charge Time	ta				20		
Discharge Time	tb				15		
Reverse Recovery Charge	Q_{RR}				40		nC

TYPICAL PERFORMANCE CURVES

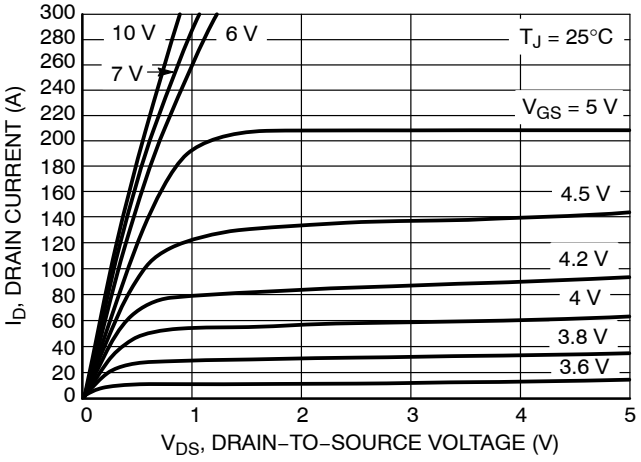


Figure 1. On−Region Characteristics

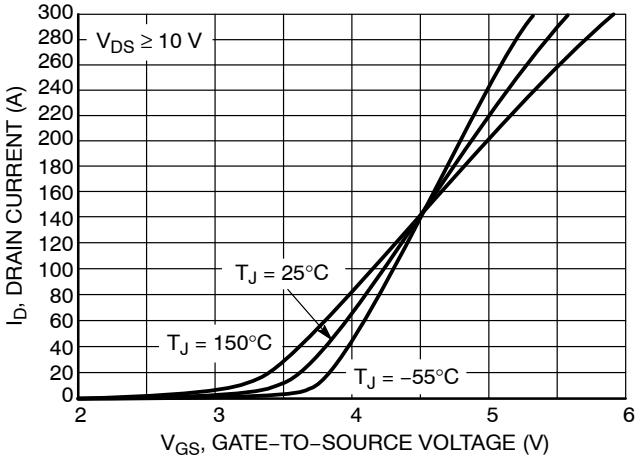


Figure 2. Transfer Characteristics

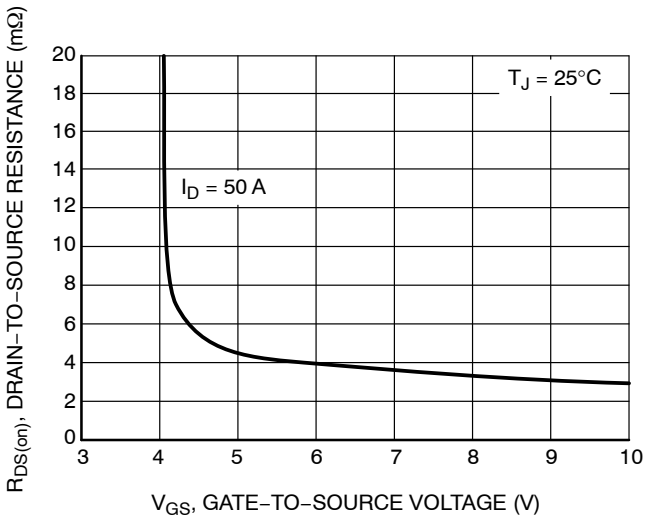


Figure 3. On−Resistance vs. Drain Current

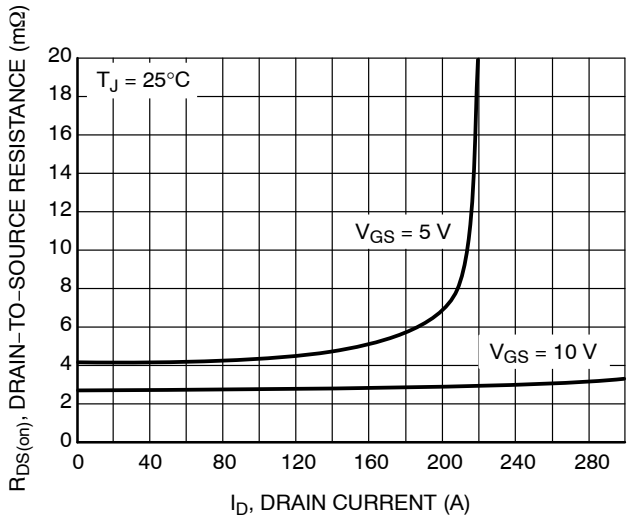


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

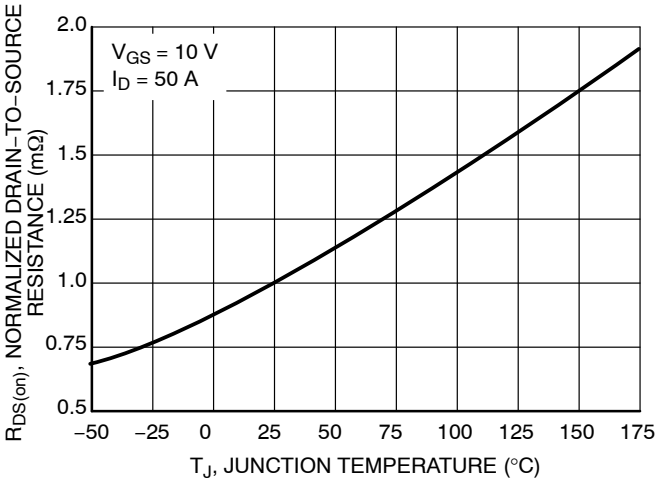


Figure 5. On−Resistance Variation with Temperature

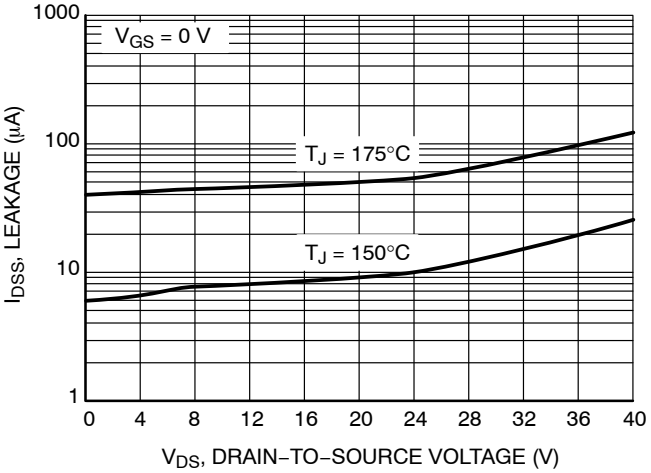


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

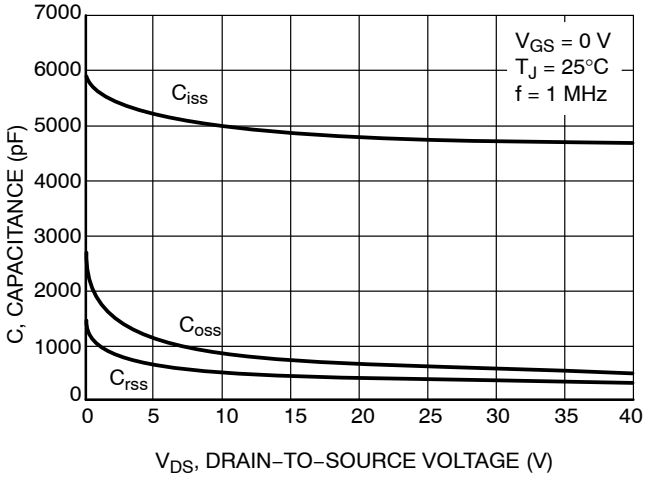


Figure 7. Capacitance Variation

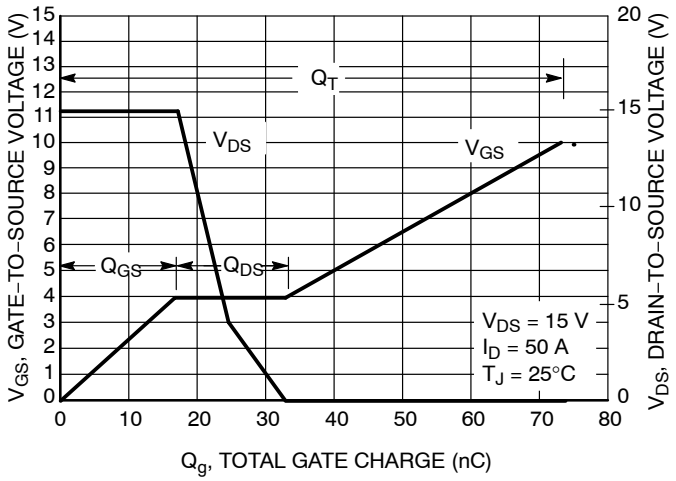


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

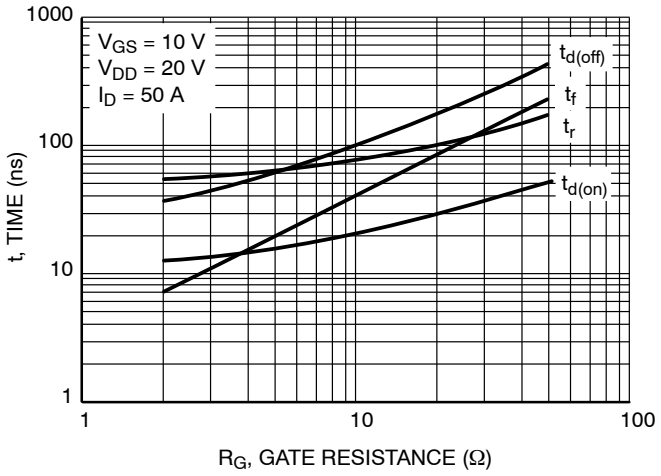


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

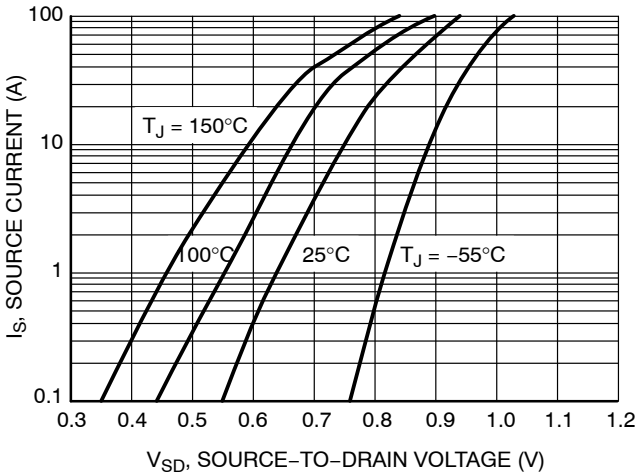


Figure 10. Diode Forward Voltage vs. Current

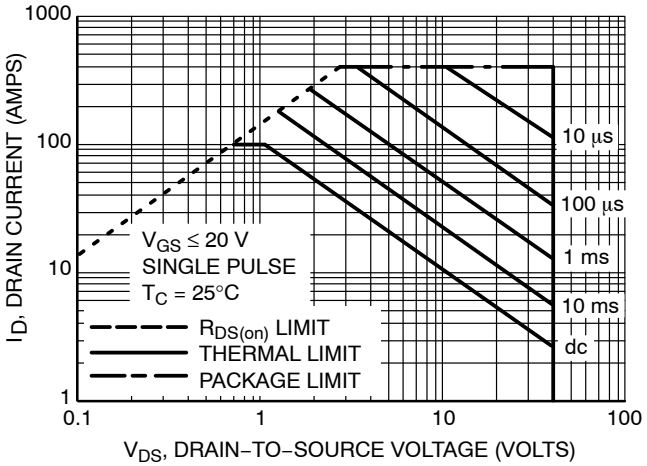


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES

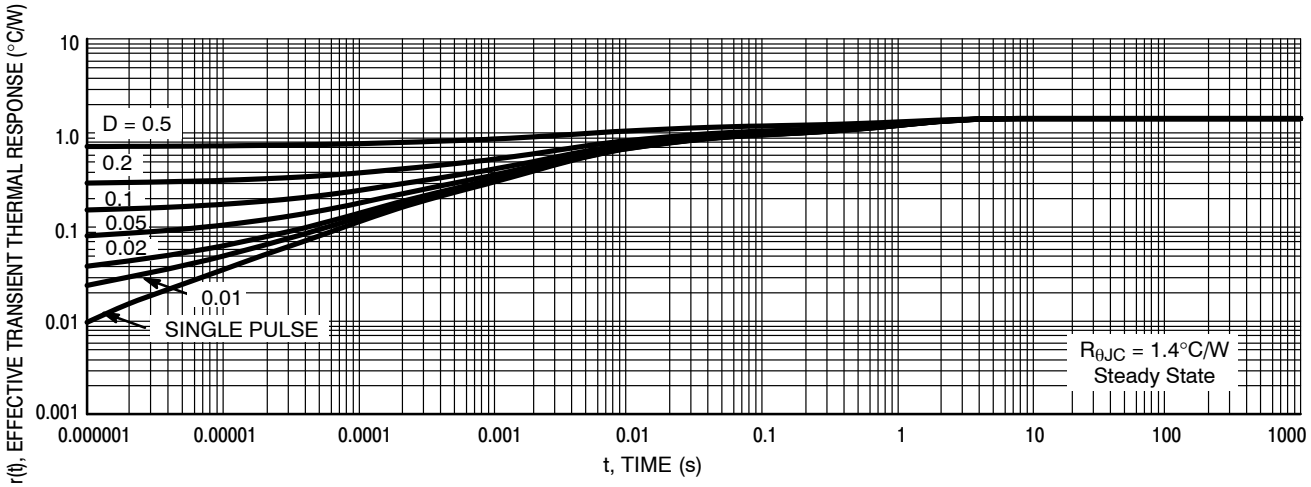


Figure 12. Thermal Response

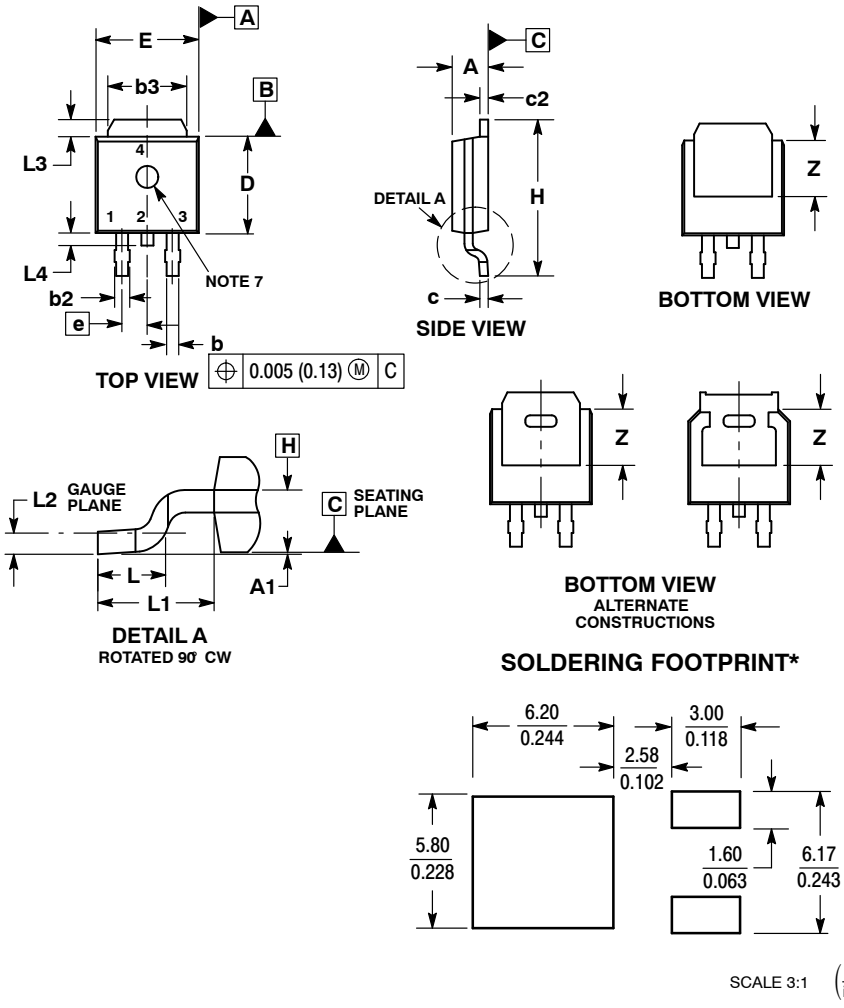
ORDERING INFORMATION

Order Number	Package	Shipping†
NVD5890NT4G	DPAK (Pb−Free)	2500/Tape & Reel
NVD5890NT4G−VF01	DPAK (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*

SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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