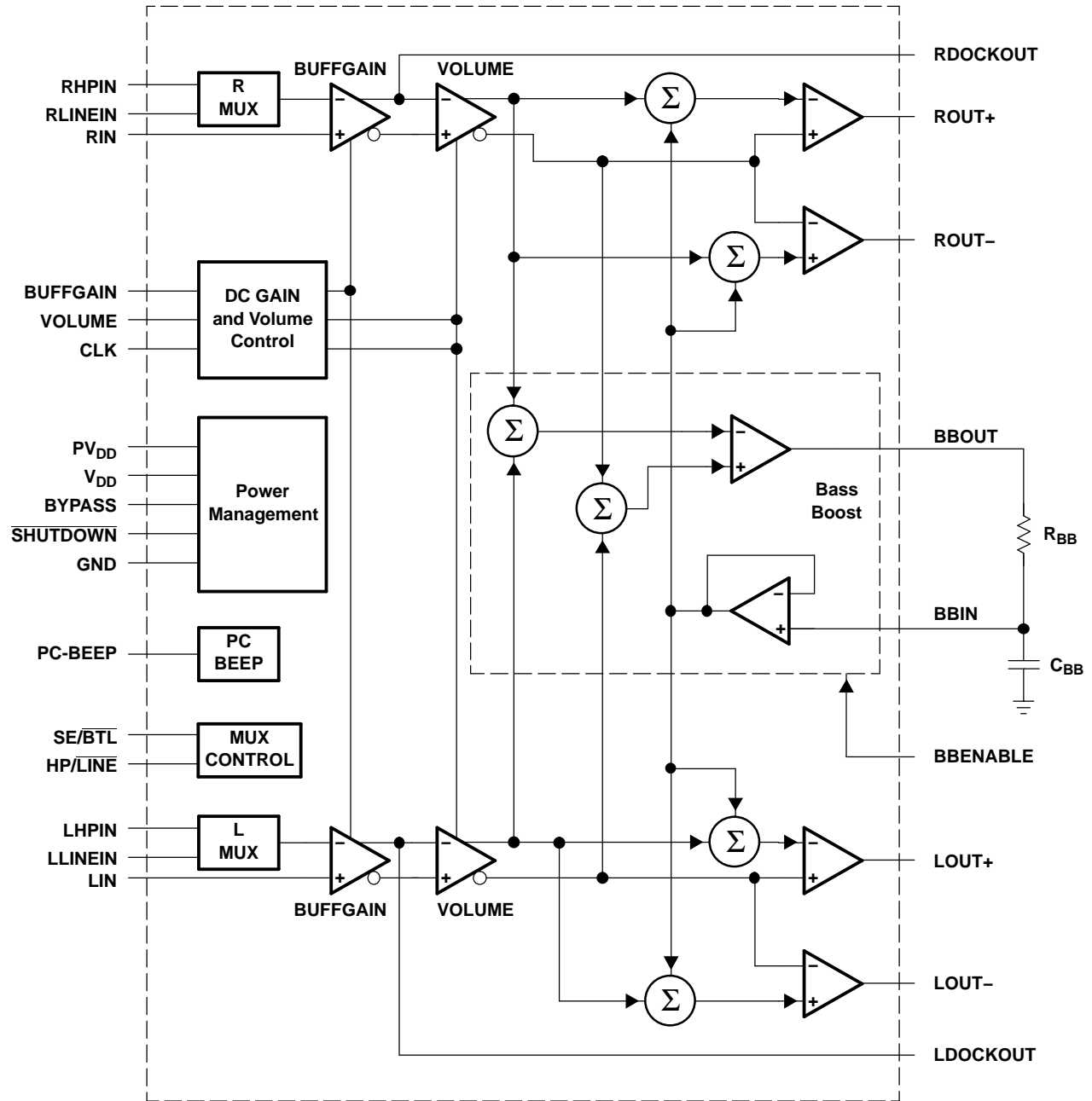


The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA6010A4 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

FUNCTIONAL BLOCK DIAGRAM





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP ⁽¹⁾ (PWP)
-40°C to 85°C	TPA6010A4PWP

- (1) The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA6010A4PWPR).

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BBENABLE	3	I	BBENABLE is the bass boost control input. When this terminal is held high, the extra bass from the bass boost circuitry is added to the output signal. When this terminal is held low, no extra bass is added.
BBIN	21	I	BBIN is the buffered input to the power amplifier from the bass boost circuitry.
BBOUT	20	O	BBOUT is the bass boost output. A low pass filter must be placed from BBOUT to BBIN to select the low frequencies to be boosted.
BYPASS	4		Tap to voltage divider for internal midsupply bias generator
CLK	27	I	If a 47-nF capacitor is attached, the TPA6010A4 generates an internal clock. An external clock can override the internal clock input to this terminal.
BUFFGAIN	24	I	The gain of the dockout buffer is adjustable from -52 dB to 8 dB to LDOCKOUT and RDOCKOUT, and is set by a dc voltage from 0 V to 3.54 V. When the dc level is over 3.54 V, the device is muted.
GND	1, 15		Ground connection for circuitry. Connected to thermal pad.
HP/LINE	13	I	MUX control input, hold high to select LHPIN or RHPIN, hold low to select LLINEIN or RLINEIN.
LHPIN	6	I	Left channel headphone input, selected when HP/LINE is held high
LIN	5	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	7	I	Left channel line negative input, selected when HP/LINE is held low
LDOCKOUT	26	O	LDOCKOUT is the buffered output of LLINEIN or LHPIN. Use BUFFGAIN for volume adjustment of this pin.
LOUT+	28	O	Left channel positive output in BTL mode and positive output in SE mode
LOUT-	2	O	Left channel negative output in BTL mode and high-impedance in SE mode
PC-BEEP	8	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1.5-V (peak-to-peak) square wave is input to PC-BEEP. AC ground if use is not desired.
PV _{DD}	19, 25	I	Power supply for output stage
RHPIN	10	I	Right channel headphone input, selected when HP/LINE is held high
RIN	11	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	9	I	Right channel line input, selected when HP/LINE is held low
RDOCKOUT	18	O	RDOCKOUT is the buffered output of RLINEIN or RHPIN. Use BUFFGAIN for volume adjustment of this pin.
ROUT+	16	O	Right channel positive output in BTL mode and positive output in SE mode
ROUT-	14	O	Right channel negative output in BTL mode and high-impedance in SE mode
SE/BTL	17	I	Output MUX control. When this terminal is high, SE outputs are selected. When this terminal is low, the BTL outputs are selected.
SHUTDOWN	12	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
V _{DD}	22	I	Analog V _{DD} input supply. This terminal needs to be isolated from PV _{DD} to achieve highest performance.
VOLUME	23	I	VOLUME detects the dc level at the terminal and sets the gain for 31 discrete steps covering a range of 20 dB to -40 dB for dc levels of 0.15 V to 3.54. When the dc level is over 3.54 V, the device is muted.
Thermal Pad			Connect to GND. The pad must be soldered down in all applications in order to properly secure the device to the PCB.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	UNIT
V _{DD} Supply voltage	6 V
V _I Input voltage	-0.3 V to V _{DD} +0.3 V
Continuous total power dissipation	Internally Limited (see Dissipation Rating Table)
T _A Operating free-air temperature range	-40°C to 85°C
T _J Operating junction temperature range	-40°C to 150°C
T _{stg} Storage temperature range	-65°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C	DERATING FACTOR	T _A = 70°C	T _A = 85°C
PWP	2.7 W ⁽¹⁾	21.8 mW/°C	1.7 W	1.4 W

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report (SLMA002)*, for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
V _{DD} Supply voltage	4.5	5.5	V
V _{IH} High-level input voltage	SE/BTL, HP/LINE	0.8 × V _{DD}	V
	SHUTDOWN, BBENABLE	2	
V _{IL} Low-level input voltage	SE/BTL, HP/LINE	0.6 × V _{DD}	V
	SHUTDOWN, BBENABLE	0.8	
T _A Operating free-air temperature	-40	85	°C

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS} Output offset voltage (measured differentially)	A _V = 6 dB			35	mV
PSRR Power supply rejection ratio	V _{DD} = 4.9 V to 5.1 V		67		dB
I _{IH} High-level input current	SHUTDOWN, SE/BTL, HP/LINE, VOLUME, BUFFGAIN, BBENABLE V _{DD} = 5.5 V, V _I = V _{DD}			1	μA
I _{IL} Low-level input current	SHUTDOWN, SE/BTL, HP/LINE, VOLUME, BUFFGAIN, BBENABLE V _{DD} = 5.5 V, V _I = 0 V			1	μA
I _{DD} Supply current	BTL mode, SHUTDOWN = 2 V, SE/BTL = 0.6 × V _{DD}		12	18	mA
	SE mode, SHUTDOWN = 2 V, SE/BTL = 0.8 × V _{DD}		6.5	10	
I _{DD(SD)} Supply current, shutdown mode	PC-BEEP = 2.5 V, SHUTDOWN = 0 V		95	250	μA
	PC-BEEP = 0 V, SHUTDOWN = 0 V		62	200	

OPERATING CHARACTERISTICS
 $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 4\ \Omega$, Gain = 6 dB, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	$R_L = 3\ \Omega$, $f = 1\ \text{kHz}$	THD = 10%		2.7		W
			THD = 1%		2.2		
THD + N	Total harmonic distortion plus noise	$P_O = 1\ \text{W}$,	$f = 20\ \text{Hz to } 15\ \text{kHz}$		0.45%		
B_{OM}	Bandwidth, maximum output power	THD = 1%			>15		kHz
k_{SVR}	Supply ripple rejection ratio	$f = 20\ \text{Hz to } 20\ \text{kHz}$, $C_{Bypass} = 1\ \mu\text{F}$, $V_{ripple} = 200\ \text{mV}_{pp}$	BTL mode		56		dB
V_n	Output noise voltage	$C_{Bypass} = 1\ \mu\text{F}$, $f = 20\ \text{Hz to } 20\ \text{kHz}$	BTL mode		50		μV_{RMS}
			SE mode		32		
xtalk	Crosstalk	$f = 20\ \text{Hz to } 20\ \text{kHz}$	BTL mode		-80		dB

OPERATING CHARACTERISTICS
 $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 8\ \Omega$, Gain = 6 dB, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.06%,	$f = 1\ \text{kHz}$		1		W
THD + N	Total harmonic distortion plus noise	$P_O = 0.5\ \text{W}$,	$f = 20\ \text{Hz to } 15\ \text{kHz}$		0.5%		
B_{OM}	Bandwidth, maximum output power	THD = 1%			>15		kHz
k_{SVR}	Supply ripple rejection ratio	$f = 20\ \text{Hz to } 20\ \text{kHz}$, $C_{Bypass} = 1\ \mu\text{F}$, $V_{ripple} = 200\ \text{mV}_{pp}$	BTL mode		56		dB
V_n	Output noise voltage	$C_B = 1\ \mu\text{F}$, $f = 20\ \text{Hz to } 20\ \text{kHz}$	BTL mode		50		μV_{RMS}
			SE mode		32		
xtalk	Crosstalk	$f = 20\ \text{Hz to } 20\ \text{kHz}$	BTL mode		-80		dB

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
THD + N	Total harmonic distortion + noise	vs Output power
		vs Dockout voltage
		vs Frequency

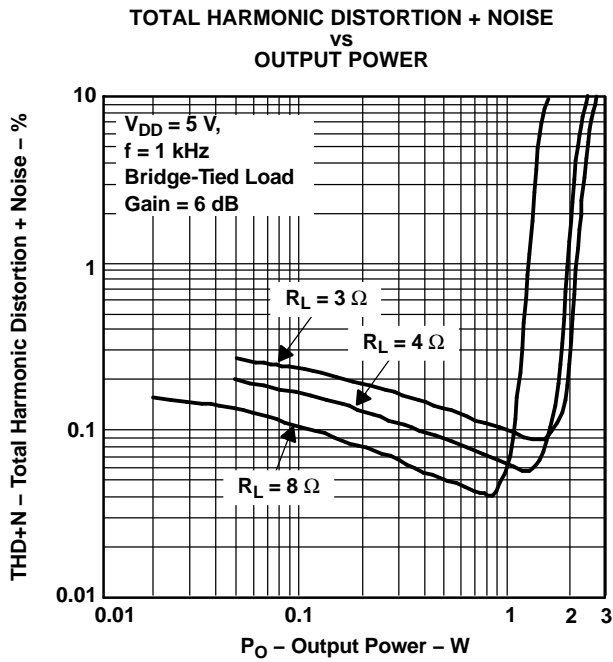


Figure 1.

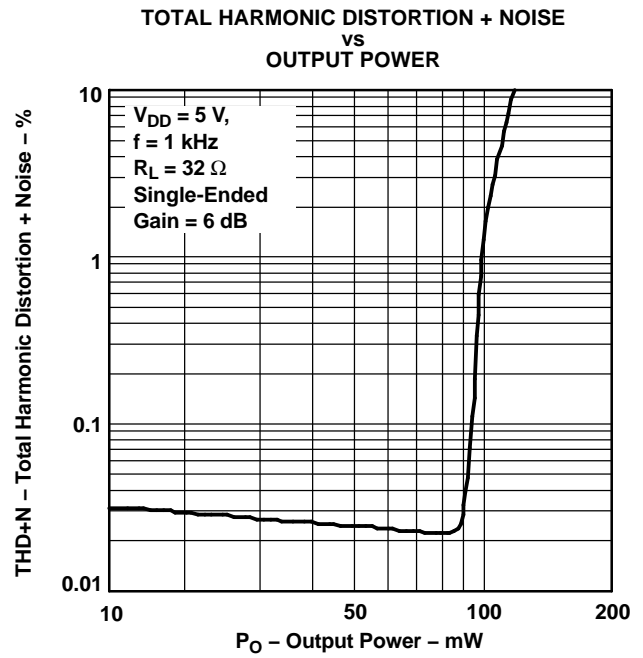


Figure 2.

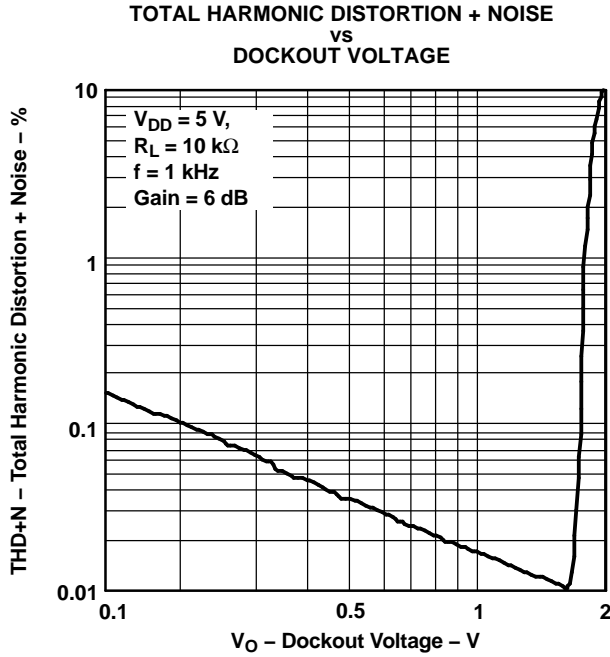


Figure 3.

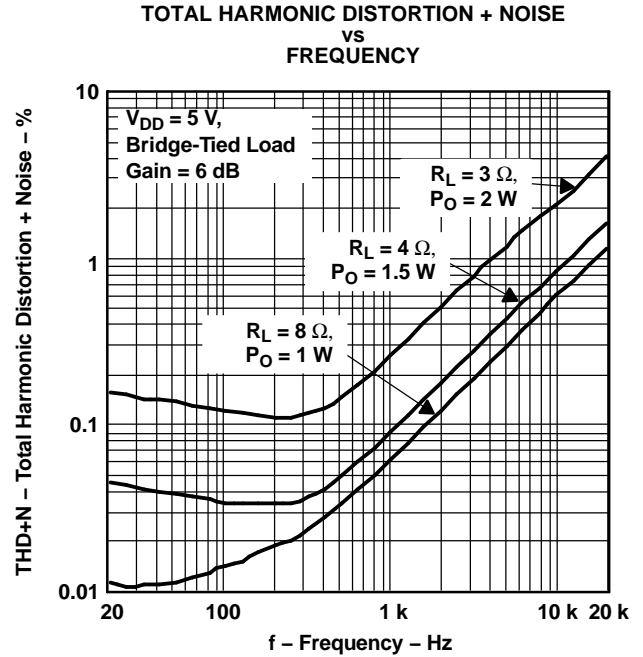


Figure 4.

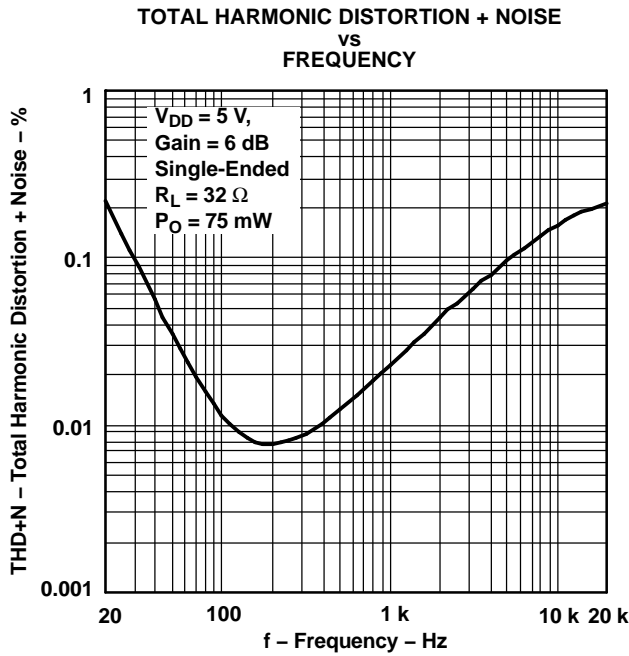


Figure 5.

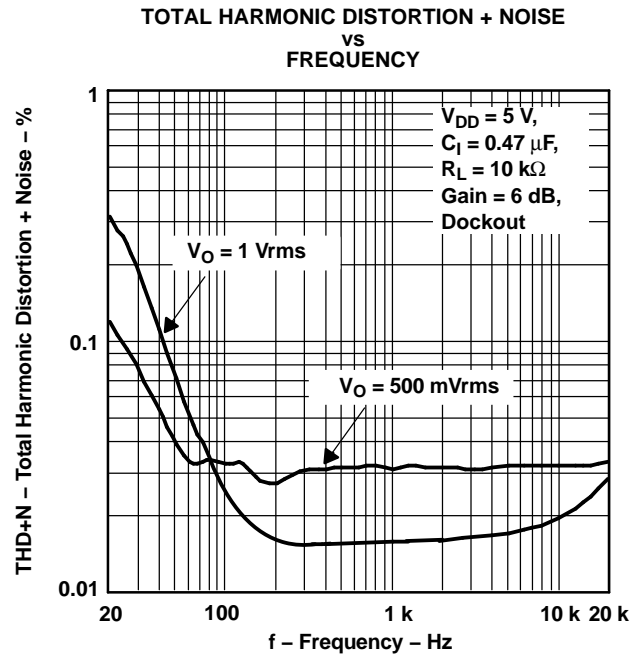


Figure 6.

APPLICATION INFORMATION

INTERNAL BUFFER GAIN AND VOLUME GAIN

The typical voltage and gain levels are shown in Table 1 and Table 2.

Table 1. BUFFGAIN Voltage and Gain Values

BUFFGAIN (Terminal 24)		TYPICAL GAIN OF AMPLIFIER (VOLUME Stage) ⁽¹⁾	
Inceasing Voltage (V) ⁽²⁾⁽³⁾	Decreasing Voltage (V) ⁽²⁾⁽³⁾	Internal Gain (dB)	DOCKOUT Gain (dB)
0.00 – 0.20	0.16 – 0.00	14	8
0.21 – 0.31	0.27 – 0.17	12	6
0.32 – 0.42	0.38 – 0.28	10	4
0.43 – 0.54	0.50 – 0.39	8	2
0.55 – 0.65	0.61 – 0.51	6	0
0.66 – 0.76	0.72 – 0.62	4	-2
0.77 – 0.88	0.84 – 0.73	2	-4
0.89 – 0.99	0.96 – 0.85	0	-6
1.00 – 1.11	1.07 – 0.97	-2	-8
1.12 – 1.22	1.19 – 1.08	-4	-10
1.23 – 1.34	1.30 – 1.20	-6	-12
1.35 – 1.45	1.42 – 1.31	-8	-14
1.46 – 1.56	1.53 – 1.43	-10	-16
1.57 – 1.68	1.64 – 1.54	-12	-18
1.69 – 1.79	1.76 – 1.65	-14	-20
1.80 – 1.91	1.88 – 1.77	-16	-22
1.92 – 2.02	1.99 – 1.89	-18	-24
2.03 – 2.14	2.11 – 2.00	-20	-26
2.15 – 2.25	2.23 – 2.12	-22	-28
2.26 – 2.37	2.34 – 2.24	-24	-30
2.38 – 2.48	2.47 – 2.35	-26	-32
2.49 – 2.60	2.57 – 2.46	-28	-34
2.61 – 2.71	2.69 – 2.58	-30	-36
2.72 – 2.83	2.81 – 2.70	-32	-38
2.84 – 2.95	2.92 – 2.82	-34	-40
2.96 – 3.06	3.04 – 2.93	-36	-42
3.07 – 3.18	3.15 – 3.05	-38	-44
3.19 – 3.29	3.27 – 3.16	-40	-46
3.30 – 3.41	3.39 – 3.28	-42	-48
3.42 – 3.52	3.50 – 3.40	-44	-50
3.53 – 3.63	3.62 – 3.51	-46	-52
3.64 – 5.00	5.00 – 3.63	-75	-81

(1) Typical gain values can vary by ± 2 dB.

(2) To set the Internal and DOCKOUT gain to a fixed value upon power up, use the appropriate voltage range in the Decreasing Voltage column.

(3) For best results, set the voltage to the middle of the appropriate voltage range.

Table 2. VOLUME Voltage and Gain Values

VOLUME (Terminal 23)		TYPICAL GAIN OF AMPLIFIER (VOLUME Stage) ⁽¹⁾	
Inceasing Voltage (V) ⁽²⁾⁽³⁾	Decreasing Voltage (V) ⁽²⁾⁽³⁾	BTL Gain (dB)	SE Gain (dB)
0.00 – 0.20	0.16 – 0.00	20	14
0.21 – 0.31	0.27 – 0.17	18	12
0.32 – 0.42	0.38 – 0.28	16	10
0.43 – 0.54	0.50 – 0.39	14	8
0.55 – 0.65	0.61 – 0.51	12	6
0.66 – 0.76	0.72 – 0.62	10	4
0.77 – 0.88	0.84 – 0.73	8	2
0.89 – 0.99	0.96 – 0.85	6	0
1.00 – 1.11	1.07 – 0.97	4	-2
1.12 – 1.22	1.19 – 1.08	2	-4
1.23 – 1.34	1.30 – 1.20	0	-6
1.35 – 1.45	1.42 – 1.31	-2	-8
1.46 – 1.56	1.53 – 1.43	-4	-10
1.57 – 1.68	1.64 – 1.54	-6	-12
1.69 – 1.79	1.76 – 1.65	-8	-14
1.80 – 1.91	1.88 – 1.77	-10	-16
1.92 – 2.02	1.99 – 1.89	-12	-18
2.03 – 2.14	2.11 – 2.00	-14	-20
2.15 – 2.25	2.23 – 2.12	-16	-22
2.26 – 2.37	2.34 – 2.24	-18	-24
2.38 – 2.48	2.47 – 2.35	-20	-26
2.49 – 2.60	2.57 – 2.46	-22	-28
2.61 – 2.71	2.69 – 2.58	-24	-30
2.72 – 2.83	2.81 – 2.70	-26	-32
2.84 – 2.95	2.92 – 2.82	-28	-34
2.96 – 3.06	3.04 – 2.93	-30	-36
3.07 – 3.18	3.15 – 3.05	-32	-38
3.19 – 3.29	3.27 – 3.16	-34	-40
3.30 – 3.41	3.39 – 3.28	-36	-42
3.42 – 3.52	3.50 – 3.40	-38	-44
3.53 – 3.63	3.62 – 3.51	-40	-46
3.64 – 5.00	5.00 – 3.63	-95	-95

(1) Typical gain values can vary by ± 2 dB.

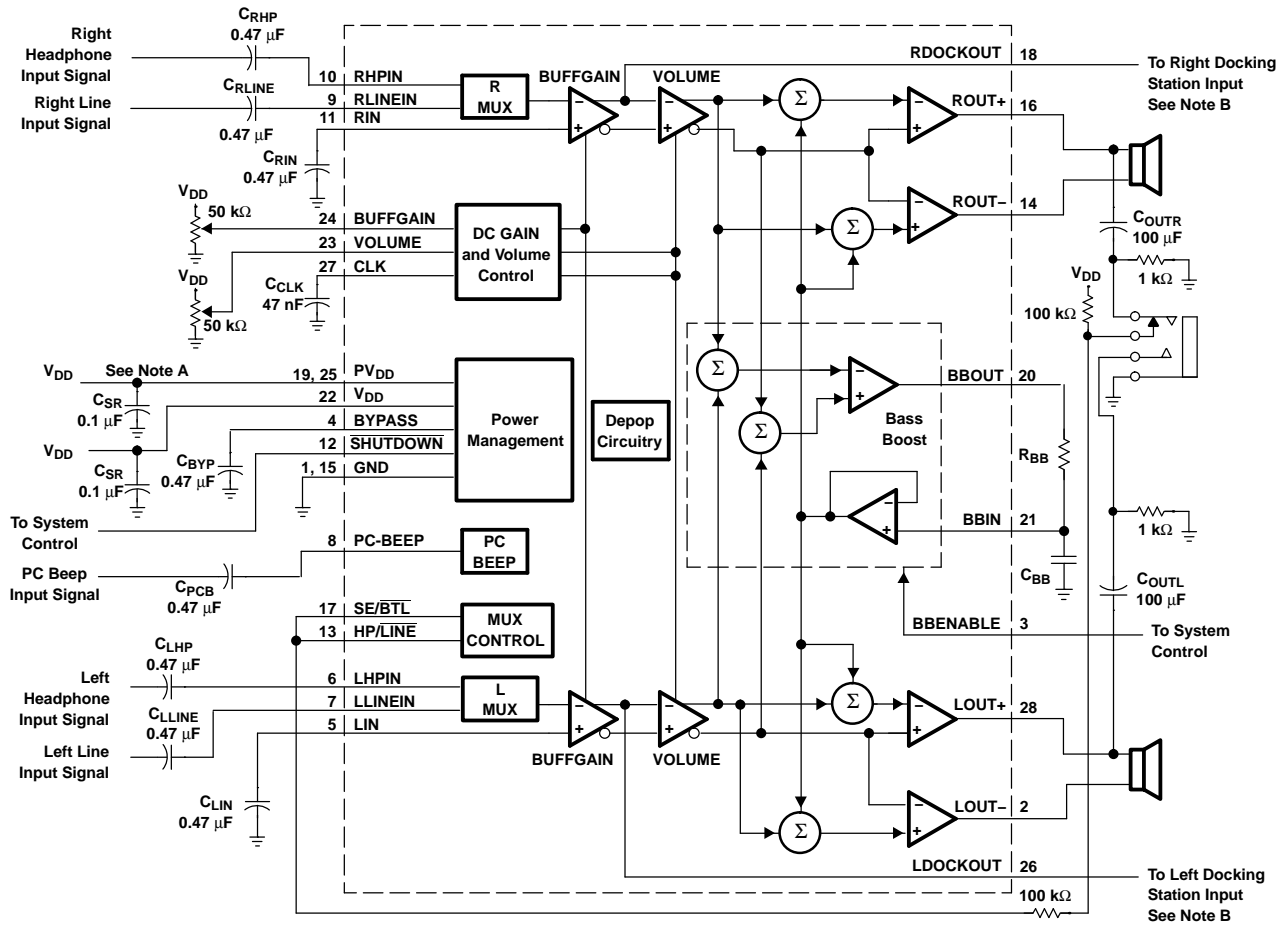
(2) To set the Internal and DOCKOUT gain to a fixed value upon power up, use the appropriate voltage range in the Decreasing Voltage column.

(3) For best results, set the voltage to the middle of the appropriate voltage range.

The total gain of the amplifier can be determined using the following equations:

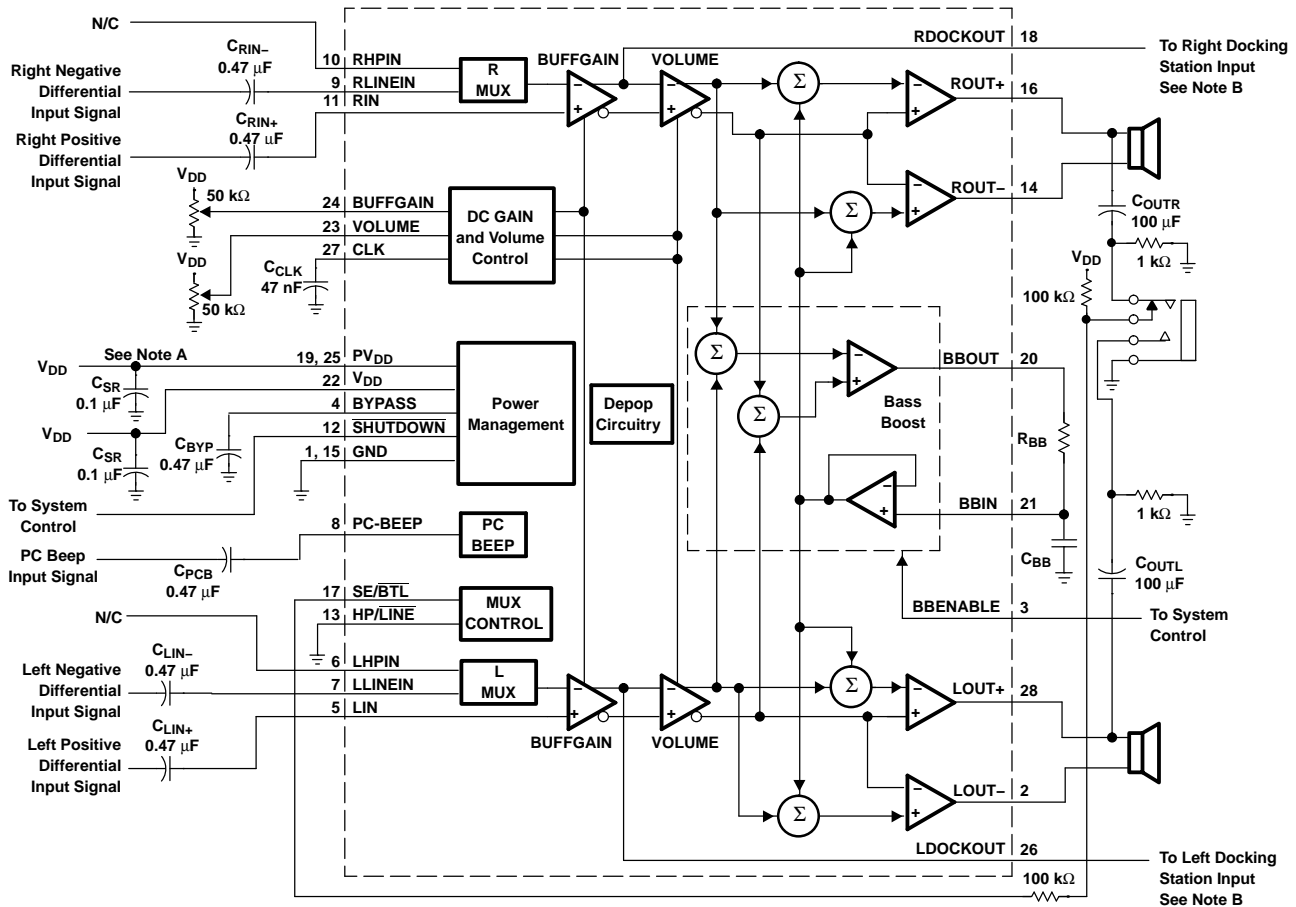
Total gain = Internal gain (dB) + BTL gain (dB), if outputs are bridge-tied.

Total gain = Internal gain (dB) + SE gain (dB), if outputs are single-ended.



- A. A 0.1-μF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 μF or greater should be placed near the audio power amplifier.
- B. A DC-blocking capacitor should be placed at each input to the amplifier in the docking station, as the RDOCKOUT and LDOCKOUT pins are biased to $V_{DD}/2$.

Figure 7. Typical TPA6010A4 Application Circuit Using Single-Ended Inputs and Input MUX



- A. A 0.1- μF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 μF or greater should be placed near the audio power amplifier.
- B. A DC-blocking capacitor should be placed at each input to the amplifier in the docking station, as the RDOCKOUT and LDOCKOUT pins are biased to $V_{\text{DD}}/2$.

Figure 8. Typical TPA6010A4 Application Circuit Using Differential Inputs

INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the -3 dB or cut-off frequency also changes by over 6 times.

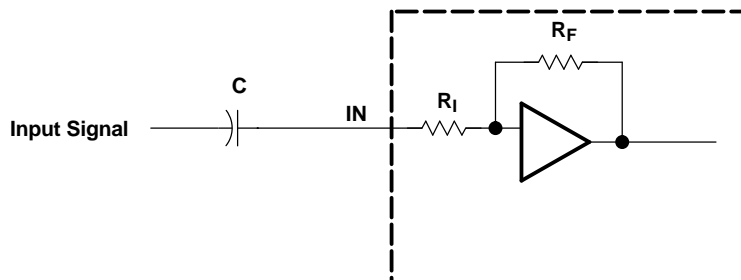
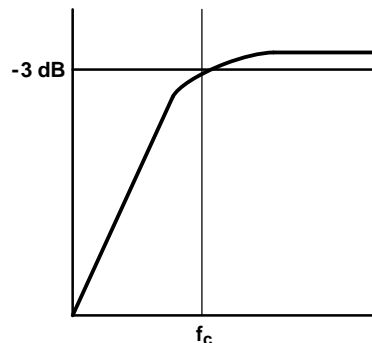


Figure 9. Resistor-On Input for Cut-Off Frequency

INPUT CAPACITOR, C_I

In the typical application an input capacitor, C_I , is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input resistance of the amplifier, R_I , form a high-pass filter with the corner frequency determined in Equation 1.

$$f_c = \frac{1}{2\pi R_I C_I}$$



(1)

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 70 k Ω and the specification calls for a flat bass response down to 40 Hz. Equation 1 is reconfigured as Equation 2.

$$C_I = \frac{1}{2\pi R_I f_c}$$

(2)

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 μ F. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

POWER SUPPLY DECOUPLING, C_S

The TPA6010A4 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μ F placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μ F or greater placed near the audio power amplifier is recommended.

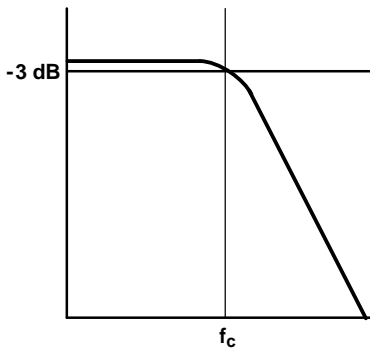
MIDRAIL BYPASS CAPACITOR, C_{BYP}

The midrail bypass capacitor, C_{BYP} , is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

For the bypass capacitor, C_{BYP} , 0.47 μ F to 1 μ F ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

BASS BOOST OPERATION

The bass boost feature of the TPA6010A4 sums the left and right inputs, adds gain, filters out the high frequencies, and adds the bass-boosted signal back into the current-gain stage of the amplifier. The cutoff frequency is set by R_{BB} and C_{BB} as shown in Equation 3.



$$f_c = \frac{1}{2\pi R_{BB} C_{BB}}$$

(3)

The gain of the bass boost is set internally at 12 dB if bass is present in both the right and left channels. If bass is only present in one of the channels, the boost is reduced to 9.5 dB.

The total bass boost gain may be determined by using Equation 4.

$$\text{Bass Boost Gain} = 12 \text{ dB} + 20\text{Log} \left(\frac{R_2}{R_1 + R_2} \right) \quad (\text{bass present on both channels})$$

$$\text{Bass Boost Gain} = 9.5 \text{ dB} + 20\text{Log} \left(\frac{R_2}{R_1 + R_2} \right) \quad (\text{bass present on only one channel}) \quad (4)$$

Consider the following example application. The desired cutoff frequency for the bass boost is 300 Hz and the desired bass boost gain is 6 dB. The filter components could be $R_{BB} = 1.1 \text{ k}\Omega$ and $C_{BB} = 0.47 \text{ }\mu\text{F}$.

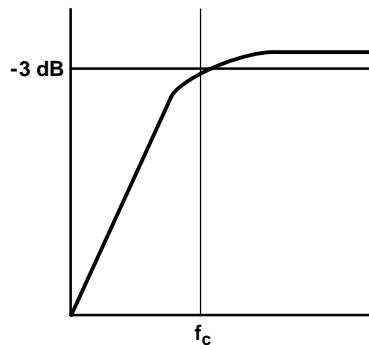
If the bass boost feature is not to be used or if the user wishes to disable the boost, the BBENABLE pin should be pulled low.

Finally, as illustrated in the functional block diagram, the bass boost is only applied to the speaker outputs, not to the docking station outputs.

OUTPUT COUPLING CAPACITOR, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 5.

$$f_c = \frac{1}{2\pi R_L C_C}$$



(5)

The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 μF is chosen and loads vary from 3 Ω , 4 Ω , 8 Ω , 32 Ω , 10 k Ω , and 47 k Ω . Table 3 summarizes the frequency response characteristics of each configuration.

Table 3. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R _L	C _C	LOWEST FREQUENCY
3 Ω	330 μF	161 Hz
4 Ω	330 μF	120 Hz
8 Ω	330 μF	60 Hz
32 Ω	330 μF	15 Hz
10,000 Ω	330 μF	0.05 Hz
47,000 Ω	330 μF	0.01 Hz

As Table 3 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

BRIDGED-TIED LOAD VERSUS SINGLE-ENDED MODE

Figure 10 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA6010A4 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4x the output power from the same supply rail and load impedance as in Equation 6.

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$Power = \frac{V_{(rms)}^2}{R_L}$$

(6)

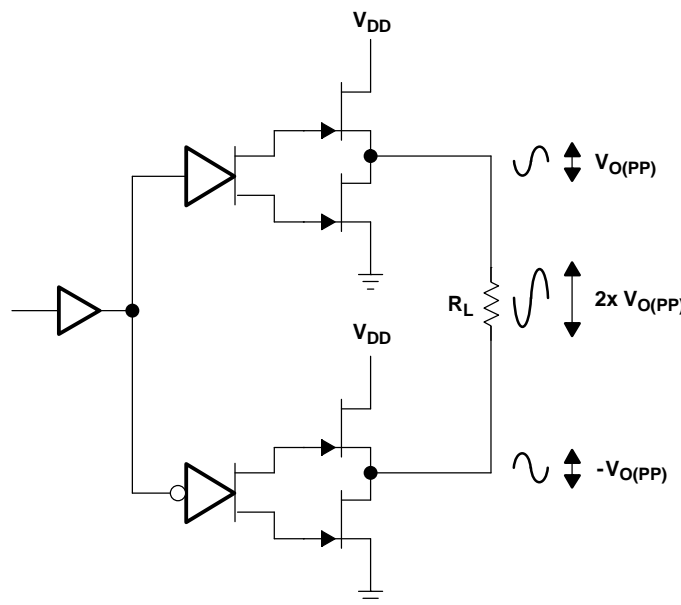


Figure 10. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 11. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with Equation 7.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (7)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

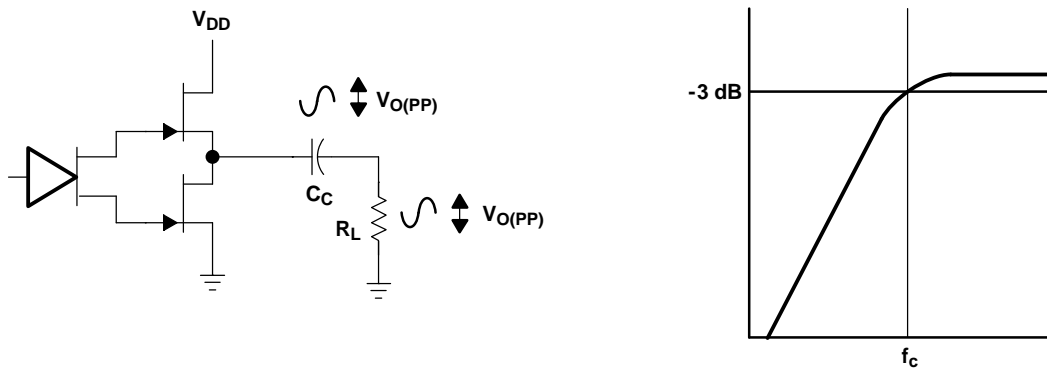


Figure 11. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *CREST FACTOR and THERMAL CONSIDERATIONS* section.

SINGLE-ENDED OPERATION

In SE mode (see Figure 10 and Figure 11), the load is driven from the primary amplifier output for each channel (OUT+, terminals 28 and 16).

The amplifier switches single-ended operation when the SE/BTL terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1 V/V.

BTL AMPLIFIER EFFICIENCY

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_DD. The internal voltage drop multiplied by the RMS value of the supply current, I_DD,rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 12).

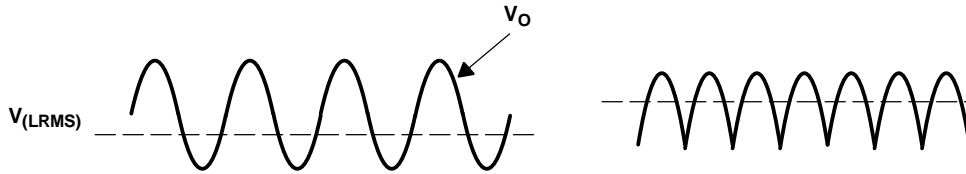


Figure 12. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. Equation 8 and Equation 9 are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{8}$$

Where:

$$P_L = \frac{V_{Lrms}^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD} I_{DDavg} \quad \text{and} \quad I_{DDavg} = \frac{1}{\pi} \int_0^{\pi} \frac{V_P}{R_L} \sin(t) dt = -\frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2 V_{DD} V_P}{\pi R_L}$$

Substituting P_L and P_{SUP} into equation 8,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P^2}{2R_L}}{\frac{2 V_{DD} V_P}{\pi R_L}} = \frac{\pi V_P}{4 V_{DD}}$$

Where:

$$V_P = \sqrt{2 P_L R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2 P_L R_L}}{4 V_{DD}}$$

- P_L = Power delivered to load
- P_{SUP} = Power drawn from power supply
- V_{LRMS} = RMS voltage on BTL load
- R_L = Load resistance
- V_P = Peak voltage on BTL load
- I_{DDavg} = Average current drawn from the power supply
- V_{DD} = Power supply voltage
- η_{BTL} = Efficiency of a BTL amplifier

(9)

Table 4 employs equation 9 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased, resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 4. Efficiency vs Output Power in 5-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47 ⁽¹⁾	0.53

(1) High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to the utmost advantage when possible. Note that in Equation 9, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

CREST FACTOR AND THERMAL CONSIDERATIONS

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the TPA6010A4 data sheet, one can see that when the TPA6010A4 is operating from a 5-V supply into a 3-Ω speaker that 4-W peaks are available. Converting watts to dB as in Equation 10:

$$P_{dB} = 10 \text{Log} \frac{P_W}{P_{ref}} = 10 \text{Log} \frac{4 \text{ W}}{1 \text{ W}} = 6 \text{ dB} \quad (10)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

$$6 \text{ dB} - 15 \text{ dB} = -9 \text{ dB} \text{ (15 dB crest factor)}$$

$$6 \text{ dB} - 12 \text{ dB} = -6 \text{ dB} \text{ (12 dB crest factor)}$$

$$6 \text{ dB} - 9 \text{ dB} = -3 \text{ dB} \text{ (9 dB crest factor)}$$

$$6 \text{ dB} - 6 \text{ dB} = 0 \text{ dB} \text{ (6 dB crest factor)}$$

$$6 \text{ dB} - 3 \text{ dB} = 3 \text{ dB} \text{ (3 dB crest factor)}$$

Converting dB back into watts as in Equation 11:

$$\begin{aligned} P_W &= 10^{P_{dB}/10} \times P_{ref} \\ &= 63 \text{ mW (18 dB crest factor)} \\ &= 125 \text{ mW (15 dB crest factor)} \\ &= 250 \text{ mW (9 dB crest factor)} \\ &= 500 \text{ mW (6 dB crest factor)} \\ &= 1000 \text{ mW (3 dB crest factor)} \\ &= 2000 \text{ mW (15 dB crest factor)} \end{aligned} \quad (11)$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA6010A4 and maximum ambient temperatures are shown in Table 5.

Table 5. TPA6010A4 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2000 mW (3 dB)	1.7	-3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	85°C ⁽¹⁾

(1) Package limited to 85°C ambient.

Table 6. TPA6010A4 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5	1250 mW (3 dB crest factor)	0.55	85°C ⁽¹⁾
2.5	1000 mW (4 dB crest factor)	0.62	85°C ⁽¹⁾
2.5	500 mW (7 dB crest factor)	0.59	85°C ⁽¹⁾
2.5	250 mW (10 dB crest factor)	0.53	85°C ⁽¹⁾

(1) Package limited to 85°C ambient.

The maximum dissipated power, $P_{D(max)}$, is reached at a much lower output power level for an 8-Ω load than for a 3-Ω load. As a result, for calculating $P_{D(max)}$ for an 8-Ω application, use Equation 12:

$$P_{D(max)} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{12}$$

However, in the case of a 3-Ω load, $P_{D(max)}$ occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the $P_{D(max)}$ formula for a 3-Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the Dissipation Rating Table. To convert this to θ_{JA} use Equation 13:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45^\circ\text{C/W} \tag{13}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given θ_{JA} , the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with Equation 14. The maximum recommended junction temperature for the TPA6010A4 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$\begin{aligned} T_A \text{ Max} &= T_J \text{ Max} - \theta_{JA} P_D \\ &= 150 - 45(0.6 \times 2) = 96^\circ\text{C (15 dB crest factor)} \end{aligned} \tag{14}$$

- A. Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel. Due to package limitations the actual $T_A \text{ Max}$ is 85°C.

Table 5 and Table 6 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA6010A4 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 5 and Table 6 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

INPUT MUX OPERATION

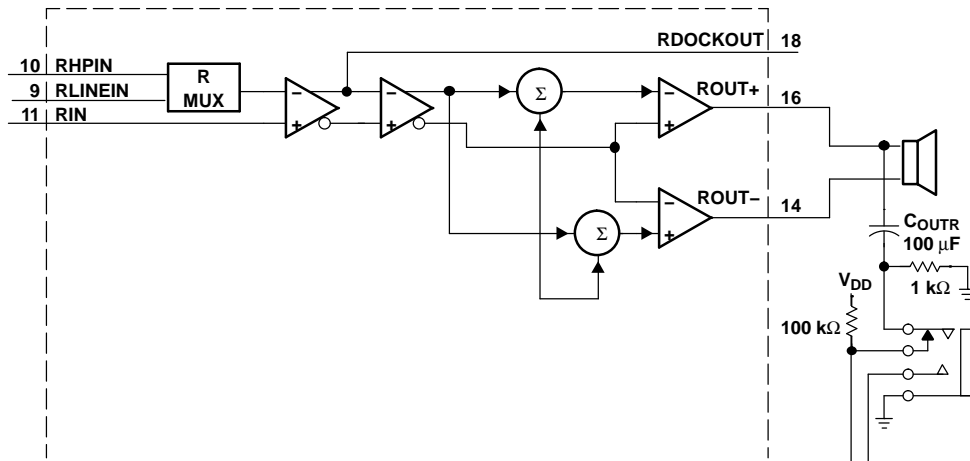


Figure 14. TPA6010A4 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to -1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/BTL OPERATION section for a description of the headphone jack control circuit.

SHUTDOWN MODES

The TPA6010A4 employs a shutdown mode of operation designed to reduce supply current, I_{DD} , to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

Table 7. Shutdown and Mute Mode Functions

INPUTS ⁽¹⁾		AMPLIFIER STATE	
SE/BTL	SHUTDOWN	INPUT	OUTPUT
Low	High	Line	BTL
X	Low	X ⁽²⁾	Mute
High	High	HP	SE

(1) Inputs should never be left unconnected.
 (2) X = do not care

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6010A4PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA6010	Samples
TPA6010A4PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA6010	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6010A4PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6010A4PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

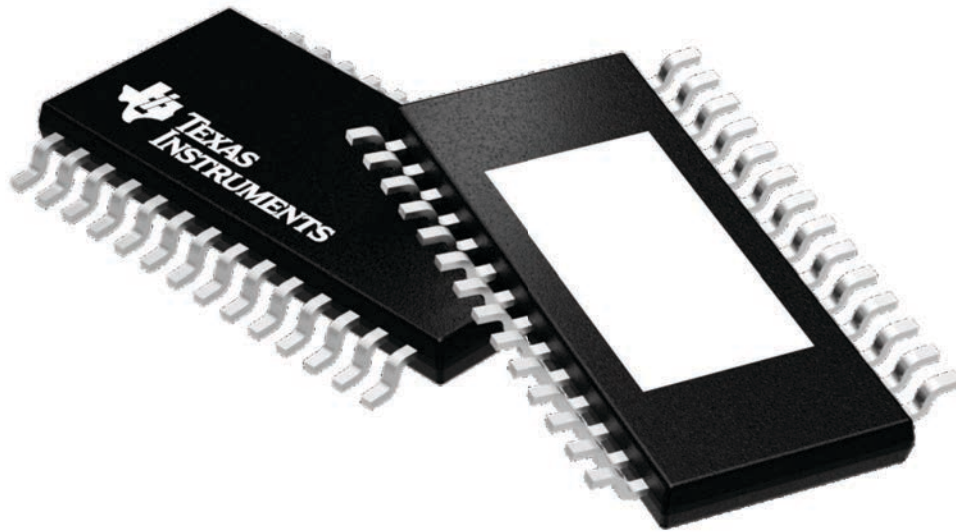
GENERIC PACKAGE VIEW

PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE



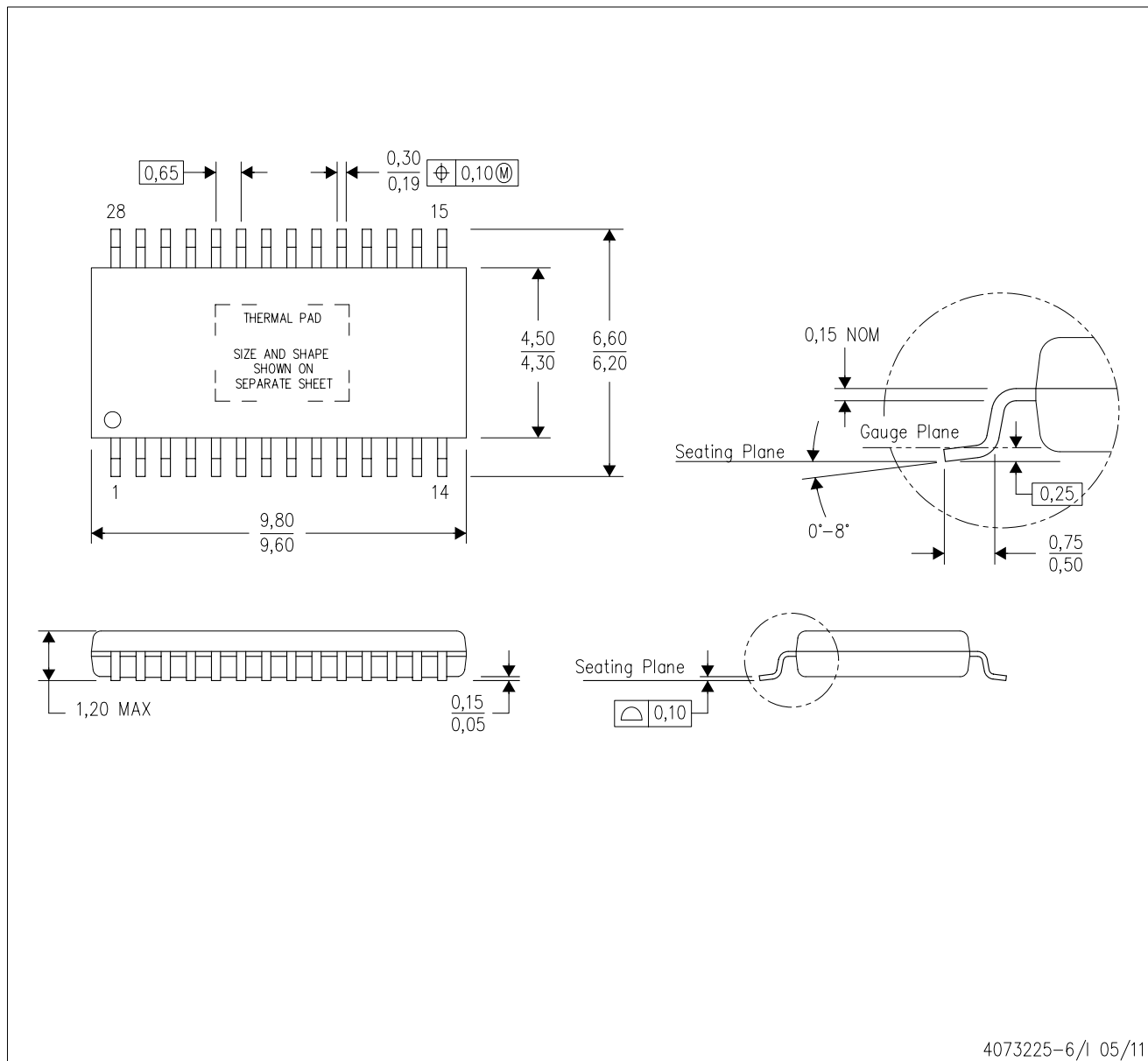
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224765/A

MECHANICAL DATA

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-6/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

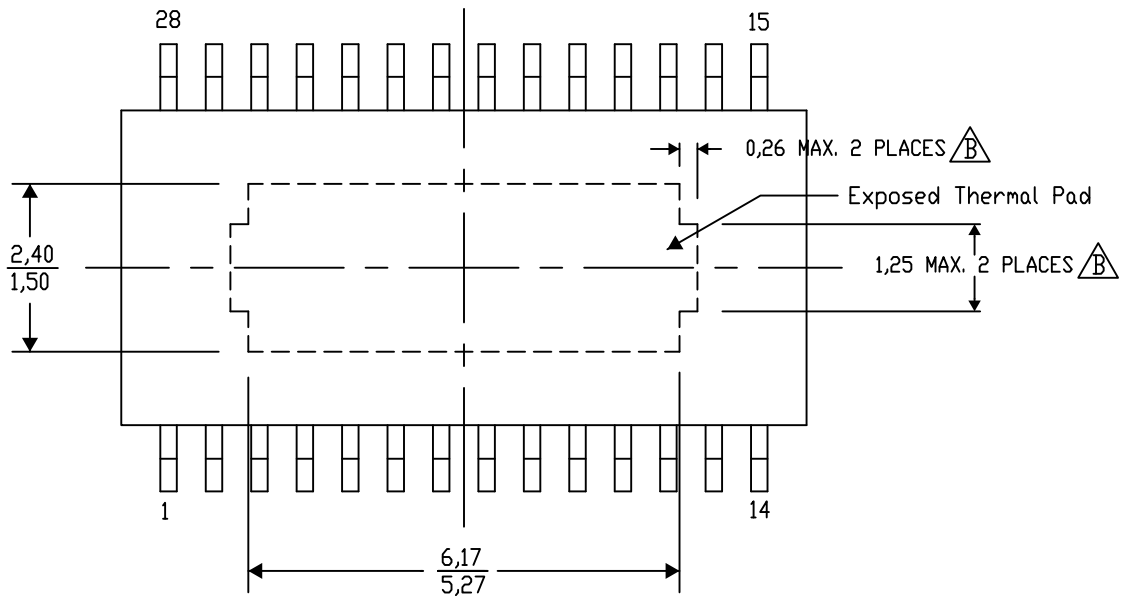
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

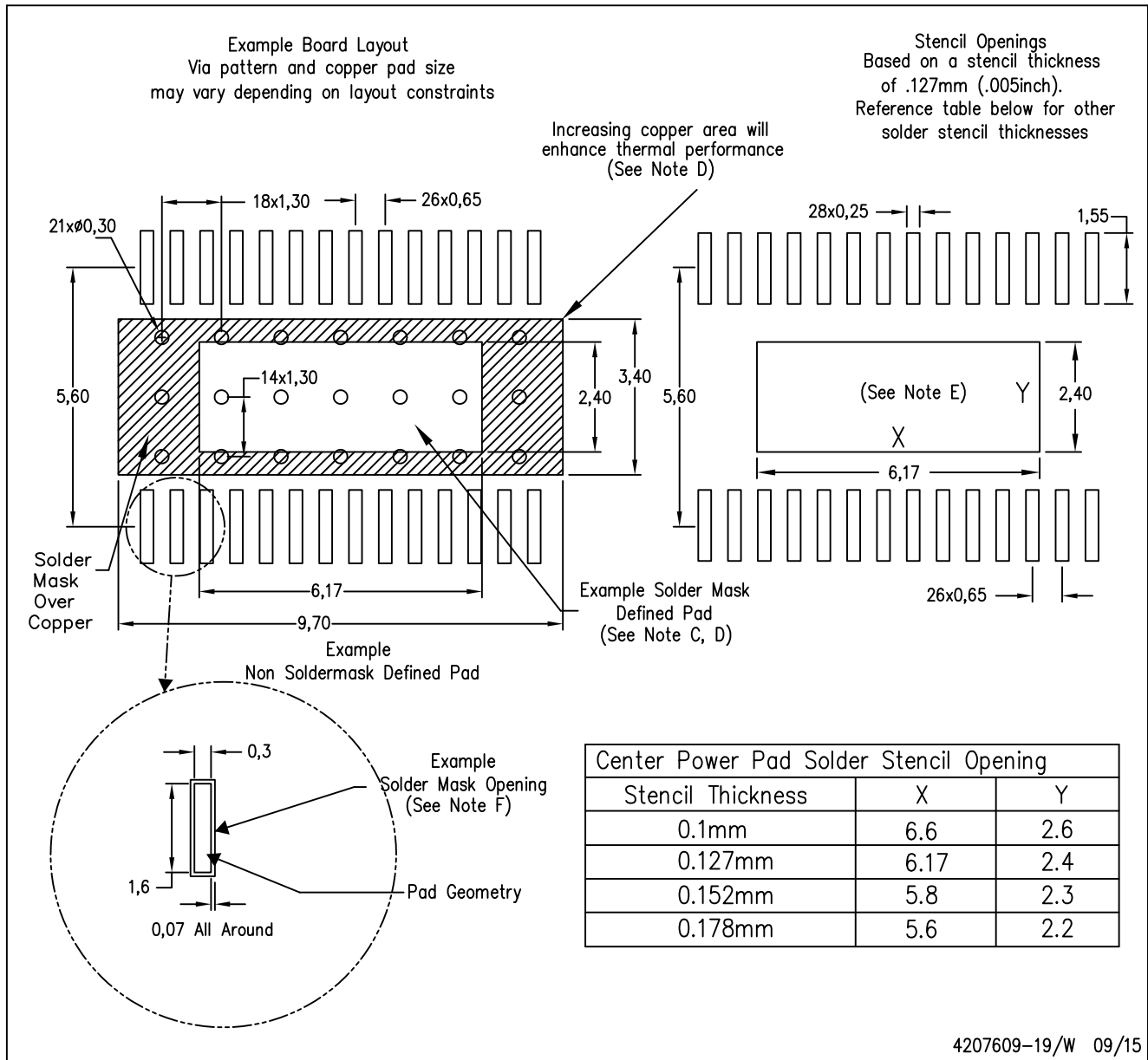
4206332-33/AO 01/16

NOTE: A. All linear dimensions are in millimeters
 $\triangle B$. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
- E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated