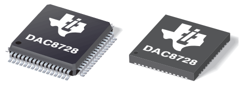


DAC8728

Octal, 16-Bit, Low-Power, High-Voltage Output, Parallel Input DIGITAL-TO-ANALOG CONVERTER

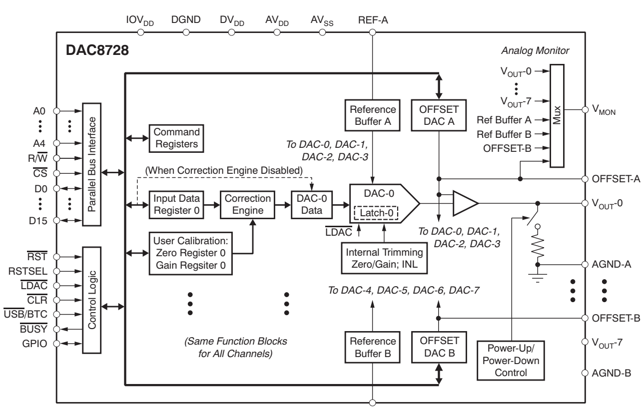
Check for Samples: DAC8728

FEATURES

- **Bipolar Output: ±3V, up to ±16.5V**
- **Unipolar Output: 0V to +33V**
- **16-Bit Resolution**
- **Low Power: 13.5mW/Ch**
- **Relative Accuracy: 4 LSB Max**
- **Flexible User Calibration**
- **Low Zero/Full-Scale Error**
  - **Before User Calibration: ±10 LSB Max**
  - **After User Calibration: ±1 LSB**
- **Low Glitch: 4nV-s**
- **Settling Time: 15µs**
- **Channel Monitor Output**
- **Programmable Gain: x4, x6**
- **Programmable Offset**
- **16-Bit Parallel Interface: 50MHz (Write Operation)**
- **Packages: QFN-56 (8mm x 8mm), TQFP-64 (10mm x 10mm)**

APPLICATIONS

- **Automatic Test Equipment**
- **PLC and Industrial Process Control**
- **Communications**



DESCRIPTION

The DAC8728 is a low-power, octal, 16-bit digital-to-analog converter (DAC). With a 5V reference, the output can either be a bipolar ±15V voltage when operating from a dual ±15.5V (or higher) power supply, or a unipolar 0V to +30V voltage when operating from a +30.5V power supply. With a 5.5V reference, the output can either be a ±16.5V for a dual ±17V (or higher) power supply, or a unipolar 0V to +33V voltage when operating from a +33.5V (or higher) power supply. This DAC provides low-power operation, good linearity, and low glitch over the specified temperature range of –40°C to +105°C. This device is trimmed in manufacturing and has very low zero and full-scale error. In addition, user calibration can be performed to achieve ±1 LSB bipolar zero/full-scale error for a bipolar supply, or ±1 LSB zero-code/full-scale error for a unipolar supply over the entire signal chain. The output range can be offset by using the DAC Offset Register.

The DAC8728 features a standard, high-speed, 16-bit parallel interface that operates at up to 50MHz and is 1.8V, 3V, and 5V logic compatible, to communicate with a DSP or microprocessor. The eight DACs and the auxiliary registers are addressed with five address lines. The device features double-buffered interface logic. An asynchronous load input ($\overline{\text{LDAC}}$) transfers data from the DAC data register to the DAC latch. The asynchronous $\overline{\text{CLR}}$ input sets the output of all eight DACs to AGND. The V_{MON} pin is a monitor output that connects to the individual analog outputs, the offset DAC, and the reference buffer outputs through a multiplexer (mux).

The DAC8728 is pin-to-pin compatible with the DAC8228 (14-bit) and the DAC7728 (12-bit).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION[1]

PRODUCT	RELATIVE ACCURACY (LSB)	DIFFERENTIAL LINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC8728	±4	±1	QFN-56	RTQ	–40°C to +105°C	DAC8728
	±4	±1	TQFP-64	PAG	–40°C to +105°C	DAC8728

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range (unless otherwise noted).

			DAC8728	UNIT
AV_{DD} to AV_{SS}			–0.3 to 38	V
AV_{DD} to AGND			–0.3 to 38	V
AV_{SS} to AGND, DGND			–19 to 0.3	V
DV_{DD} to DGND			–0.3 to 6	V
IOV_{DD} to DGND			–0.3 to DV_{DD} + 0.3	V
AGND to DGND			–0.3 to 0.3	V
Digital input voltage to DGND			–0.3 to IOV_{DD} + 0.3	V
V_{OUT}-x, V_{MON} to AV_{SS}			–0.3 to AV_{DD} + 0.3	V
REF-A, REF-B to AGND			–0.3 to DV_{DD}	V
$\overline{BUSY}$, GPIO to DGND			–0.3 to IOV_{DD} + 0.3	V
Maximum current from V_{MON}			3	mA
Operating temperature range			–40 to +105	°C
Storage temperature range			–65 to +150	°C
Maximum junction temperature (T_J max)			+150	°C
ESD ratings	Human body model (HBM)		4	kV
	Charged device model (CDM)	TQFP	1000	V
		QFN	500	V
	Machine model (MM)		200	V
Thermal impedance	Junction-to-ambient, θ_{JA}	TQFP	55	°C/W
		QFN	21.7	°C/W
	Junction-to-case, θ_{JC}	TQFP	21	°C/W
		QFN	20.4	°C/W
Power dissipation			(T_J max – T_A) / θ_{JA}	W

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: Dual-Supply

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +16.5V, AV_{SS} = –16.5V, DV_{DD} = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, and Offset DAC A and Offset DAC B are at default values(1), unless otherwise noted.

PARAMETER	CONDITIONS	DAC8728 MIN	TYP	MAX	UNIT
STATIC PERFORMANCE					
Resolution		16			Bits
Linearity error	Measured by line passing through codes 0000h and FFFFh			±4	LSB
Differential linearity error	Measured by line passing through codes 0000h and FFFFh			±1	LSB
Bipolar zero error	T_A = +25°C, before user calibration, gain = 6, code = 8000h			±10	LSB
	T_A = +25°C, before user calibration, gain = 4, code = 8000h			±15	LSB
	T_A = +25°C, after user calib., gain = 4 or 6, code = 8000h		±1		LSB
Bipolar zero error TC	Gain = 4 or 6, code = 8000h		±0.5	±2	ppm FSR/°C
Zero-code error	T_A = +25°C, gain = 6, code = 0000h			±10	LSB
	T_A = +25°C, gain = 4, code = 0000h			±15	LSB
Zero-code error TC	Gain = 4 or 6, code = 0000h		±0.5	±3	ppm FSR/°C
Gain error	T_A = +25°C, gain = 6			±10	LSB
	T_A = +25°C, gain = 4			±15	LSB
Gain error TC	Gain = 4 or 6		±1	±3	ppm FSR/°C
Full-scale error	T_A = +25°C, before user calibration, gain = 6, code = FFFFh			±10	LSB
	T_A = +25°C, before user calibration, gain = 4, code = FFFFh			±15	LSB
	T_A = +25°C, after user calib., gain = 4 or 6, code = FFFFh		±1		LSB
Full-scale error TC	Gain = 4 or 6, code = FFFFh		±0.5	±3	ppm FSR/°C
DC crosstalk(2)	Measured channel at code = 8000h, full-scale change on any other channel		0.2		LSB

(1) Offset DAC A and Offset DAC B are trimmed in manufacturing to minimize the error for symmetrical output. The default value may vary no more than ±10 LSB from the nominal number listed in Table 8. These pins are not intended to drive an external load, and must not be connected during dual-supply operation.
(2) The DAC outputs are buffered by op amps that share common AV_{DD} and AV_{SS} power supplies. DC crosstalk indicates how much dc change in one or more channel outputs may occur when the dc load current changes in one channel (because of an update). With high-impedance loads, the effect is virtually immeasurable. Multiple AV_{DD} and AV_{SS} terminals are provided to minimize dc crosstalk.

ELECTRICAL CHARACTERISTICS: Dual-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +16.5V, AV_{SS} = –16.5V, DV_{DD} = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, and Offset DAC A and Offset DAC B are at default values [1], unless otherwise noted.

PARAMETER	CONDITIONS	DAC8728 MIN	TYP	MAX	UNIT
ANALOG OUTPUT (V_{OUT}-0 to V_{OUT}-7)[3]					
Voltage output[4]	V_{REF} = +5V	–15		+15	V
	V_{REF} = +1.5V	–4.5		+4.5	V
Output impedance	Code = 8000h			0.5	Ω
Short-circuit current[5]			±10		mA
Load current	See Figure 37		±3		mA
Output drift vs time	T_A = +25°C, device operating for 500 hours, full-scale output		3.4		ppm of FSR
	T_A = +25°C, device operating for 1000 hours, full-scale output		4.3		ppm of FSR
Capacitive load stability				500	pF
Settling time	To 0.03% of FSR, C_L = 200pF, R_L= 10kΩ, code from 0000h to FFFFh and FFFFh to 0000h		10		µs
	To 1 LSB, C_L = 200pF, R_L = 10kΩ, code from 0000h to FFFFh and FFFFh to 0000h		15		µs
	To 1 LSB, C_L = 200pF, R_L = 10kΩ, code from 7F00h to 8100h and 8100h to 7F00h		6		µs
Slew rate[6]			6		V/µs
Power-on delay[7]	From IOV_{DD} ≥ +1.8V and DV_{DD} ≥ +2.7V to $\overline{CS}$ low		200		µs
Power-down recovery time			50		µs
Digital-to-analog glitch[8]	Code from 7FFFh to 8000h and 8000h to 7FFFh		4		nV-s
Glitch impulse peak amplitude	Code from 7FFFh to 8000h and 8000h to 7FFFh		5		mV
Channel-to-channel isolation[9]	V_{REF} = $4V_{PP}$, f = 1kHz		88		dB
DAC-to-DAC crosstalk[10]	DACs in the same group		10		nV-s
	DACs among different groups		1		nV-s
Digital crosstalk[11]			1		nV-s
Digital feedthrough[12]			1		nV-s
Output noise	T_A = +25°C at 10kHz, gain = 6		200		nV/√Hz
	T_A = +25°C at 10kHz, gain = 4		130		nV/√Hz
	0.1Hz to 10Hz, gain = 6		20		μV_{PP}
Power-supply rejection[13]	AV_{DD} = ±15.5V to ±16.5V		0.05		LSB

(3) Specified by design.
(4) The analog output range of V_{OUT}-0 to V_{OUT}-7 is equal to (6 × V_{REF} – 5 × OUTPUT_OFFSET_DAC) for gain = 6. The maximum value of the analog output must not be greater than (AV_{DD} – 0.5V), and the minimum value must not be less than (AV_{SS} + 0.5V). All specifications are for a ±16.5V power supply and a ±15V output, unless otherwise noted.
(5) When the output current is greater than the specification, the current is clamped at the specified maximum value.
(6) Slew rate is measured from 10% to 90% of the transition when the output changes from 0 to full-scale.
(7) *Power-on delay* is defined as the time from when the supply voltages reach the specified conditions to when $\overline{CS}$ goes low, for valid digital communication.
(8) *Digital-to-analog glitch* is defined as the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 7FFFh and 8000h in straight binary format.
(9) *Channel-to-channel isolation* refers to the ratio of the signal amplitude at the output of one DAC channel to the amplitude of the sinusoidal signal on the reference input of another DAC channel. It is expressed in dB and measured at midscale.
(10) *DAC-to-DAC crosstalk* is the glitch impulse that appears at the output of one DAC as a result of both the full-scale digital code and subsequent analog output change at another DAC. It is measured with LDAC tied low and expressed in nV-s.
(11) *Digital crosstalk* is the glitch impulse transferred to the output of one converter as a result of a full-scale code change in the DAC input register of another converter. It is measured when the DAC output is not updated, and is expressed in nV-s.
(12) *Digital feedthrough* is the glitch impulse injected to the output of a DAC as a result of a digital code change in the DAC input register of the same DAC. It is measured with the full-scale digital code change without updating the DAC output, and is expressed in nV-s.
(13) The output must not be greater than (AV_{DD} – 0.5V) and not less than (AV_{SS} + 0.5V).

ELECTRICAL CHARACTERISTICS: Dual-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +16.5V, AV_{SS} = –16.5V, DV_{DD} = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, and Offset DAC A and Offset DAC B are at default values (1), unless otherwise noted.

PARAMETER	CONDITIONS	DAC8728 MIN	TYP	MAX	UNIT
OFFSET DAC OUTPUT (14) (15)					
Voltage output	V_{REF} = +5V	0		5	V
Full-scale error	T_A = +25°C		±4		LSB
Zero-code error	T_A = +25°C		±2		LSB
Linearity error			±6		LSB
Differential linearity error				±1	LSB
ANALOG MONITOR PIN (V_{MON})					
Output impedance (16)	T_A = +25°C		2000		Ω
Three-state leakage current			100		nA
REFERENCE INPUT					
Reference input voltage range (17)		1.0		5.5	V
Reference input dc impedance			10		MΩ
Reference input capacitance			10		pF
DIGITAL INPUT (14)					
High-level input voltage, V_{IH}	IOV_{DD} = +4.5V to +5.5V	3.8		0.3 + IOV_{DD}	V
	IOV_{DD} = +2.7V to +3.3V	2.3		0.3 + IOV_{DD}	V
	IOV_{DD} = +1.7V to 2.0V	1.5		0.3 + IOV_{DD}	V
Low-level input voltage, V_{IL}	IOV_{DD} = +4.5V to +5.5V	–0.3		0.8	V
	IOV_{DD} = +2.7V to +3.3V	–0.3		0.6	V
	IOV_{DD} = +1.7V to 2.0V	–0.3		0.3	V
Input current	$\overline{CLR}$, $\overline{LDAC}$, $\overline{RST}$, A0 to A4, R/$\overline{W}$, and $\overline{CS}$			±1	μA
	$\overline{USB}$/BTC, RSTSEL, and D0 to D15, and GPIO			±5	μA
Input capacitance	$\overline{CLR}$, $\overline{LDAC}$, $\overline{RST}$, A0 to A4, R/$\overline{W}$, and $\overline{CS}$		5		pF
	$\overline{USB}$/BTC, RSTSEL, and D0 to D15		12		pF
	GPIO		14		pF
DIGITAL OUTPUT (14)					
High-level output voltage, V_{OH} (D0 to D15)	IOV_{DD} = +2.7V to +5.5V, sourcing 1mA	IOV_{DD} – 0.4		IOV_{DD}	V
	IOV_{DD} = +1.8V, sourcing 200μA	1.6		IOV_{DD}	V
Low-level output voltage, V_{OL} (D0 to D15, $\overline{BUSY}$, and GPIO)	IOV_{DD} = +2.7V to +5.5V, sinking 1mA	0		0.4	V
	IOV_{DD} = +1.8V, sinking 200μA	0		0.2	V
High-impedance leakage current	D0 to D13, $\overline{BUSY}$, and GPIO			±5	μA
High-impedance output capacitance	$\overline{BUSY}$ and GPIO			14	pF

(14) Specified by design.
(15) Offset DAC A and Offset DAC B are trimmed in manufacturing to minimize the error for symmetrical output. The default value may vary no more than ±10 LSB from the nominal number listed in Table 8. These pins are not intended to drive an external load, and must not be connected during dual-supply operation.
(16) 8000Ω when V_{MON} is connected to Reference Buffer A or B.
(17) Reference input voltage ≤ DV_{DD}.

ELECTRICAL CHARACTERISTICS: Dual-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +16.5V, AV_{SS} = –16.5V, DV_{DD} = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, and Offset DAC A and Offset DAC B are at default values [(1)], unless otherwise noted.

PARAMETER	CONDITIONS	DAC8728 MIN	DAC8728 TYP	DAC8728 MAX	UNIT
POWER SUPPLY					
AV_{DD}		+4.5		+18	V
AV_{SS}		–18		–4.5	V
DV_{DD}		+2.7		+5.5	V
IOV_{DD}		+1.7		DV_{DD}	V
AI_{DD}	Normal operation, midscale code, output unloaded		4	6	mA
	Power down, output unloaded		35		µA
AI_{SS}	Normal operation, midscale code, output unloaded	–4	–2.5		mA
	Power down, output unloaded		–35		µA
DI_{DD}	Normal operation		75		µA
	Power down		35		µA
IOI_{DD}	Normal operation, $V_{IH} = IOV_{DD}$, V_{IL} = DGND		5		µA
	Power down, $V_{IH} = IOV_{DD}$, V_{IL} = DGND		5		µA
Power dissipation	Normal operation, ±16.5V supplies, midscale code		107	165	mW
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

ELECTRICAL CHARACTERISTICS: Single-Supply

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +32V, AV_{SS} = 0V, DV_{DD} = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, and OFFSET-A = OFFSET-B = AGND, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8728 MIN	DAC8728 TYP	DAC8728 MAX	UNIT
STATIC PERFORMANCE					
Resolution		16			Bits
Linearity error	Measured by line passing through codes 0100h and FFFFh			±4	LSB
Differential linearity error	Measured by line passing through codes 0100h and FFFFh			±1	LSB
Unipolar zero error	T_A = +25°C, before user calibration, gain = 6, code = 0100h			±10	LSB
	T_A = +25°C, before user calibration, gain = 4, code = 0100h			±15	LSB
	T_A = +25°C, after user calib., gain = 4 or 6, code = 0100h		±1		LSB
Unipolar zero error TC	Gain = 4 or 6, code = 0100h		±0.5	±3	ppm FSR/°C
Gain error	T_A = +25°C, gain = 6			±10	LSB
	T_A = +25°C, gain = 4			±15	LSB
Gain error TC	Gain = 4 or 6		±1	±3	ppm FSR/°C
Full-scale error	T_A = +25°C, before user calibration, gain = 6, code = FFFFh			±10	LSB
	T_A = +25°C, before user calibration, gain = 4, code = FFFFh			±15	LSB
	T_A = +25°C, after user calib., gain = 4 or 6, code = FFFFh		±1		LSB
Full-scale error TC	Gain = 4 or 6, code = FFFFh		±0.5	±3	ppm FSR/°C
DC crosstalk(1)	Measured channel at code = 8000h, full-scale change on any other channel		0.2		LSB
ANALOG OUTPUT (V_{OUT}-0 to V_{OUT}-7)(2)					
Voltage output(3)	V_{REF} = +5V	0		+30	V
	V_{REF} = +1.5V	0		+9	V
Output impedance	Code = 8000h			0.5	Ω
Short-circuit current(4)			±10		mA
Load current	See Figure 89 and Figure 90		±3		mA
Output drift vs time	T_A = +25°C, device operating for 500 hours, full-scale output		3.4		ppm of FSR
	T_A = +25°C, device operating for 1000 hours, full-scale output		4.3		ppm of FSR
Capacitive load stability				500	pF
Settling time	To 0.03% of FSR, C_L = 200pF, R_L= 10kΩ, code from 0100h to FFFFh and FFFFh to 0100h		10		µs
	To 1 LSB, C_L = 200pF, R_L = 10kΩ, code from 0100h to FFFFh and FFFFh to 0100h		15		µs
	To 1 LSB, C_L = 200pF, R_L = 10kΩ, code from 7F00h to 8100h and 8100h to 7F00h		6		µs
Slew rate(5)			6		V/µs
Power-on delay(6)	From IOV_{DD} ≥ +1.8V and DV_{DD} ≥ +2.7V to $\overline{CS}$ low		200		µs
Power-down recovery time			50		µs
Digital-to-analog glitch(7)	Code from 7FFFh to 8000h and 8000h to 7FFFh		4		nV-s
Glitch impulse peak amplitude	Code from 7FFFh to 8000h and 8000h to 7FFFh		5		mV

(1) The DAC outputs are buffered by op amps that share common AV_{DD} and AV_{SS} power supplies. DC crosstalk indicates how much dc change in one or more channel outputs may occur when the dc load current changes in one channel (because of an update). With high-impedance loads, the effect is virtually immeasurable. Multiple AV_{DD} and AV_{SS} terminals are provided to minimize dc crosstalk.
(2) Specified by design.
(3) The analog output range of V_{OUT}-0 to V_{OUT}-7 is equal to (6 × V_{REF}) for gain = 6. The maximum value of the analog output must not be greater than (AV_{DD} – 0.5V). All specifications are for a +32V power supply and a 0V to +30V output, unless otherwise noted.
(4) When the output current is greater than the specification, the current is clamped at the specified maximum value.
(5) Slew rate is measured from 10% to 90% of the transition when the output changes from 0 to full-scale.
(6) *Power-on delay* is defined as the time from when the supply voltages reach the specified conditions to when $\overline{CS}$ goes low, for valid digital communication.
(7) *Digital-to-analog glitch* is defined as the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 7FFFh and 8000h in straight binary format.

ELECTRICAL CHARACTERISTICS: Single-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +32V, AV_{SS} = 0V, DV_{DD} = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, and OFFSET-A = OFFSET-B = AGND, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8728 MIN	DAC8728 TYP	DAC8728 MAX	UNIT
Channel-to-channel isolation(8)	$V_{REF} = 4V_{PP}$, f = 1kHz		88		dB
DAC-to-DAC crosstalk(9)	DACs in the same group		10		nV-s
	DACs among different groups		1		nV-s
Digital crosstalk(10)			1		nV-s
Digital feedthrough(11)			1		nV-s
Output noise	T_A = +25°C at 10kHz, gain = 6		200		nV/√Hz
	T_A = +25°C at 10kHz, gain = 4		130		nV/√Hz
	0.1Hz to 10Hz, gain = 6		20		μV_{PP}
Power-supply rejection(12)	AV_{DD} = +33V to +36V		0.05		LSB
ANALOG MONITOR PIN (V_{MON})					
Output impedance(13)	T_A = +25°C		2000		Ω
Three-state leakage current			100		nA
REFERENCE INPUT					
Reference input voltage range(14)		1.0		5.5	V
Reference input dc impedance			10		MΩ
Reference input capacitance			10		pF
DIGITAL INPUT(15)					
High-level input voltage, V_{IH}	IOV_{DD} = +4.5V to +5.5V	3.8		0.3 + IOV_{DD}	V
	IOV_{DD} = +2.7V to +3.3V	2.3		0.3 + IOV_{DD}	V
	IOV_{DD} = +1.7V to 2.0V	1.5		0.3 + IOV_{DD}	V
Low-level input voltage, V_{IL}	IOV_{DD} = +4.5V to +5.5V	–0.3		0.8	V
	IOV_{DD} = +2.7V to +3.3V	–0.3		0.6	V
	IOV_{DD} = +1.7V to 2.0V	–0.3		0.3	V
Input current	$\overline{CLR}$, $\overline{LDAC}$, $\overline{RST}$, A0 to A4, R/$\overline{W}$, and $\overline{CS}$			±1	μA
	$\overline{USB}$/BTC, RSTSEL, and D0 to D15, and GPIO			±5	μA
Input capacitance	$\overline{CLR}$, $\overline{LDAC}$, $\overline{RST}$, A0 to A4, R/$\overline{W}$, and $\overline{CS}$		5		pF
	$\overline{USB}$/BTC, RSTSEL, and D0 to D15		12		pF
	GPIO		14		pF
DIGITAL OUTPUT(15)					
High-level output voltage, V_{OH} (D0 to D15)	IOV_{DD} = +2.7V to +5.5V, sourcing 1mA	IOV_{DD} – 0.4		IOV_{DD}	V
	IOV_{DD} = +1.8V, sourcing 200μA	1.6		IOV_{DD}	V
Low-level output voltage, V_{OL} (D0 to D15, $\overline{BUSY}$, and GPIO)	IOV_{DD} = +2.7V to +5.5V, sinking 1mA	0		0.4	V
	IOV_{DD} = +1.8V, sinking 200μA	0		0.2	V
High-impedance leakage current	D0 to D13, $\overline{BUSY}$, and GPIO			±5	μA
High-impedance output capacitance	$\overline{BUSY}$ and GPIO			14	pF

(8) *Channel-to-channel isolation* refers to the ratio of the signal amplitude at the output of one DAC channel to the amplitude of the sinusoidal signal on the reference input of another DAC channel. It is expressed in dB and measured at midscale.
(9) *DAC-to-DAC crosstalk* is the glitch impulse that appears at the output of one DAC as a result of both the full-scale digital code and subsequent analog output change at another DAC. It is measured with LDAC tied low and expressed in nV-s.
(10) *Digital crosstalk* is the glitch impulse transferred to the output of one converter as a result of a full-scale code change in the DAC input register of another converter. It is measured when the DAC output is not updated, and is expressed in nV-s.
(11) *Digital feedthrough* is the glitch impulse injected to the output of a DAC as a result of a digital code change in the DAC input register of the same DAC. It is measured with the full-scale digital code change without updating the DAC output, and is expressed in nV-s.
(12) The analog output must not be greater than (AV_{DD} – 0.5V).
(13) 8000Ω when V_{MON} is connected to Reference Buffer A or B.
(14) Reference input voltage ≤ DV_{DD}.
(15) Specified by design.

ELECTRICAL CHARACTERISTICS: Single-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +32V, AV_{SS} = 0V, DV_{DD} = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, and OFFSET-A = OFFSET-B = AGND, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8728 MIN	TYP	MAX	UNIT
POWER SUPPLY					
AV_{DD}		+9		+36	V
DV_{DD}		+2.7		+5.5	V
IOV_{DD}		+1.7		DV_{DD}	V
AI_{DD}	Normal operation, midscale code, output unloaded		4.5	7	mA
	Power down, output unloaded		35		µA
DI_{DD}	Normal operation		75		µA
	Power down		35		µA
IOI_{DD}	Normal operation, $V_{IH} = IOV_{DD}$, V_{IL} = DGND		5		µA
	Power down, $V_{IH} = IOV_{DD}$, V_{IL} = DGND		5		µA
Power dissipation	Normal operation		144	224	mW
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

FUNCTIONAL BLOCK DIAGRAM

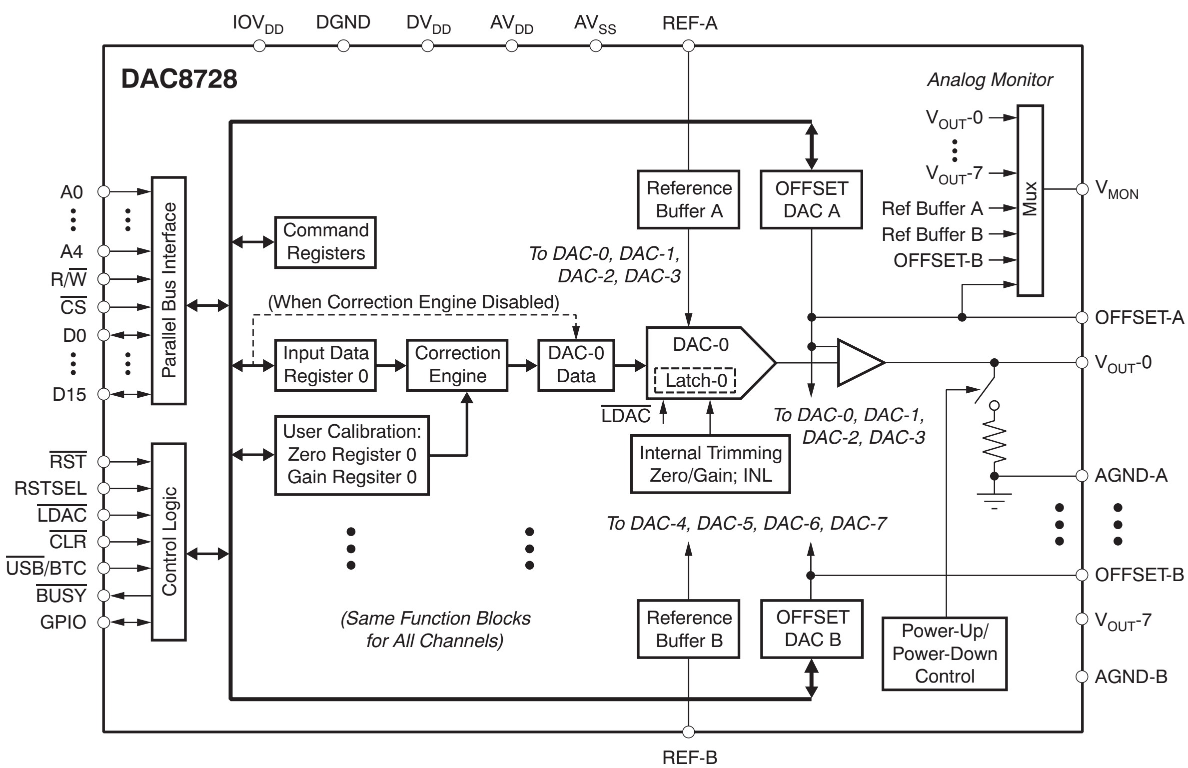
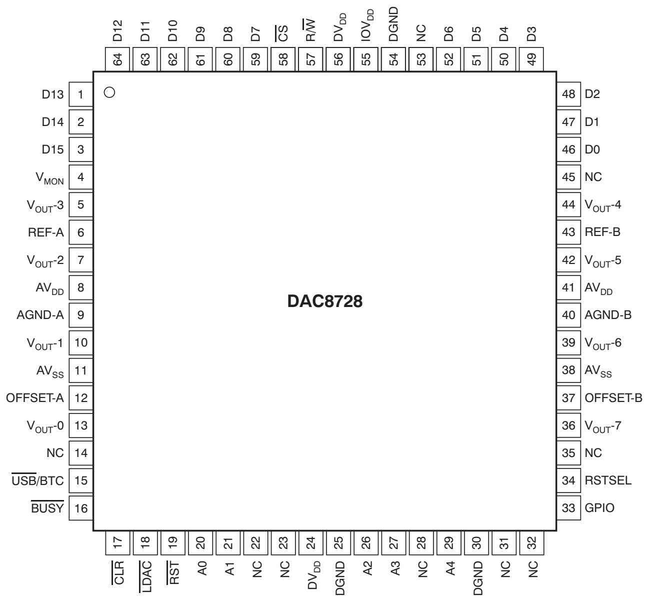


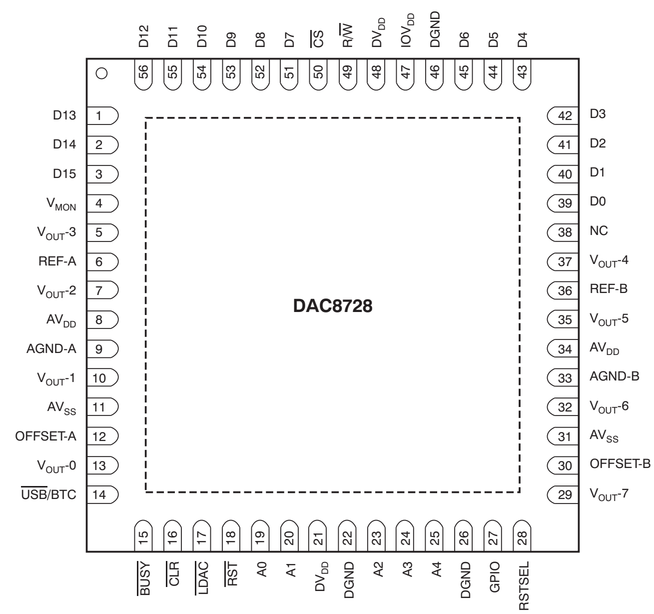
Figure 1. Functional Block Diagram

PIN CONFIGURATIONS

PAG PACKAGE
TQFP-64
(TOP VIEW)



RTQ PACKAGE
QFN-56
(TOP VIEW)



(1) The thermal pad is internally connected to the substrate. This pad can be connected to AV_{SS} or left floating. Keep the thermal pad separate from the digital ground, if possible.

PIN DESCRIPTIONS

PIN NAME	PIN NO. QFN-56	PIN NO. TQFP-64	I/O	DESCRIPTION
D13	1	1	I/O	Data bit 13
D14	2	2	I/O	Data bit 14
D15	3	3	I/O	Data bit 15
V_{MON}	4	4	O	Analog monitor output. This pin is either in Hi-Z status, or connected to one of the DAC outputs, reference buffer outputs, or offset DAC outputs, depending on the content of the Monitor Register.
V_{OUT}-3	5	5	O	DAC-3 output
REF-A	6	6	I	Group A[1] reference input
V_{OUT}-2	7	7	O	DAC-2 output
AV_{DD}	8	8	I	Positive analog power supply
AGND-A	9	9	I	Group A[1] analog ground and the ground of REF-A. This pin must be tied to AGND-B and DGND.
V_{OUT}-1	10	10	O	DAC-1 output
AV_{SS}	11	11	I	Negative analog power supply. Connect to AGND in single-supply operation.
OFFSET-A	12	12	O	OFFSET DAC-A analog output. Must be connected to AGND-A during single power-supply operation (AV_{SS} = 0V). This pin is not intended to drive an external load.
V_{OUT}-0	13	13	O	DAC-0 output
$\overline{USB}$/BTC	14	15	I	Input data format selection. Input data are in straight binary format when connected to DGND or in twos complement format when connected to IOV_{DD}. Command data are always in straight binary format.
$\overline{BUSY}$	15	16	O	This pin is an open drain and requires an external pullup resistor. $\overline{BUSY}$ goes low when the correction engine is running; see the *Busy Pin* section for details.
$\overline{CLR}$	16	17	I	Level trigger. When the $\overline{CLR}$ pin is logic '0', all V_{OUT}-X pins connect to AGND-x through switches and an internal 15kΩ resistor. When the $\overline{CLR}$ pin is logic '1' and $\overline{LDAC}$ is logic '0', all V_{OUT}-X pins connect to the amplifier outputs.

(1) Group A consists of DAC-0, DAC-1, DAC-2, and DAC-3. Group B consists of DAC-4, DAC-5, DAC-6, and DAC-7.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NO.		I/O	DESCRIPTION
	QFN-56	TQFP-64		
$\overline{\text{LDAC}}$	17	18	I	Load DAC latch control input (active low). When $\overline{\text{LDAC}}$ is low, the DAC latch is transparent and the contents of the DAC Data Register are transferred to it. The DAC output changes to the corresponding level simultaneously when the DAC latch is updated. See the *DAC Output Update* section for details. If asynchronous mode is desired, $\overline{\text{LDAC}}$ must be permanently tied low before power is applied to the device. If synchronous mode is desired, $\overline{\text{LDAC}}$ must be logic high during power-on.
$\overline{\text{RST}}$	18	19	I	Reset input (active low). Logic low on this pin resets the DAC registers and DACs to the values defined by the RSTSEL pin. $\overline{\text{CS}}$ must be at logic high when $\overline{\text{RST}}$ is used.
A0	19	20	I	Address bit A0 to specify the internal registers.
A1	20	21	I	Address bit A1 to specify the internal registers.
DV_{DD}	21	24	I	Digital power supply
DGND	22	25	I	Digital ground
A2	23	26	I	Address bit A2 to specify the internal registers.
A3	24	27	I	Address bit A3 to specify the internal registers.
A4	25	29	I	Address bit A4 to specify the internal registers.
DGND	26	30	I	Digital ground
GPIO	27	33	I/O	General-purpose digital input/output. This pin is a bidirectional, open-drain, digital input/output, and requires an external pullup resistor. See the *GPIO Pin* section for details.
RSTSEL	28	34	I	Output reset selection. Selects the output voltage on the V_{OUT} pin after power-on or hardware reset. Refer to the *Power-On Reset* section for details.
V_{OUT}-7	29	36	O	DAC-7 output
OFFSET-B	30	37	O	OFFSET DAC-B analog output. Must be connected to AGND-B during single-supply operation (AV_{SS} = 0V). This pin is not intended to drive an external load.
AV_{SS}	31	38	I	Negative analog power supply. Connect to AGND in single-supply operation.
V_{OUT}-6	32	39	O	DAC-6 output
AGND-B	33	40	I	Group B(2) analog ground and the ground of REF-B. This pin must be tied to AGND-A and DGND.
AV_{DD}	34	41	I	Positive analog power supply
V_{OUT}-5	35	42	O	DAC-5 output
REF-B	36	43	I	Group B(2) reference input
V_{OUT}-4	37	44	O	DAC-4 output
NC	38	14, 22, 23, 28, 31, 32, 35, 45, 53	—	Not connected
D0	39	46	I/O	Data bit 0
D1	40	47	I/O	Data bit 1
D2	41	48	I/O	Data bit 2
D3	42	49	I/O	Data bit 3
D4	43	50	I/O	Data bit 4
D5	44	51	I/O	Data bit 5
D6	45	52	I/O	Data bit 6
DGND	46	54	I	Digital ground
IOV_{DD}	47	55	I	Digital interface power supply
DV_{DD}	48	56	I	Digital power supply
R/$\overline{\text{W}}$	49	57	I	Read and write signal. High for reading operation; low for writing operation.
$\overline{\text{CS}}$	50	58	I	Chip select input (active low)
D7	51	59	I/O	Data bit 7
D8	52	60	I/O	Data bit 8
D9	53	61	I/O	Data bit 9
D10	54	62	I/O	Data bit 10
D11	55	63	I/O	Data bit 11
D12	56	64	I/O	Data bit 12

(2) Group A consists of DAC-0, DAC-1, DAC-2, and DAC-3. Group B consists of DAC-4, DAC-5, DAC-6, and DAC-7.

TIMING DIAGRAMS

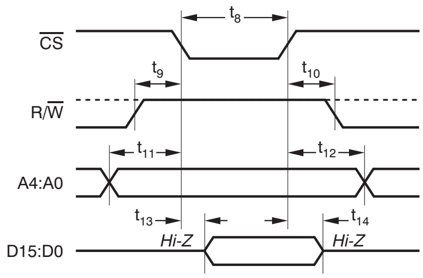
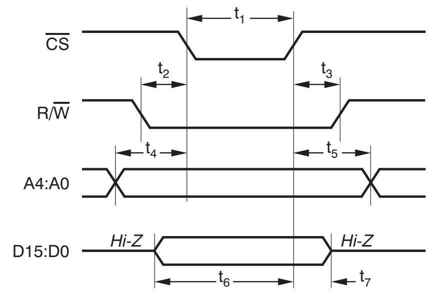


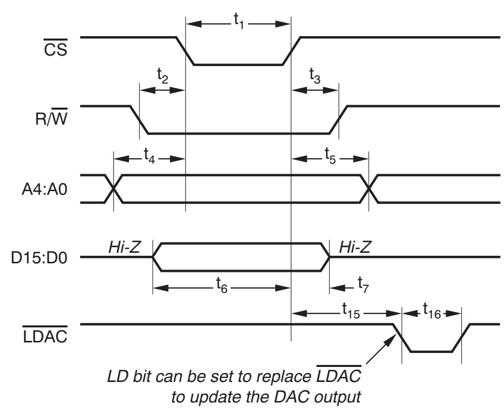
Figure 2. Read Operation



Write Operation 1:

1. Writing to the Configuration Register, Offset Register, Monitor Register, GPIO Register.
2. Writing to the DAC Input Registers, Zero Registers, and Gain Registers in Asynchronous mode ($\overline{LDAC}$ pin is tied low).

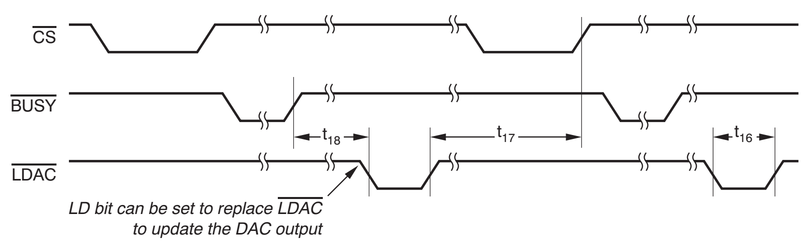
Figure 3. Write Operation 1



Write Operation 2:

Writing to the DAC Input Data Registers, Zero Registers, and Gain Registers when the correction engine is disabled and DAC outputs are updated in Synchronous mode.

Figure 4. Write Operation 2



Write Operation 3:

Writing to the DAC Input Data Registers, Zero Registers, and Gain Registers when the correction engine is enabled (SCE = 1) and the DAC outputs are updated in Synchronous mode. The update trigger (either $\overline{LDAC}$ or the LD bit) activates after the correction completes.

Figure 5. Write Operation 3

TIMING CHARACTERISTICS(1) (2) (3) (4) (5)

At –40°C to +105°C, DV_{DD} = +5V to +5.5V, and IOV_{DD} = +5V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_1	$\overline{CS}$ width for write operation	15		ns
t_2	Delay from R/$\overline{W}$ falling edge to $\overline{CS}$ falling edge	2		ns
t_3	Delay from $\overline{CS}$ rising edge to R/$\overline{W}$ rising edge	2		ns
t_4	Delay from address valid to $\overline{CS}$ falling edge	0		ns
t_5	Delay from $\overline{CS}$ rising edge to address change	0		ns
t_6	Delay from data valid to $\overline{CS}$ rising edge	15		ns
t_7	Delay from $\overline{CS}$ rising to data change	5		ns
t_8	$\overline{CS}$ width for read operation	30		ns
t_9	Delay from R/$\overline{W}$ rising edge to $\overline{CS}$ falling edge	2		ns
t_{10}	Delay from $\overline{CS}$ rising edge to R/$\overline{W}$ falling edge	2		ns
t_{11}	Delay from address valid to $\overline{CS}$ falling edge	0		ns
t_{12}	Delay from $\overline{CS}$ rising to address change	0		ns
t_{13}	Delay from $\overline{CS}$ falling edge to data valid		25	ns
t_{14}	Delay from $\overline{CS}$ rising to data bus off (Hi-Z)	2		ns
t_{15}	Delay from $\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	0		ns
t_{16}	$\overline{LDAC}$ pulse width	10		ns
t_{17}	Delay from $\overline{LDAC}$ rising edge to next $\overline{CS}$ rising edge	20		ns
t_{18}	Delay from $\overline{BUSY}$ rising edge to next $\overline{LDAC}$ falling edge	0		ns
t_{19}	Delay from $\overline{CS}$ rising edge to next $\overline{LDAC}$ falling edge	30		ns
t_{20}	Delay from $\overline{CS}$ rising edge to $\overline{BUSY}$ falling edge		20	ns
t_{21}	Delay from $\overline{LDAC}$ falling edge to $\overline{BUSY}$ rising edge	50		ns

(1) Specified by design; not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.
(3) Rise and fall times of all digital input signals are 3ns.
(4) Rise and fall times of all digital outputs are 3ns for a 10pF capacitor load.
(5) For sequential writes to the same address, there must be a minimum of 30ns between the $\overline{CS}$ rising edges.

TIMING CHARACTERISTICS(1) (2) (3) (4) (5)

At –40°C to +105°C, DV_{DD} = +3V to +5V, and IOV_{DD} = +3V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_1	$\overline{\text{CS}}$ width for write operation	25		ns
t_2	Delay from R/$\overline{\text{W}}$ falling edge to $\overline{\text{CS}}$ falling edge	2		ns
t_3	Delay from $\overline{\text{CS}}$ rising edge to R/$\overline{\text{W}}$ rising edge	2		ns
t_4	Delay from address valid to $\overline{\text{CS}}$ falling edge	6		ns
t_5	Delay from $\overline{\text{CS}}$ rising edge to address change	0		ns
t_6	Delay from data valid to $\overline{\text{CS}}$ rising edge	25		ns
t_7	Delay from $\overline{\text{CS}}$ rising to data change	5		ns
t_8	$\overline{\text{CS}}$ width for read operation	50		ns
t_9	Delay from R/$\overline{\text{W}}$ rising edge to $\overline{\text{CS}}$ falling edge	2		ns
t_{10}	Delay from $\overline{\text{CS}}$ rising edge to R/$\overline{\text{W}}$ falling edge	2		ns
t_{11}	Delay from address valid to $\overline{\text{CS}}$ falling edge	6		ns
t_{12}	Delay from $\overline{\text{CS}}$ rising to address change	0		ns
t_{13}	Delay from $\overline{\text{CS}}$ falling edge to data valid		40	ns
t_{14}	Delay from $\overline{\text{CS}}$ rising to data bus off (Hi-Z)	2		ns
t_{15}	Delay from $\overline{\text{CS}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	5		ns
t_{16}	$\overline{\text{LDAC}}$ pulse width	10		ns
t_{17}	Delay from $\overline{\text{LDAC}}$ rising edge to next $\overline{\text{CS}}$ rising edge	20		ns
t_{18}	Delay from $\overline{\text{BUSY}}$ rising edge to next $\overline{\text{LDAC}}$ falling edge	0		ns
t_{19}	Delay from $\overline{\text{CS}}$ rising edge to next $\overline{\text{LDAC}}$ falling edge	30		ns
t_{20}	Delay from $\overline{\text{CS}}$ rising edge to $\overline{\text{BUSY}}$ falling edge		20	ns
t_{21}	Delay from $\overline{\text{LDAC}}$ falling edge to $\overline{\text{BUSY}}$ rising edge	50		ns

(1) Specified by design; not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.
(3) Rise and fall times of all digital input signals are 5ns.
(4) Rise and fall times of all digital outputs are 5ns for a 10pF capacitor load.
(5) For sequential writes to the same address, there must be a minimum of 50ns between the $\overline{\text{CS}}$ rising edges.

TIMING CHARACTERISTICS(1) (2) (3) (4) (5)

At –40°C to +105°C, DV_{DD} = +3V to +5V, and IOV_{DD} = +1.8V, unless otherwise noted.

	PARAMETER	MIN	MAX	UNIT
t_1	$\overline{CS}$ width for write operation	35		ns
t_2	Delay from R/$\overline{W}$ falling edge to $\overline{CS}$ falling edge	2		ns
t_3	Delay from $\overline{CS}$ rising edge to R/$\overline{W}$ rising edge	2		ns
t_4	Delay from address valid to $\overline{CS}$ falling edge	12		ns
t_5	Delay from $\overline{CS}$ rising edge to address change	0		ns
t_6	Delay from data valid to $\overline{CS}$ rising edge	35		ns
t_7	Delay from $\overline{CS}$ rising to data change	5		ns
t_8	$\overline{CS}$ width for read operation	60		ns
t_9	Delay from R/$\overline{W}$ rising edge to $\overline{CS}$ falling edge	2		ns
t_{10}	Delay from $\overline{CS}$ rising edge to R/$\overline{W}$ falling edge	2		ns
t_{11}	Delay from address valid to $\overline{CS}$ falling edge	12		ns
t_{12}	Delay from $\overline{CS}$ rising to address change	0		ns
t_{13}	Delay from $\overline{CS}$ falling edge to data valid		50	ns
t_{14}	Delay from $\overline{CS}$ rising to data bus off (Hi-Z)	2		ns
t_{15}	Delay from $\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	5		ns
t_{16}	$\overline{LDAC}$ pulse width	10		ns
t_{17}	Delay from $\overline{LDAC}$ rising edge to next $\overline{CS}$ rising edge	30		ns
t_{18}	Delay from $\overline{BUSY}$ rising edge to next $\overline{LDAC}$ falling edge	0		ns
t_{19}	Delay from $\overline{CS}$ rising edge to next $\overline{LDAC}$ falling edge	50		ns
t_{20}	Delay from $\overline{CS}$ rising edge to $\overline{BUSY}$ falling edge		30	ns
t_{21}	Delay from $\overline{LDAC}$ falling edge to $\overline{BUSY}$ rising edge	50		ns

(1) Specified by design; not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.
(3) Rise and fall times of all digital input signals are 8ns.
(4) Rise and fall times of all digital outputs are 12ns for a 10pF capacitor load.
(5) For sequential writes to the same address, there must be a minimum of 50ns between the $\overline{CS}$ rising edges.

TYPICAL CHARACTERISTICS: Dual-Supply

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +16.5V, AV_{SS} = –16.5V, and gain = 6, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

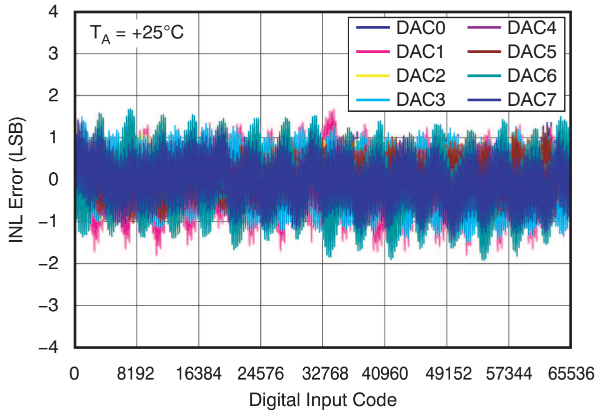


Figure 6.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

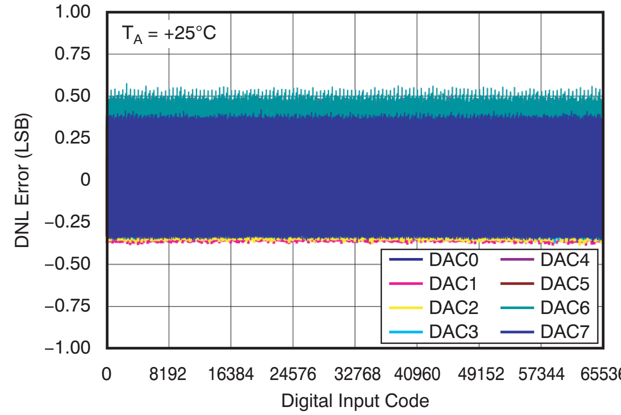


Figure 7.

LINEARITY ERROR vs DIGITAL INPUT CODE

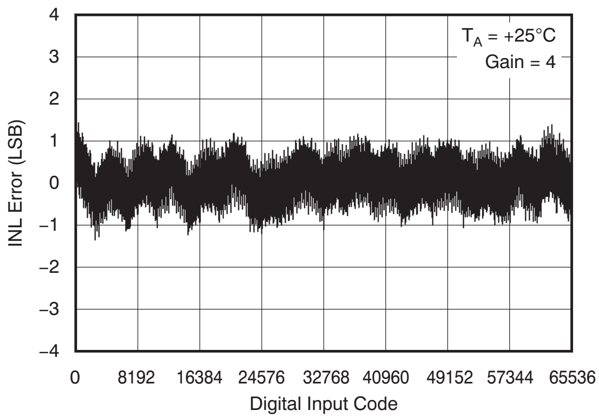


Figure 8.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

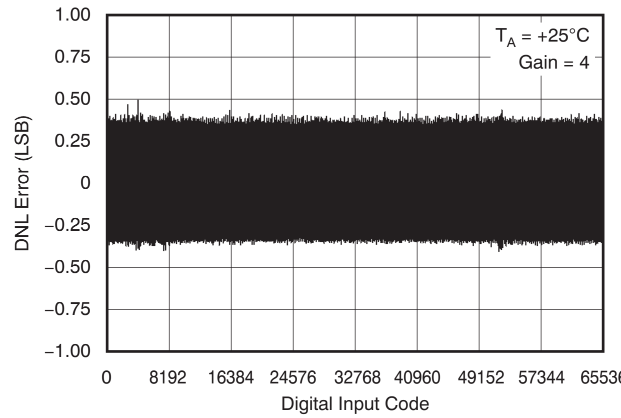


Figure 9.

TYPICAL CHARACTERISTICS: Dual-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +16.5V, AV_{SS} = –16.5V, and gain = 6, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

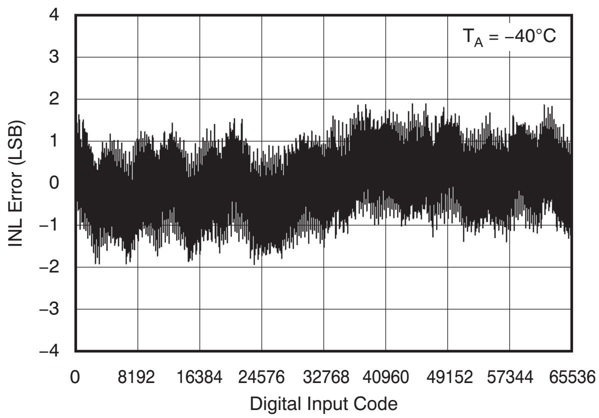


Figure 10.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

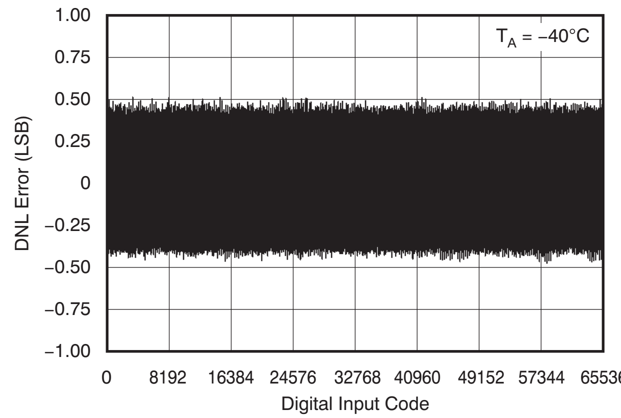


Figure 11.

LINEARITY ERROR vs DIGITAL INPUT CODE

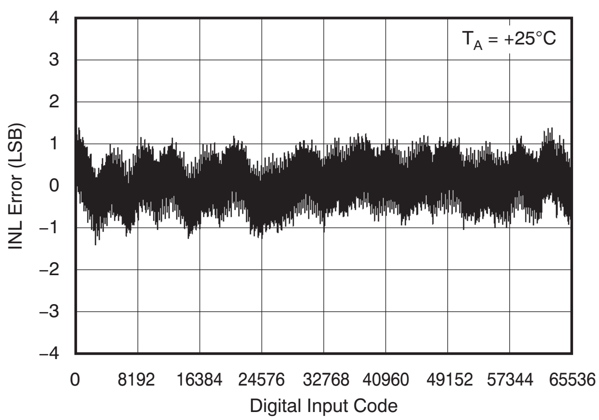


Figure 12.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

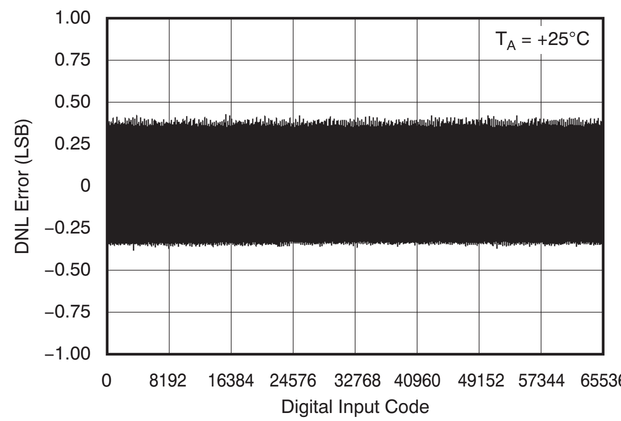


Figure 13.

LINEARITY ERROR vs DIGITAL INPUT CODE

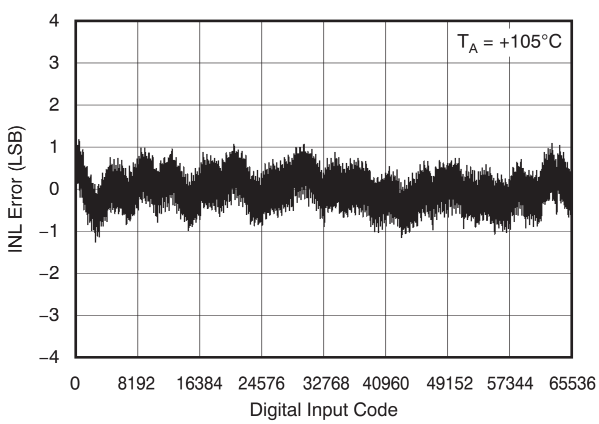


Figure 14.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

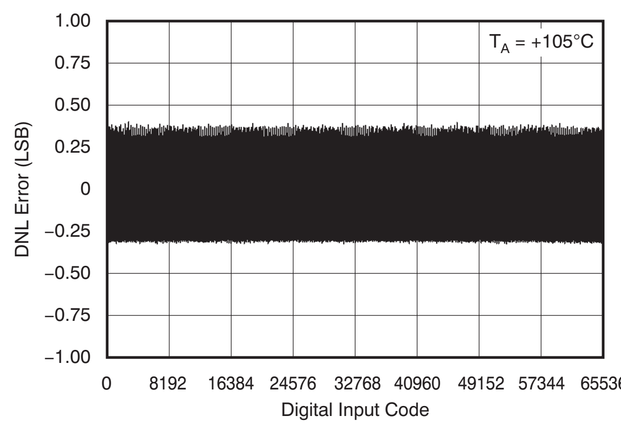


Figure 15.

TYPICAL CHARACTERISTICS: Dual-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +16.5V, AV_{SS} = –16.5V, and gain = 6, unless otherwise noted.

LINEARITY ERROR vs TEMPERATURE

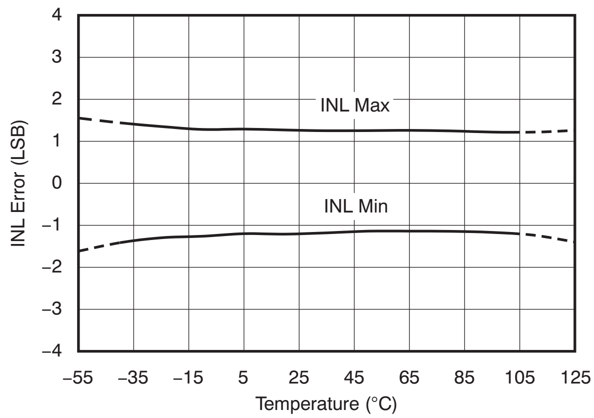


Figure 16.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

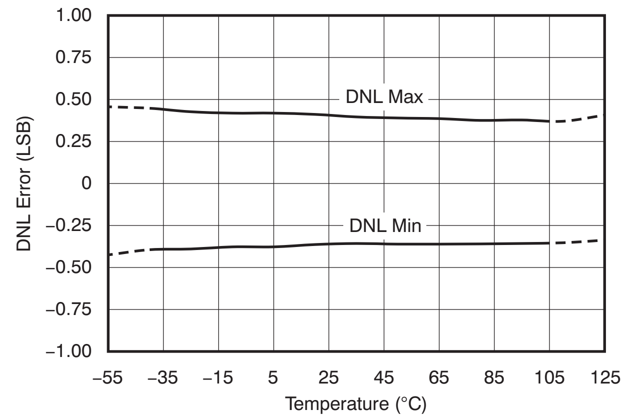


Figure 17.

LINEARITY ERROR vs TEMPERATURE

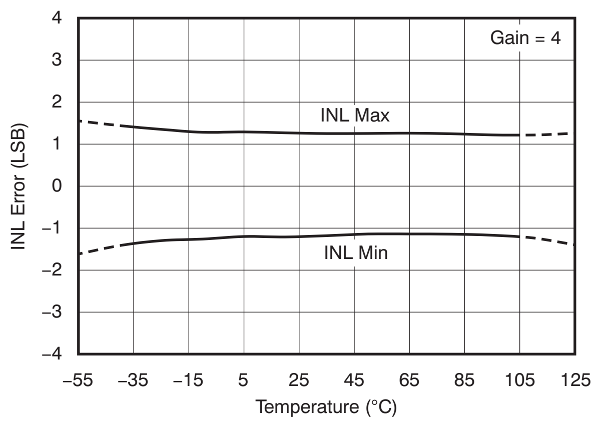


Figure 18.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

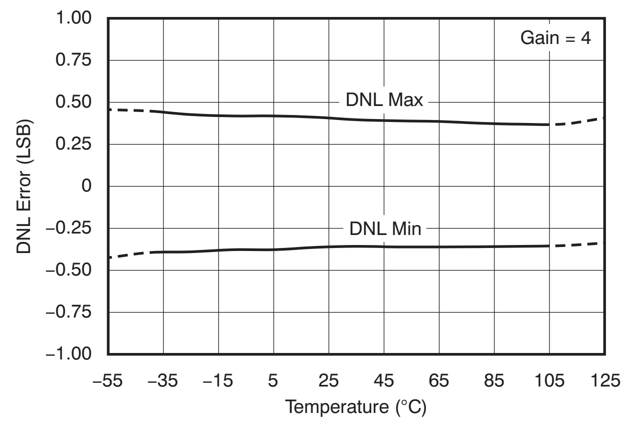


Figure 19.

BIPOLAR ZERO ERROR vs TEMPERATURE

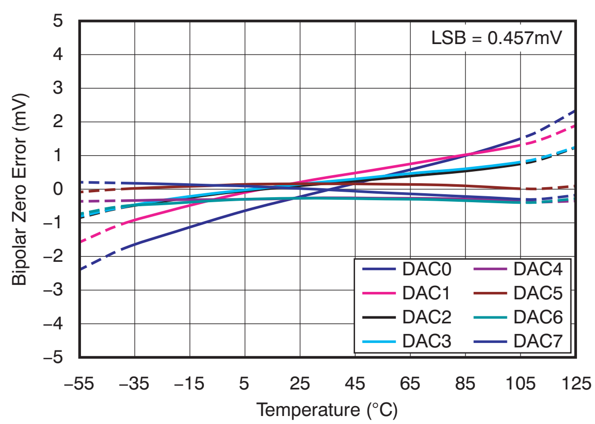


Figure 20.

BIPOLAR ZERO ERROR vs TEMPERATURE

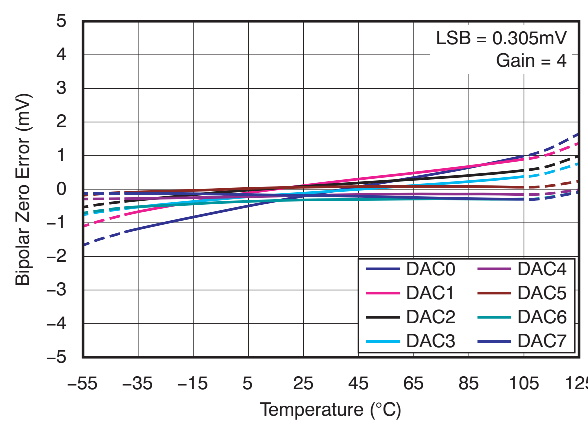


Figure 21.

TYPICAL CHARACTERISTICS: Dual-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +16.5V, AV_{SS} = –16.5V, and gain = 6, unless otherwise noted.

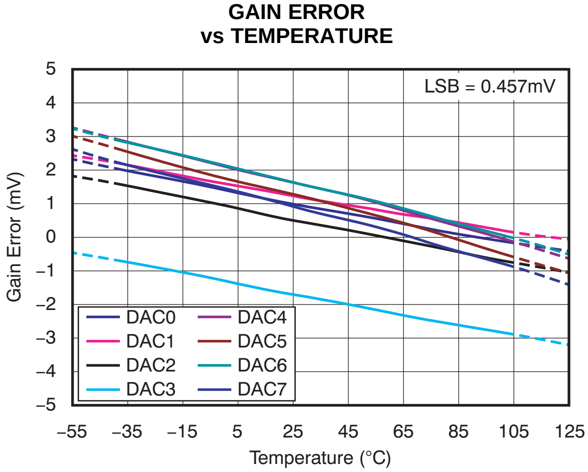


Figure 22.

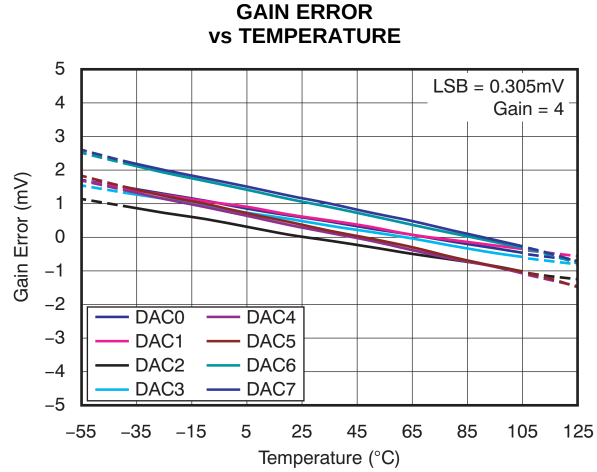


Figure 23.

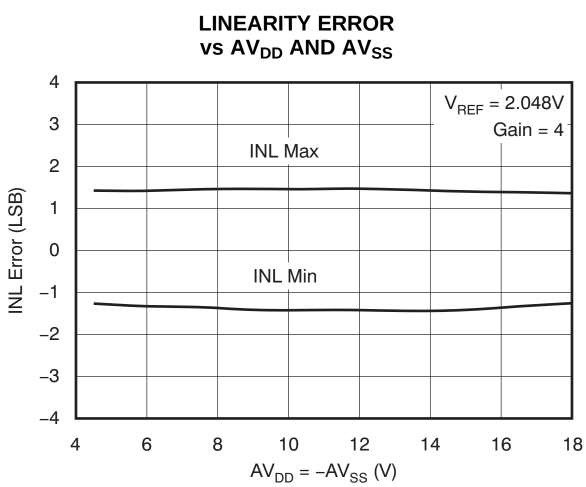


Figure 24.

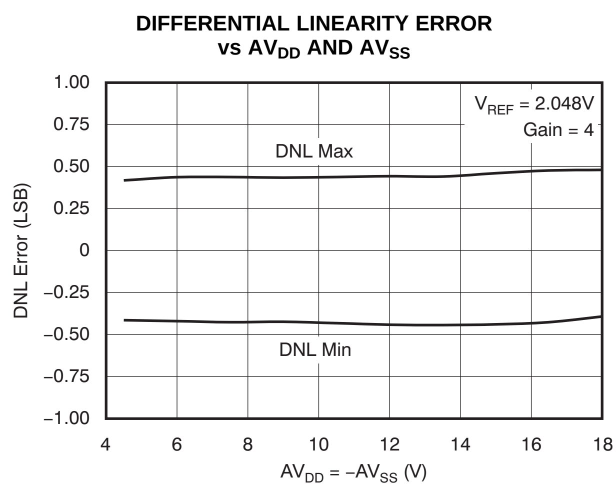


Figure 25.

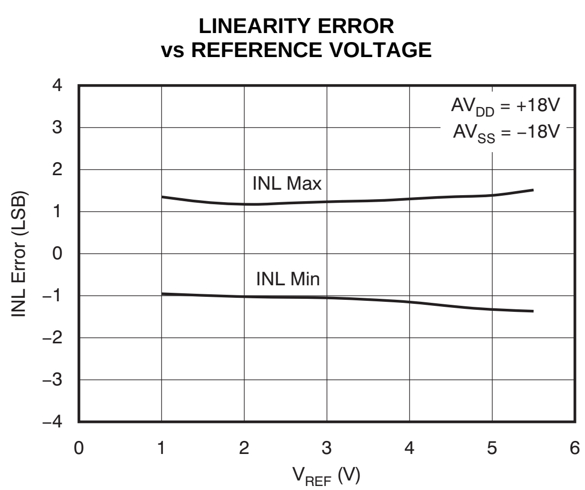


Figure 26.

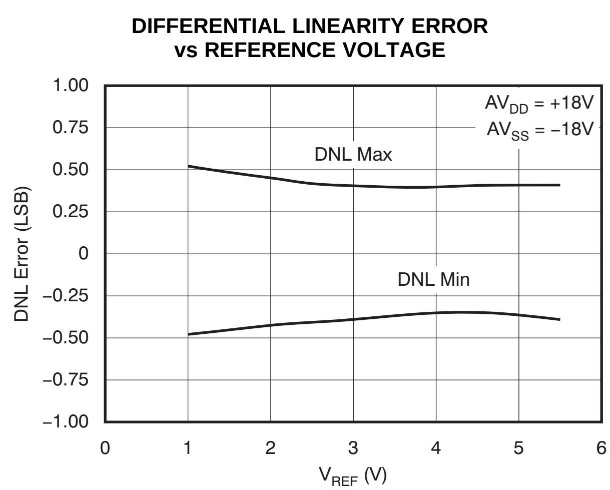


Figure 27.

TYPICAL CHARACTERISTICS: Dual-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +16.5V, AV_{SS} = –16.5V, and gain = 6, unless otherwise noted.

BIPOLAR ZERO ERROR vs AV_{DD} AND AV_{SS}

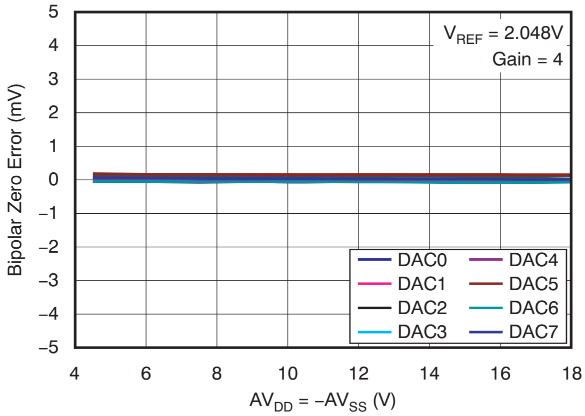


Figure 28.

GAIN ERROR vs AV_{DD} AND AV_{SS}

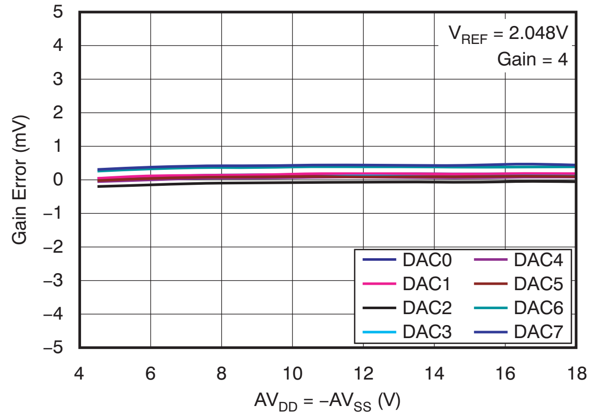


Figure 29.

BIPOLAR ZERO ERROR vs REFERENCE VOLTAGE

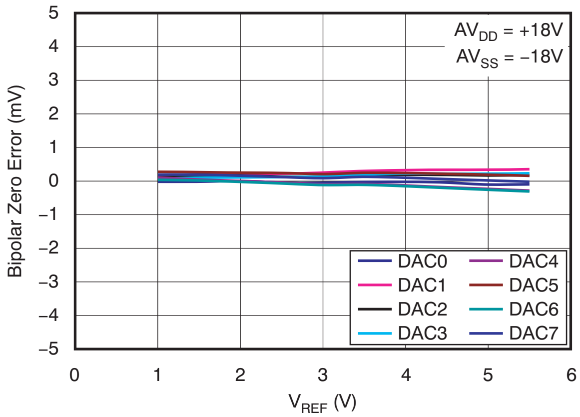


Figure 30.

BIPOLAR ZERO ERROR vs REFERENCE VOLTAGE

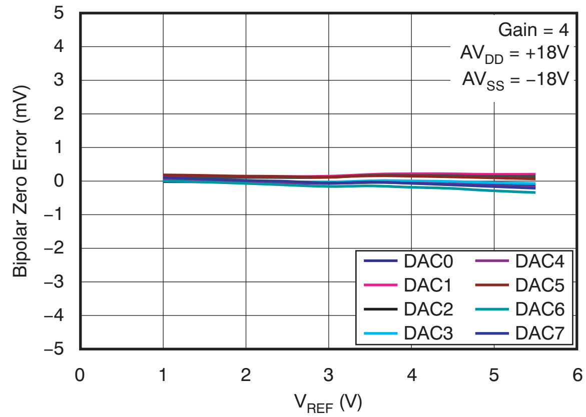


Figure 31.

GAIN ERROR vs REFERENCE VOLTAGE

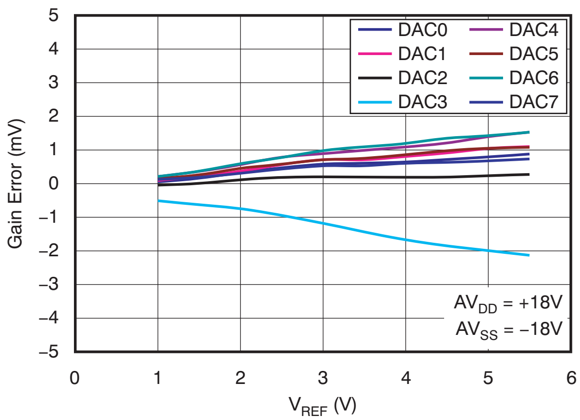


Figure 32.

GAIN ERROR vs REFERENCE VOLTAGE

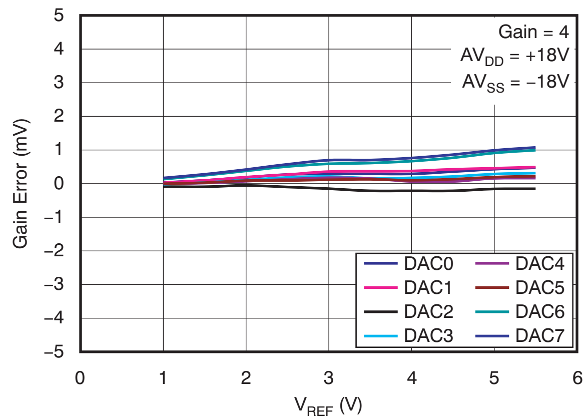


Figure 33.

TYPICAL CHARACTERISTICS: Dual-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +16.5V, AV_{SS} = –16.5V, and gain = 6, unless otherwise noted.

QUIESCENT CURRENTS vs TEMPERATURE

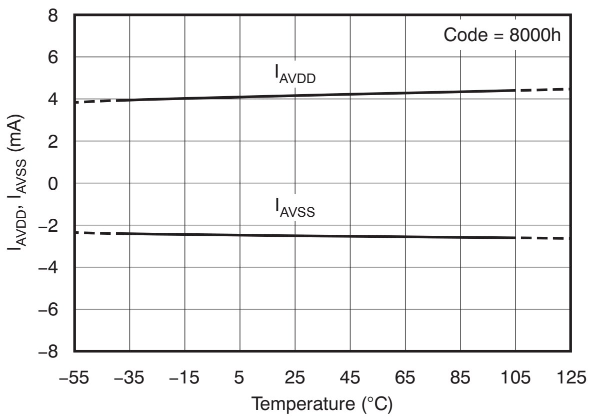


Figure 34.

QUIESCENT CURRENTS vs DIGITAL INPUT CODE

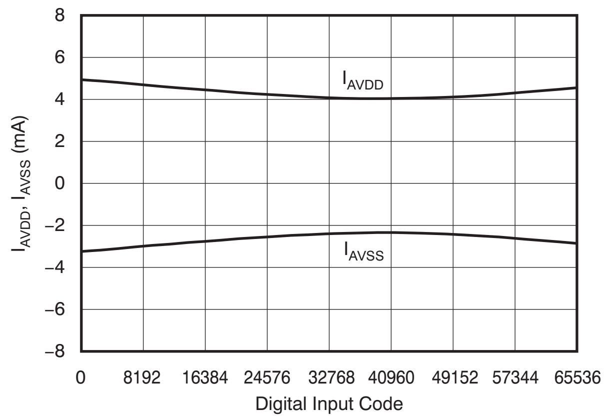


Figure 35.

QUIESCENT CURRENTS vs REFERENCE VOLTAGE

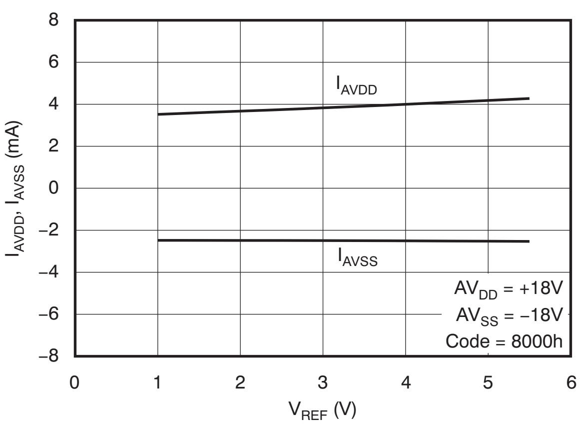


Figure 36.

DELTA OUTPUT VOLTAGE vs SOURCE/SINK CURRENTS

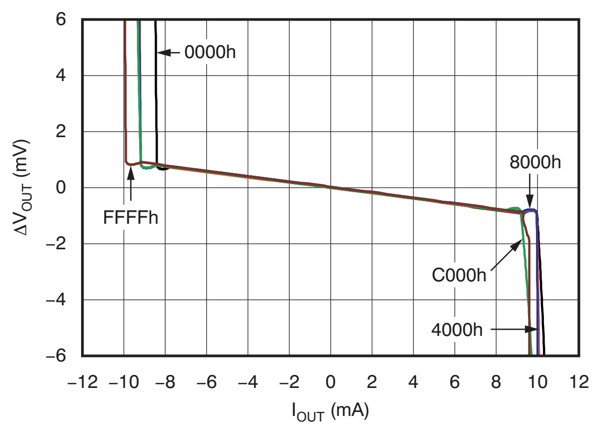


Figure 37.

SETTLING TIME –15V TO +15V TRANSITION

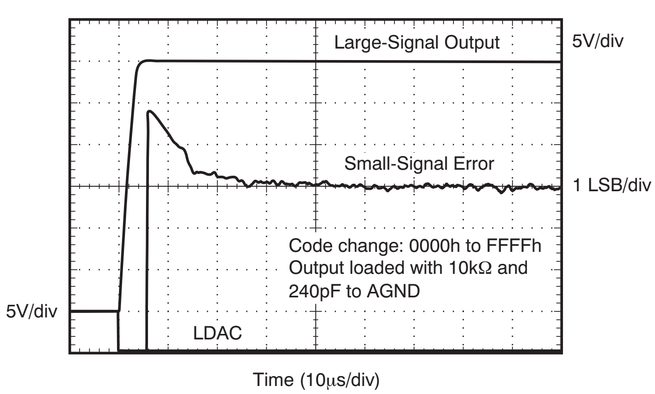


Figure 38.

SETTLING TIME +15V TO –15V TRANSITION

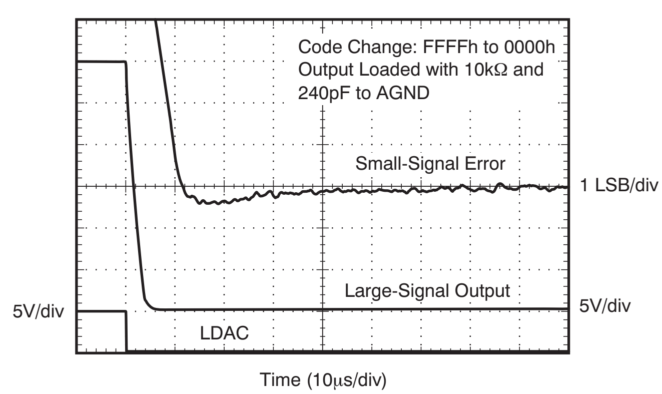


Figure 39.

TYPICAL CHARACTERISTICS: Dual-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +16.5V, AV_{SS} = –16.5V, and gain = 6, unless otherwise noted.

SETTLING TIME
1/4 TO 3/4 FULL-SCALE TRANSITION

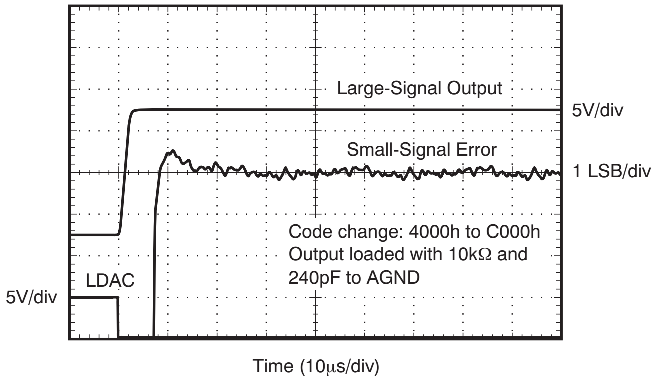


Figure 40.

SETTLING TIME
3/4 TO 1/4 FULL-SCALE TRANSITION

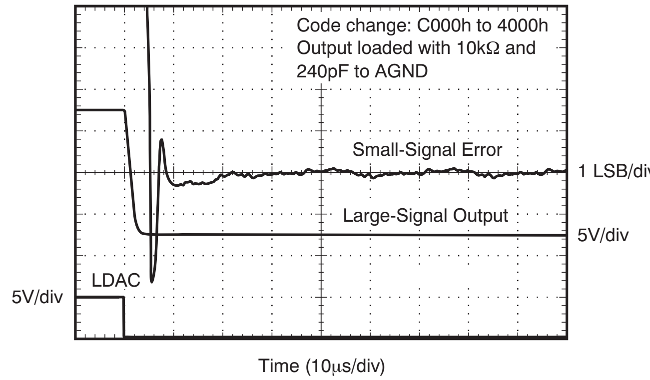


Figure 41.

MAJOR CARRY GLITCH

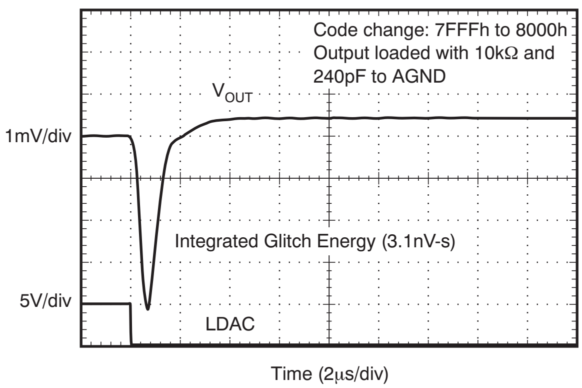


Figure 42.

MAJOR CARRY GLITCH

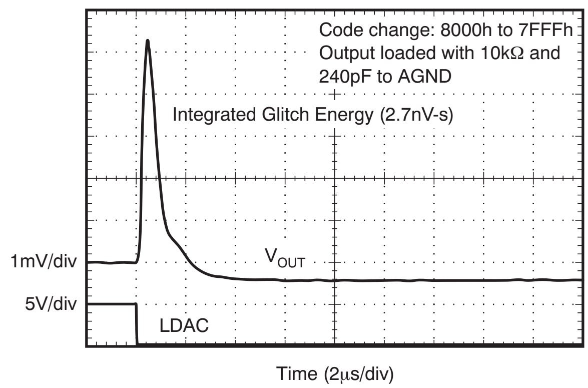


Figure 43.

0.1Hz TO 10Hz NOISE
FOR MIDSCALE CODE

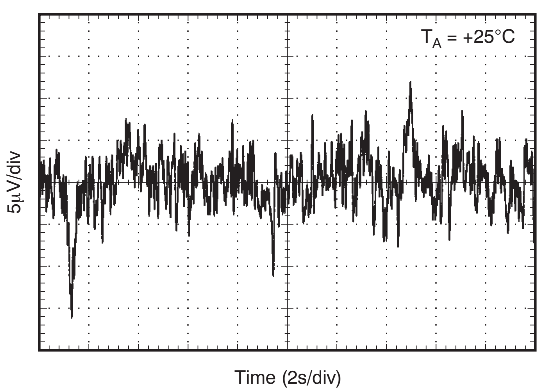


Figure 44.

0.1Hz TO 10Hz NOISE
FOR MIDSCALE CODE

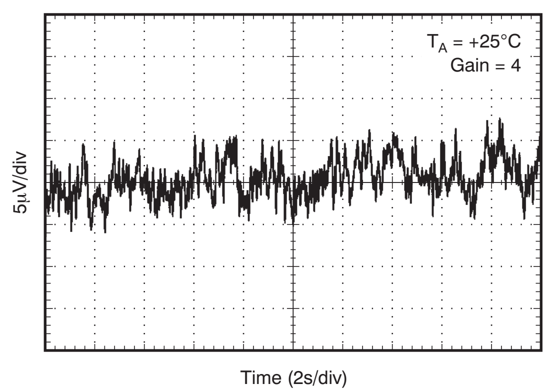


Figure 45.

TYPICAL CHARACTERISTICS: Dual-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +16.5V, AV_{SS} = –16.5V, and gain = 6, unless otherwise noted.

OUTPUT NOISE SPECTRAL DENSITY vs FREQUENCY

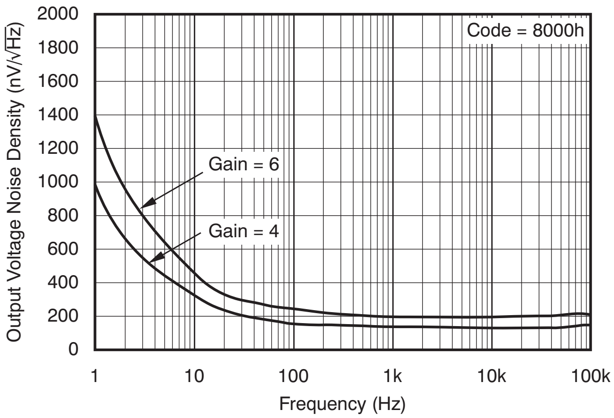


Figure 46.

IOV$_{DD}$ SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

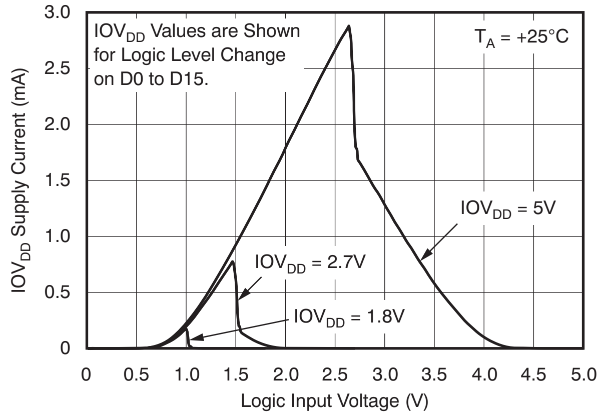


Figure 47.

BIPOLAR ZERO ERROR PRODUCTION DISTRIBUTION

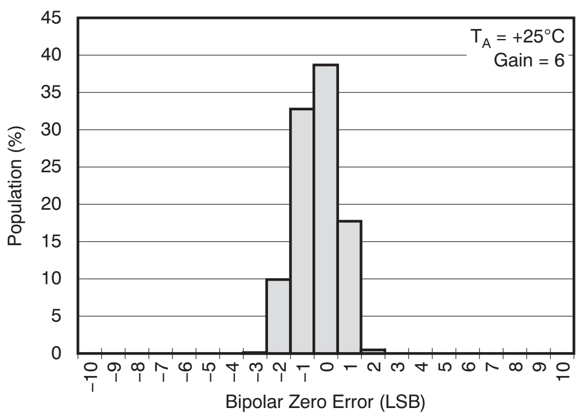


Figure 48.

BIPOLAR ZERO ERROR PRODUCTION DISTRIBUTION

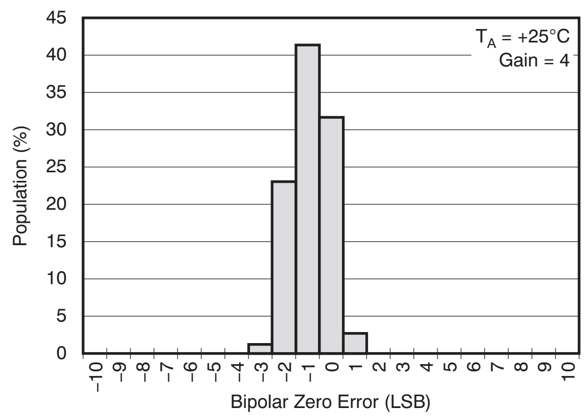


Figure 49.

GAIN ERROR PRODUCTION DISTRIBUTION

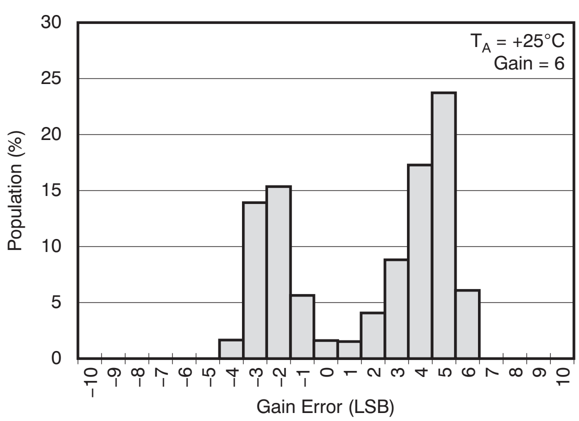


Figure 50.

GAIN ERROR PRODUCTION DISTRIBUTION

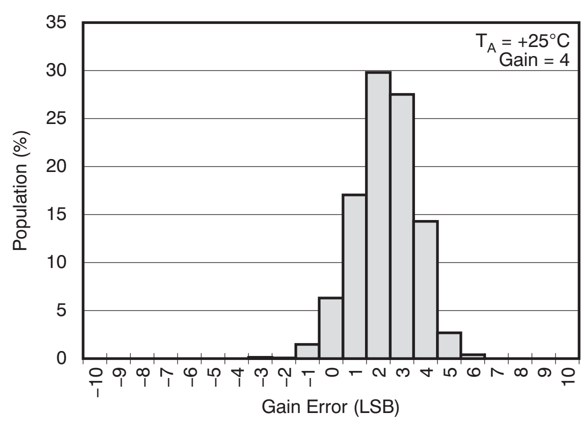


Figure 51.

TYPICAL CHARACTERISTICS: Single-Supply

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +32V, and gain = 6, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

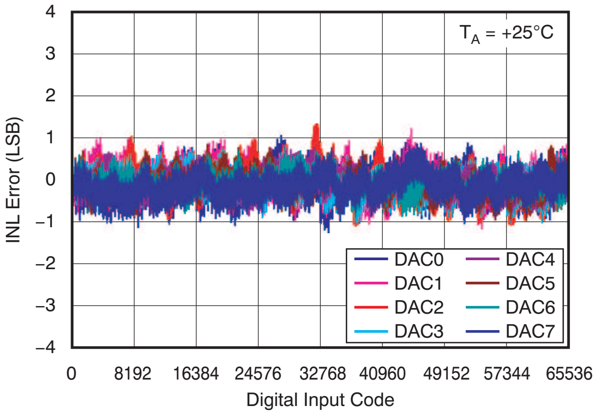


Figure 52.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

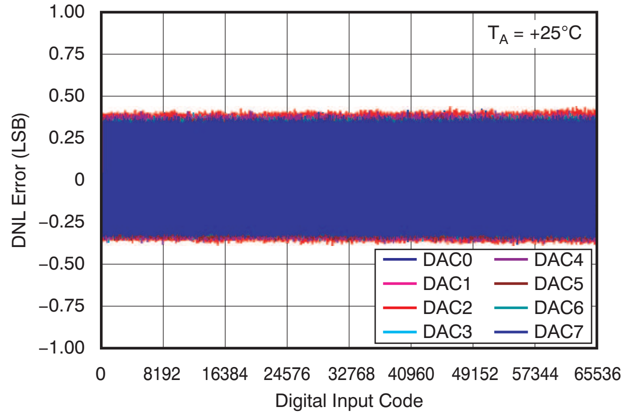


Figure 53.

LINEARITY ERROR vs DIGITAL INPUT CODE

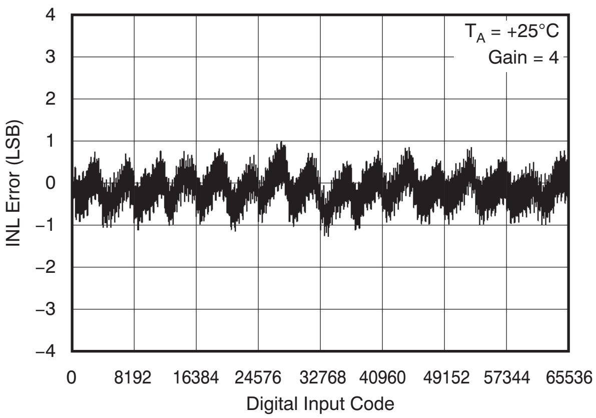


Figure 54.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

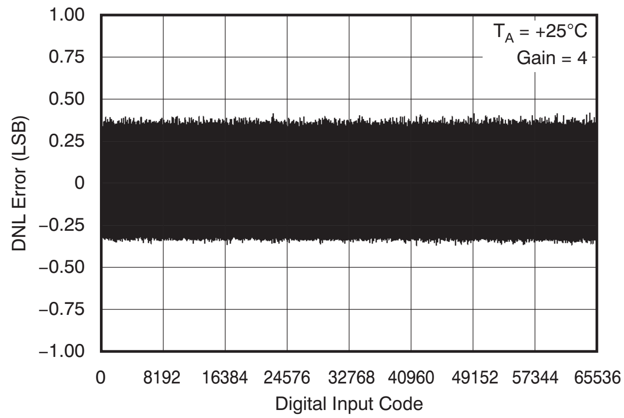


Figure 55.

TYPICAL CHARACTERISTICS: Single-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +32V, and gain = 6, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

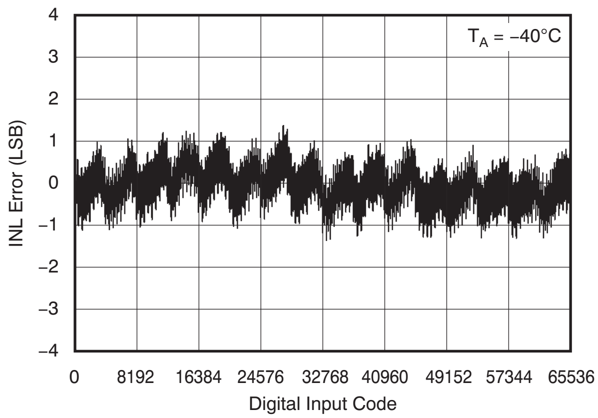


Figure 56.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

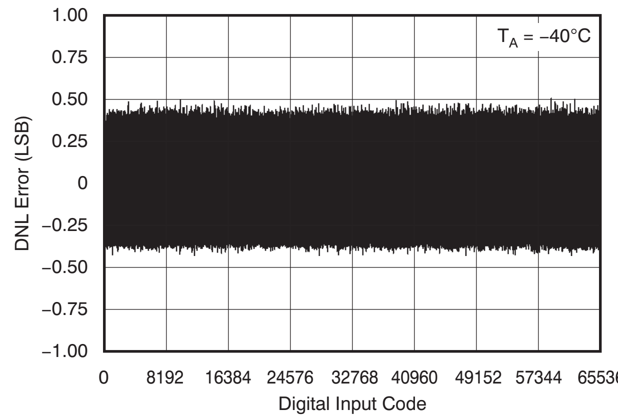


Figure 57.

LINEARITY ERROR vs DIGITAL INPUT CODE

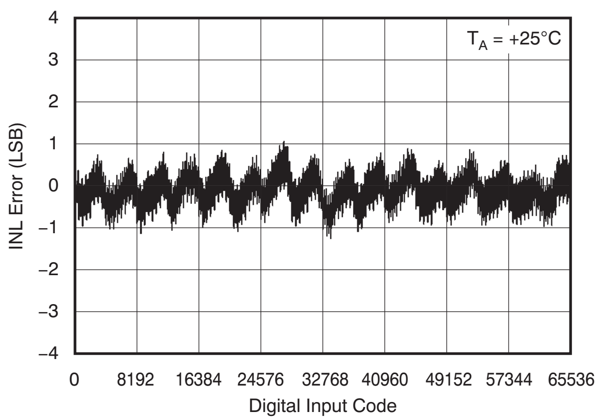


Figure 58.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

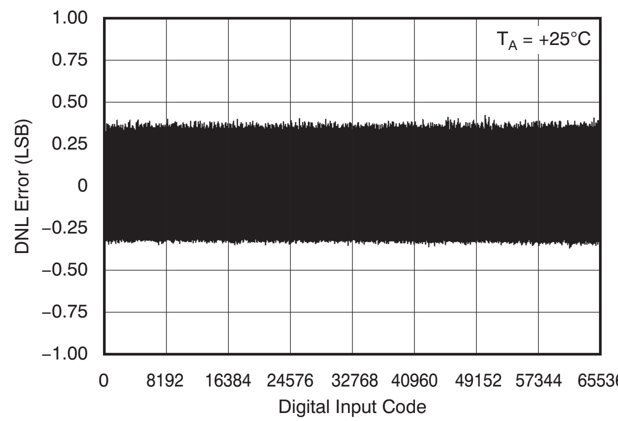


Figure 59.

LINEARITY ERROR vs DIGITAL INPUT CODE

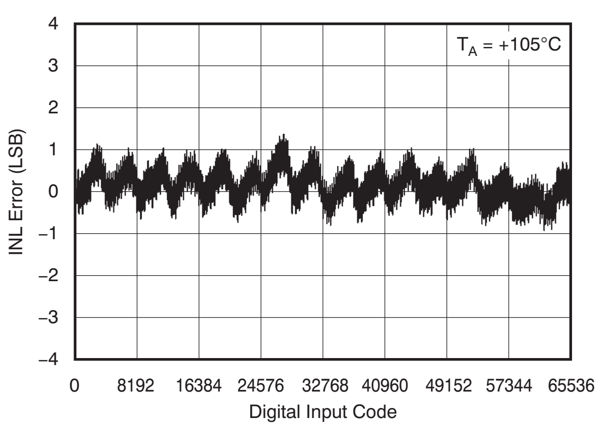


Figure 60.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

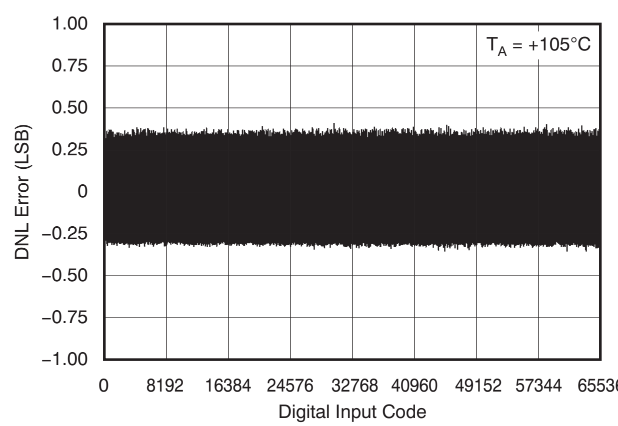


Figure 61.

TYPICAL CHARACTERISTICS: Single-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +32V, and gain = 6, unless otherwise noted.

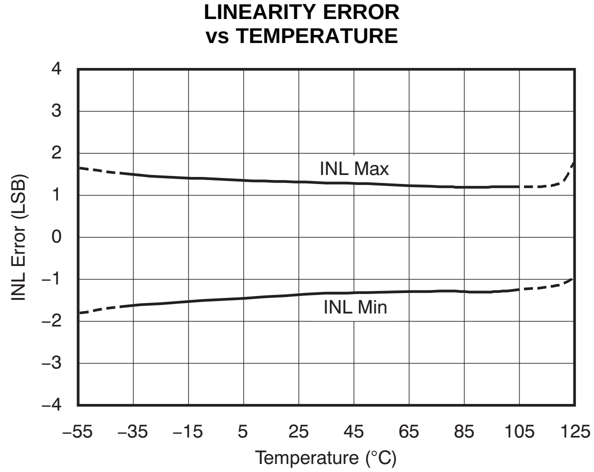


Figure 62.

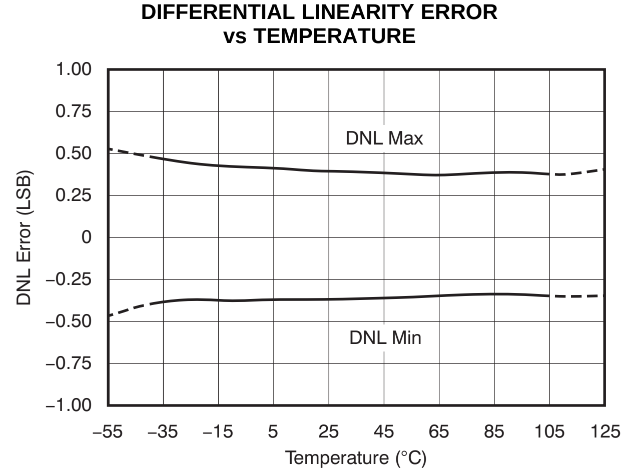


Figure 63.

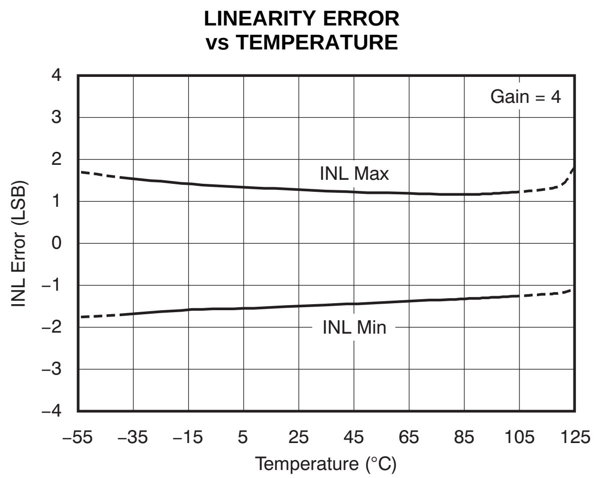


Figure 64.

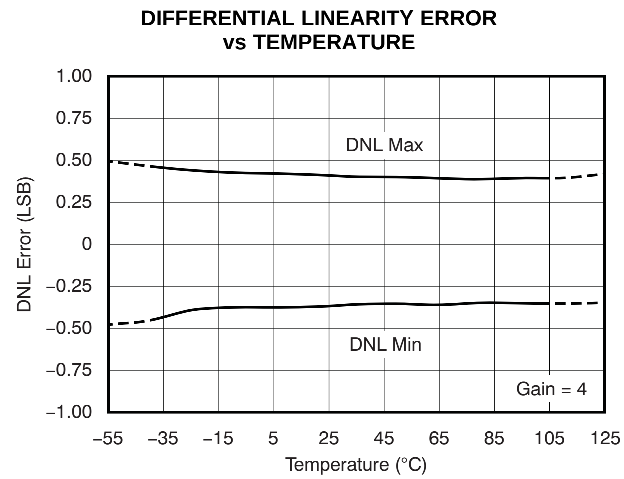


Figure 65.

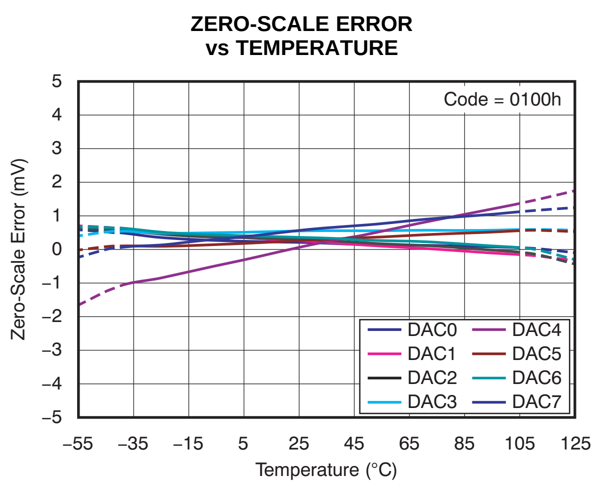


Figure 66.

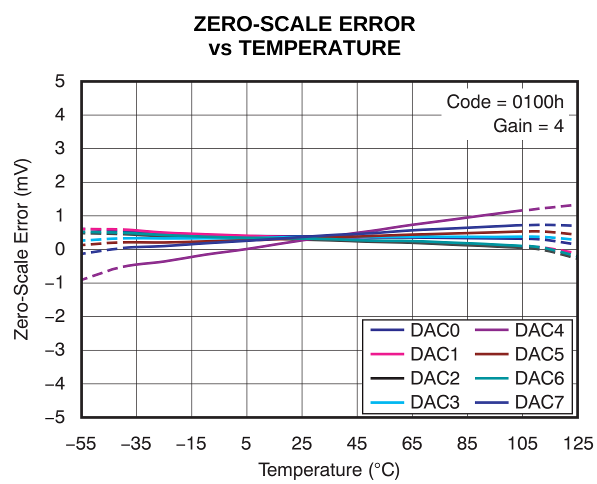


Figure 67.

TYPICAL CHARACTERISTICS: Single-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +32V, and gain = 6, unless otherwise noted.

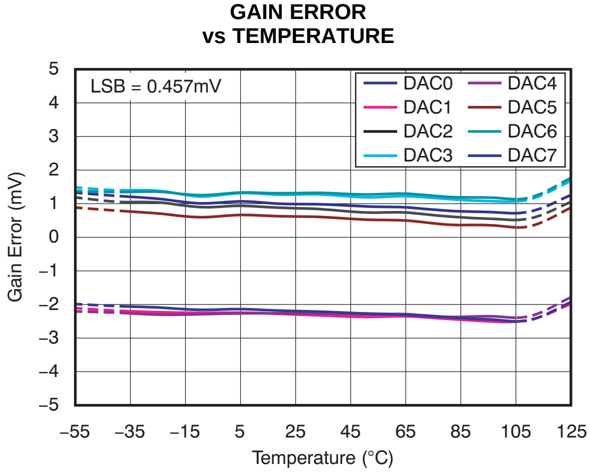


Figure 68.

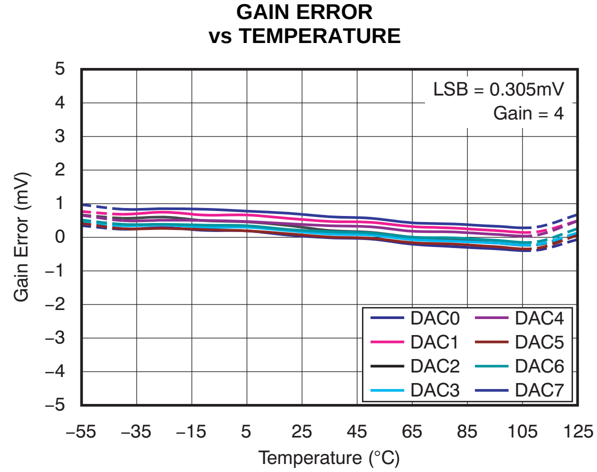


Figure 69.

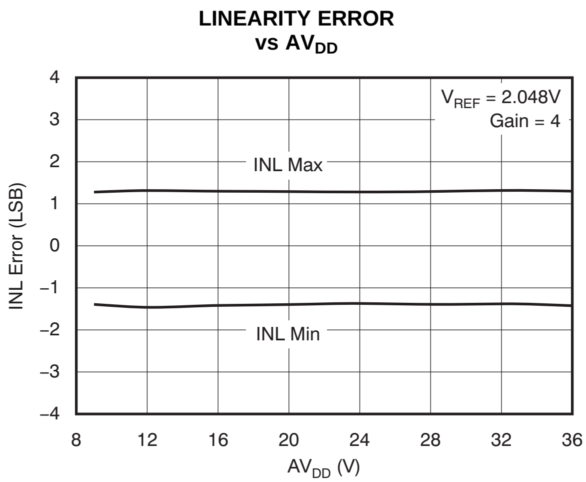


Figure 70.

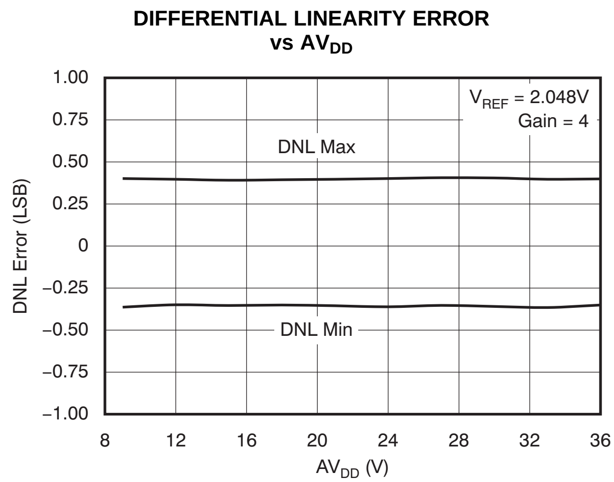


Figure 71.

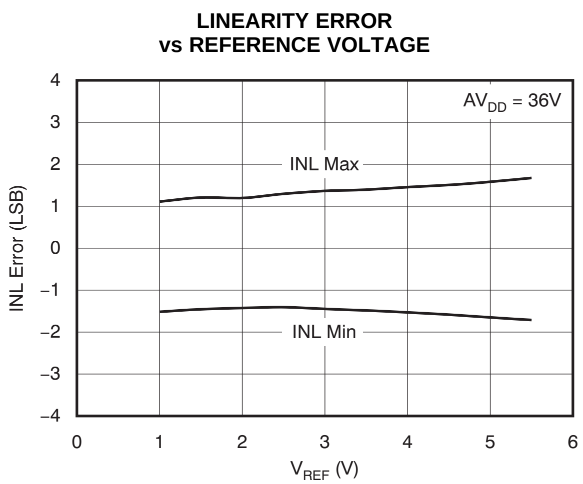


Figure 72.

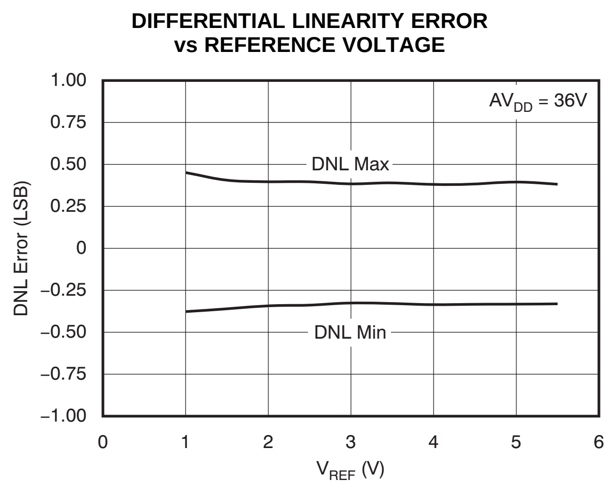


Figure 73.

TYPICAL CHARACTERISTICS: Single-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +32V, and gain = 6, unless otherwise noted.

ZERO-SCALE ERROR vs AV_{DD}

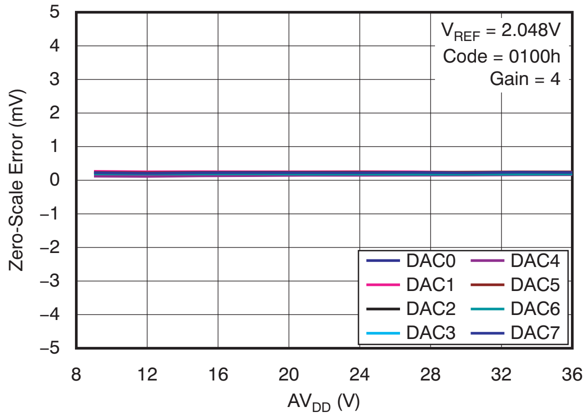


Figure 74.

GAIN ERROR vs AV_{DD}

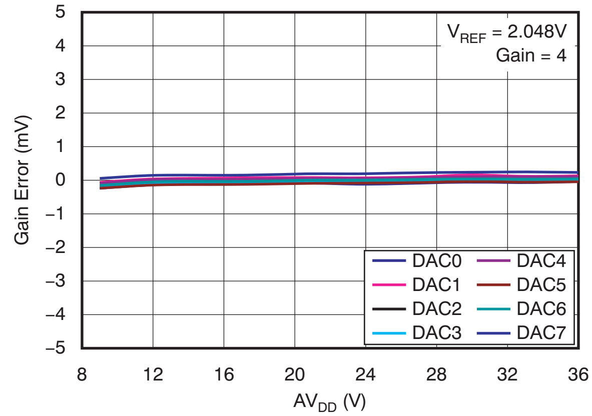


Figure 75.

ZERO-SCALE ERROR vs REFERENCE VOLTAGE

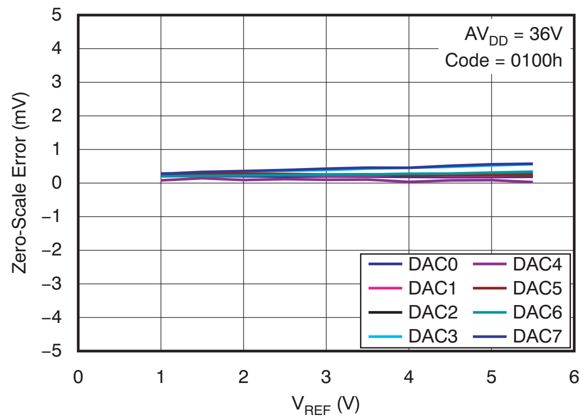


Figure 76.

ZERO-SCALE ERROR vs REFERENCE VOLTAGE

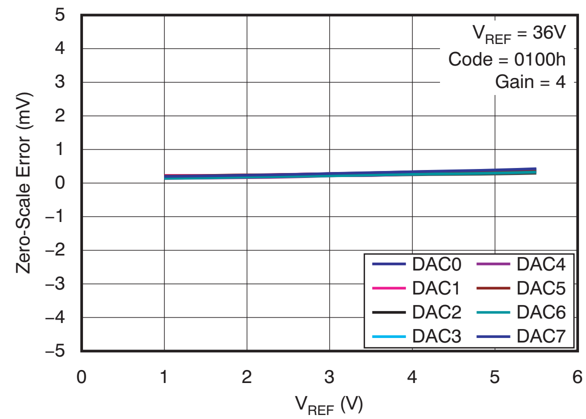


Figure 77.

GAIN ERROR vs REFERENCE VOLTAGE

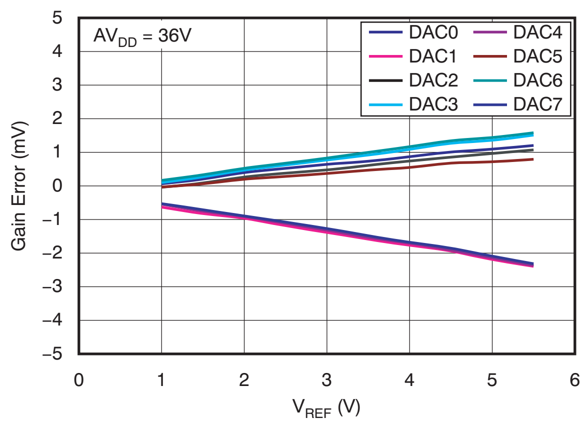


Figure 78.

GAIN ERROR vs REFERENCE VOLTAGE

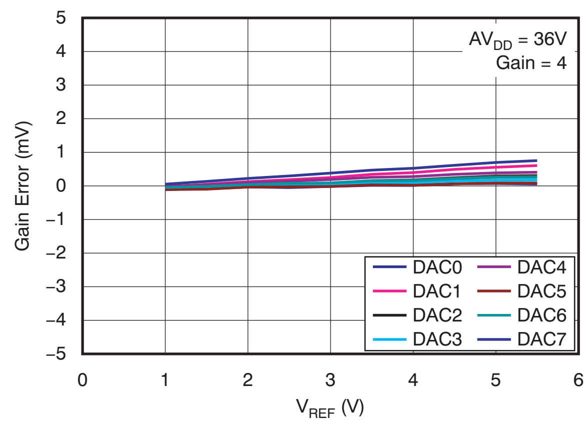


Figure 79.

TYPICAL CHARACTERISTICS: Single-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +32V, and gain = 6, unless otherwise noted.

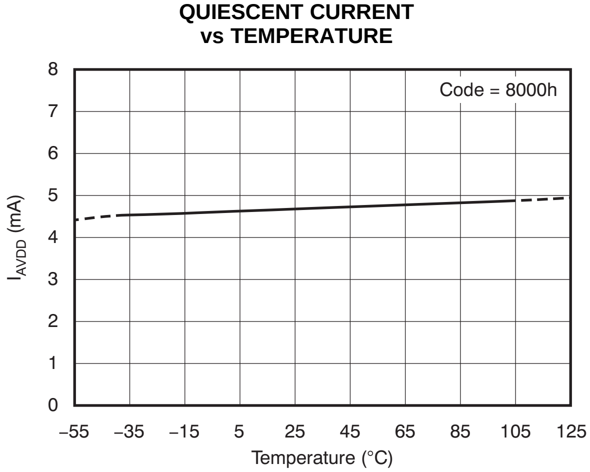


Figure 80.

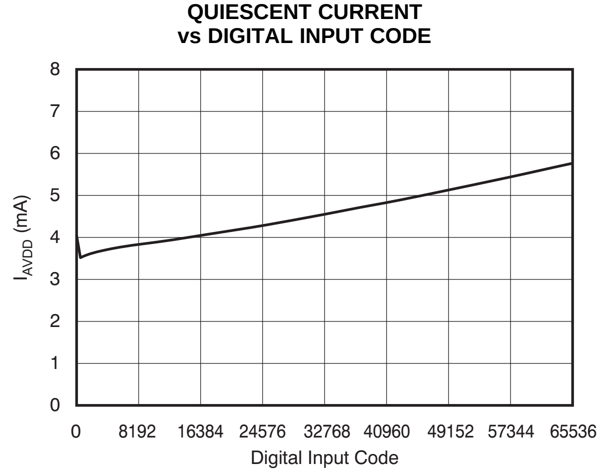


Figure 81.

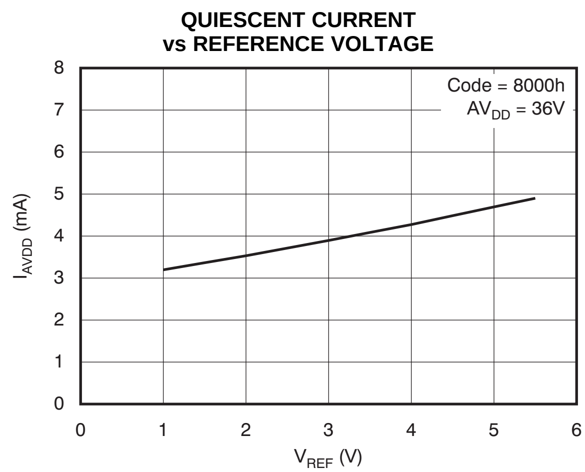


Figure 82.

TYPICAL CHARACTERISTICS: Single-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +32V, and gain = 6, unless otherwise noted.

SETTLING TIME
0V TO 30V TRANSITION

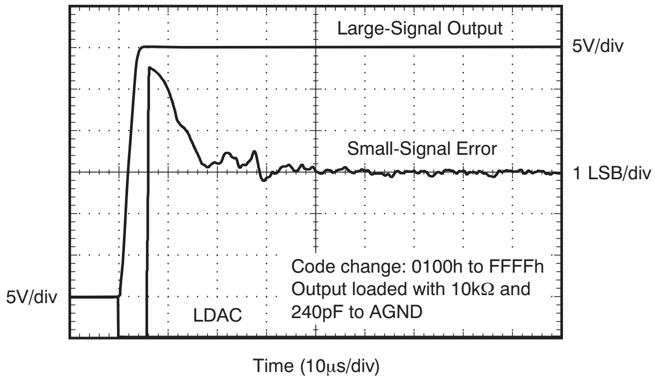


Figure 83.

SETTLING TIME
30V TO 0V TRANSITION

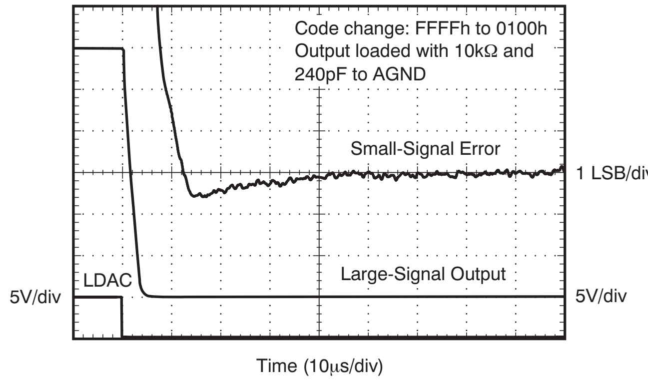


Figure 84.

SETTLING TIME
1/4 TO 3/4 FULL-SCALE TRANSITION

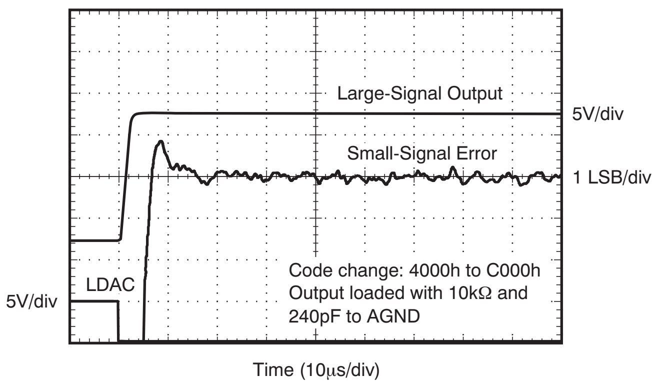


Figure 85.

SETTLING TIME
3/4 TO 1/4 FULL-SCALE TRANSITION

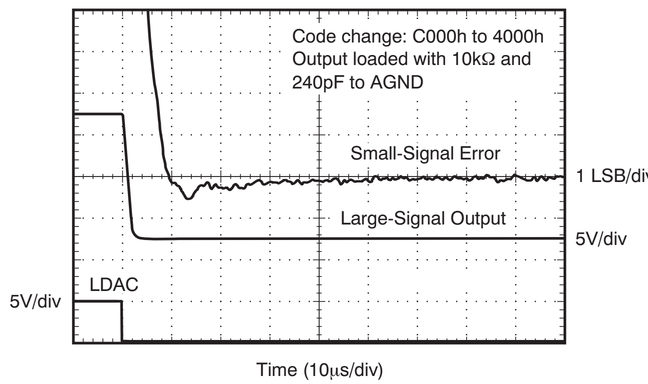


Figure 86.

MAJOR CARRY GLITCH

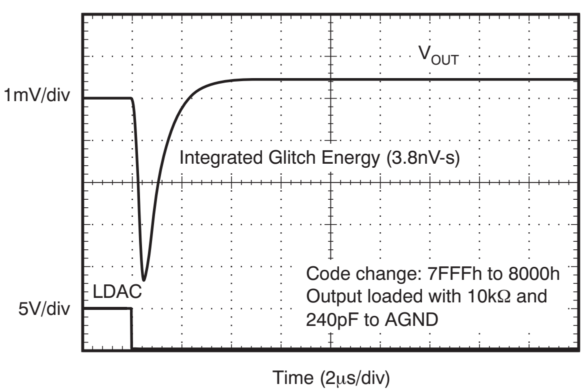


Figure 87.

MAJOR CARRY GLITCH

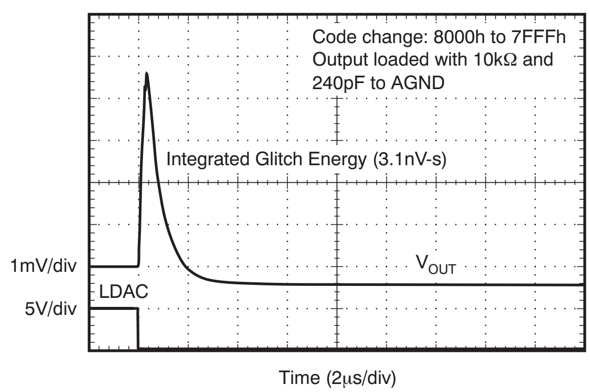


Figure 88.

TYPICAL CHARACTERISTICS: Single-Supply (continued)

At T_A = +25°C, V_{REF} = +5V, AV_{DD} = +32V, and gain = 6, unless otherwise noted.

OUTPUT VOLTAGE vs SINK CURRENT CAPABILITY

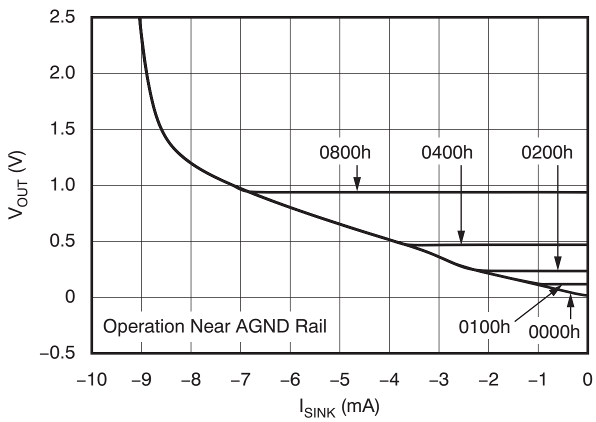


Figure 89.

OUTPUT VOLTAGE vs SOURCE CURRENT CAPABILITY

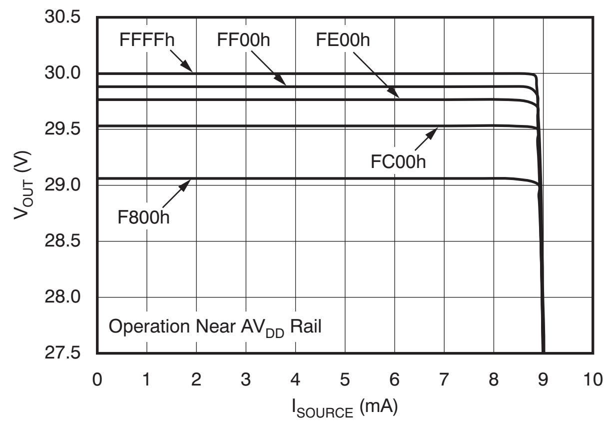


Figure 90.

ZERO-SCALE ERROR PRODUCTION DISTRIBUTION

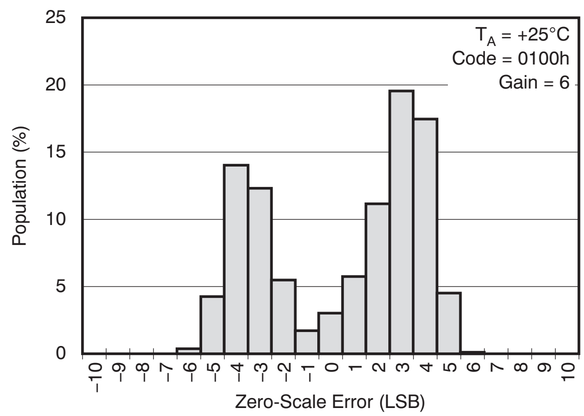


Figure 91.

ZERO-SCALE ERROR PRODUCTION DISTRIBUTION

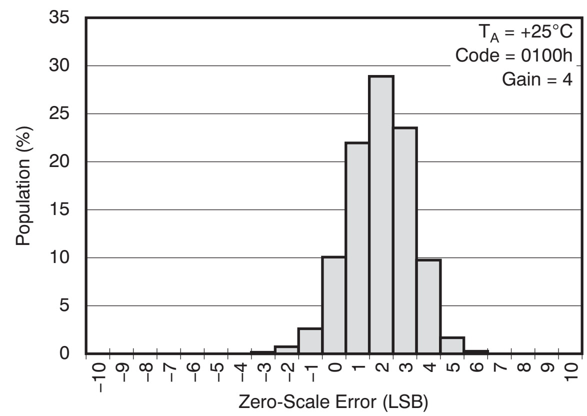


Figure 92.

GAIN ERROR PRODUCTION DISTRIBUTION

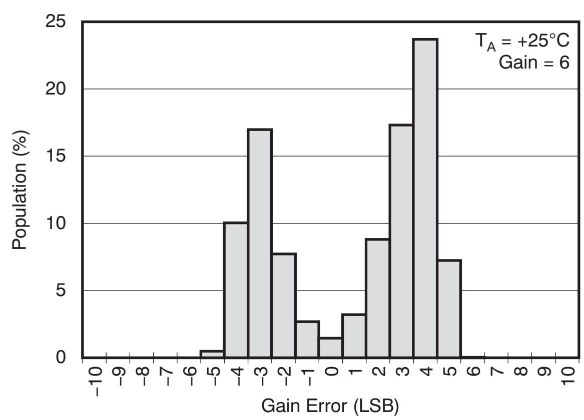


Figure 93.

GAIN ERROR PRODUCTION DISTRIBUTION

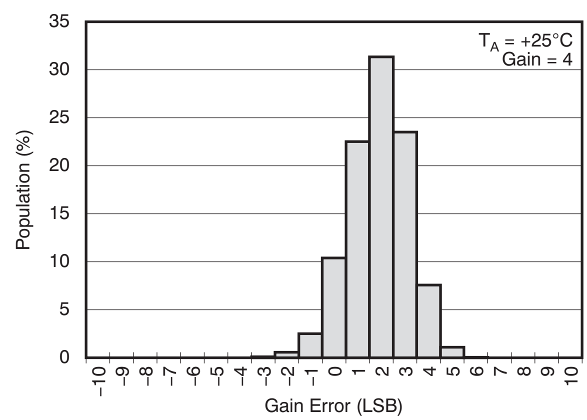


Figure 94.

THEORY OF OPERATION

GENERAL DESCRIPTION

The DAC8728 contains eight DAC channels and eight output amplifiers in a single package. Each channel consists of a resistor-string DAC followed by an output buffer amplifier. The resistor-string section is simply a string of resistors, each with a value of R, from REF to AGND, as shown in Figure 95. This type of architecture provides DAC monotonicity. The 16-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed into the output amplifier. The output amplifier multiplies the DAC output voltage by a gain of six or four. The output span is 9V with a 1.5V reference, 18V with a 3V reference, and 30V for a 5V reference when using dual power supplies of ±16.5V and a gain of 6.

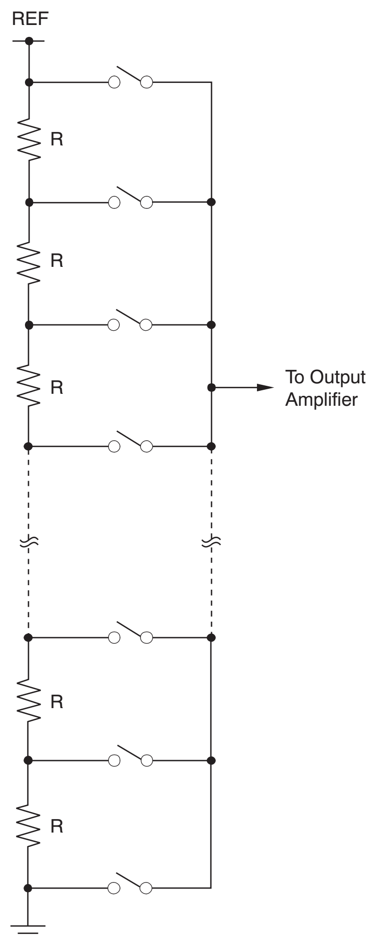


Figure 95. Resistor String

CHANNEL GROUPS

The eight DAC channels and two Offset DACs are arranged into two groups (A and B) with four channels and one Offset DAC per group. Group A consists of DAC-0, DAC-1, DAC-2, DAC-3, and Offset DAC-A. Group B consists of DAC-4, DAC-5, DAC-6, DAC-7, and Offset DAC-B. Group A derives its reference voltage from REF-A, and Group B derives its reference voltage from REF-B.

USER-CALIBRATION FOR ZERO ERROR AND GAIN ERROR

The DAC8728 implements a digital user-calibration function that allows for trimming gain and zero errors on the entire signal chain. This function can eliminate the need for external adjustment circuits. Each DAC channel has a Zero Register and Gain Register. Using the correction engine, the data from the Input Data Register are operated on by a digital adder and multiplier controlled by the contents of Zero and Gain registers, respectively. The calibrated DAC data are then stored in the DAC Data Register where they are finally transferred into the DAC latch and set the DAC output. Each time the data are written to the Input Data Register (or to the Gain or Zero registers), the data in the Input Data Register are corrected, and the results automatically transferred to DAC Data Register.

The range of the gain adjustment coefficient is 0.5 to 1.5. The range of the zero adjustment is –32768 LSB to +32767 LSB, or ±50% of full scale.

There is only one correction engine in the DAC8728, which is shared among all channels. Each channel has an individual busy flag (BF-x) in the Busy Flag register. When the channel is accessed, the respective BF-x bit is set if either the Input Data Register, Zero Register, or Gain Register are written to. When the DAC data are adjusted by the correction engine and transferred into DAC Data Register, the BF-x bit is cleared. It takes approximately 500ns per channel for the correction to complete.

The correction engine calibrates the individual channels according to priority. DAC-0 has the highest priority, while DAC-7 has the lowest. Correction of lower-priority channels is not performed until correction of higher-priority channels completes. Repeatedly accessing higher-priority channels may block the correction of lower-priority channels. Table 1 lists the correction engine channel priority.

Table 1. Correction Engine Priority

CHANNEL	PRIORITY
DAC-0	1 (highest)
DAC-1	2
DAC-2	3
DAC-3	4
DAC-4	5
DAC-5	6
DAC-6	7
DAC-7	8 (lowest)

The device also provides a global busy flag (GBF) and a logic output from the $\overline{\text{BUSY}}$ pin to indicate the correction engine status. When the correction engine is running, the GBF bit is set ('1'), and the $\overline{\text{BUSY}}$ pin is low. When the engine stops, GBF is cleared ('0'), and the $\overline{\text{BUSY}}$ pin goes high (or Hi-Z if no pull-up resistor is used). Note that when the correction engine is disabled, the GBF bit is always cleared, and the $\overline{\text{BUSY}}$ pin is always in a Hi-Z state.

To avoid any potential conflicts caused by the correction process, the input data must be written properly. Either one of the following approaches can be used to update the DAC Input Data Register, Zero Register, or Gain Register:

1. Writing to any channel when the $\overline{\text{BUSY}}$ pin is high or when the GBF bit = '0'.
2. Writing to an individual channel when the corresponding BF-x bit = '0'.
3. Tracking the correction time. It takes approximately 500ns to correct one channel for each input data, zero or gain change.

The individual channel can be rewritten only if the corrections are completed for that channel and for all other channels that have higher priority. For example, if DAC-0, DAC-1, and DAC-2 are written to first, and then DAC-1 is written to again, the second writing to DAC-1 is not permitted until the correction of the first DAC-1 writing is complete (that is, approximately 1000ns after writing to DAC-0, or 500ns after the first writing to DAC-1). However, if writing to DAC-0, DAC-1, DAC-2, and then DAC-2 again, the second writing of DAC-2 is prohibited until the correction for the first writing to DAC-2 is complete (that is, approximately 1500ns after writing to DAC-0, or 500ns after the first writing to DAC-2).

If the user-calibration function is not needed, the correction engine can be turned off to speed up the device. Setting the SCE bit in the Configuration Register to '0' turns off the correction engine. Setting SCE to '1' enables the correction engine. When SCE = '0' (default), the data are directly transferred to the DAC Data Register. In this case, writing to the Gain Register or Zero Register updates the Gain and Zero registers but does not start a math engine calculation. Reading these registers returns the written values.

ANALOG OUTPUTS (V_{OUT}-0 to V_{OUT}-7, with reference to the ground of REF-x)

When the correction engine is off (SCE = '0'):

$$V_{OUT} = V_{REF} \times Gain \times \left(\frac{INPUT\_CODE}{65536}\right) - V_{REF} \times (Gain - 1) \times \left(\frac{OFFSETDAC\_CODE}{65536}\right) \quad (1)$$

When the correction engine is on (SCE = '1'):

$$V_{OUT} = V_{REF} \times Gain \times \left(\frac{DAC\_DATA\_CODE}{65536}\right) - V_{REF} \times (Gain - 1) \times \left(\frac{OFFSETDAC\_CODE}{65536}\right) \quad (2)$$

Where:

$$DAC\_DATA\_CODE = \left(\frac{INPUT\_CODE \times (USER\_GAIN + 2^{15})}{2^{16}}\right) + USER\_ZERO$$

Gain = the DAC gain defined by the GAIN bit in the Configuration Register.

INPUT_CODE = the data written into the Input Data Register.

OFFSETDAC_CODE = the data written into the Offset DAC Register.

USER_GAIN = the code of the Gain Register.

USER_ZERO = the code of the Zero Register.

For single-supply operation, the OFFSET-A pin must be connected to the AGND-A pin and the OFFSET-B pin must be connected to the AGND-B pin. Offset DAC-A and Offset DAC-B are in a power-down state.

For dual-supply operation, the OFFSET-A and OFFSET-B default code for a gain of 6 is 39322 with a ±10 LSB variation, depending on the linearity of the Offset DACs. The default code for a gain of 4 is 43691 with a ±10 LSB variation. The default code of OFFSET-A and OFFSET-B are independently factory trimmed for both gains of 6 and 4.

The power-on default value of the Gain Register is 32768, and the default value of the Zero Register is '0'. The DAC input registers are set to a default value of 0000h.

Note that the maximum output voltage must not be greater than (AV_{DD} – 0.5V) and the minimum output voltage must not be less than (AV_{SS} + 0.5V); otherwise, the output may be saturated.

INPUT DATA FORMAT

The $\overline{\text{USB}}$/BTC pin defines the input data format and the Offset DAC format. When this pin connects to DGND, the Input DAC data and Offset DAC data are straight binary, as shown in Table 2 and Table 4. When this pin is connected to IOV_{DD}, the Input DAC data and Offset DAC data are twos complement, as shown in Table 3 and Table 5.

Table 2. Bipolar Output vs Straight Binary Code Using Dual Power Supplies with Gain = 6

USB CODE	NOMINAL OUTPUT	DESCRIPTION
FFFFh	$+3 \times V_{REF} \times (32767/32768)$	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
8001h	$+3 \times V_{REF} \times (1/32768)$	+1 LSB
8000h	0	Zero
7FFFh	$-3 \times V_{REF} \times (1/32768)$	–1 LSB
••• •••	••• •••	••• •••
0000h	$-3 \times V_{REF} \times (32768/32768)$	–Full-Scale

Table 3. Bipolar Output vs Twos Complement Code Using Dual Power Supplies with Gain = 6

BTC CODE	NOMINAL OUTPUT	DESCRIPTION
7FFFh	$+3 \times V_{REF} \times (32767/32768)$	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
0001h	$+3 \times V_{REF} \times (1/32768)$	+1 LSB
0000h	0	Zero
FFFFh	$-3 \times V_{REF} \times (1/32768)$	–1 LSB
••• •••	••• •••	••• •••
8000h	$-3 \times V_{REF} \times (32768/32768)$	–Full-Scale

Table 4. Unipolar Output vs Straight Binary Code Using Single Power Supply with Gain = 6

USB CODE	NOMINAL OUTPUT	DESCRIPTION
FFFFh	$+6 \times V_{REF} \times (65535/65536)$	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
8001h	$+6 \times V_{REF} \times (32769/65536)$	Midscale + 1 LSB
8000h	$+6 \times V_{REF} \times (32768/65536)$	Midscale
7FFFh	$+6 \times V_{REF} \times (32767/65536)$	Midscale – 1 LSB
••• •••	••• •••	••• •••
0000h	0	0

Table 5. Unipolar Output vs Twos Complement Code Using Single Power Supply with Gain = 6

BTC CODE	NOMINAL OUTPUT	DESCRIPTION
7FFFh	$+6 \times V_{REF} \times (65535/65536)$	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
0001h	$+6 \times V_{REF} \times (32769/65536)$	Midscale + 1 LSB
0000h	$+6 \times V_{REF} \times (32768/65536)$	Midscale
FFFFh	$+6 \times V_{REF} \times (32767/65536)$	Midscale – 1 LSB
••• •••	••• •••	••• •••
8000h	0	0

The data written to the Gain Register are always in straight binary, data to the Zero Register are in twos complement, and data to all other control registers are as specified in the definitions, regardless of the $\overline{\text{USB}}$/BTC pin status.

In reading operation, the read-back data are in the same format as written.

OFFSET DACS

There are two 16-bit Offset DACs: one for Group A, and one for Group B. The Offset DACs allow the entire output curve of the associated DAC groups to be shifted by introducing a programmable offset. This offset allows for asymmetric bipolar operation of the DACs or unipolar operation with bipolar supplies. Thus, subject to the limitations of headroom, it is possible to set the output range of Group A and/or Group B to be unipolar positive, unipolar negative, symmetrical bipolar, or asymmetrical bipolar, as shown in Table 6 and Table 7. Increasing the digital input codes for the offset DAC shifts the outputs of the associated channels in the negative direction. The default codes for the Offset DACs in the DAC8728 are factory trimmed to provide optimal offset and gain performance for the default output range and span of symmetric bipolar operation. When the output range is adjusted by changing the value of the Offset DAC, an extra offset is introduced as a result of the linearity and offset errors of the Offset DAC. Therefore, the actual shift in the output span may vary slightly from the ideal calculations. For optimal offset and gain performance in the default symmetric bipolar operation, the Offset DAC input codes should not be changed from the default power-on values. The maximum allowable offset depends on the reference and the power supply. If *INPUT_CODE* from Equation 1 or *DAC_DATA_CODE* from Equation 2 is set to 0, then these equations simplify to Equation 3:

$$V_{OUT} = -V_{REF} \times (\text{Gain} - 1) \times \left(\frac{\text{OFFSETDAC\_CODE}}{65536}\right) \tag{3}$$

This equation shows the transfer function of the Offset DAC to the output of the DAC channels. In any case, the analog output must not go beyond the specified range shown in the *Analog Outputs* section. After power-on or reset, the Offset DAC is set to the value defined by the selected data format and the selected analog output voltage. If the DAC gain setting is changed, the offset DAC code is reset to the default value corresponding to the new DAC gain setting. Refer to the *Power-On Reset* and *Hardware Reset* sections for details.

For single-supply operation (AV_{SS} = 0V), the Offset DAC is turned off, and the output amplifier is in a Hi-Z state. The OFFSET-x pin must be connected to the AGND-x pin through a low-impedance connection. For dual-supply operation, this pin provides the output of the Offset DAC. The OFFSET-x pin is not intended to drive an external load. See Figure 96 for the internal Offset DAC and output amplifier configuration.

Table 6. Example of Offset DAC Codes and Output Ranges with Gain = 6 and V_{REF} = 5V

OFFSET DAC CODE	OFFSET DAC VOLTAGE	DAC CHANNELS MFS VOLTAGE	DAC CHANNELS PFS VOLTAGE
999Ah(1)	3.0V	–15V	+15V – 1 LSB
0000h	0V	0V	+30V – 1 LSB
FFFFh	~5.0V	–25V	+5V – 1 LSB
6666h	~2.0V	–10V	+20V – 1 LSB
CCCDh	~4.0V	–20V	+10V – 1 LSB

(1) This is the default code for symmetric bipolar operation; actual codes may vary ±10 LSB. Codes are in straight binary format.

Table 7. Example of Offset DAC Codes and Output Ranges with Gain = 4 and V_{REF} = 5V

OFFSET DAC CODE	OFFSET DAC VOLTAGE	DAC CHANNELS MFS VOLTAGE	DAC CHANNELS PFS VOLTAGE
AAABh(1)	~3.33333V	–10V	+10V – 1 LSB
0000h	0V	0V	+20V – 1 LSB
FFFFh	~5.0V	–15V	+5V – 1 LSB
5555h	~1.666V	–5V	+15V – 1 LSB
8000h	2.5V	–7.5V	+12.5V – 1 LSB
D555h	~4.1666V	–12.5V	+7.5V – 1 LSB

(1) This is the default code for symmetric bipolar operation; actual codes may vary ±10 LSB. Codes are in straight binary format.

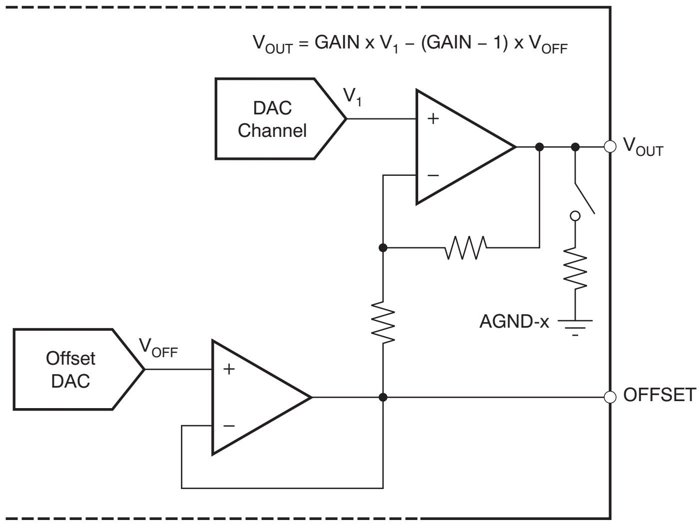


Figure 96. Output Amplifier and Offset DAC

OUTPUT AMPLIFIERS

The output amplifiers can swing to 0.5V below the positive supply and 0.5V above the negative supply. This condition limits how much the output can be offset for a given reference voltage. The maximum range of the output for ±17V power and a +5.5V reference is –16.5V to +16.5V for gain = 6.

Each output amplifier is implemented with individual over-current protection. The amplifier is clamped at 10mA, even if the output current goes over 10mA.

GENERAL-PURPOSE INPUT/OUTPUT PIN (GPIO)

The GPIO pin is a general-purpose, bidirectional, digital input/output, as shown in Figure 97. When the GPIO pin acts as an output, the pin status is determined by the corresponding GPIO bit in the GPIO Register. The pin output is high-impedance when the GPIO bit is set to '1', and is logic low when the GPIO bit is cleared to '0'. Note that a pull-up resistor to IOV_{DD} is required when using the GPIO pin as an output. When the GPIO pin acts as an input, the digital value on the pin is acquired by reading the GPIO bit. After power-on reset, or any forced hardware or software reset, the GPIO bit is set to '1', and is in a high-impedance state. If not used, the GPIO pin must be tied to either DGND or to IOV_{DD} through a pull-up resistor. Leaving the GPIO pin floating can cause high IOV_{DD} supply currents.

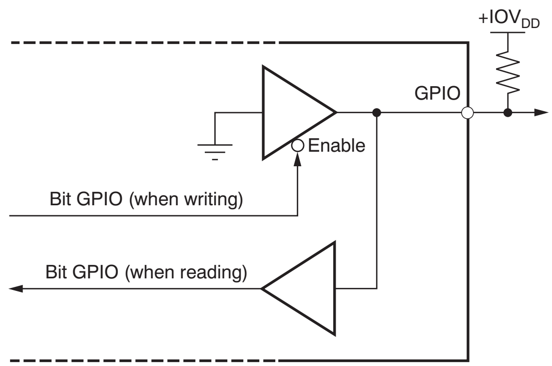


Figure 97. GPIO Pin

$\overline{\text{BUSY}}$ Pin

The $\overline{\text{BUSY}}$ pin is an open-drain output. When the correction engine runs, the GBF bit in the Configuration Register is set and the $\overline{\text{BUSY}}$ pin is low. When multiple DAC8728 devices may be used in one system, the $\overline{\text{BUSY}}$ pins can be tied together. When each device has finished updating the DAC Data Register, the respective $\overline{\text{BUSY}}$ pin is released. If another device has not finished updating the DAC Data Register, it will hold $\overline{\text{BUSY}}$ low. This configuration is useful when it is required that no DAC in any device is updated until all other DACs are ready.

ANALOG OUTPUT PIN ($\overline{\text{CLR}}$)

The $\overline{\text{CLR}}$ pin is an active low input that should be high for normal operation. When this pin is in logic '0', all V_{OUT} outputs connect to AGND-x through internal 15kΩ resistors and are cleared to 0 V, and the output buffer is in a Hi-Z state. While $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is taken high again while the $\overline{\text{LDAC}}$ is high, the DAC outputs remain cleared until $\overline{\text{LDAC}}$ is taken low. However, if $\overline{\text{LDAC}}$ is tied low, taking $\overline{\text{CLR}}$ back to high sets the DAC output to the level defined by the value of the DAC latch. The contents of the Zero Registers, Gain Registers, Input Data Registers, DAC Data Registers, and DAC latches are not affected by taking $\overline{\text{CLR}}$ low.

POWER-ON RESET

The DAC8728 contains a power-on reset circuit that controls the output during power-on and power down. This feature is useful in applications where the known state of the DAC output during power-on is important. The Offset DAC Registers, DAC Data Registers, and DAC latches are loaded with the value defined by the RSTSEL pin, as shown in Table 8. The Gain Registers and Zero Registers are loaded with default values. The Input Data Register is reset to 0000h, independent of the RSTSEL state.

Table 8. Bipolar Output Reset Values for Dual Power-Supply Operation

RSTSEL PIN	$\overline{USB}$/BTC PIN	INPUT FORMAT	VALUE OF DAC DATA REGISTER AND DAC LATCH	VALUE OF OFFSET DAC REGISTER FOR GAIN = 6 (1)	V_{OUT}
DGND	DGND	Straight Binary	0000h	999Ah	–Full-Scale
IOV_{DD}	DGND	Straight Binary	8000h	999Ah	0 V
DGND	IOV_{DD}	Twos Complement	8000h	199Ah	–Full-Scale
IOV_{DD}	IOV_{DD}	Twos Complement	0000h	199Ah	0 V

(1) Offset DAC A and Offset DAC B are trimmed in manufacturing to minimize the error for symmetrical output. The default value may vary no more than ±10 LSB from the nominal number listed in this table.

In single-supply operation, the Offset DAC is turned off and the output is unipolar. The power-on reset is defined as shown in Table 9.

Table 9. Unipolar Output Reset Values for Single Power-Supply Operation

RSTSEL PIN	$\overline{USB}$/BTC PIN	INPUT FORMAT	VALUE OF DAC DATA REGISTER AND DAC LATCH	V_{OUT}
DGND	DGND	Straight Binary	0000h	0 V
IOV_{DD}	DGND	Straight Binary	8000h	Midscale
DGND	IOV_{DD}	Twos Complement	8000h	0 V
IOV_{DD}	IOV_{DD}	Twos Complement	0000h	Midscale

HARDWARE RESET

When the $\overline{RST}$ pin is low, the device is in hardware reset. All the analog outputs (V_{OUT}-0 to V_{OUT}-7), the DAC registers, and the DAC latches are set to the reset values defined by the RSTSEL pin as shown in Table 8 and Table 9. In addition, the Gain and Zero registers are loaded with default values, communication is disabled, and the signals on R/$\overline{W}$, $\overline{CS}$, [D0:D15], and [A0:A4] are ignored (note that [D0:D15] are in a high-impedance state). The Input Data Register is reset to 0000h, independent of the RSTSEL state. On the rising edge of $\overline{RST}$, the analog outputs (V_{OUT}-0 to V_{OUT}-7) maintain the reset value as defined by the RSTSEL pin until a new value is programmed. After $\overline{RST}$ goes high, the parallel interface returns to normal operation. $\overline{CS}$ must be set to a logic high whenever $\overline{RST}$ is used.

UPDATING THE DAC OUTPUTS

Depending on the status of both $\overline{CS}$ and $\overline{LDAC}$, and after data have been transferred into the DAC Data registers, the DAC outputs can be updated either in asynchronous mode or synchronous mode. This update mode is established at power-on. If asynchronous mode is desired, the $\overline{LDAC}$ pin must be permanently tied low before power is applied to the device. If synchronous mode is desired, $\overline{LDAC}$ must be logic high before and during power-on.

The DAC8728 updates a DAC latch only if it has been accessed since the last time $\overline{LDAC}$ was brought low or if the LD bit is set to '1', thereby eliminating any unnecessary glitch. Any DAC channels that were not accessed are not loaded again. When the DAC latch is updated, the corresponding output changes to the new level immediately.

Asynchronous Mode

In this mode, the $\overline{LDAC}$ pin is set low at power-up. This action places the DAC8728 into Asynchronous mode, and the LD bit and $\overline{LDAC}$ signal are ignored. When the correction engine is off (SCE bit = '0'), the DAC Data Registers and DAC latches are updated immediately when $\overline{CS}$ goes high. When the correction engine is on (SCE bit = '1'), each DAC latch is updated individually when the correction engine updates the corresponding DAC Data Register.

Synchronous Mode

To activate this mode, take $\overline{LDAC}$ low or set the LD bit to '1' after $\overline{CS}$ goes high. If $\overline{LDAC}$ goes low or if the LD bit is set to '1' when SCE = '0', all DAC latches are updated simultaneously. If $\overline{LDAC}$ goes low or if the LD bit is set to '1' when SCE = '1' and the $\overline{BUSY}$ pin is high (GBF bit = '0'), all DAC latches are updated simultaneously. If $\overline{LDAC}$ goes low or the LD bit is set to '1' when SCE = '1' and the $\overline{BUSY}$ pin is low (GBF bit = '1'), the DAC latches are not updated immediately because the correction engine is still running. Instead, all DAC latches are updated simultaneously when the GBF bit is cleared to '0'. At that time, the correction engine is finished.

In this mode, when $\overline{LDAC}$ stays high, the DAC latch is not updated; therefore, the DAC output does not change. The DAC latch is updated by taking $\overline{LDAC}$ low (or by setting the LD bit in the Configuration Register to '1') any time after the delay of t_{15} from the rising edge of $\overline{CS}$ (when the correction engine is disabled), or after the delay of t_{18} from the rising edge of $\overline{BUSY}$ (when the correction engine is enabled). If the timing requirements of t_{15} or t_{18} is not satisfied, invalid data are loaded. Refer to the *Timing Diagrams* and the Configuration Register (Table 11) for details.

MONITOR OUTPUT PIN (V_{MON})

The V_{MON} pin is the channel monitor output. It monitors either of the DAC outputs, offset DAC outputs, or reference buffer outputs. The channel monitor function consists of an analog multiplexer addressed via the parallel interface, allowing any channel output, reference buffer output, or offset DAC output to be routed to the V_{MON} pin for monitoring using an external ADC. The monitor function is controlled by the Monitor Register, which allows the monitor output to be enabled or disabled. When disabled, the monitor output is high-impedance; therefore, several monitor outputs may be connected in parallel with only one enabled at a time.

Note that the multiplexer is implemented as a series of analog switches. Care should be taken to ensure the maximum current from the V_{MON} pin must not be greater than the given specification because this could conceivably cause a large amount of current to flow from the input of the multiplexer (that is, from V_{OUT}-X) to the output of the multiplexer (V_{MON}). Refer to the *Monitor Register* section and Table 12 for more details.

POWER-DOWN MODE

The DAC8728 is implemented with a power-down function to reduce power consumption. Either the entire device or each individual group can be put into power-down mode. If the proper power-down bit (PD-x) in the Configuration Register is set to '1', the individual group is put into power down mode. During power-down mode, the analog outputs (V_{OUT}-0 to V_{OUT}-7) connect to AGND-X through an internal 15kΩ resistor, and the output buffer is in Hi-Z status. When the entire device is in power-down, the bus interface remains active in order to continue communication and receive commands from the host controller, but all other circuits are powered down. The host controller can wake the device from power-down mode and return to normal operation by clearing the PD-x bit; it takes 200μs or less for recovery to complete.

POWER-ON RESET SEQUENCING

The DAC8728 permanently latches the status of some of the digital pins at power-on. These digital levels should be well-defined before or while the digital supply voltages are applied. Therefore, it is advised to have a pull up resistor to IOV_{DD} or DGND for the digital initialization pins ($\overline{LDAC}$, $\overline{CLR}$, $\overline{RST}$, $\overline{CS}$, and RSTSEL) to ensure that these levels are set correctly while the digital supplies are raised.

For proper power-on initialization of the device, IOV_{DD} and the digital pins must be applied before or at the same time as DV_{DD}. If possible, it is preferred that IOV_{DD} and DV_{DD} can be connected together in order to simplify the supply sequencing requirements. Pull-up resistors should go to either supply. AV_{DD} should be applied after the digital supplies (IOV_{DD} and DV_{DD}) and digital initialization pins ($\overline{LDAC}$, $\overline{CLR}$, $\overline{RST}$, $\overline{CS}$, and RSTSEL). AV_{SS} can be applied at the same time as or after AV_{DD}. The REF-x pins must be applied last.

PARALLEL INTERFACE

The DAC8728 interfaces with microprocessors using a 16-bit data bus. The interface is double-buffered, allowing simultaneous updating of all DACs. Each DAC has an input data register, DAC data register, user-calibration gain register, user-calibration zero register, and DAC latch. When user calibration is enabled, the input data register receives data from the data bus, the DAC Data Register stores the data after internal calibration, and the DAC latch sets the analog output level. When user calibration is disabled (default), the DAC data register stores data from the data bus, and the DAC latch sets the analog output level. Five address lines (A0:A4) select which DAC or auxiliary register is addressed. Table 10 shows the register map.

Table 10. Register Map

ADDRESS BITS					DATA BITS													
A4	**A3**	**A2**	**A1**	**A0**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3:D0**	**REGISTER**
0	0	0	0	0	A/B	LD	RST	PD-A	PD-B	SCE	GBF	GAIN-A	GAIN-B	Don't Care(1)				Configuration Register
0	0	0	0	1	DAC-7	DAC-6	DAC-5	DAC-4	DAC-3	DAC-2	DAC-1	DAC-0	Offset DAC-A	Offset DAC-B	Ref Buffer -A	Ref Buffer -B	Don't Care(1)	Monitor Register
0	0	0	1	0	GPIO	Don't Care(1)												GPIO Register
0	0	0	1	1	D15:D0, default = 39322 (999Ah)													Offset DAC-A Data Register
0	0	1	0	0	D15:D0 , default = 39322 (999Ah)													Offset DAC-B Data Register
0	0	1	0	1	BF-7	BF-6	BF-5	BF-4	BF-3	BF-2	BF-1	BF-0	Don't Care(1)					Busy Flag Register
0	0	1	1	0	Reserved(2)													Reserved
0	0	1	1	1	Reserved(2)													Reserved
0	1	0	0	0	DB15:DB0													DAC-0
0	1	0	0	1	DB15:DB0													DAC-1
0	1	0	1	0	DB15:DB0													DAC-2
0	1	0	1	1	DB15:DB0													DAC-3
0	1	1	0	0	DB15:DB0													DAC-4
0	1	1	0	1	DB15:DB0													DAC-5
0	1	1	1	0	DB15:DB0													DAC-6
0	1	1	1	1	DB15:DB0													DAC-7
1	0	0	0	0	Z15:Z0, default = 0 (0000h), twos complement													Zero Register-0
1	1	0	0	0	G15:G0, default = 32768 (8000h), straight binary													Gain Register-0
1	0	0	0	1	Z15:Z0, default = 0 (0000h), twos complement													Zero Register-1
1	1	0	0	1	G15:G0, default = 32768 (8000h), straight binary													Gain Register-1
1	0	0	1	0	Z15:Z0, default = 0 (0000h), twos complement													Zero Register-2
1	1	0	1	0	G15:G0, default = 32768 (8000h), straight binary													Gain Register-2
1	0	0	1	1	Z15:Z0, default = 0 (0000h), twos complement													Zero Register-3
1	1	0	1	1	G15:G0, default = 32768 (8000h), straight binary													Gain Register-3
1	0	1	0	0	Z15:Z0, default = 0 (0000h), twos complement													Zero Register-4
1	1	1	0	0	G15:G0, default = 32768 (8000h), straight binary													Gain Register-4
1	0	1	0	1	Z15:Z0, default = 0 (0000h), twos complement													Zero Register-5
1	1	1	0	1	G15:G0, default = 32768 (8000h), straight binary													Gain Register-5
1	0	1	1	0	Z15:Z0, default = 0 (0000h), twos complement													Zero Register-6
1	1	1	1	0	G15:G0, default = 32768 (8000h), straight binary													Gain Register-6
1	0	1	1	1	Z15:Z0, default = 0 (0000h), twos complement													Zero Register-7
1	1	1	1	1	G15:G0, default = 32768 (8000h), straight binary													Gain Register-7

(1) Writing to a Don't Care bit has no effect; reading the bit returns '0'.
(2) Writing to a reserved bit has no effect; reading the bit returns '0'.

INTERNAL REGISTERS

The DAC8728 internal registers consist of the Configuration Register, the Monitor Register, the DAC Input Data Registers, the Zero Registers, the Gain Registers, the DAC Data Registers, and the Busy Flag Register, and are described in the following section.

The Configuration Register specifies which actions are performed by the device. Table 11 shows the details.

Table 11. Configuration Register (Default = 8000h)

BIT	NAME	DEFAULT VALUE	DESCRIPTION
D15	A/B	1	A/B bit. When A/B = '0', reading DAC-x returns the value in the Input Data Register. When A/B = '1', reading DAC-x returns the value in the DAC Data Register. When the correction engine is enabled, the data returned from the Input Data Register are the original data written to the bus, and the value in the DAC Data Register is the corrected data.
D14	LD	0	Synchronously update DAC bits. When $\overline{LDAC}$ is tied high, setting LD = '1' at any time after the write operation and the correction process complete synchronously updates all DAC latches with the content of the corresponding DAC Data Register, and sets V_{OUT} to a new level. The DAC8728 updates the DAC latch only if it has been accessed since the last time $\overline{LDAC}$ was brought low or the LD bit was set to '1', thereby eliminating unnecessary glitch. Any DACs that were not accessed are not reloaded. After updating, the bit returns to '0'. When the $\overline{LDAC}$ pin is tied low, this bit is ignored. When the correction engine is off, the LD bit can be issued any time after the write operation is finished, and the DAC latch is immediately updated when $\overline{CS}$ goes high.
D13	RST	0	Software reset bit. Set the RST bit to '1' to reset the device; functions the same as a hardware reset. After reset completes, the RST bit returns to '0'.
D12	PD-A	0	Power-down bit for Group A. Setting the PD-A bit to '1' places Group A (DAC-0, DAC-1, DAC-2, and DAC-3) into power-down mode. All output buffers are in Hi-Z and all analog outputs (V_{OUT}-X) connect to AGND-A through an internal 15kΩ resistor. Setting the PD-A bit to '0' returns group A to normal operation.
D11	PD-B	0	Power-down bit for Group B. Setting the PD-B bit to '1' places Group B (DAC-4, DAC-5, DAC-6, and DAC-7) into power-down operation. All output buffers are in Hi-Z and all analog outputs (V_{OUT}-X) connect to AGND-B through an internal 15kΩ resistor. Setting the PD-B bit to '0' returns group B to normal operation.
D10	SCE	0	System-calibration enable bit. Set the SCE bit to '1' to enable the correction engine. When the engine is enabled, the input data are adjusted by the correction engine according to the contents of the corresponding Gain Register and Zero Register. The results are transferred to the corresponding DAC Data Register, and finally loaded into the DAC latch, which sets the V_{OUT}-x pin output level. Set the SCE bit to '0' to turn off the correction engine. When the engine is turned off, the input data are transferred to the corresponding DAC Data Register, and then loaded into the DAC latch, which sets the output voltage. Refer to the *User Calibration for Zero Error and Gain Error* section for details.
D9 (Read Only)	GBF	0	Global correction engine busy flag. GBF = '1' when the correction engine is running, indicating that at least one channel has not been corrected. GBF = 0' 'when the correction engine stops, indicating that no more correction is needed. When the SCE bit = '0', GBF is always cleared ('0').
D8	GAIN-A	0	Gain bit for Group A (DAC-0, DAC-1, DAC-2, and DAC-3). Set the GAIN-A bit to '0' for an output span = 6 × REF-A. Set the GAIN-A bit to '1' for an output span = 4 × REF-A. Updating this bit to a new value automatically resets the Offset DAC-A Register to its factory-trimmed value for the new gain setting.
D7	GAIN-B	0	Gain bit for Group B (DAC-4, DAC-5, DAC-6, and DAC-7). Set the GAIN-B bit to '0' for an output span = 6 × REF-B. Set the GAIN-B bit to '1' for an output span = 4 × REF-B. Updating this bit to a new value automatically resets the Offset DAC-B Register to its factory-trimmed value for the new gain setting.
D6:D0	—	0	Don't care. Writing to these bits has no effect; reading these bits returns '0'.

Monitor Register (default = 0000h).

The Monitor Register selects one of the DAC outputs, reference buffer outputs, or offset DAC outputs to be monitored through the V_{MON} pin. Only one bit at a time can be set to '1'. When bits [D15:D4] = '0', the monitor is disabled and V_{MON} is in a Hi-Z state.

Note that if any value is written other than those specified in Table 12, the Monitor Register stores the invalid value; however, the V_{MON} pin is forced into a Hi-Z state.

Table 12. Monitor Register (Default = 0000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3:D0	V_{MON} CONNECTS TO
0	0	0	0	0	0	0	0	0	0	0	1	X(1)	Reference buffer B output
0	0	0	0	0	0	0	0	0	0	1	0	X	Reference buffer A output
0	0	0	0	0	0	0	0	0	1	0	0	X	Offset DAC B output
0	0	0	0	0	0	0	0	1	0	0	0	X	Offset DAC A output
0	0	0	0	0	0	0	1	0	0	0	0	X	DAC-0
0	0	0	0	0	0	1	0	0	0	0	0	X	DAC-1
0	0	0	0	0	1	0	0	0	0	0	0	X	DAC-2
0	0	0	0	1	0	0	0	0	0	0	0	X	DAC-4
0	0	0	1	0	0	0	0	0	0	0	0	X	DAC-4
0	0	1	0	0	0	0	0	0	0	0	0	X	DAC-5
0	1	0	0	0	0	0	0	0	0	0	0	X	DAC-6
1	0	0	0	0	0	0	0	0	0	0	0	X	DAC-7
0	0	0	0	0	0	0	0	0	0	0	0	X	Monitor function disabled, Hi-Z (default)
All other codes													Monitor function disabled, Hi-Z

(1) X = don't care. Writing to this bit has no effect; reading the bit returns '0'.

Input Data Register for DAC-n (where n = 0 to 7). Default = 0000h.

This register stores the DAC data written to the device when the SCE bit = '1'. When the SCE bit = '0' (default), the DAC Data Register stores the DAC data written to the device. When the data are loaded into the corresponding DAC latch, the DAC output changes to the new level defined by the DAC data. The default value after power-on or reset is 0000h.

Table 13. DAC-n(1) Input Data Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DB15(2)	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

(1) n = 0, 1, 2, 3, 4, 5, 6, or 7.
(2) DB15:DB0 are the DAC data bits

Zero Register n (where n = 0 to 7). Default = 0000h.

The Zero Register stores the user-calibration data that are used to eliminate the offset error, as shown in Table 14. The data are 16 bits wide, 1 LSB/step, and the total adjustment is –32768 LSB to +32767 LSB, or ±50% of full-scale range. The Zero Register uses a twos complement data format.

Table 14. Zero Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Z15	Z14	Z13	Z12	Z11	Z10	Z9	Z8	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0

Z15:Z0—OFFSET BITS	ZERO ADJUSTMENT
7FFFh	+32767 LSB
7FFEh	+32766 LSB
••• ••• •••	••• ••• •••
0001h	+1 LSB
0000h	0 LSB (default)
FFFFh	–1 LSB
••• ••• •••	••• ••• •••
8001h	–32767 LSB
8000h	–32768 LSB

Gain Register n (where n = 0 to 7). Default = 8000h.

The Gain Register stores the user-calibration data that are used to eliminate the gain error, as shown in Table 15. The data are 16 bits wide, 0.0015% FSR/step, and the total adjustment range 0.5 to 1.5. The Gain Register uses a straight binary data format.

Table 15. Gain Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0

G15:G0—GAIN-CODE BITS	GAIN ADJUSTMENT COEFFICIENT
FFFFh	1.499985
FFFEh	1.499969
••• ••• •••	••• ••• •••
8001h	1.000015
8000h	1 (default)
7FFFh	0.999985
••• ••• •••	••• ••• •••
0001h	0.500015
0000h	0.5

GPIO Register. Default = 8000h.

The GPIO Register determines the status of the GPIO pin.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GPIO	X(1)	X	X	X	X	X	X	X	X	X	X	X	X	X	X

(1) X = don't care. Writing to this bit has no effect; reading the bit returns '0'.

GPIO

For write operations, the GPIO pin operates as an output. Writing a '1' to the GPIO bit sets the GPIO pin to high impedance, and writing a '0' sets the GPIO pin to logic low. An external pull-up resistor is required when using the GPIO pin as an output.

For read operations, the GPIO pin operates as an input. Read the GPIO bit to receive the status of the GPIO pin. Reading a '0' indicates that the GPIO pin is low, and reading a '1' indicates that the GPIO pin is high.

After power-on reset, or any forced hardware or software reset, the GPIO bit is set to '1', and is in a high-impedance state.

Busy Flag Register (read-only). Default = 0000h.

Busy flag bit of DAC-x. The Busy Flag Register Each channel has an individual busy flag (BF-x) in the Busy Flag register. When the channel is accessed and the correction engine is enabled, the respective BF-x bit is set if either the Input Data Register, Zero Register, or Gain Register are written to. When the DAC data is adjusted by the correction engine and transferred into the DAC Data Register, the BF-x bit is cleared. It takes approximately 500ns per channel for the correction to complete.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BF-7	BF-6	BF-5	BF-4	BF-3	BF-2	BF-1	BF-0	X(1)	X	X	X	X	X	X	X

(1) X = don't care. Writing to this bit has no effect; reading the bit returns '0'.

BF-7:0

BF-x = '1' if the input data of DAC-x has not been corrected or if the correction engine is not finished.

BF-x = '0' when the input data has been corrected or the correction engine is turned off.

APPLICATION INFORMATION

PRECISION VOLTAGE REFERENCE SELECTION

To achieve the optimum performance from the DAC8728 over the full operating temperature range, a precision voltage reference must be used. Careful consideration should be given to the selection of a precision voltage reference. The DAC8728 has two reference inputs, REF-A and REF-B. The voltages applied to the reference inputs are used to provide a buffered positive reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the device. There are four possible sources of error to consider when choosing a voltage reference for high-accuracy applications: initial accuracy, temperature coefficient of the output voltage, long-term drift, and output voltage noise. Initial accuracy error on the output voltage of an external reference can lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with low initial accuracy error specification is preferred. Long-term drift is a measure of how much the reference output voltage drifts over time. A reference with a tight, long-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime. The temperature coefficient of a reference output voltage affects the output drift when the temperature changes. Choose a reference with a tight temperature coefficient specification to reduce the dependence of the DAC output voltage on ambient conditions. In high-accuracy applications, which have a relatively low noise budget, the reference output voltage noise also must be considered. Choosing a reference with as low an output noise voltage as practical for the required system resolution is important. Precision voltage references such as TI's REF50xx (2V to 5V) and REF32xx (1.25V to 4V) provide a low-drift, high-accuracy reference voltage.

POWER-SUPPLY NOISE

The DAC8728 must have ample supply bypassing of 1μF to 10μF in parallel with 0.1μF on each supply, located as close to the package as possible; ideally, immediately next to the device. The 1μF to 10μF capacitors must be the tantalum-bead type. The 0.1μF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI), such as common ceramic types, which provide a low-impedance path to ground at high frequencies to handle transient currents because of internal logic switching. The power-supply lines must be as large a trace as possible to provide low-impedance paths and reduce the effects of glitches on the power-supply line. Apart from these considerations, the wideband noise on the AV_{DD}, AV_{SS}, DV_{DD} and IOV_{DD} supplies should be filtered before feeding to the DAC to obtain the best possible noise performance.

LAYOUT

Precision analog circuits require careful layout, adequate bypassing, and a clean, well-regulated power supply to obtain the best possible dc and ac performance. Careful consideration of the power-supply and ground-return layout helps to meet the rated performance. DGND is the return path for digital currents and AGND is the power ground for the DAC. For the best ac performance, care should be taken to connect DGND and AGND with very low resistance back to the supply ground. The printed circuit board (PCB) must be designed so that the analog and digital sections are separated and confined to certain areas of the board. If multiple devices require an AGND-to-DGND connection, the connection is to be made at one point only. The star ground point is established as close as possible to the device.

The power-supply lines must be as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power-supply line. Fast switching signals must never be run near the reference inputs. It is essential to minimize noise on the reference inputs because it couples through to the DAC output. Avoid crossover of digital and analog signals. Traces on opposite sides of the board must run at right angles to each other. This configuration reduces the effects of feedthrough on the board. A microstrip technique may be considered, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder-side.

Each DAC group has a ground pin, AGND-x, which is the ground of the output from the DACs in the group. It must be connected directly to the corresponding reference ground in low-impedance paths to get the best performance. AGND-A must be connected with REFGND-A and AGND-B must be connected with REFGND-B. AGND-A and AGND-B must be tied together and connected to the analog power ground and DGND.

During single-supply operation, the OFFSET-x pins must be connected to AGND-x with a low-impedance path because these pins carry DAC-code-dependent current. Any resistance from OFFSET-x to AGND-x causes a voltage drop by this code-dependent current. Therefore, it is very important to minimize routing resistance to AGND-x or to any ground plane that AGND-x is connected to.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8728SPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-4-260C-72 HR	-40 to 105	DAC8728	Samples
DAC8728SPAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	NIPDAU	Level-4-260C-72 HR	-40 to 105	DAC8728	Samples
DAC8728SRTQR	ACTIVE	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	DAC8728	Samples
DAC8728SRTQT	ACTIVE	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	DAC8728	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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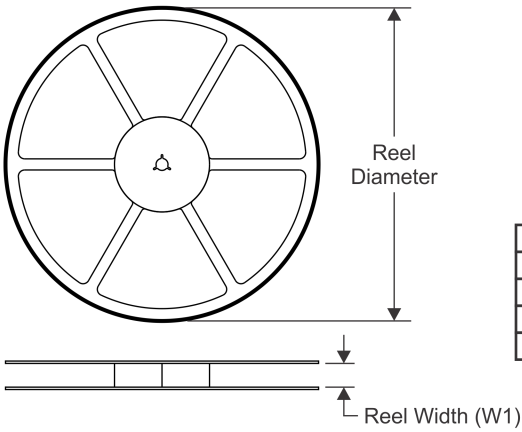
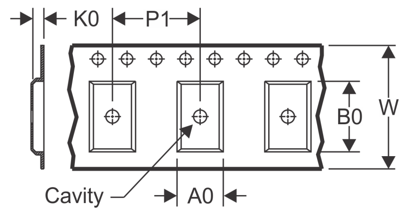
TAPE AND REEL INFORMATION

REEL DIMENSIONS

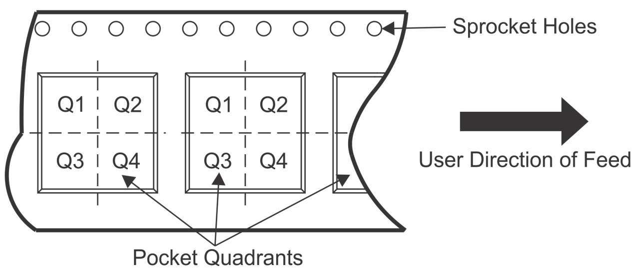


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

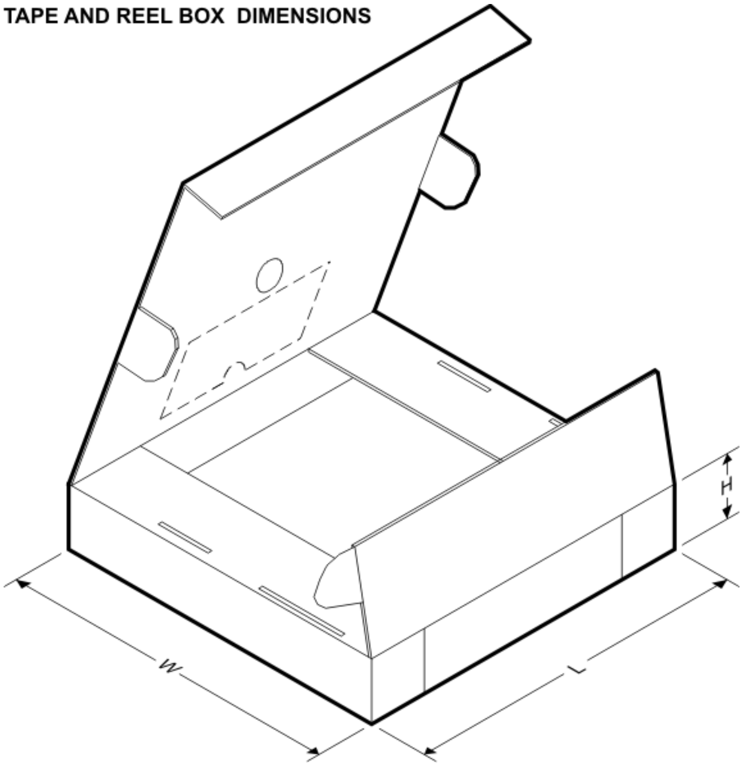
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8728SPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
DAC8728SRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
DAC8728SRTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

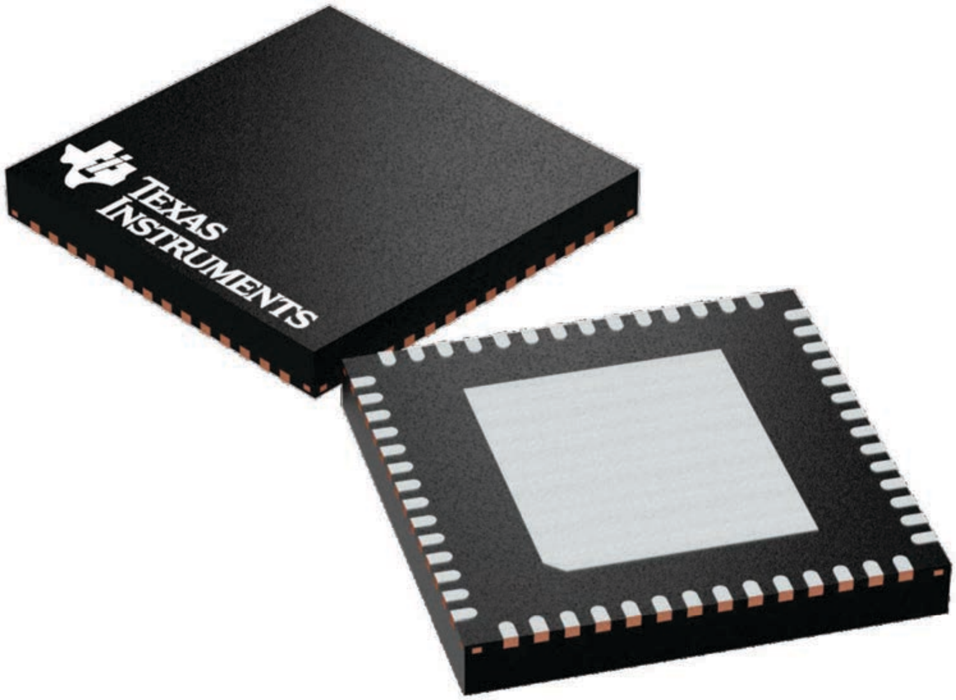
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8728SPAGR	TQFP	PAG	64	1500	350.0	350.0	43.0
DAC8728SRTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
DAC8728SRTQT	QFN	RTQ	56	250	213.0	191.0	55.0

RTQ 56

VQFN - 1 mm max height

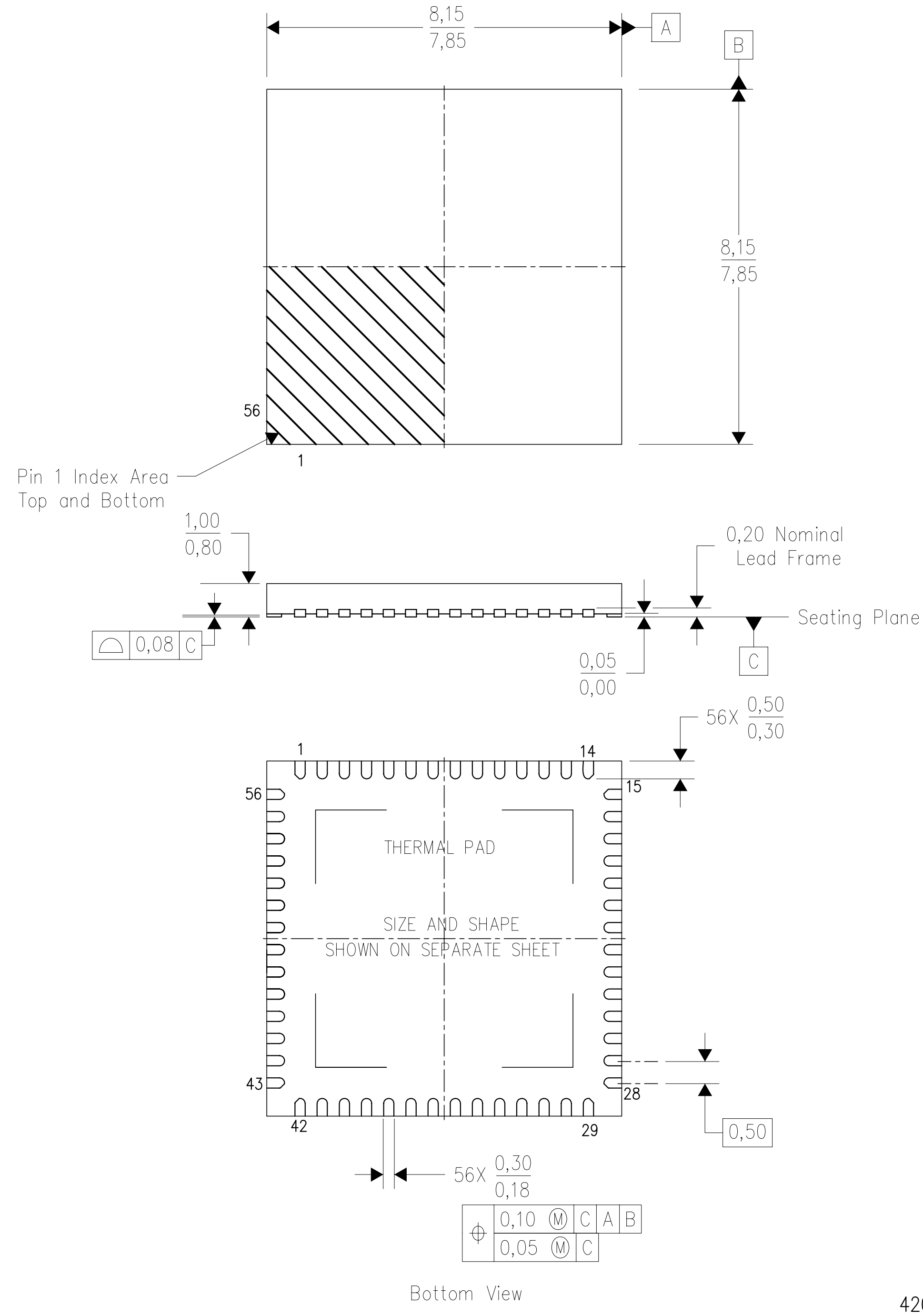
8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RTQ (S-PVQFN-N56) PLASTIC QUAD FLATPACK NO-LEAD



4206089/D 08/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220.

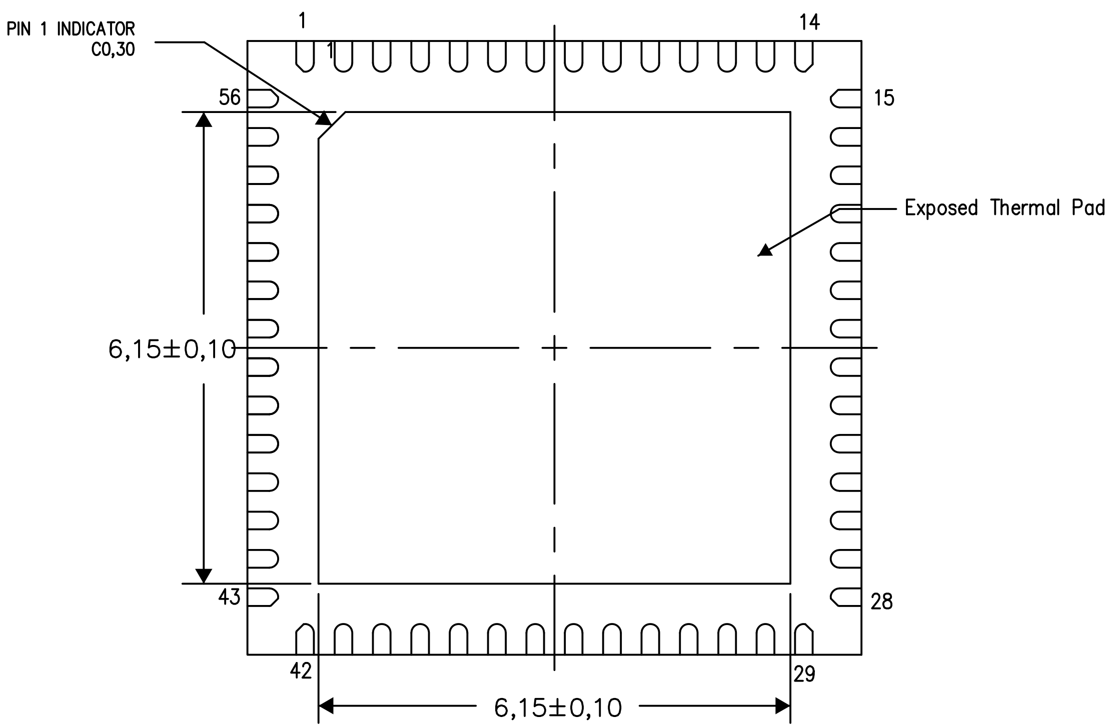
RTQ (S-PVQFN-N56) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206252-3/Q 03/15

NOTE: All linear dimensions are in millimeters

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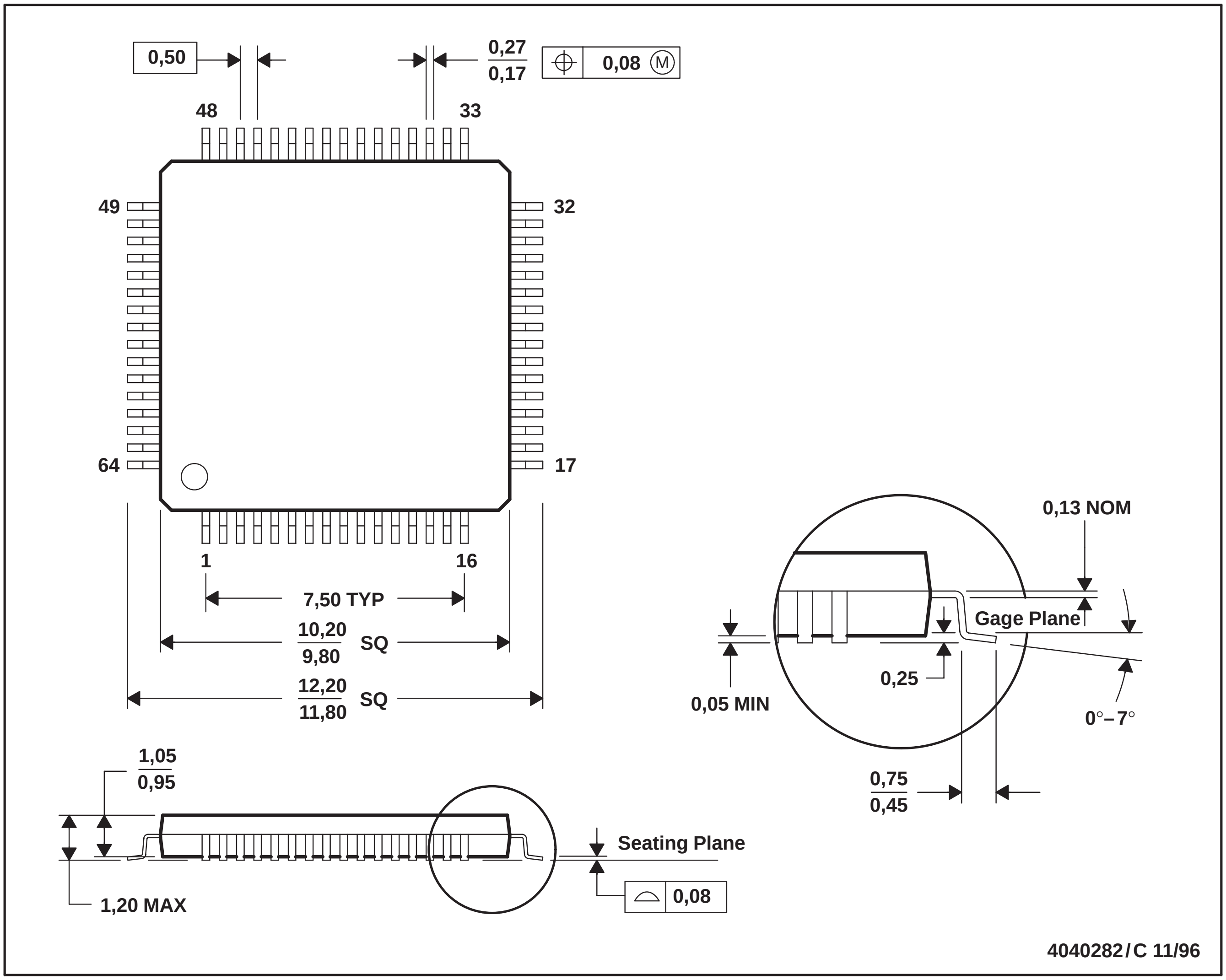
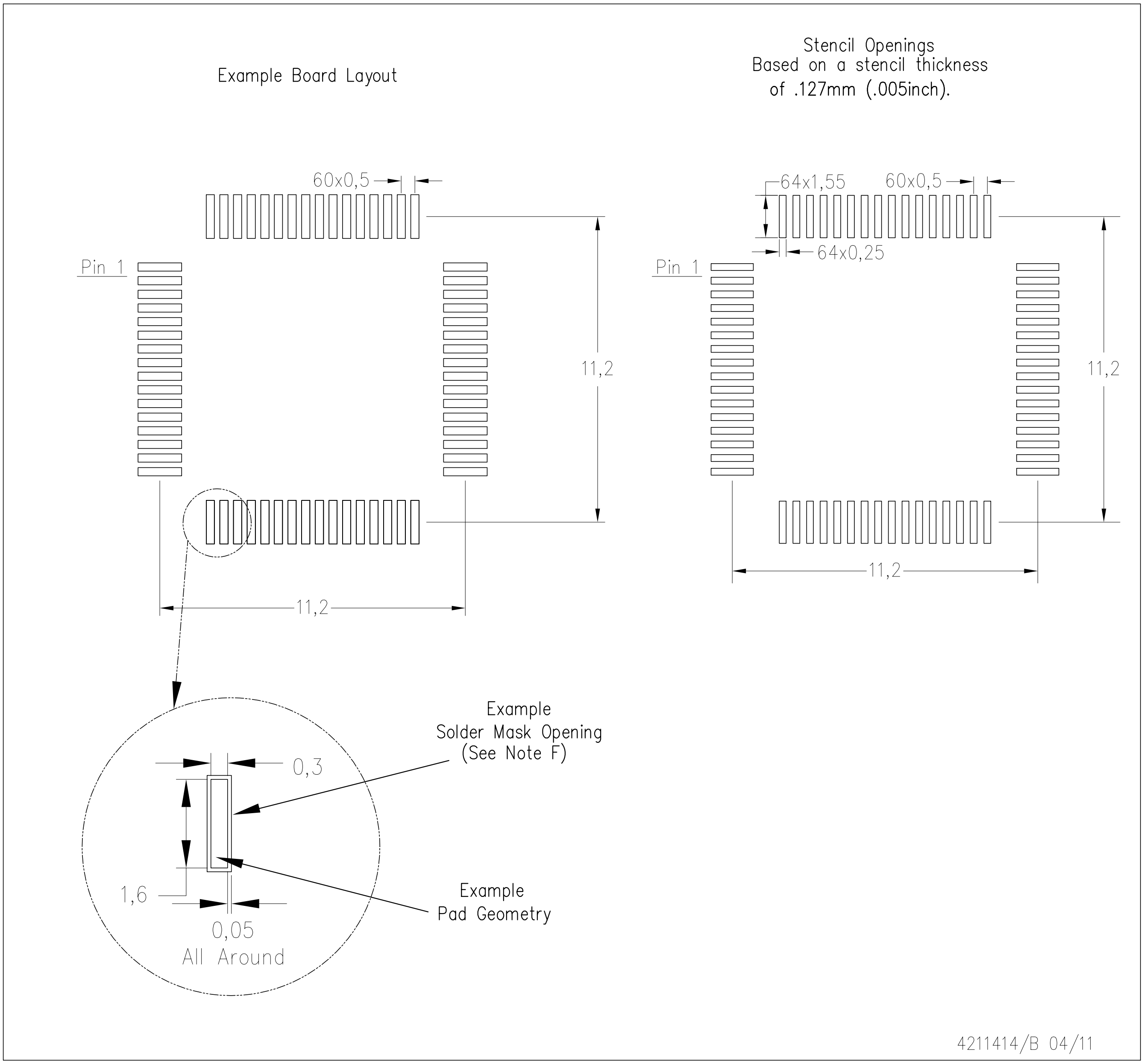
PAG (S-PQFP-G64) PLASTIC QUAD FLATPACK



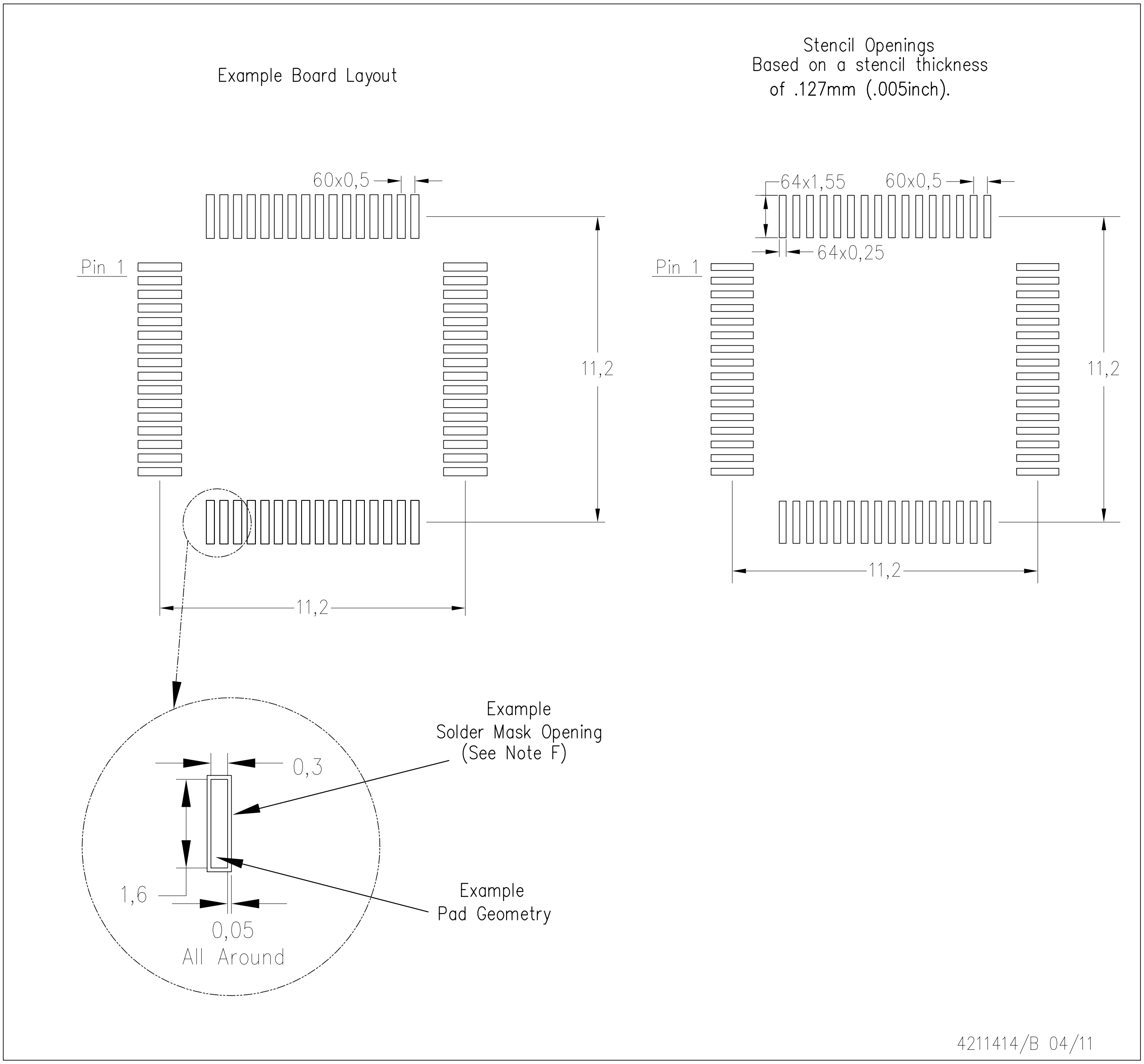
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PAG (S-PQFP-G64) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PAG (S-PQFP-G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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