BCM53262M

Managed Switch with 24 FE Ports + 4-GbE Interface

GENERAL DESCRIPTION

The BCM53262M is a ninth-generation RoboSwitch™ design based on the field-proven BCM5324 device. This integrated 0.13µ-CMOS device combines all the functions of a high-speed switch system including packet buffers, PHY transceivers, Media Access Controllers (MACs), address management, and a nonblocking switch fabric. It is designed to be fully compliant with the IEEE 802.3 and IEEE 802.3x specifications, including the MAC control PAUSE frame, auto-negotiation and with all industry-standard Ethernet and Fast Ethernet devices.

The BCM53262M contains 24 full-duplex 10Base-T/100Base-TX Fast Ethernet transceivers with Advanced Cable Diagnostics support. Each performs all physical layer interface functions for 10Base-T Ethernet on Category 3, 4, or 5 Unshielded Twisted Pair (UTP) cable and 100Base-TX Fast Ethernet on Category 5 UTP cable. The BCM53262M has four SGMII interfaces that provide flexible 10/100/1000Base-TX/FX connectivity. An additional MAC is included for CPU connection via RvMII/MII (Rev. A)/GMII (Rev. B) interface.

The BCM53262M has a rich feature set suitable for streaming VoIP, video, and data traffic for multimedia applications. The BCM53262M supports up to four QoS queues per port. Traffic QoS can be assigned based on Port-ID, MAC Address, 802.1p or DiffServ. Together with 4K entries, 802.1Q VLAN, 802.1x EAPOL protocol filtering, MAC-based link aggregation with dynamic failover, per-port bandwidth/rate control, MAC address locking, and IGMP snooping at Layer 3 allow system vendors to build advanced L2+ switch systems for the Multitenant/Multidweller Unit (MTU/MDU) markets.The BCM53262M provides 70+ on-chip MIB counters to collect receive and transmit statistics for each port.

FEATURES

- Ninth-generation L2+ Fast Ethernet switch with four SGMII interfaces.
  - 24-port 10/100 transceivers for TX/EFX.
  - Advanced Cable Diagnostic support.
  - 25 10/100 MACs.
  - Four Gigabit MACs.
  - 3-Mbit (384 KB) packet buffer and control memory.
  - Management Port with RvMII/MII interface (Rev. A).
  - Management Port with RvMII/MII/GMII interface (Rev. B).
- Nonblocking switch fabric for 24 FE + 4 GbE ports.
- Jumbo frame support up to 2048 bytes.
- Flexible TCAM-based Compact Field Processor for packet classification and filtering.
- Packet Remarking, VID Replacement.
  - 802.1p PCP, DSCP remarking.
- Optimized for managed switch design.
- 802.1p, Port, MAC, Protocol, Customer_VID, and DiffServ (IPv4/IPv6) based QoS packet classification with four priority queues.
- Port-based VLAN.
- 802.1Q-based VLAN with 4K entries.
- MAC-based VLAN with 512 entries.
- Protocol-based VLAN with 16 entries.
- VLAN Translation.
- Double tagging.
  - UNI/NNI configuration per port for edge access application.
  - QinQ packet transmission through NNI port.
  - Programmable global SP_TPID.
  - Programmable SP_VID through flexible mapping.
- Link Aggregation support with automatic link fail-over.
- Programmable per-port Bandwidth/Rate control.
- Protected port security feature.
- Port mirroring (Ingress/Egress), IGMP Layer 3. snooping and MLD snooping.
- Spanning Tree support (802.1d/1s/1w).
- Supports 802.1x EAPOL higher layer protocol.
- Programmable Broadcast, Multicast, and Unknown Unicast storm control.8K MAC addresses with automatic learning and aging.
- MDC/MDIO and SPI interfaces.
- 4K-entry Multicast Address table.
- Hardware supports SNMP, RMON.
- Internal oscillator simplifies design and reduces cost.
- JTAG.
- 2.5V and 1.2V, typical power consumption: ~ 4.3W.
- 676-pin PBGA package.

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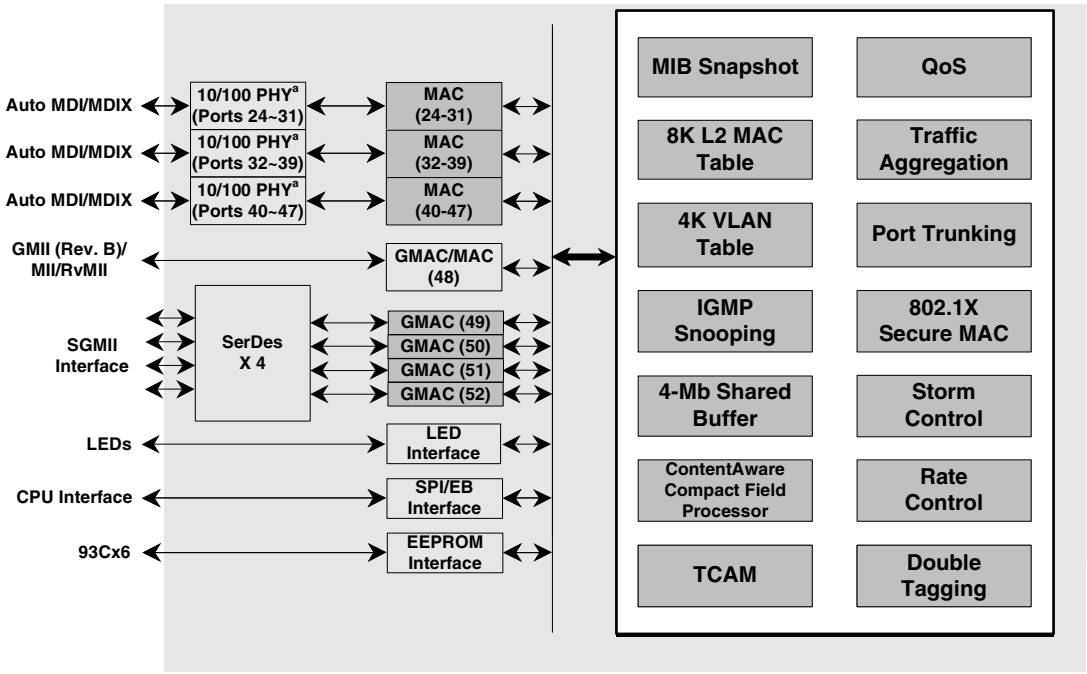

[a] Broadcom SDK maps these ports to logical ports 0, 1, … and 23 respectively

Figure 1: Functional Block Diagram

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REVISION HISTORY

Revision	*Date*	*Change Description*
53262M-DS302-R	07/28/11	**Updated:** • Table 48: "Hardware Signal Descriptions," on page 137 • Table 64: "LED Control Register (Page 00h: Address 5Ah)," on page 175 • Table 255: "802.1Q Control 3 Register (Pages: 34h, Address 08h–0Fh)," on page 304 • Table 291: "Port MIB Registers (Page 68h–84h)," on page 336 **Removed:** • Second note in "Programming Example" on page 86.
53262M-DS301-R	04/15/09	**Updated:** • Figure 49, "BCM53262 LED Register Structure Diagram," on page 113. • General: Low-power mode is not supported.
53262M-DS300-R	04/30/08	Initial release

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About This Document

Purpose and Audience

This document provides details of the functional, operational, and electrical characteristics of the Broadcom® BCM53262M. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

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Section 1: Introduction

Overview

The Broadcom® BCM53262M is a single-chip, 24-port 10/100Base-TX and 4-port 10/100/1000Base-T SGMII switch device. This device integrates the following functions:

- 24 fully integrated 10/100Base-TX/EFX compatible PHY transceivers
- Four-port 10/100/1000 SGMII interface
- 25 integrated 10/100 MACs
- Management Port with RvMII/MII interface (Rev. A)
- Management Port with RvMII/MII/GMII interface (Rev. B)
- A Serial Peripheral Interface (SPI) and MDC/MDIO Interface allowing the device to be custom-configured
- Flexible TCAM-based Compact Field Processor
- High speed management EB Bus for register access
- High-performance integrated packet buffer memory
- An address resolution engine
- Nonblocking switch controller
- Set of Management Information Base (MIB) statistics registers

The Serial Peripheral Interface allows the device to be custom-configured and bridge management to be implemented.

The integrated 10/100Base-TX transceivers perform all the physical layer interface functions for 100Base-TX full-duplex or half-duplex Ethernet on CAT-5 twisted pair cable and 10Base-T full-duplex or half-duplex Ethernet on CAT-3, -4, or -5 cable. Each of the integrated transceiver ports of the BCM53262M connects directly to the network media through isolation transformers. The integrated transceiver is fully compliant with the IEEE 802.3 and 802.3u standards.

Each MAC supports full and half-duplex for 10 Mbps and 100 Mbps and the Gigabit MACs additional support full-duplex operation at 1 Gbps. Flow control is provided in half-duplex mode with backpressure. In full-duplex mode, 802.3x frame-based flow control is provided. The MAC is 802.3 compliant and supports a maximum frame size of 2048 bytes.

The BCM53262M supports advanced ContentAware™ processing via a Compact Fast Field Processor (CFP). Up to three intelligent ContentAware processes are performed in parallel for every packet. This flexible engine uses a TCAM-based architecture with wildcard capabilities; specific areas of the incoming packet to be masked and matched can be defined. Furthermore, multiple actions can be performed per packet as a result of a match. Action examples include dropping, changing of the port forwarding map, changing priority of frame, etc. These advanced ContentAware processes are well suited for both Access Control List and Security protection, for example, DOS prevention.

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An integrated address management engine provides address learning and recognition functions at maximum frame rates. The address table provides capacity for up to 8K unicast and multicast addresses. Addresses are added to the table after receiving an error-free packet. Broadcast and multicast frames are forwarded to all ports within the VLAN domain except the port where it was received.

The MIB statistics registers collect receive and transmit statistics for each port, and provide direct hardware support for the Etherlike MIB, Bridge MIB, MIB II (Interfaces), and the first four groups of the RMON MIB. All nine groups of RMON can be supported by using additional capabilities, such as port mirroring/snooping, together with an external microcontroller to process some MIB attributes. The MIB registers can be accessed through the Serial Peripheral Interface Port by an external microcontroller.

Audience

This document is for designers interested in integrating the BCM53262M switch into their hardware designs, and others who need specific data about the physical characteristics and operation of the BCM53262M switch.

Data Sheet Information

The following notational conventions are used in this document:

- Signal names are shown in UPPERCASE letters. For example: DATA
- A bar over a signal name indicates that it is active low. For example: $\overline{CE}$.
- In register and signal descriptions, [n:m] indicates a range from bit n to bit m. For example: [7:0] indicates bits 7 through 0, inclusive.
- The use of R or RESERVED indicates that a bit or field is reserved by Broadcom for future use. Typically R is used for individual bits and RESERVED is used for fields.
- Numerical modifiers such as K or M follow traditional usage. For example, 1 KB means 1,024 bytes, 100 Mbps (referring to Fast Ethernet speed) means 100,000,000 bits per second, and 133 MHz means 133,000,000 Hertz.

Where it seems helpful, cross-reference links have been incorporated in the data sheet. The cross-reference is denoted in blue text. When using a PDF version of the data sheet, jump to other sections of the data sheet by clicking on the blue text using the PDF hand tool.

> ***Example:*** Clicking on the text: "Features and Operation" on page 36 jumps to the next section. To return, press the left-arrow key while holding down the alt key. It returns to the previous view. Likewise, pressing the right-arrow key while holding down the alt key jumps to next view.

As always, every effort is made to improve the data sheet and other documentation. To submit suggestions, send e-mail to RoboDocs@broadcom.com. For technical questions, please contact your local sales representative.

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Section 2: Features and Operation

Overview

The BCM53262M includes the following features:

- "Quality of Service" on page 37
- "Port-Based VLANs" on page 42
- "802.1Q VLANs" on page 43
- "MAC-based VLANs" on page 43
- "Protocol-based VLANs" on page 43
- "Customer-Tag-Based VLANs" on page 43
- "Double Tagging" on page 45
- "Link Aggregation" on page 51
- "Rate Control" on page 52
- "Protected Ports" on page 54
- "Port Mirroring" on page 55
- "IGMP and MLD Snooping" on page 56
- "Jumbo Frame Support" on page 56
- "802.1x Port-Based Security" on page 56
- "Dynamic Secure MAC Mode" on page 57
- "Address Management" on page 57
- "Bridge Management" on page 63
- "Compact Field Processor" on page 65
- "Packet Remarking" on page 73
- "VID Replacement" on page 74

Each topic is discussed in more detail in the following sections.

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Quality of Service

The Quality of Service (QoS) feature provides up to four internal queues per port to support four different traffic priorities. These priorities can be programmed in such a way that higher-priority traffic experiences less delay in the switch under congested conditions than the latency of lower-priority traffic. This can be important in minimizing latency for delay-sensitive traffic. The BCM53262M can assign the packet to one of the four egress transmit queues according to information in:

- "Port-Based QoS" on page 38 (ingress port ID)
- "802.1p QoS" on page 38
- "Protocol-Based QoS" on page 39
- "MAC SA-Based QoS" on page 39
- "DiffServ Based QoS" on page 40
- "Reason Code Based QoS" on page 41

Note: Only 1Q or 4Q mode is supported

Note: As a part of the QoS discussion, it is important to understand the BCM53262M Egress port Queue structure.

Egress Transmit Queues

Each egress port can support up to four transmit queues. Each egress transmit queue contains a list specifying the packet transmission order. Every incoming frame is forwarded to one of the four egress transmit queues of the assigned egress port, based on its priority. The egress port transmits packets from each of the four transmit queues according to a configurable scheduling algorithm, which can be a combination of Strict Priority (SP) and/or Weighted Round Robin (WRR). The following scheduling algorithm combinations are available in the BCM53262M:

- Four Strict Priority queues
- Four Weighted Round Robin queues
- One Strict Priority and three Weighted Round Robin queues
- Two Strict Priority and two Weighted Round Robin queues

When a queue is designated as the strict-priority queue, all other lower-priority queues are prevented from transmitting packets until the strict-priority queue is empty. Furthermore, the traffic at each egress port is gated by a Shaper, so that the aggregated output from the queues can be scheduled by a programmable Egress Rate Control, with a granularity of 64 Kbps. Egress Rate Control details are further described within this data sheet.

Figure 2 shows the Shaping-Scheduling structure of each Egress port.

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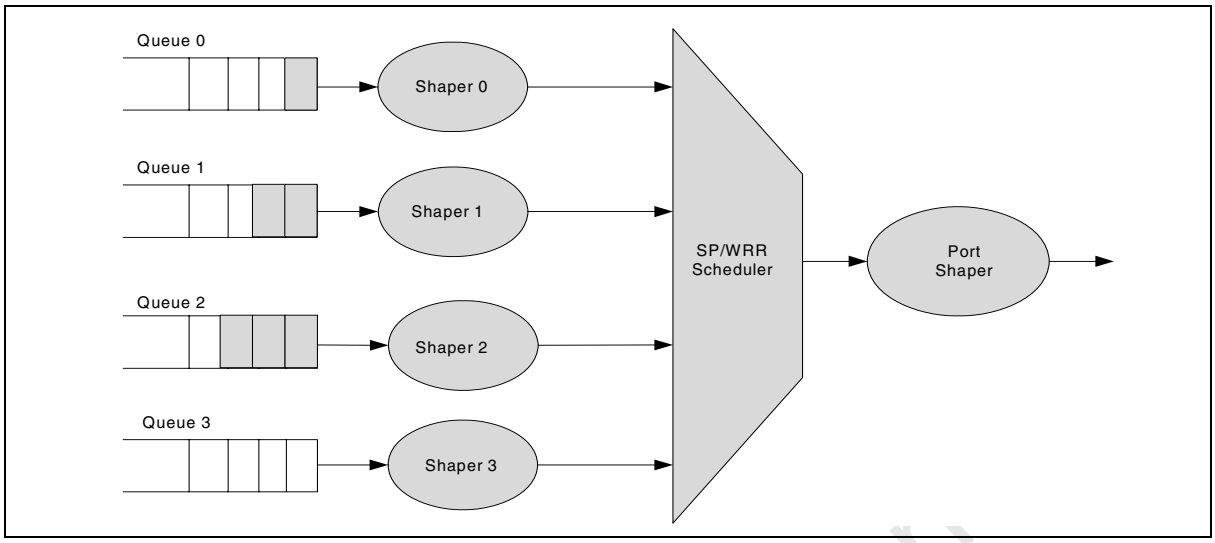

Figure 2: Shaping-Scheduling Structure of Each Egress port

Port-Based QoS

When using the port-based priority mechanism, the port-based priority of each ingress port determines the egress queue assigned to frames arriving via the associated ingress port. The frames will be assigned to the priority queue based on the upper 3-bit per port COS value programmed in the 802.1Q Default Port Tag.

Follow the sequence below to enable Port-Based QoS:

1). Enable bit[63], as shown in Table 238: “QoS Control Register (Pages: 30h, Address 10h–17h),” on page 287.

2). Enable bits[59:58] of QoS Control register.

3). Program the upper 3-bit of per-port COS value as shown in Table 258: “802.1Q Default Port Tag Register (Page: 34h, Address 40h–79h),” on page 307.

4). To select the desired queue, program the register shown in Table 242: “Priority Threshold Register (Page 30h: Address 30h–31h),” on page 290.

802.1p QoS

When using 802.1p priority mechanism, the packet is examined for the presence of a valid 802.1p priority tag. If the tag is present, the packet is assigned to a programmable egress queue based on the value of the tagged priority. The tagged priority can be designated to any of the available queues.

Follow the sequence below to enable 802.1p QoS:

1). Enable bit[63], as shown in Table 238: “QoS Control Register (Pages: 30h, Address 10h–17h),” on page 287.

2). Enable bits[59:58] of QoS Control register.

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3). To select the desired queue, program the register shown in Table 242: “Priority Threshold Register (Page 30h: Address 30h–31h),” on page 290.

Protocol-Based QoS

When using Protocol Based QoS, the EtherType field carried with the incoming packet is used to map the packet to one of the available output queues at the destination port. Protocol-based QoS shares the same control bit and 16-entry Protocol to VLAN mapping table with Protocol-based VLAN. The upper 3-bit in the Protocol to VLAN mapping table is used to program the Protocol-Based priority select field. This mapping can be enabled/disabled per port, but the mapping table is configured globally.

Follow the sequence below to enable Protocol-Based QoS:

1. Enable bit[63], of the QoS Control register (see Table 238: “QoS Control Register (Pages: 30h, Address 10h–17h),” on page 287).
2. Enable bits[59:58] of the QoS Control register.
3. Program the 3-bits of the per-port COS value in the Protocol to VLAN mapping table. (see TBL_DATA_0[30:28] of Table 135: “Multitable Data 0 Register (Page 05h: Address 38h–3Fh),” on page 231
4. To select the desired queue, program the Priority Threshold Register (see Table 242: “Priority Threshold Register (Page 30h: Address 30h–31h),” on page 290).
5. Program the Protocol to VLAN Control register (see Table 264: “Protocol To VLAN Control Register (Pages: 34h, Address B0h–B7h),” on page 313) to enable/disable per-port Protocol-Based QoS.

MAC SA-Based QoS

When using MAC SA-Based QoS, the source address field carried with the incoming packet is used to map the packet to one of the available output queues at the destination port. MAC-Based QoS shares the same control bit and 512-entry MAC to VLAN mapping table with MAC-Based VLAN. The upper 3-bits in the MAC to VLAN mapping table is used to program the MAC-Based priority select field. This mapping can be enabled/disabled per port, but the mapping table is configured globally.

Follow the sequence below to enable MAC SA-Based QoS:

1. Enable bit[63], of the QoS Control register (see Table 238: “QoS Control Register (Pages: 30h, Address 10h–17h),” on page 287).
2. Enable bits[59:58] of the QoS Control register.
3. Program the 3-bits of the per-port COS value in the MAC to VLAN mapping table. (see TBL_DATA_0[62:60] of Table 135: “Multitable Data 0 Register (Page 05h: Address 38h–3Fh),” on page 231
4. To select the desired queue, program the Priority Threshold Register (see Table 242: “Priority Threshold Register (Page 30h: Address 30h–31h),” on page 290).
5. Program MAC to VLAN Control register. See Table 263: “MAC To VLAN Control Register (Pages: 34h, Address A8h–AFh),” on page 312) to enable/disable per port MAC-Based QoS.

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DiffServ Based QoS

When using the DiffServ priority mechanism, the packet is classified based on the DSCP field in the IP header. If the tag is present, the packet is assigned to a programmable egress queue based on the value of the tagged priority. The tagged priority can be designated to any of the available queues.

Follow the sequence below to enable DiffServ-Based QoS:

1. Enable bit[63], of the QoS Control register (see Table 238: "QoS Control Register (Pages: 30h, Address 10h–17h)," on page 287).
2. Enable bits[59:58] of the QoS Control register.
3. To select the desired queue, program the Table 243: "DiffServ DSCP Priority Register 1 (Page 30h: Address 40h–47h)," on page 291) and Table 244: "DiffServ DSCP Priority Register 2 (Page 30h: Address 48h–4Fh)," on page 291.

QoS Resolution Tree

The resolution tree shown in the next figure determines which priority based QoS is used. There are two levels of determining which queue of egress port the packet is going to be assigned. The first level of how incoming packet QoS is determined is shown in Figure 3, the QoS value from the first level QoS resolution is then muxed with the QoS value from the Compact Field Processor to be the final QoS value for the egress queue. The second level QoS resolution tree is shown in Figure 4 on page 42.

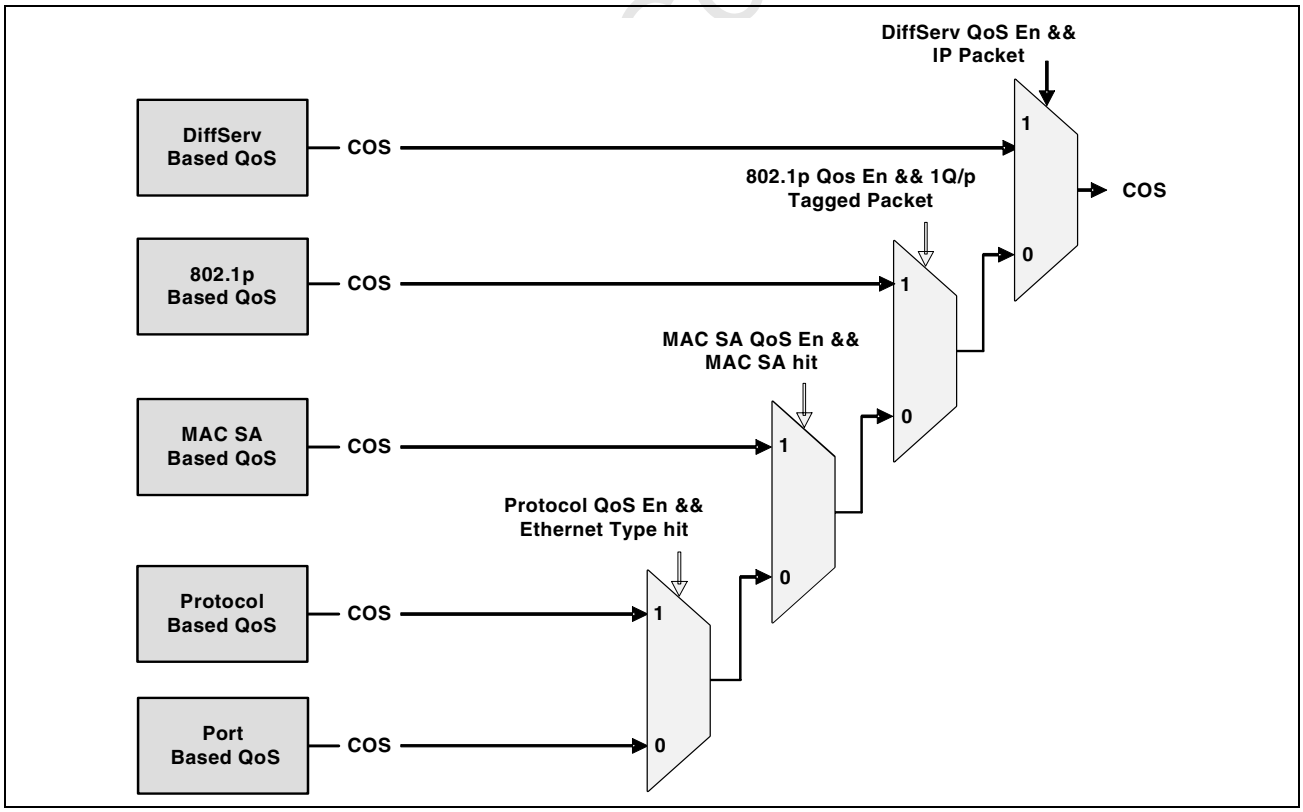

Figure 3: First Level QoS Resolution Tree

Reason Code Based QoS

When the IMP port is configured as the management port, the BCM53262M provides a Reason Code Based QoS for packets being forwarded to the CPU through the IMP port. When the IMP port is configured as a regular data port, the packets are forwarded based on the QoS schemes mentioned above.

Table 1 lists the conditions where packets can be forwarded to the CPU, descriptions, and their default QoS levels. Note that the default QoS values are configurable (see Table 245: "QoS Reason Code Enable Register (Page 30h: Address 58h–59h)," on page 292). The QoS value for Mirroring and SA Learning conditions must be programmed with a lower, or equal value, compared to the other conditions. This prevents out-of-order flow delivery of identical packets to the CPU.

Table 1: Reasons and QoS for CPU Traffic

Condition	*Description*	*Default QoS level*
Mirroring	The packet is forwarded (copied) through the IMP port because it needs to be mirrored to the CPU as the capturing port.	0
SA learning	The packet is forwarded through the IMP port because the SA must be learned by the CPU.	0
Switching	The packet is forwarded through the IMP port, either because the CPU is one of the intended destination hosts of the packet, or because the switch logic determines to flood the packet to all potential destinations.	2
Protocol Termination	The packet is forwarded through the IMP port because it implies an IEEE 802.1 defined L2 protocol that needs to be terminated by the CPU.	3
Protocol Snooping	The packet is forwarded through the IMP port because it implies an L3 or application level protocol that needs to be monitored by the CPU for network security or operation efficiency.	2
Exception Processing/ Flooding	The packet is forwarded through the IMP port for some special processing even though the CPU is not the intended destination or because the switch makes the flooding decision to reach all potential destinations.	1

The Figure 4 shows the complete QoS Resolution tree structure.

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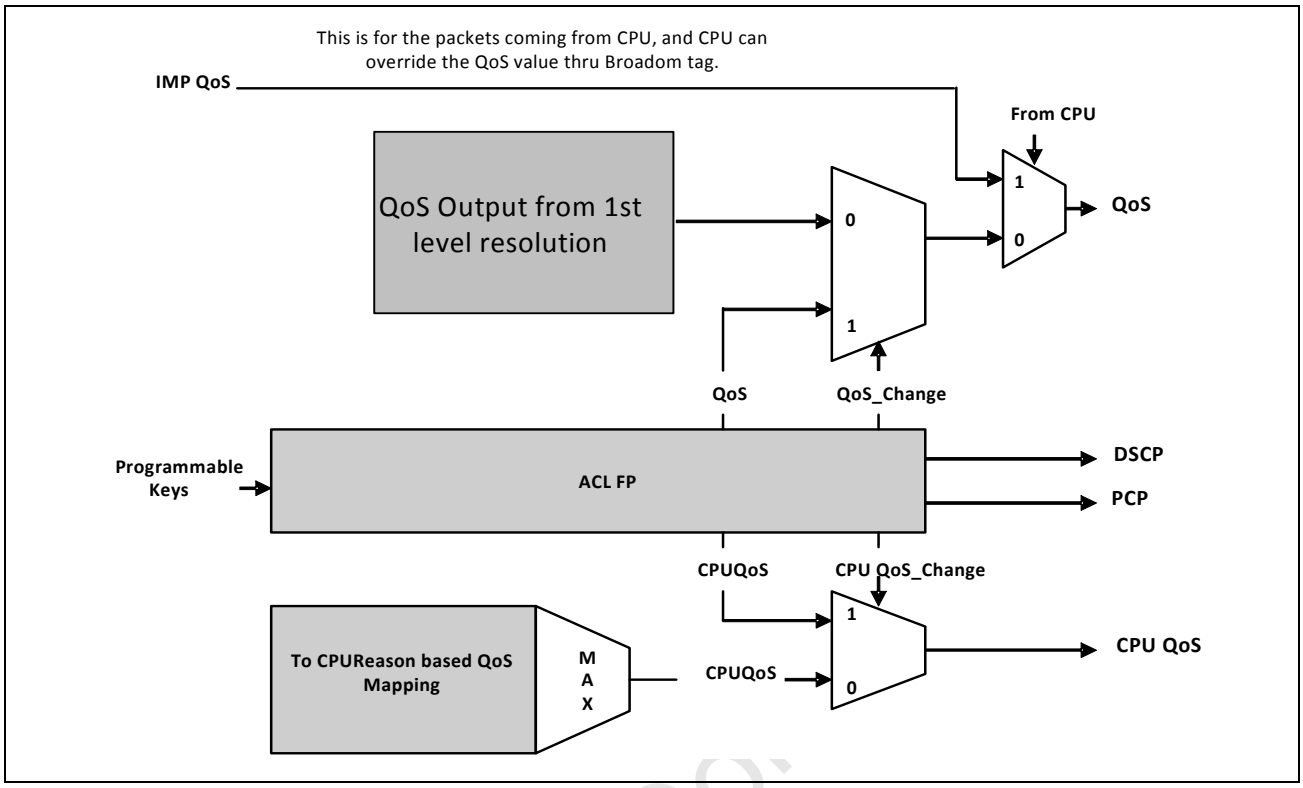

Figure 4: Final level QoS Resolution Tree

Port-Based VLANs

The port-based virtual LAN (VLAN) feature partitions the switching ports into virtual private domains designated on a per port basis. Data switching outside of the port's private domain is not allowed. The BCM53262M provides flexible VLAN configuration for each ingress (receiving) port.

The port-based VLAN feature works as a filter, filtering out traffic destined to nonprivate domain ports. The private domain ports are selected for each ingress port. Because the port selection is individual to each ingress port, it is possible for two ingress ports to not be granted bi-directional access. For each received packet, the ARL resolves the DA and obtains a forwarding vector (list of ports to which the frame shall be forwarded). The ARL then applies the VLAN filter to the forwarding vector, effectively masking out the nonprivate domain ports. The frame is only forwarded to those ports that meet the ARL table criteria, as well as the port-based VLAN criteria.

802.1Q VLANs

The BCM53262M supports IEEE 802.1Q VLAN and up to approximately 4K VLAN table entries that reside in the internal embedded memory. Once the VLAN table is programmed and maintained by the CPU, the BCM53262M will autonomously handle all protocol operations. These actions include the stripping or adding of the 802.1Q tag depending on the requirements of the individual transmitting port. It also performs all VLAN and MAC L2 lookups necessary to determine the correct packet routing.

MAC-based VLANs

The BCM53262M supports MAC-based VLAN and up to 512 VLAN table entries that reside in the internal embedded memory. When the MAC-based VLAN is enabled, the VID is derived through the mapping table indexed by the MAC Source Address field embedded in the incoming packet. This mapping can be enabled/disabled per port, but the mapping table is configured globally. Once the VLAN mapping table is programmed and maintained by the CPU, the BCM53262M will autonomously handle all operations of the protocol.

Protocol-based VLANs

The BCM53262M supports Protocol-based VLAN and up to 16 VLAN table entries that reside in the internal embedded memory. When Protocol-based VLAN is enabled, the VID is derived through the mapping table indexed by the EtherType field embedded in the incoming packet. This mapping can be enabled/disabled per port, but the mapping table is configured globally. Once the VLAN mapping table is programmed and maintained by the CPU, the BCM53262M will autonomously handle all operations of the protocol.

Flow-based VLANs

The BCM53262M supports Flow-based VLAN. For more details, see “VID Replacement” on page 74.

Customer-Tag-Based VLANs

The BCM53262M supports customer-tag-based VLANs and up to 4K VLAN table entries that reside in the internal embedded memory. When customer-tag-based VLAN is enabled, the VID is derived through the mapping table indexed by the customer-tag VID embedded in the incoming packet. Each mapping entry may be configured for VLAN appending (Double Tagging) or VLAN replacement (VLAN Translation) operation. Once the VLAN mapping table is programmed and maintained by the CPU, the BCM53262M will autonomously handle all operations.

The Figure 5 shows the VLAN resolution tree.

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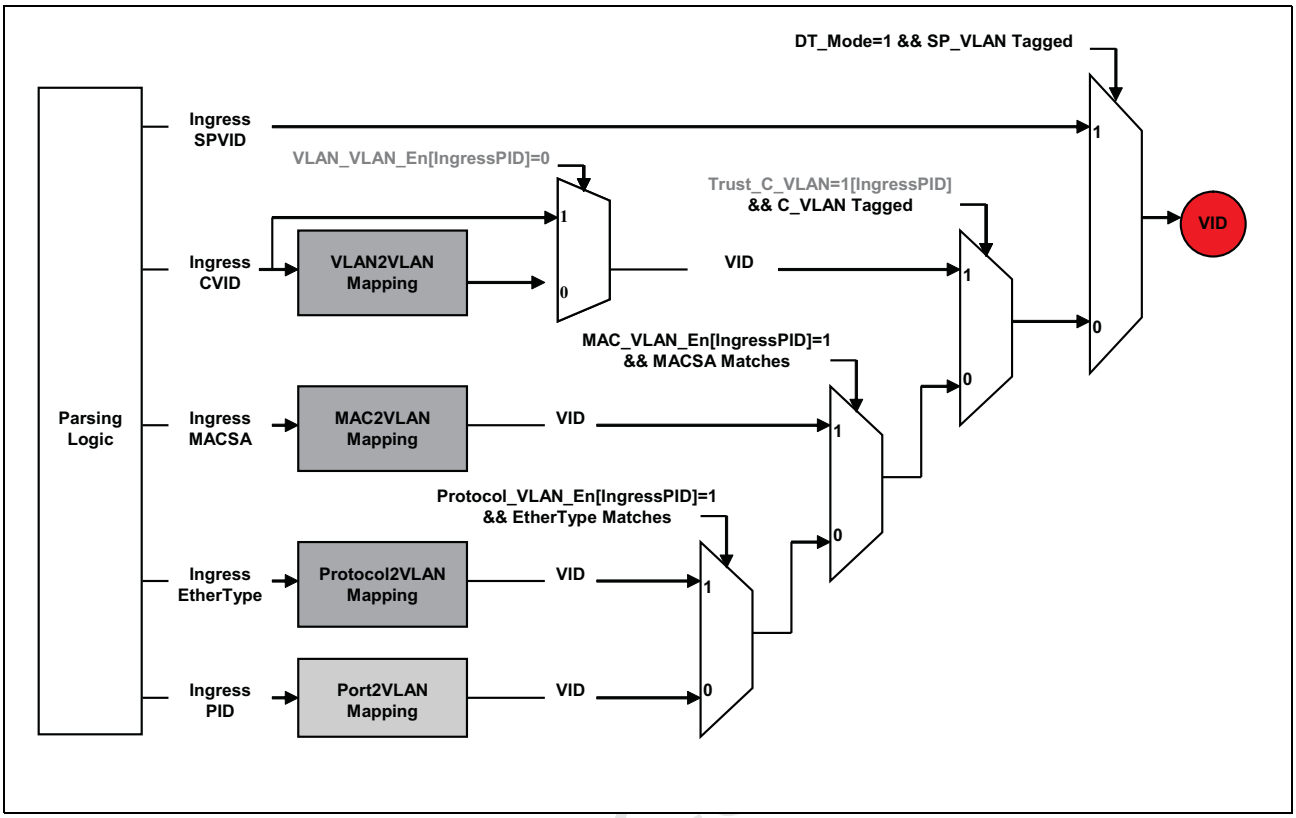

Figure 5: VLAN Resolution Tree

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Double Tagging

BCM53262M can be configured to operate either in Double Tagging mode for Edge Access Network Switching applications, or in Nondouble Tagging mode for traditional Local Area Network Switching applications. The Double Tagging mode is also referred as QinQ.

In **Double Tagging** mode,

- An Ethernet port can be configured either as a Network-Network Interface (NNI) port or as a User-Network Interface (UNI) port.
- There are four possible traffic profiles. Each possible traffic profile is described below, and illustrated in diagrams.
  - Incoming packets from NNI, and being forwarded to NNI (applies to Edge Access application)
  - Incoming packets from UNI, and being forwarded to NNI (applies to Edge Access application)
  - Incoming packets from NNI, and being forwarded to UNI
  - Incoming packets from UNI, and being forwarded to UNI

NNI to NNI

The numbered process described below corresponds to the number in the diagram.

1. Over a NNI/NNI link, all incoming packets are expected to have a Service Provider (SP) Tag for normal switching traffic forwarding or untagged for peer CPU communication across the NNI link. (C-tagged (customer) or Priority-tagged packets are not supposed to be forwarded across a NNI link.
2. VLAN table is dedicated for Service Provider domain VLAN control.(The VID used to index the VLAN table is Service Provider Control for packet forwarding and learning operation, and the untag control can strip SP_Tag only.)
3. With the Double Tagging (QinQ) process being performed, the VLAN translation operations are performed concurrently, either through the ingress VLAN remapping operations, or through the CFP action with the egress VLAN remapping operations.
4. Local CPU generated packets (incoming packets through IMP port with Broadcom tag) have options to preserve the untagged status or to be processed as normal input packets.

Figure 6 shows how the extra (SP) tag is added to the incoming packets (tagged or untagged), and how the added tag can be output as is or be replaced.

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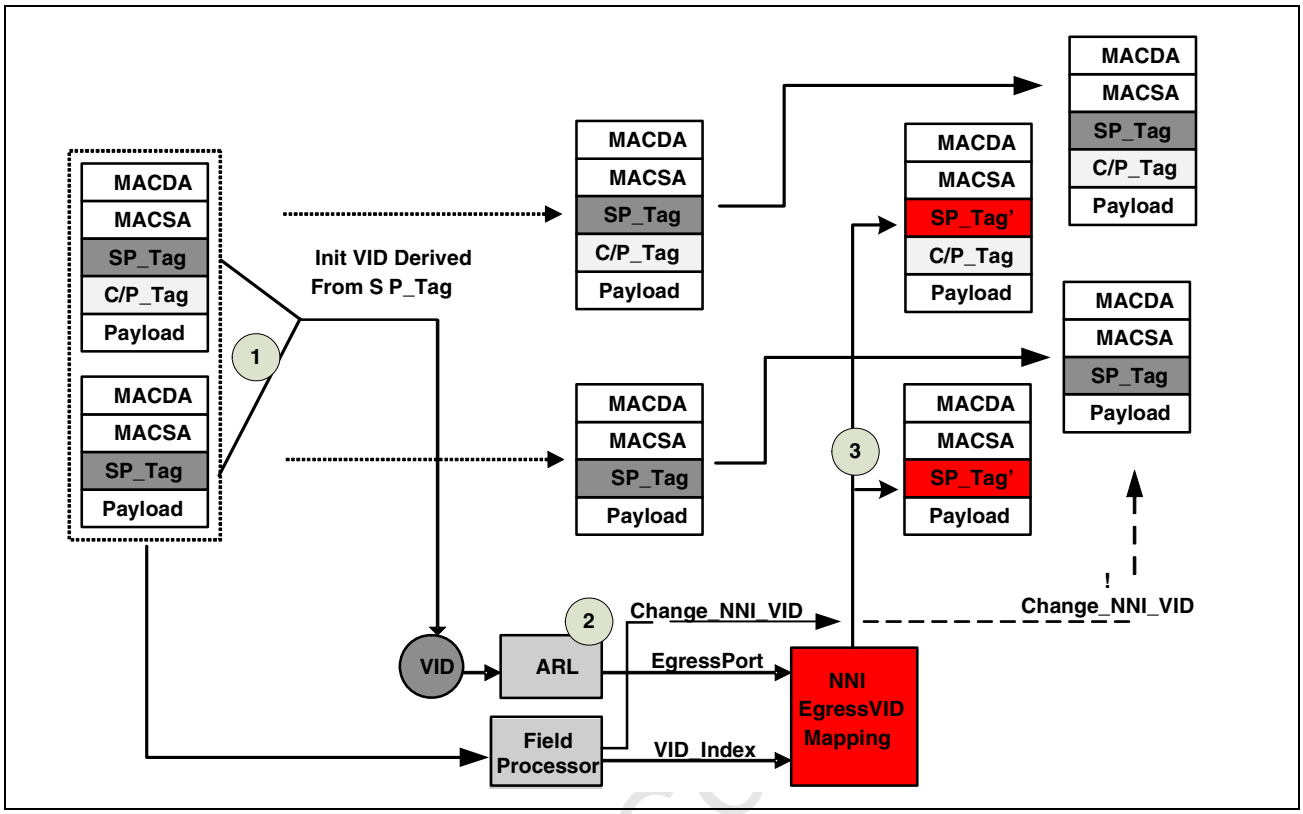

Figure 6: NNI to NNI Tag Handling

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UNI to NNI

The numbered process described below corresponds to the number in the diagram.

1. Over a UNI/NNI link, incoming packets can be Untagged, Priority tagged, or C tagged. (SP-tagged packets should not be forwarded across an UNI link.
2. When an incoming packet from a UNI (customer) port is received, the packet is processed through the initial VID generation process (Port/ Protocol/ MACSA/ C_VID-based mapping) to generate an SP tag and the SP tag is used to access the ARL table.
3. If the process is QinQ (double tagging or VLAN translation), the SP tag can be added as an outer tag, or the SP tag can be used to replace the original customer tag.
4. With the Double Tagging (QinQ) process being performed, the VLAN translation operations are performed through the CFP action with the egress VLAN remapping operations. If the matched rule indicates VID is present, the SP tag is replaced with the newly mapped SP tag at the NNI port for transmission.
5. Local CPU generated packets (incoming packets through IMP port with Broadcom tag) have options to preserve the untagged status or to be processed as normal input packets.

Figure 7 shows how the extra (SP) tag is added to the incoming packets (tagged or untagged), and how the added tag can be output as is or be replaced.

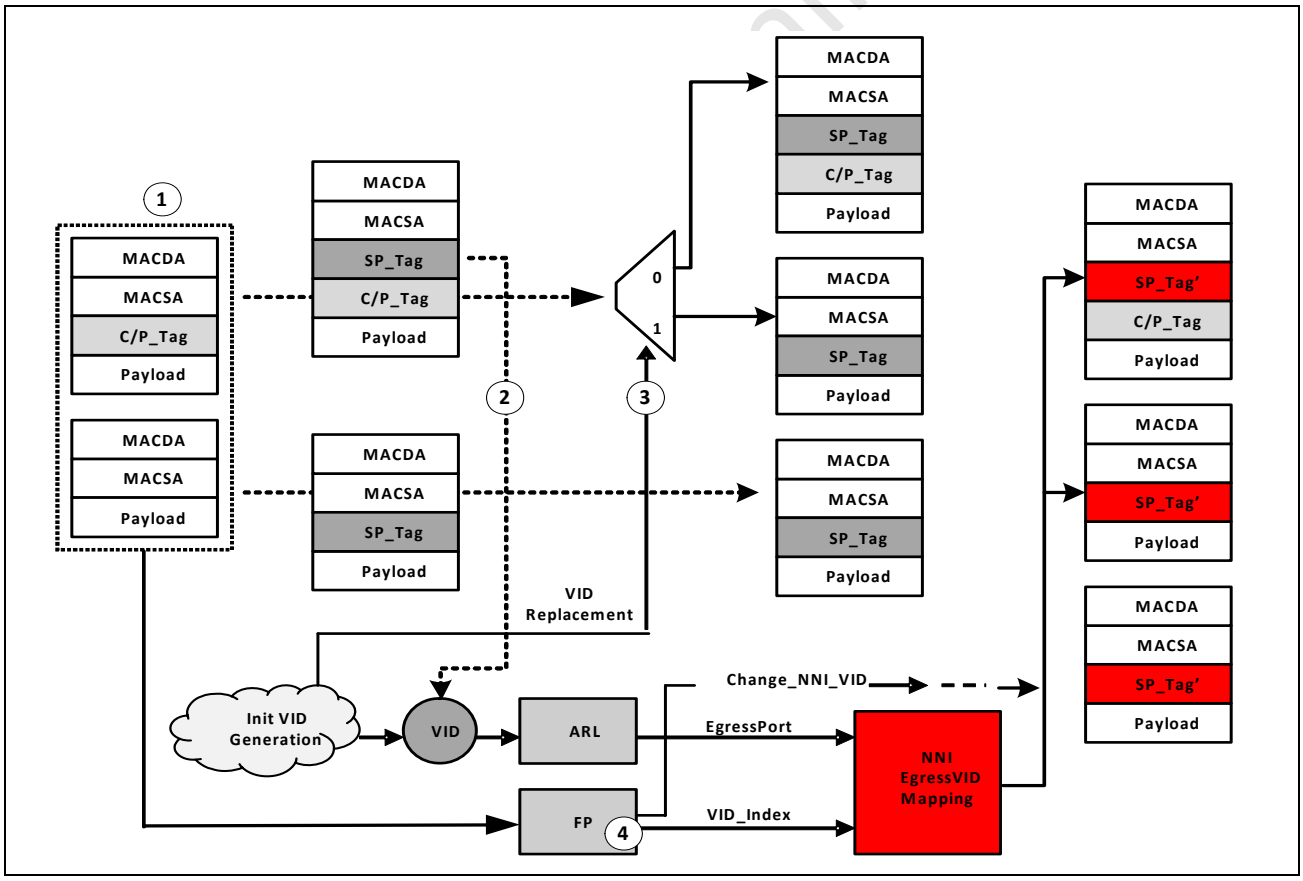

Figure 7: UNI to NNI

NNI to UNI

The numbered process described below corresponds to the number in the diagram.

1. Over a NNI/UNI link, all incoming packets are expected to have a Service Provider (SP) Tag for normal switching traffic forwarding or untagged for peer CPU communication across the NNI link. (C-tagged (customer) or Priority-tagged packets are not supposed to be forwarded across a NNI link.
2. VLAN table is dedicated for Service Provider domain VLAN control. The VID used to index the VLAN table is Service Provider Control for packet forwarding and learning operation, and the untag control can strip SP_Tag only.
3. With the Double Tagging (QinQ) process being performed, the VLAN translation operations are performed concurrently, either through the ingress VLAN remapping operations, or through the CFP action with the egress VLAN remapping operations.
4. Local CPU generated packets (incoming packets through the IMP port with a Broadcom tag) have options to preserve the untagged status or to be processed as normal input packets.

Figure 8 shows how the extra (SP) tag is added to the incoming packets (tagged or untagged), and how the added tag can be output as is or be replaced.

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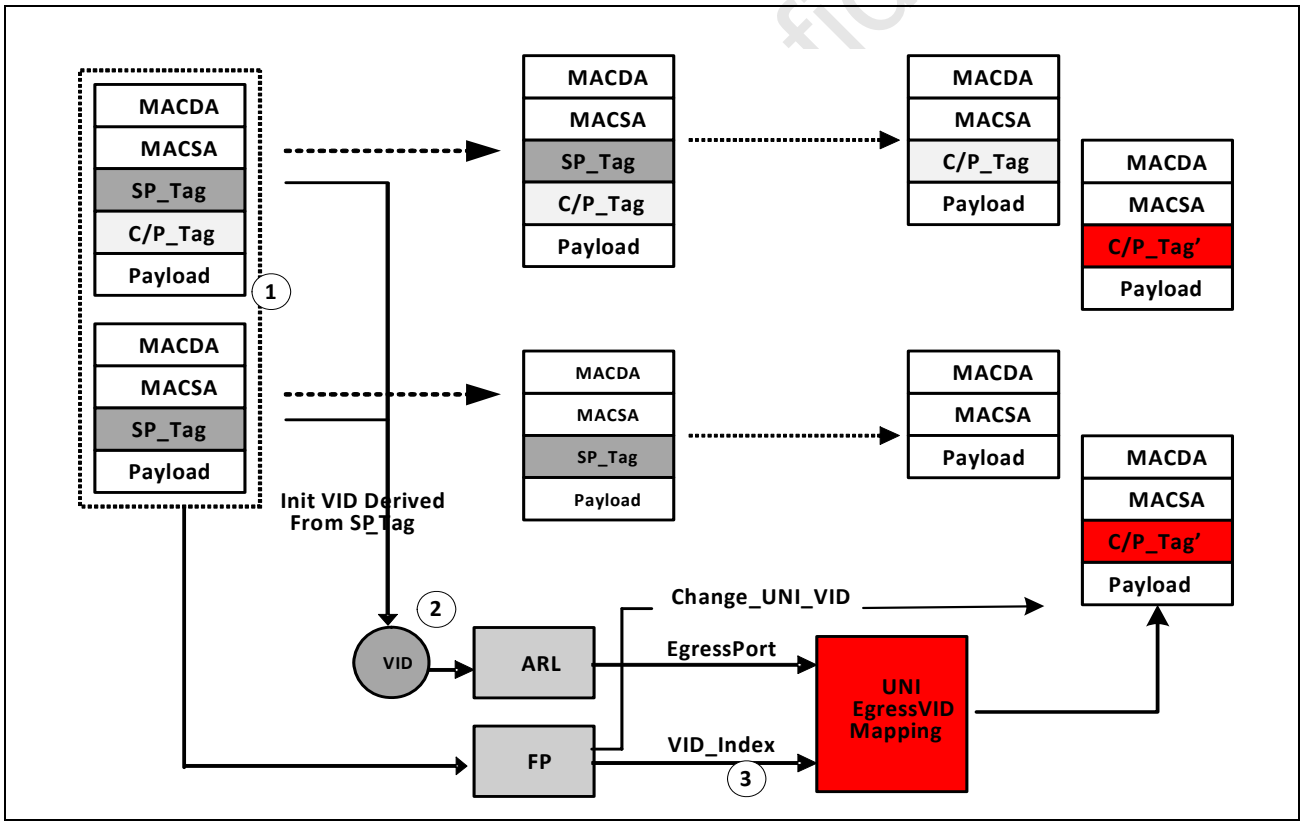

Figure 8: NNI to UNI

UNI to UNI

The numbered process described below corresponds to the number in the diagram.

1. Over a UNI/UNI link, incoming packets can be Untagged, Priority tagged, or C tagged. (SP-tagged packets are not supposed to be forwarded across a UNI link.
2. VLAN table is dedicated for Service Provider domain VLAN control. (The VID used to index the VLAN table is Service Provider Control for packet forwarding and learning operation, and the untag control can strip SP_Tag only.)
3. With the Double Tagging (QinQ) process being performed, the VLAN translation operations are performed concurrently, either through the ingress VLAN remapping operations, or through the CFP action with the egress VLAN remapping operations.
4. Local CPU generated packets (incoming packets through IMP port with Broadcom tag) have options to preserve the untagged status or to be processed as normal input packets.

Figure 9 shows how the extra (SP) tag is added to the incoming packets (tagged or untagged), and how the added tag can be output as is or be replaced.

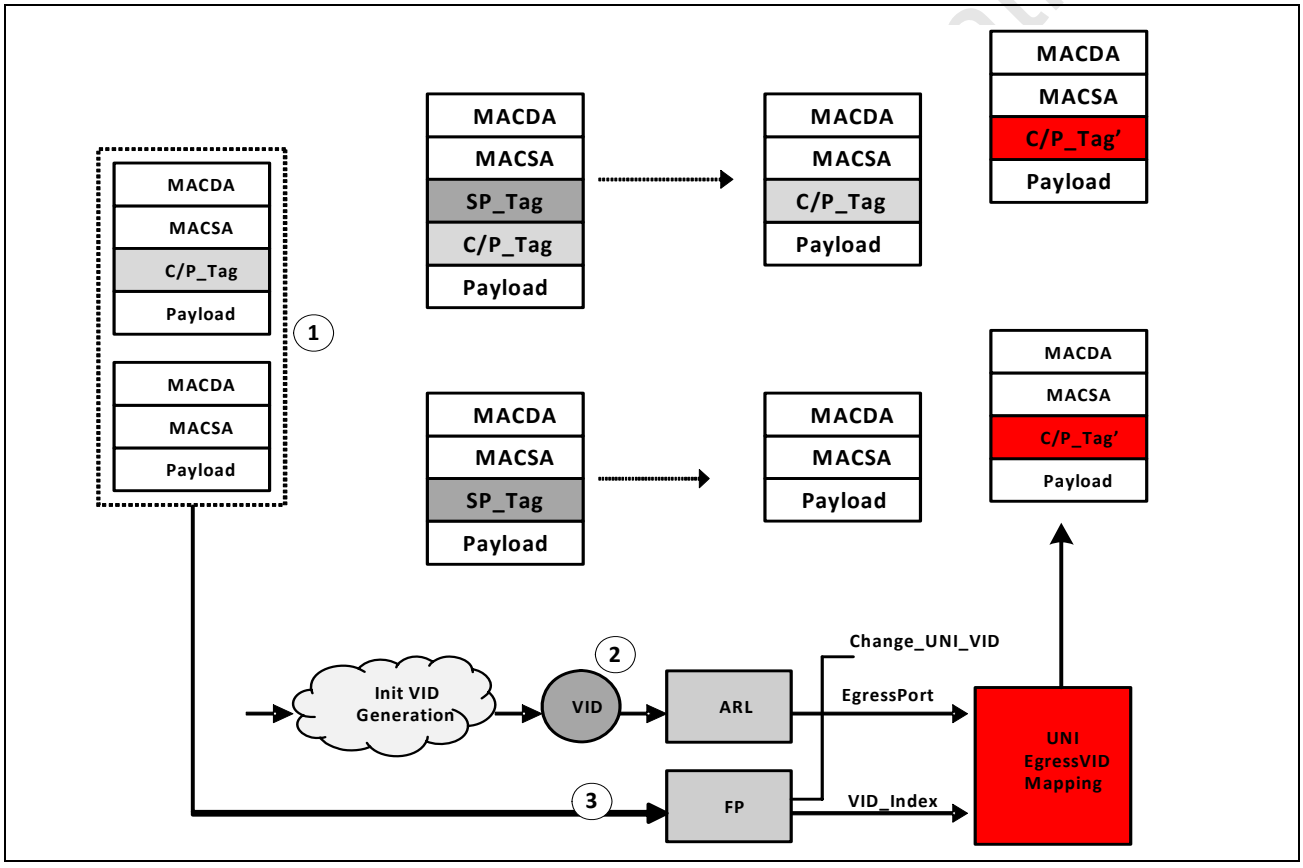

Figure 9: UNI to UNI

In **Non _ Double Tagging** mode, the following definitions will be used throughout the description of the Non-Double Tagging operation. See Figure 10.

- All Ethernet ports are treated same (as if they are all UNI ports).
- Incoming packets can be Untagged, Priority tagged, or C tagged. (SP-tagged packets are not supposed to be forwarded across an UNI link.)

- The VLAN Table is dedicated for Customer domain VLAN control. (The VID used to index the VLAN Table is Customer's property for packet forwarding and learning operations)
- Local CPU-generated packets have option to preserve the CPU intended untag status.
- The VLAN translation operation may be performed, either through the ingress VLAN remapping operations or through the CFP action with the egress VLAN remapping operations.

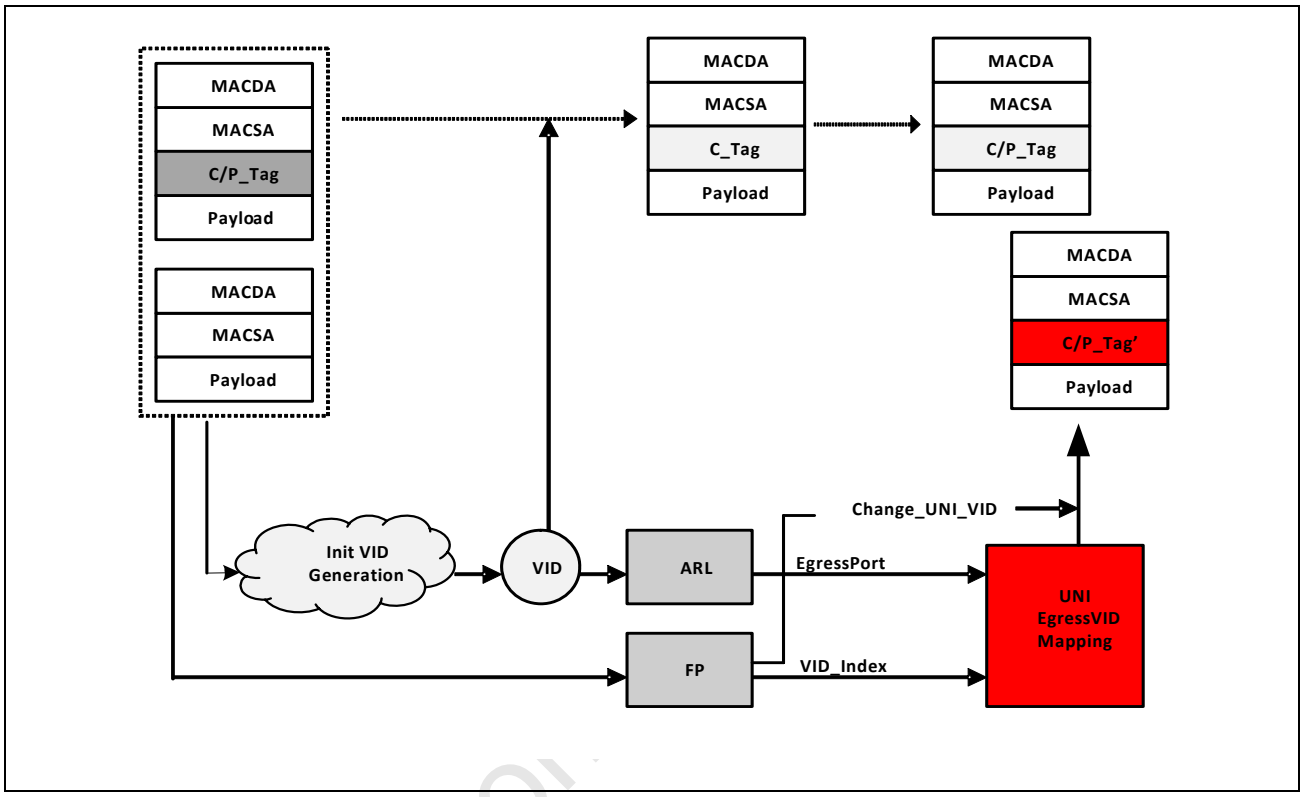

Figure 10: Non_Double Tagging Mode UNI to UNI

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Link Aggregation

The BCM53262M supports MAC-based aggregation. The aggregation feature allows up to eight ports to be grouped together as a single-link connection between two switch devices. This increases the effective bandwidth through a link and provides redundancy. BCM53262M allows up to 14 aggregation groups. Aggregations are composed of predetermined ports and can be enabled via a register. Ports within an aggregation group must be of the same linked speed. By performing a dynamic hashing algorithm on the MAC address, each packet destined for the aggregation is forwarded to one of the valid ports within the aggregation group. This method has several key advantages. By dynamically performing this function, the traffic patterns can be more balanced across the ports within an aggregation. In addition, the MAC-based algorithm provides dynamic failover. If a port within an aggregation group fails, the other ports within the aggregation automatically assume all traffic designated for the aggregation. It allows for a seamless, automatic redundancy scheme. This hashing function can be performed on either the DA, SA, IPv4DA, IPv4SA, or any combination of four depending on the Aggregation Hash Selector bit.

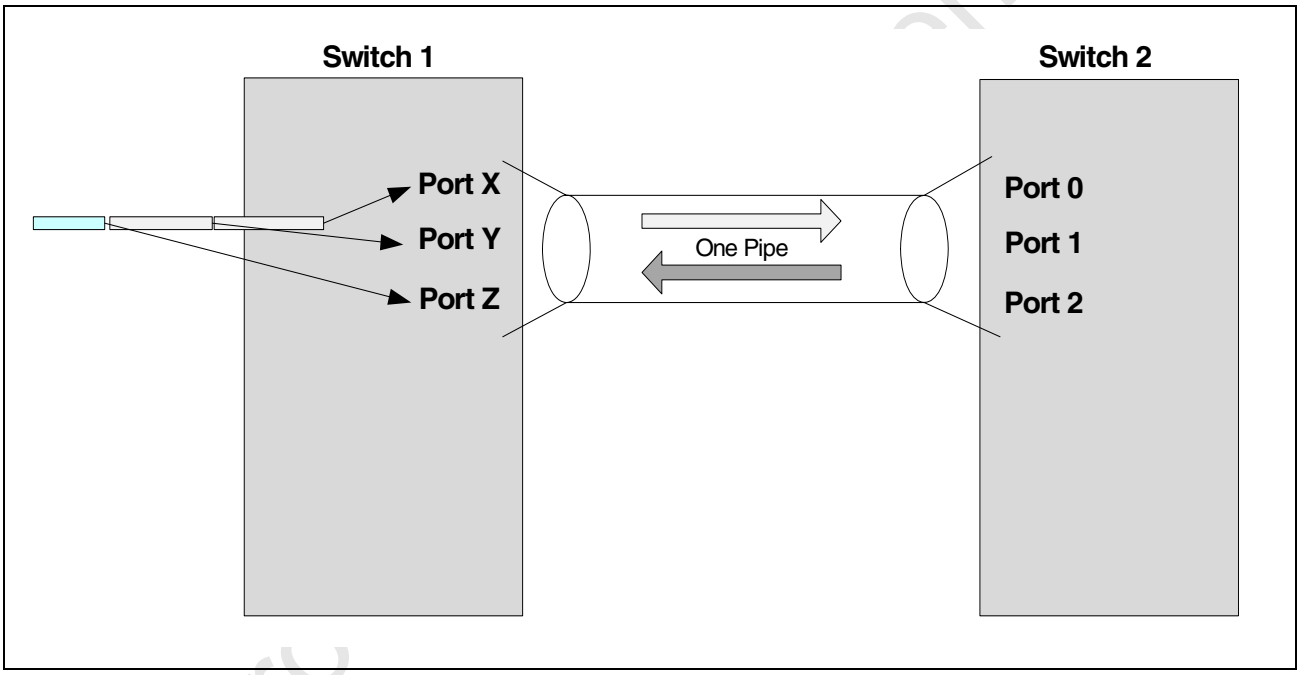

Figure 11: Link Aggregation

Rate Control

Forwarding broadcast traffic consumes switch resources, which can negatively impact the forwarding of other traffic. The rate-based broadcast storm suppression mechanism is used to protect regular traffic from an over abundance of broadcast or multicast traffic. This feature monitors the rate of ingressed traffic of programmable packet types. If the rates of these packet types exceed the programmable maximum rate, the packets are dropped or flow control is activated.

The broadcast storm mechanism works on a credit-based rate system that figuratively uses a bucket to track the bandwidth of each port (see Figure 12 on page 53) on the basis of egress or ingress data flow. Credit is continually added to the bucket at a programmable Bucket Bit Rate. Credit is decremented from the bucket whenever one of the programmable packet types is ingressed at the port. If no packets are ingressed for a considerable length of time, the bucket credit will continue to increase up to a programmable maximum bucket size. If a heavy burst of traffic is suddenly ingressed at the port, the bucket credit will become drained. When the bucket is emptied, incoming traffic will be constrained to the Bucket Bit Rate, the rate at which credit is added to the bucket. At this point, excess packets will be either dropped or deterred via flow control.

Egress Rate Control

The egress rate control employs a single bucket system to track the bandwidth usage of all egressed packets. Each port has the queue structure as shown in Figure 2 on page 38, each queue has a shaper can control the egress rate, and each port has a shaper can control the egress rate per port basis. The simple but effective method can be enabled on a per-port and per queue basis with a granularity of 64Kbps.

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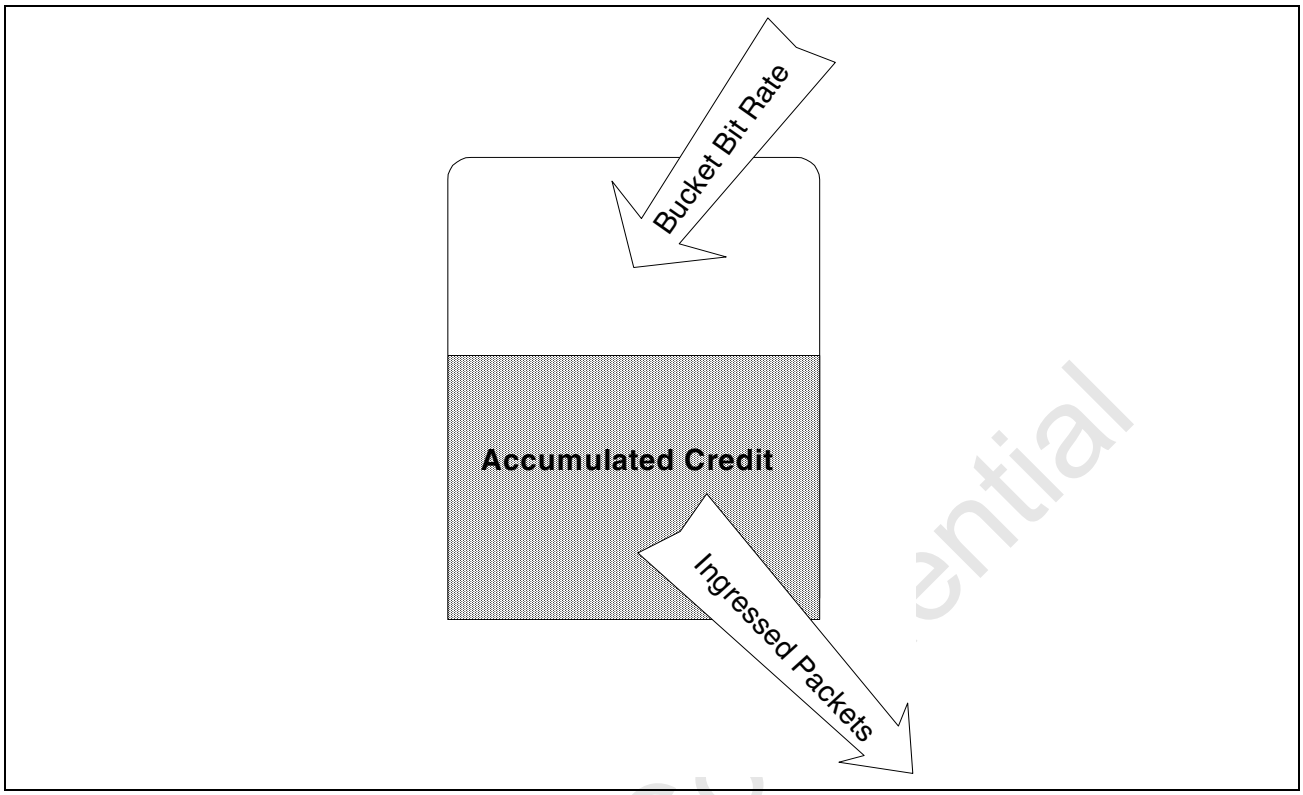

Figure 12: Ingress Bucket Flow

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Ingress Rate Control: The Three-Bucket System

For added flexibility, the BCM53262M ingress rate control employs three buckets to track the rate of ingressed packets. Each of the three buckets, Bucket 0, Bucket 1, and Bucket 2, can be programmed to monitor different packet types. For example, Bucket 0 could monitor broadcast packets, while Bucket 1 and Bucket 2 monitor other types of packets. Multiple packet types can be monitored by each bucket, and a packet type can be monitored by both buckets.

The rates of each bucket can be programmed individually. For example, the broadcast packets of Bucket 0 could have a maximum rate of 3 Mbps, whereas the multicast packets of Bucket 1 could be allowed up to 80 Mbps, with the granularity of each bucket at 64 Kbps. The size of each bucket can be programmed individually as well. This determines the maximum credit than can accumulate in each bucket. The bucket rate can be specified as an absolute rate or a normalized rate, which is scaled to the link speed of the given ingress port. The rate control can be enabled or disabled on a per-port basis.

Protected Ports

The Protected Ports feature allows certain ports to be designated as protected. All other ports are unprotected. Traffic between protected port group members is blocked. However, protected ports are able to send traffic to unprotected ports. Unprotected ports can send traffic to any port. There are the following application benefits:

- Aggregator: All of the available ports are designated as protected ports, except a single aggregator port. All traffic incoming to the protected ports will not be sent within the protected ports group. Any flooded traffic is forwarded only to the aggregator port.
- To prevent unsecured ports from monitoring important information on a server port, the server port and unsecured ports are designated as protected. The unsecured ports will not be able to receive traffic from the server port.

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Port Mirroring

The BCM53262M supports port mirroring, allowing ingress and/or egress traffic to be monitored by a single port that is defined as mirror capture port. The mirror capture port can be any 10/100 port, 10/100/1000 port or the Management port. The BCM53262M can be configured to mirror the ingress traffic and/or egress traffic of any other port(s). Mirroring multiple ports is possible, but can create congestion at the mirror capture port. Filtering can be used to decrease the port congestion. In addition, each ingress port can be configured to randomly pick the received packets and send to the CPU for Sflow packet sampling purpose.

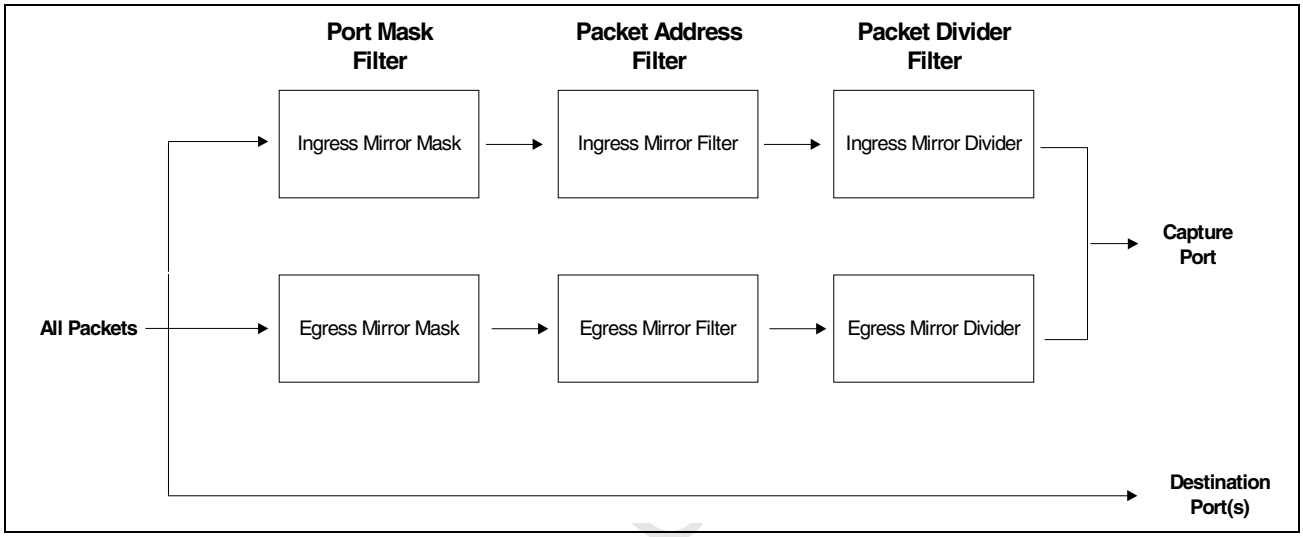

Figure 13: Mirror Filter Flow

Mirror Filtering Rules

Mirror Filtering Rules consist of a set of three filter operations

- "Port Mask Filter"
- "Packet Address Filter"
- "Packet Divider Filter" on page 56

Port Mask Filter

The most basic of filtering, the Port Mask filter, allows for the selection of a limited number of ports to be monitored based on egress or ingress packet flow. Any number of ingress/egress ports can be programmed to be mirrored, but bandwidth restrictions on the one mirror capture port should be taken under advisement, so as not to cause congestion or packet loss.

Packet Address Filter

The Packet Address filter further filters the mirrored ingress/egress frames based on the following criteria:

- Mirror all received frames

- Mirror received frames with DA = x
- Mirror received frames with SA = x

Where x is programmed 48-bit MAC address.

Packet Divider Filter

The Packet Divider filter allows further statistical sampling to be performed. Only one out of every n ingress/egress frames is forwarded to the mirror capture port, where n is a programmable integer. Combined with the packet address filter it allows the following capabilities:

- Mirror every n^{th} received frame
- Mirror every n^{th} received frame with DA = x
- Mirror every n^{th} received frame with SA = x

IGMP and MLD Snooping

The BCM53262M supports IP layer IGMP and MLD Snooping. When IGMP and MLD is enabled, the BCM53262M forwards IGMP and MLD frames to the frame management port. The external management entity programs the multicast membership information to the ARL table.

When the IP layer IGMP and MLD snooping is enabled, a frame with a value of 2 in the IP header protocol field and not a IGMP query will be forwarded to the CPU port. The Management CPU can then determine, from the IGMP control packets, which port should participate in the multi group session. The management CPU proactively programs the multicast address in the ARL table or the Multiport Address Entries.

Jumbo Frame Support

The BCM53262M can receive and transmit frames of extended length on all linked ports. Referred to as jumbo frames, these packets may be longer than 1518 bytes (when untagged), up to 2048 bytes. This feature is automatically enabled upon power up.

802.1x Port-Based Security

IEEE 802.1x is a port-based authentication protocol based on the exchange of Extensive Authentication Protocol over LAN (EAPOL) packets. When enabled the BCM53262M 802.1x feature forwards these packet types to the management CPU. Based on the receipt of these packets, the management CPU has the prerogative to modify per-port 802.1x-based security status.

When 802.1x feature is enabled, all traffic is blocked except EAPOL and ARP frames. The default state for all switch ports is a nonforwarding state. As ports become authenticated via the management CPU, these port states are modified via the CPU. Thus packet forwarding can commence.

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Dynamic Secure MAC Mode

Another security feature that can be used in with the 802.1x feature, the Dynamic Secure MAC Mode allows the management CPU control of the dynamic Source Address (SA) learning process. When enabled, the maximum number of learned SA ARL entries is set. When this maximum has been reached, the learning process is no longer active. Incoming frames with an unknown source address will be dropped without dynamically learning them into the ARL table. The learning process will continue when the aging process removes existing learned entries from the ARL table. This feature does not account for statically programmed ARL entries via the management CPU.

Address Management

The BCM53262M Address Resolution Logic contains the following features:

- Two bins per bucket address table configuration.
- Hashing of the MAC/VID address to generate the address table pointer.

The address management unit of the BCM53262M provides wire-speed learning and recognition functions. The address table supports 8K unicast/mulitcast addresses using on-chip memory.

Address Table Organization

The MAC addresses are stored in embedded SRAM. Each bucket contains two entries (or bins). The address table has 4K buckets.

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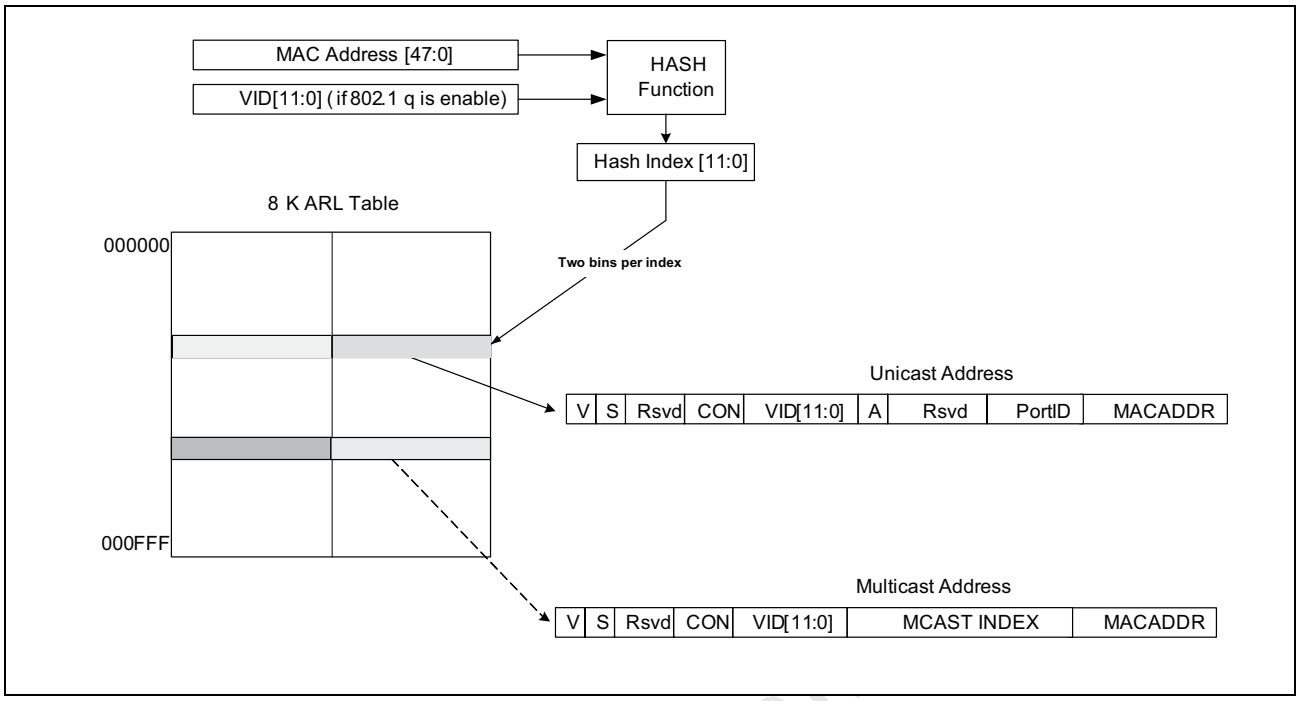

Figure 14: BCM53262M Address Table Organization

The index to the address table is computed using a hash algorithm based on the MAC address and the VLAN ID (VID) if enabled. The hash algorithm uses the CRC-CCITT polynomial. The input to the hash is reduced to a 16-bit CRC hash value. Bits 11:0 of the hash are used as an index to the 4K buckets of the address table.

The CRC-CCITT polynomial is:

$x^{16}+x^{12}+x^{5}+1$

Address Learning

Information is gathered from received unicast packets, and learned or stored for the future purpose of forwarding frames addressed to the receiving port. During the receive process the frame information, such as the source address (SA) and VID, is saved until completion of the packet. An entry is created in the ARL table memory if the following conditions are met:

- The packet has been received without error
- The packet is of legal length
- The packet has a unicast SA
- If using 802.1Q VLAN, the packet is from a SA that belongs to the indicated VLAN domain
- The packet does not have a reserved multicast destination address
- There is free space available in memory to which the hashed index points.

When unicast packets are dynamically learned, the VALID bit is set, the AGE bit is set, and the STATIC bit is cleared in the entry.

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Reserved Addresses

The BCM53262M treats certain of the 802.1 administered reserved multicast destination addresses in specific ways, dependent on the mode of operation. Packets identified with these destination addresses are handled uniquely since they are designed for special functions.

Table 2: Behavior for Reserved Multicast Addresses

MAC Address	*Function*	*802.1 Specified Action*	*Unmanaged Mode Action (Note 1)*	*Managed Mode Action*
01-80-C2-00-00-00	Bridge Group Address	Drop Frame	Forward Frame	Forward Frame to Frame Management Port Only (Note 2)
01-80-C2-00-00-01	IEEE Std 802.3x MAC Control Frame	Drop Frame	Receive MAC Determines if Valid PAUSE Frame and acts accordingly	Receive MAC Determines if Valid PAUSE Frame and acts accordingly
01-80-C2-00-00-02	RESERVED	Drop Frame	Drop Frame	Forward Frame to Management Port Only
01-80-C2-00-00-03	RESERVED	Drop Frame	Drop Frame	Forward Frame to Management Port Only
01-80-C2-00-00-04~ 01-80-C2-00-00-0F	RESERVED	Drop Frame	Drop Frame	Forward Frame to Management Port Only
01-80-C2-00-00-10	All LANs Bridge Management Group Address	Forward Frame	Forward Frame	Forward Frame to all Ports Including Frame Management Port
01-80-C2-00-00-20	GMRP address	Forward Frame	Forward Frame	Forward Frame to all Ports Except Frame Management Port (Note 3)
01-80-C2-00-00-21	GVRP address	Forward Frame	Forward Frame	Forward Frame to all Ports Except Frame Management Port (Note 3)
01-80-C2-00-00-22~ 01-80-C2-00-00-2F	RESERVED	Forward Frame	Forward Frame	Forward Frame to all Ports Except Frame Management Port

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Table 2: Behavior for Reserved Multicast Addresses (Cont.)

MAC Address	Function	802.1 Specified Action	Unmanaged Mode Action (Note 1)	Managed Mode Action

Note:

1. Unmanaged Mode disables the frame management port option. The IMP does not receive frame data when in this mode. The MII port will be treated as a normal network port and have frames forwarded to it in accordance with the entries in the address table.

2. Frames with the reserved multicast address corresponding to the BridgeGroup Address (01-80-C2-00-00-00) are forwarded to the programmed Frame Management Port based on the contents of the BPDU Multicast Address Register (in the ARL Control Register Page). Changing this register from the default value causes frames with the new address to be forwarded to the Frame Management Port, and BPDUs are flooded to all ports except the Frame Management Port. The RX_BPDU_EN bit of Management Configuration Register must be enabled.

3. Frames with the reserved multicast address corresponding to the GMRP or GVRP Addresses (01-80-C2-00-00-20 or 01-80-C2-00-00-21) are forwarded to all ports except the source and Frame Management Ports. If the switch product implements either of these protocols, then the BCM53262M should be programmed to use the Managed Mode, and the multicast address should be instantiated in the address table, with a Port ID that forwards the frame to the chip and port with the defined Frame Management Port.

Learning

During the receive process the source address (SA) of the packet is saved until completion of the packet. The address is stored in the address table memory if the following conditions are met:

- The packet is not from the Management port.
- The packet has been received without error.
- The packet is of legal length.
- The packet has a unicast address.
- There is a free space available in one of the two entries (STATIC=0 and VALID=0) in the bucket that the hashed address indexes to. If there is no free space available in the bucket, the address is not learned.

When learning, the MAC address and the source port ID is stored into the address table. The VALID bit is set, the AGE bit is set, and the STATIC bit is reset in the entry.

Static Address

The BCM53262M supports static filtering entries that are created and updated by software through the Serial Management Port. Bridge management software can create these entries by directly writing the entry location of the buffer memory, and setting the STATIC bit of the entry. Static entries do not have new MAC addresses or port associations learned automatically, and are not aged out by the automatic internal aging process (i.e., the AGE bit is subject to aging and refreshing processes, however, the entry can only be invalidated by CPU.).

For instance, addresses associated with a switch's network ports and the management port should be instantiated as Static entries in the address table by the management processor, with the source port ID and as the physical management port. All the specific register information is temporary and subject to be change in the final version of the data sheet.

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Resolution

The destination address (DA) of the received packet is used by the address resolution function to search the address table and assign a destination port for the packet. The destination port is assigned by locating a matching address in the address table and selecting the source port identifier field as the destination port. The search for a matching address occurs only for unicast packets. The address resolution function for unicast packets proceeds as follows:

- The lower 12 bits of the DA are used as a pointer into the address table memory and both entries in the bucket are retrieved. The address resolution logic processes the two entries in parallel.
- If the valid indicator is set and the address stored at one of the locations matches the DA of the packet received, the port identifier is assigned to be the destination port of the packet.
- If the destination port matches the source port, the packet is not forwarded.
- If the valid indicator is not set or the address stored does not match the DA address of the packet, the packet is forwarded as a broadcast packet and will be transmitted to all other ports.

If SW_FWDG_MODE is Unmanaged, packets with the group address bit set in the DA are handled as follows:

- If the DA matches the globally assigned multicast address of the 802.3x MAC Control PAUSE frame of 01-80-C2-00-00-01, the packet is not forwarded.
- If the DA matches the Bridge Group Address, the packet is forwarded to all ports except the source port.
- If the DA matches one of the other globally assigned reserved address (between 01-80-C2-00-00-02 and 01-80-C2-00-00-0F), the packet is not forwarded.
- All other multicast and broadcast packets are forwarded to all ports except the source port and the Management Port.

If SW_FWDG_MODE is Managed, packets with the group address bit set in the DA are handled as follows:

- If the DA matches the globally assigned multicast address of the 802.3x MAC control PAUSE frame of 01-80-C2-00-00-01, the packet is not forwarded.
- If the DA matches one of the globally assigned reserved address (between 01-80-C2-00-00-00 and 01-80-C2-00-00-0F excluding 802.3x MAC Control PAUSE frame address), the packet is forwarded to the Management port.
- If the DA matches the All LANs Bridge Management Group Address of 01-80-C2-00-00-10, or the GARP addresses of 01-80-C2-00-00-20 to 01-80-C2-00-00-2F, the packet is forwarded to all ports except the source port and the Management Port.
- All other multicast and broadcast packets are forwarded to all ports except the source port. The Management Port can selectively have broadcast packets and/or multicast packets individually disabled based on the RX_MCST_DISABLE and RX_BCST_DISABLE bits in the Port Control Register for the IMP (MII).

Hash Function

The address resolution logic incorporates a hash function to randomize storage location for the MAC address.

ARL Mishs Options

When an ARL miss occurs, the BCM53262M allows for the programming of two registers to decide what to do with the ARL missed packet:

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- MLF_FWD_MAP is for Multicast packet
- ULF_FWD_MAP is for unicast packet

When a unicast ARL miss occurs, the BCM53262M forwards it according to the ULF_FWD_MAP value. When a Multicast ARL miss occurs, the BCM53262M forwards it according to the MLF_FWD_MAP value.

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Bridge Management

BCM53262M provides the following services:

- 802.1D—Spanning Tree Protocol
- 802.1s—Multiple Spanning Trees
- 802.1W—Rapid Reconfiguration of Spanning Tree
- Bridge Management state register access through the CPU interface
- Bridge Protocol Data Unit (BPDU) frame forwarding through the CPU interface or the MII interface

Spanning Tree Port State

The BCM53262M device supports the Spanning Tree Protocol (STP) by providing the spanning tree state in the Port Control Register for each of the network ports. Each Port Control Register (PCR) contains three bits dedicated to STP state (STP_STATE[2:0]) as well as additional bits to control the operation of the MAC port.

In the unmanaged compatible mode of operation (SW_FWDG_MODE = Unmanaged), the default state of the STP_STATE[2:0] bits are all 0s, and no spanning tree state is maintained. Write operations to the spanning tree state bits are ignored. Frames are forwarded based only on their DA. Known unicast address frames are forwarded to their single defined destination port, and unknown unicast, as well as all multicast/broadcast addressed frames, are flooded to all ports, with the exception of the management port, providing SW_FWDG_EN = 1. BPDU frames, are one of the 802.1 reserved multicast addresses that the unmanaged mode floods.

The BCM53262M reacts to the STP state bits as written by the management CPU, as described in the following sections (providing SW_FWDG_EN = 1).

Disable

In this state, all frames received by the port are discarded. The port also does not forward any transmit frames, queued by either BCM53262M receive network ports, or frames cast by the management entity via the IMP. Addresses are not learned by ports in the Disabled state. This is the default state that the BCM53262M will power up in when SW_FWDG_MODE = Managed.

Blocking

In this state, the MAC port forwards received BPDUs to the designated Management port (IMP). All other frames received by the port are discarded and the addresses are not learned. The port will also not forward any transmit frames, queued by other BCM53262M receive network ports.

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Listening

In this state, the MAC port forwards received BPDUs to the designated Management port (IMP). All other frames received by the port are discarded and the addresses are not learned. The port also does not forward any transmit frames, queued by other BCM53262M receive network ports, but transmits frames cast by the management entity, via the MSP or IMP, as expected (such as BPDUs). Note that the Learning and Listening states of all BCM53262M ports are identical. The external management processor running the STP algorithm must distinguish these two states using the STP algorithm, but is able to store the Learning and Listening state information into the BCM53262M for consistency.

Learning

In this state the MAC port forwards received BPDUs to the Management port, transmits BPDUs sent into the Management port, and learns MAC addresses. All other frames received by the port are discarded.

Forwarding

In this state the MAC port forwards received BPDUs to the Management port, transmits BPDUs sent into the Management port, forwards all other frames and learns all incoming frame's MAC addresses.

Table 3: Spanning Tree State

Spanning Tree State	*Receive BPDU*	*Transmit BPDU*	*Normal Frame*	*Learning State*	*STP_State*
No Spanning Tree OR Spanning Tree Disable	Treated as Multicast	Flood to all ports	Forward	Learn	000
Disable State	Disabled	Disabled	Don't Forward	Don't Learn	001
Blocking State	Forward to Management	Disabled	Don't Forward	Don't Learn	010
Listening State	Forward to Management	Enabled	Don't Forward	Don't Learn	011
Learning State	Forward to Management	Enabled	Don't Forward	Learn	100
Forwarding State	Forward to Management	Enabled	Forward	Learn	101

The Multiple Spanning Tree Protocol (MSTP), which uses the Rapid Spanning Tree protocol (RSTP) to provide rapid convergence, enables VLANs to be grouped into a spanning-tree instance, provides for multiple forwarding paths for data traffic, and enables load balancing. It improves the fault tolerance of the network because a failure in one instance (forwarding path) does not affect other instances (forwarding paths). The most common initial deployment of MSTP and RSTP is in the backbone and distribution layers of a Layer 2 switched network; this deployment provides the highly-available network required in a service-provider environment. Both RSTP and MSTP improve the operation of the spanning tree while maintaining backward compatibility with equipment that is based on the (original) 802.1D spanning tree. The BCM53262M can support up to 256 Spanning Trees.

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The BCM53262M also supports per-port aging.

Management Frames

Management frames received by the BCM53262M are forwarded to the Bridge Management entity (an external CPU or microcontroller) through the GMII/MII Port. When the GMII/MII is used as the interface to the external management subsystem the port is referred to as the In-band Management Port (IMP). When operating in the unmanaged mode, management frames are treated differently. The following frames are forwarded to the Bridge Management entity in the BCM53262M mode:

- BPDU Frames—BPDUs are identified by the Bridge Group Address (01-80-C2-00-00-00) in the destination address field of a frame. The STP_STATE bits in the Port Control Register must be configured to permit BPDU reception on a particular port. A BPDU received on such a port will be forwarded, with the Port ID of the receiving port, to the port configured in the Management Port ID register.
- Reserved Multicast Addressed Frames—Frames with 802.1 administered Reserved Multicast Addresses (between 01-80-C2-00-00-02 and 01-80-C2-00-00-0F in their DA field are forwarded only to the Management Port, with a header which includes the Port ID of the port from which the frame was received. Frames with thee All LANs Bridge Management Group Address (01-80-C2-00-00-10) as the DA are forwarded to all ports, with the Management Port again receiving the header information to identify the Port ID from which the frame was received.
- Directed Management Agent Frames—Packets with the DA equal to one of the MAC addresses associated with the Management Port. These addresses are generally entered as Static addresses by the management entity itself.
- Mirrored Frames—Ingress or egress port frames that have been assigned to be mirrored to the management port.

Compact Field Processor

BCM53262M provides a TCAM based Compact Field Processor (CFP) to support ACL implementation and packet classification. CFP is a versatile filter and classification processor.

There are three CFP slices running in parallel in BCM53262M as shown in Figure 15 on page 66. As a result, multiple ContentAware processing can be executed per packet. The each CFP slice consists of Parser, Lookup Engine, Policy Engine, Metering/Statistic Engine, and Action Resolution Logic.

The input (key) to the CFP includes the predefined fields from the packet header, and/or user-defined fields within a packet. All these inputs are gathered at the receive port through the parser.

Up to 1K rules can be set for the parallel engines to search and assign the action to be taken when a match has been discovered. These rules can be distributed over the input ports in any combination. The actions supported by the BCM53262M are flooding, dropping, copying, changing the forward port map, adding forward port, and changing the priority, VID, and DSCP of a frame. The details of the actions are described in later paragraph.

Each CFP Engine (slice) consists of a Parser, a Lookup engine, a Policy engine, a Metering and Statistic engine and an Action Resolution engine.

- Parser assembles and extracts specified Ethernet standard field data and/or user-configurable UDF field data. Then, the Parser makes the assembled key available to the lookup engine. BCM53262M has

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predefined key fields for each of three slices as shown in Table 4 on page 70, Table 5 on page 70, Table 6 on page 72, and Table 7 on page 72. The most well known packet header fields may be selected, as well as any field in the packet through User-Defined Field (UDF).

- Lookup engine, which performs lookup and outputs the address of the matched location. Lookup engine compares the input (combination of fields defined in each slice) with all the entries in the TCAM memory. The result of the comparison is the address for the entry that is 100 percent matched. If there is more than one matching entry, the entry with the lowest physical address is returned. In addition, the lookup engine also has a mask per entry that selects specific bits of each memory entry that are required to be an exact match with the incoming bits from the input. This provides flexibility by allowing the Don't Care fields in the input.
- Policy engine, which contains a list of actions for the matching rule in the ContentAware lookup engine. There are as many actions as rules. Each matching index from the Lookup Engine is mapped to an action in the Policy engine.
- Metering and Statistics engines, which perform policing and statistics collection.
- Action resolution engine, which resolves multiple/conflict matches. Based on the matching results from the Lookup Engine, three possible actions from each slice are input to the Action Resolution Logic. The priority of each slice can be configured. The Action Resolution Logic sorts out the each action from each slice, and implements all the non conflicting actions. For the conflicting actions, the Action Resolution Logic picks an action from the high-priority slices.

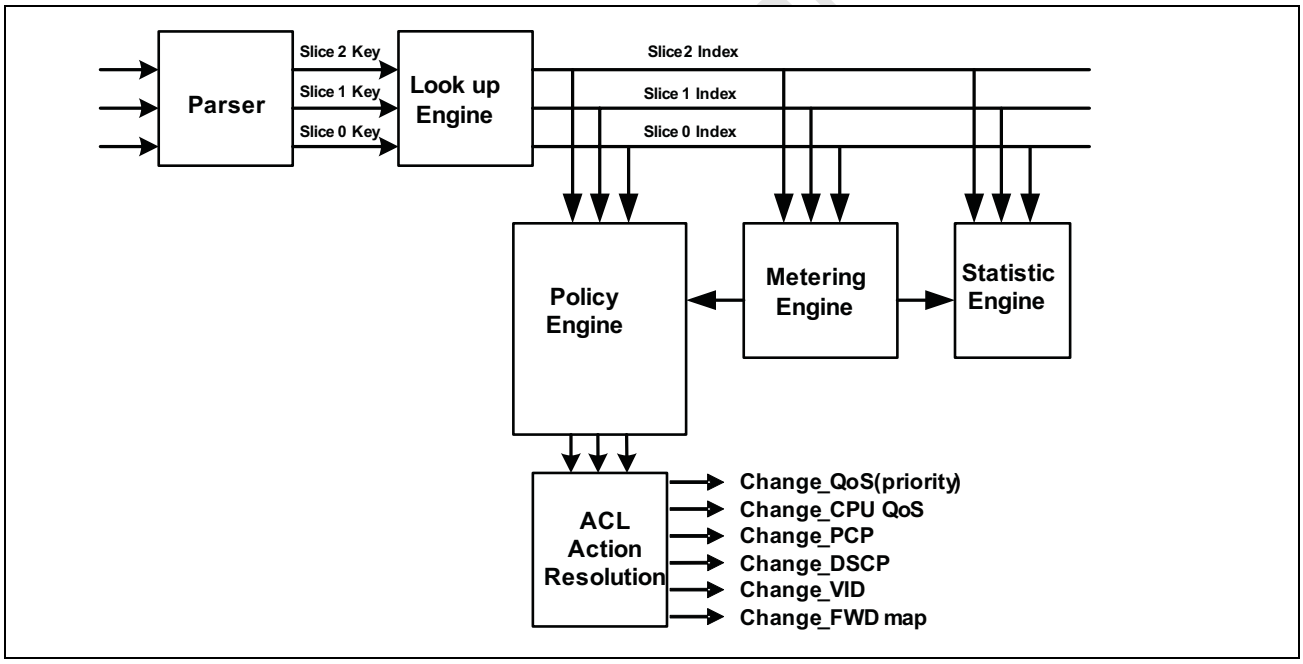

Figure 15: CFP Engines

Parser

The parser parses for standard Ethernet fields, as well as, user-defined fields. Figure 16 shows standard packet format. The parser recognizes the following predefined fields:

- EtherType (ETYPE, 16 bits)

- L2 Known Field
  - Destination MAC address (MAC_DA, 48 bits)
  - Source MAC address (MAC_SA, 48 bits)
  - Outer (Service Provider) Tag (TPID 1, 16 bits)
  - Inner (Customer) Tag (TPID2, 16 bits)
- L3 Known Field (IPv4)
  - Destination IP address (IP_DA, 32 bits)
  - Source IP address (IP_SA, 32 bits)
  - DSCP field (DSCP [6 bits] and CU [2 bits])
  - IP protocol field (IP_PROTOCOL, 8 bits)
  - TTL Range (2 bits)
  - Same IP address (Same_IPAddr, 1 bit)
- L3 Known Field (IPv6)
  - Flow ID (FlowID, 20 bits)
  - Source IP address (IP_SA, 32 bits)
  - Traffic Class (8 bits)
  - Next Header (8 bits)
  - Hop Limit Range (HopLimit_Range, 2bits)
  - Same IP address (Same_IPAddr, 1 bit)
- L4 Known Field (TCP/UDP)
  - Destination Port (DST_port, 16 bits)
  - Source Port (SRC_Port, 16 bits)
  - TCP flags (TCP_FLAG, 6 bits)
    SYN, FIN, ACK, FRAG, RST, PSH
  - Same L4 Port (Same_L4Port, 1 bit)
  - L4 Source less than 1024 (L4SRC_Less1024, 1 bit)
  - TCP Sequence number zero (TCP_Seq_Zero, 1 bit)
  - The length of TCP Header is less than min (MIN_TCP_Header, 1 bit)
- L4 Known Fields (ICMP/IGMP)
  - Type (8 bits)
  - Code (8 bits)
  - Max_ICMP (1 bit)
- Range Field
  - BCM53262M supports eight ranger mechanism: four rangers are used to detect the range of C-VID of received packets, and four rangers are used to detect the rage of TCP/UDP port of received packets. All rangers are globally configurable in terms of range setting and DST/SRC checking.
  - C_VLAN Range (4 bits): Each bit indicates whether the C_VID of the received packet falls into the corresponding range.
  - L4_Port Range (4 bits): Each bit indicates whether the L4 (DST/SRC) port of the received TCP/UDP packet falls into the corresponding range.

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- User-Defined Field
  - User-define field A0 ... A2 (UDF A, 16-bits wide) used for slice 0
  - User-define field B0 ... B10 (UDF B, 16-bits wide) used for slice 1
  - User-define field C0 ... C2 (UDF C, 16-bits wide) used for slice 2
  - User-define field D0 ... D7 (UDF D, 32-bits wide) used for slice 2
  - The four Offset parameters are used to define the location of particular UDF field within the packet. They are defined in the UDF definition registers.
  - End of Tag
  - End of EtherType
  - End of IP Header

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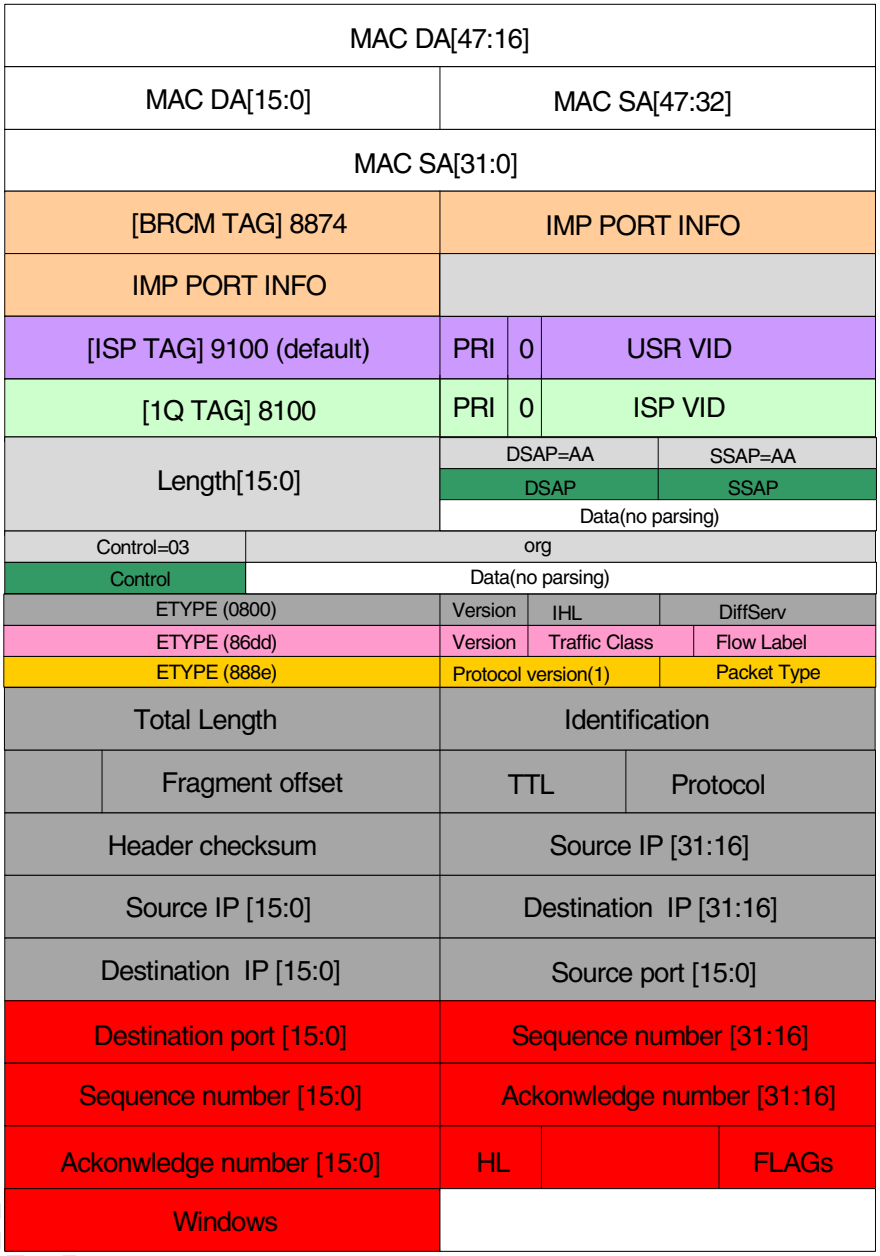

Figure 16: Standard Packet Format

Lookup Engine

The lookup engine is a highly flexible TCAM. This table contains fully user-programmable entries. Each entry has its individual corresponding mask. CFP implements three fixed rule templates, which are called Slice 0, Slice 1 and Slice 2. Table 4 on page 70, Table 5 on page 70, Table 6 on page 72, and Table 7 on page 72 show the slice key field description.

Table 4: Slice Key Common Fields

Field	Width (bits)	Bit Position	Description
Slice ID	2	1:0	Indicates the search slice number
Ingress Port Map	29	30:2	Indicates which ingress port(s) the associated ACL rule will apply
SP Tagged	1	31	Indicates whether the received packet is Service Provider tagged.
C Tagged	1	32	Indicates whether the received packet is Customer tagged.
L2 Format	2	34:33	Indicates L2 encapsulation of the received packets: • 00: L2_Others • 01: Ethernet_II • 10: IEEE_802_2_SNAP
L3 Format	2	36:35	Indicates L3 encapsulation of the received packets: • 00: L3_Others • 01: IPV4 without fragmentation • 10: IPV6 without extension
L4 Format	2	38:37	Indicates L4 encapsulation of the received packets: • 00: L4_Others. Including IPV4 with fragmentation and IPV6 with extension fields. • 01: TCP • 10: UDP • 11: ICMP/IGMP
Range Field	8	42:39	VLAN range
		46:43	L4 src/dst port range

Table 5: Slice 0 Key Field Definition

Field	Width (bits)	Bit Position[a]	Description
Slice Common Field	47	46:0	Shown in Slice Common Field table (see Table 4)
L2 Known Field	128	94:47	Destination MAC address (MAC_DA, 48 bits)
		142:95	Source MAC address (MAC_SA, 48 bits)
		158:143	Outer (Service Provider) Tag (TPID 1, 16 bits)
		174:159	Inner (Customer) Tag (TPID2, 16 bits)
Ether Type	16	190:175	–

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Table 5: Slice 0 Key Field Definition (Cont.)

Field	Width (bits)	Bit Position[a]	Description
L3 Known Field	83	–	IPv4
		222:191	• Destination IP address (IP_DA, 32 bits)
		254:223	• Source IP address (IP_SA, 32 bits)
		262:255	• DSCP (6 bits) and CU (2 bits)
		270:263	• IP protocol field (IP_PROTOCOL, 8 bits)
		272:271	• TTL Range (2 bits)
		273	• Same IP Address (Same_IPAddr, 1 bit)
L3 Known Field	83	–	IPv6
		212:191	• Flow ID (FlowID, 20 bits)
		254:213	• Source IP address (IP_SA, 32 bits)
		262:255	• Traffic Class (8 bits)
		270:263	• Next Header (8 bits)
		272:271	• Hop Limit Range (HopLimit_Range, 2 bits)
		273	• Same IP address (Same_IPAddr, 1bit)
L4 Known Field	42	–	TCP/UDP
		289:274	• Destination Port (DST_port, 16 bits)
		305:290	• Source Port (SRC_Port, 16 bits)
		311:306	• TCP flags (TCP_FLAG, 6 bits)
		–	– SYN, FIN, ACK, FRAG, RST, PSH
		312	• Same L4 Port (Same_L4Port, 1 bit)
		313	• L4 Source less than 1024 (L4SRC_Less1024, 1 bit)
		314	• TCP Sequence number zero (TCP_Seq_Zero, 1 bit)
		–	ICMP/IGMPMax_ICMP (1 bit)
		297:290	• Type (8 bits)
		305:298	• Code (8 bits)
		315	• Max_ICMP Check (1 bit)
UDF_A0_Valid, UDF_A0	17	332:316	–
UDF_A1_Valid, UDF_A1	17	349:333	–
UDF_A2_Valid, UDF_A2	17	366:350	–
Valid	4	383:380	–

a. All undefined bit positions are reserved.

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Table 6: Slice 1 Key Field Definition

Field	*Width (bits)*	*Bit Position*[a]	*Description*
Slice Common Field	47	46:0	Shown in Slice Common Field table, Table 4 on page 70
L2 Known Field	128	94:47	Destination MAC address (MAC_DA, 48 bits)
		142:95	Source MAC address (MAC_SA, 48 bits)
		158:143	Outer (Service Provider) Tag (TPID 1, 16 bits)
		174:159	Inner (Customer) Tag (TPID2, 16 bits)
UDF_B0_Valid, UDF_B0	17	191:175	–
UDF_B1_Valid, UDF_B1	17	208:192	–
UDF_B2_Valid, UDF_B2	17	225:209	–
UDF_B3_Valid, UDF_B3	17	242:226	–
UDF_B4_Valid, UDF_B4	17	259:243	–
UDF_B5_Valid, UDF_B5	17	276:260	–
UDF_B6_Valid, UDF_B6	17	293:277	–
UDF_B7_Valid, UDF_B7	17	310:294	–
UDF_B8_Valid, UDF_B8	17	327:311	–
UDF_B9_Valid, UDF_B9	17	344:328	–
UDF_B10_Valid, UDF_B10	17	361:345	–
Valid	4	383:380	–

a. All undefined bit positions are reserved.

Table 7: Slice 2 Key Field Definition

Field	*Width (bits)*	*Bit Position*[a]	*Description*
Slice Common Field	47	46:0	Shown in Slice Common Field table, see Table 4 on page 70.
UDF_C0_Valid, UDF_C0	17	63:47	–
UDF_C1_Valid, UDF_C1	17	80:64	–
UDF_C2_Valid, UDF_C2	17	97:81	–

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Table 7: Slice 2 Key Field Definition (Cont.)

Field	Width (bits)	Bit Position[a]	Description
UDF_D0_Valid, UDF_D0	33	130:98	–
UDF_D1_Valid, UDF_D1	33	163:131	–
UDF_D2_Valid, UDF_D2	33	196:164	–
UDF_D3_Valid, UDF_D3	33	229:197	–
UDF_D4_Valid, UDF_D4	33	262:230	–
UDF_D5_Valid, UDF_D5	33	295:263	–
UDF_D6_Valid, UDF_D6	33	328:296	–
UDF_D7_Valid, UDF_D7	33	361:329	–
Valid	4	383:380	–

a. All undefined bit positions are reserved.

Policy Engine

Table 4 on page 70, Table 5 on page 70, Table 6 on page 72, and Table 7 on page 72 contain one entry per lookup engine entry and the actions/policies that should be taken for the lookup engine entry. The policy entry also indicates which metering and counter entries should be used.

There are six types of actions in CFP policy.

1. The forwarding-related action. Change the destination port or add destination port. It can also drop a frame by making new_dest to 6'b11_1111 and enable change destination.
2. To change the priority of the frame. The priority queue can be specified to use by setting PRI_MAP accordingly.
3. To change the QoS of the outgoing packets.
4. To change the QoS of the CPU originated packets.
5. To change the DSCP tag of the outgoing packets.
6. To change the VID of the outgoing packets.

All six operations can be asserted in parallel, so it is possible that in the end of ContentAware processing, assign to a specific priority and also copy to CPU port and update the corresponding counter.

Packet Remarking

BCM53262M supports Packet Remarking. Remarks can be made on the PCP field of the outmost VLAN tag of the outgoing packet, or remarks can be made on the DSCP field if the outgoing packet is an IP packet. The remarking process is a part of the ChangePCP, and the ChangeDSCP actions from the CFP, and carried over through the MMU as a part of the packet descriptor information. Based on the new DSCP value, the corresponding IP checksum is also re calculated. The Remarking information is applied globally, independent to the Egress port.

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VID Replacement

BCM53262M supports VID Replacement. The VID field of the outmost VLAN tag of the outgoing packet can be replaced. The Replacement feature is port dependent, each port can be setup differently. Each Egress port supports a 16 entry FLOW to VID mapping table which is indexed by the FlowID. This is derived as a part of the ChangeVID action from the CFP, and is carried through the MMU as a part of the packet descriptor information.

One of the applications for this feature is in the IPTV distribution where the common Multicast VLAN can be dynamically associated with different subscriber's VLANs.

Metering Engine

Metering engine provides the ability to control ingress bandwidth based on packet classification. Metering determines whether a packet is inband or outband. The results of the metering engine is fed back to the policy engine for determining which actions should be processed.

Statistic Engine

The Statistics engine increments the counters based on the metering results. For each rule, there are in-profile and out-profile counters counting packets (not bytes).

ACL Action Resolution Block

The Action Resolution engine collects the information (action and metering results) from the hit entries: if more than one rule matches, the actions and meter/counters are taken from the policy associated with the matched rule with highest priority.

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Section 3: System Functional Blocks

Overview

The BCM53262M includes the following functional blocks:

- "Media Access Controller"
- "Integrated PHY" on page 77
- "Frame Management" on page 88
- "Switch Controller" on page 93
- "Integrated High-Performance Memory" on page 94
- "Clocking" on page 94
- "MIB Engine" on page 94

Each are discussed in more detail in the following sections.

Media Access Controller

The MAC automatically selects the appropriate speed, CSMA/CD or Full-duplex, based on the PHY auto-negotiation result. In FDX mode, 802.3x PAUSE-frame-based flow control is also determined through auto-negotiation. The MAC is IEEE 802.3, 802.3u, and 802.3x compliant.

Receive Function

The MAC initiates frame reception following the assertion of receive data valid indication from the physical layer. The MAC monitors the frame for the following error conditions:

- Receive error indication from the PHY
- Runt frame error if frame is fewer than 64 bytes
- CRC error
- Long frame error if frame is greater than 2048 bytes (Rev. A silicon)
- For revision B silicon, long frame error if frame is greater than MAX_RX_LIMIT, which is defined in "New Control Register (Page 00h/Addr 03h)" on page 167.

If no errors are detected, the frame is processed by the switch controller. Frames with errors are discarded. Receive functions can be disabled.

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Transmit Function

Frame transmission begins with the switch controller queuing a frame to the MAC transmitter. The frame data is transmitted as received from the switch controller. The transmit controller is responsible for preamble insertion, carrier deferral, collision backoff, and inter-packet gap enforcement.

In 10/100 half-duplex mode, when a frame is queued for transmission, the transmit controller behaves as specified by the 802.3 requirements for frame deferral. Following deferral, the transmitter adds 8 bytes of preamble and SFD to the frame data received from the switch controller. If, during frame transmission, a collision is observed and the collision window timer has not expired, the transmit controller asserts jam and then executes the backoff algorithm. The frame is retransmitted when appropriate. On the sixteenth consecutive collision, the backoff algorithm starts over at the initial state, the collision counter is reset and attempts to transmit the current frame continue. Following a late collision, the frame is aborted and the switch controller is allowed to queue the next frame for transmission.

While in full-duplex mode, the transmit controller ignores carrier activity and collision indication. Transmission begins after the switch controller queues the frame and the 96 bit-times of IPG have been observed. Transmit functions can be disabled.

Flow Control

The BCM53262M implements an intelligent flow control algorithm to minimize the system impact resulting from traffic congestion. Buffer memory allocation is adaptive to the status of each port's speed and Duplex mode, providing an optimal balance between flow management and per-port memory depth. The BCM53262M initiates flow control in response to buffer memory conditions on a per-port basis.

The MACs are capable of flow control in both full-and half-duplex modes.

10/100 Mbps Half-Duplex

In 10/100 Half-duplex mode, the MAC backpressures a receiving port by transmitting a 96-bit time-jam packet to the port. A single jam packet is asserted for each received packet for the duration of the time the port is in the flow control state.

10/100/1000 Mbps Full-Duplex

Flow control in full-duplex mode functions as specified by the IEEE 802.3x requirements. In the receiver, MAC flow control frames are recognized and, when properly received, set the flow control pause time for the transmit controller. The pause time is assigned from the 2-byte pause time field following the pause opcode. MAC control PAUSE frames are not forwarded from the receiver to the switch controller.

When the switch controller requests flow control, the transmit controller transmits a MAC control PAUSE frame with the pause time set to maximum. When the condition that caused the flow control state is no longer present, a second MAC control PAUSE frame is sent with the pause time field set to 0.

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The flow control capabilities of the BCM53262M are enabled based on the results of auto-negotiation and the state of the ENFDXFLOW and ENHDXFLOW control signals loaded during reset. Flow control in half-duplex mode is independent of the state of the link partner's flow control (802.3x) capability. See Table 8 for more information.

Table 8: Flow Control Modes

Link Partner Flow Control (802.3x)	*Control Input ENFDXFLOW*	*Control Input ENHDXFLOW*	*Auto-Negotiated Link Speed*	*Flow Control Mode*
X	X	0	Half-Duplex	Disabled
X	X	1	Half-Duplex	Jam Pattern
0	0	X	Full-Duplex	Disabled
0	1	X	Full-Duplex	Disabled
1	0	X	Full-Duplex	Disabled
1	1	X	Full-Duplex	IEEE 802.3x Flow Control

Integrated PHY

The PHY is the ethernet transceiver that appropriately processes data presented by the MAC into an analog data stream to be transmitted at the MDI interface, and performs the reverse process on data received at the MDI interface. The registers of the PHY are read/written to via the programming interface. The following sections describe the operations of the internal PHY block.

Note: The 24 integrated transceivers are referred to in this document as ports 24, 25 … and 47. Broadcom SDK maps these ports to logical ports 0, 1 … 23 respectively.

Encoder

In 10Base-T mode, Manchester encoding is performed on the data stream that is transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs pre-equalization for 100m of Category-3 cabling.

In 100Base-TX mode, the PHY transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first 2 nibbles of preamble with a start-of-stream delimiter (/J/K/ codes) and appending an end-of-stream delimiter (/T/R/ codes) to the end of the packet. The transmitter repeatedly sends the idle (/i/ code) between packets. The encoded data stream is serialized and then scrambled by the stream cipher block. The scrambled data is then encoded into MLT3 signal levels.

Decoder

In 10Base-T mode, Manchester decoding is performed on the data stream.

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In 100Base-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT3 to serial nonreturn to zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with 0h. The decoded data is driven onto the internal MAC interface. When an invalid code group is detected in the data stream, the PHY asserts the internal MII receive error signal. This signal is also asserted when the link fails or when the descrambler loses lock during packet reception.

Link Monitor

In 10Base-T mode, a link-pulse detection circuit constantly monitors the TRD± pins for the presence of valid link pulses.

In 100Base-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal is detected on the receive pair, the link monitor enters the Link Fail state and the transmission and reception of data packets is disabled. When a valid signal is detected on the receive pair for a minimum of 1 ms, the link monitor enters link-pass state and the transmit and receive functions are enabled.

Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The PHY achieves optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than 1×10^{-12} for transmissions up to 100m on Category-5 twisted-pair cabling (100m on Category-3 UTP cable for 10Base-T mode). The all-digital nature of the design drives high noise-tolerant performance. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

Analog-to-Digital Converter

Each receive channel has its own 125-MHz analog-to-digital converter (ADC) that samples the incoming data and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High power-supply noise-rejection
- Fast settling time
- Low bit-error-rate

Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 100Base-TX and 10Base-T operation.

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In 10Base-T or 100Base-TX mode, the transmit clock is locked to the 25-MHz crystal input, and the receive clock is locked to the incoming data stream.

Baseline Wander Correction

100Base-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The PHY automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

In 10Base-T mode, baseline wander correction is not performed because the Manchester coding provides perfect DC balance.

Multimode TX Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM5, MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high-frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses a current drive output that is well-balanced, and therefore, produces very low noise transmit signals.

Stream Cipher

In 100Base-TX mode, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require there to be no sequential or cross-channel correlation among symbols in the various data streams.

In 100Base-TX mode, the transmit data stream is scrambled by exclusive ORing the encoded serial data stream. This is done with the output of an 11-bit wide linear feedback shift register (LFSR), producing a 2047-bit nonrepeating sequence.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The BCM53262M enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that inter-packet gaps containing idles or frame extensions are received at expected intervals.

In 10Base-T mode, scrambling is not required to reduce radiated emissions.

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Wire Map and Pair Skew Correction

During 10/100-Mbps operation, pair swaps are corrected. Delay skew is not an issue though, because only one pair of wires is used in each direction.

Internal Loopback Mode

When enabled in this mode, all packets egressed to the integrated PHY ports are looped back internally from the TXD signals to the RXD signals. The transmitter outputs TRD± are set to high impedance, and incoming packets on the cable are ignored.

Isolate Mode

The PHY can be isolated from the internal MAC interface. When the transceiver is put into Isolate mode, all inputs from the MAC block are ignored, and all outputs to the MAC block are tristated. While in Isolate mode, the PHY still sends out link pulses or FLPs, depending on whether the PHY was configured for Forced or Auto-negotiation mode. A link is established if the link partner is forced or is advertising the same technologies. Clearing the same bit removes the device from Isolate mode.

PHY Registers

Each transceiver within the BCM53262M contains a complete set of PHY registers. The 5-bit transceiver address is assigned correspondingly to the internal port ID. All PHY registers can be accessed through the MDC and MDIO signals, or through the Serial Peripheral Interface.

100Base-FX Fiber Mode

The 10/100 port can be configured to operate in 100Base-FX compatible mode. The following sequence is required for configuring the preferred PHY ports to 100Base-FX-compatible operation using register write from the CPU. Each port's register can be programmed through page A0h-B7h, respectively.

1. Write 2100h to register (Pages A0h-B7h, Address 00h-01h). This forces the port to 100M full-duplex without auto-negotiation. Most FX applications require configuration for full-duplex.
2. Set bits 9 and 5 of register (Pages A0h-B7h, Address 20h-21h). This bypasses the scrambler and descrambler blocks (i.e., these scrambling functions are not required for 100Base-FX operation). Other bits within this register may be set, so it is best to perform a read-modified write to ensure proper setting of this register.
3. Set bit 5 of hidden register (Page A0h-B7h, Address 2Eh–2Fh). This changes the three-level MLT-3 code transmitted by the PHY to two-level binary, suitable for driving standard fiber transceivers. Additionally, the PHY receiver is configured to recognize binary signaling. This register access must also be in the form of a read-modified write.
4. Enable Internal EFX Signal Detect Function:
   a. Write 008Bh to register (Pages A0h-B7h, Address 3Eh–3Fh).
   b. Write 0200h to register (Pages A0h-B7h, Address 32h–33h).
   c. Write 0084h to register (Pages A0h-B7h, Address 3Ah–3Bh).

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d. Write 000Bh to register (Pages A0h-B7h, Address 3Eh–3Fh).

5. Configure Full-duplex Pause Capability by setting bit 63 and relevant port bits[47:24] of the Software Flow Control registers (Page 00H, Address 48h).

Refer to the *Enhanced-FX-AN1XX 100Base-FX-Compatibility Application Note* for the FX termination requirement.

Cable Analyzer Registers and Programming

Cable diagnostics can be initiated at any time by entering certain parameters in the required register bits and then setting the *start* bit. Once the start bit is set, the PHY starts the cable diagnostics and looks for opens, shorts, cable lengths on pair-A and pair-B. When this analysis is completed, it records the results and resets the start bit.

Shadow Register Description

All of the required bits for the cable analyzer are located in the shadow registers, in particular shadow registers (Pages A0h-B7h, addresses 26h and 28h). Within address 26h, there are eight subregisters 0x26-0, 0x26-1, 0x26-2, 0x26-3, 0x26-4, 0x26-5, 0x26-6, and 0x26-7.

Shadow register 0x26-n is accessed by writing an index value (n = 000b to 111b) to the shadow register at address 28h. To access shadow register 0x26-1, the index value in shadow register 28h must be set to 1. Whenever an access is made (either a read or a write) to shadow register 26h, the index value in the shadow register 28h is automatically incremented.

When changing a bit within any register, preserve the existing values of reserved bits by performing a ‘read modify’ write.

The following tables shows the cable analyzer registers and their contents.

Table 9: Shadow Register 28h (Pages A0h-B7h, Address 28h)

Address	*15–11*	*10–8*	*7–0*	*Default*
0x28	Reserved	0x26 index	Reserved	0x0000

0x26 Index [10:8]

To access shadow register 26h, first an index value from 0(000b) to 7(111b) must be written to these bits. When an access (either read or write) is made to shadow register 26h, this value automatically increments by 1 (111b after the increment, it becomes 000b).

Table 10: Shadow Register 0x26–0 (Pages A0h-B7h, Address 26h)

Address	*15–14*	*13–12*	*11–10*	*9–8*	*7–6*	*9–3*	*2*	*1*	*0*	*Default*
0x26-0	Reserved	Pair-B State	Pair-A State	Pass	Error	Reserved	Start	MP	Reserved	0x0000

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Pair-B State[13:12]

After the completion of cable analyzer, these bits indicate the status of pair-B of the cable (see Table 11 for details). Pair-B of the cable is the pair that is connected to RD± of the device.

Table 11: Pair-B State

Value	*Result for Pair-B*
00b	No fault detected
01b	Pair is open
10b	Pair is short
11b	Reserved

Note: When the cable analyzer function returns a value of 00 (No fault detected), then the attached cable is good. If the device is unable to establish a valid link, the problem is not related to the cable.

Pair-A State[11:10]

After the completion of cable analyzer, these bits indicate the status of pair-A of the cable (see Table 12 for details). Pair-A of the cable is the pair that is connected to TD± of the device.

Table 12: Pair-A State

Value	*Result for Pair-A*
00b	No fault detected
01b	Pair is open
10b	Pair is short
11b	Reserved

Note: When the cable analyzer function returns a value of 00 (No fault detected), then the attached cable is good. If the device is unable to establish a valid link, the problem is not related to the cable.

Start [2]

Setting this bit to a 1 starts the cable diagnostics function in the BCM5325EBCM5325F. This should be the last bit that is set after programming the required values in shadow registers 0x26-0, 0x26-1, 0x26-2, 0x26-3, 0x26-4, 0x26-5, 0x26-6 and 0x26-7. This bit is cleared when the cable analyzer function is complete. Once this bit is set, it is reset in approximately 5 ms.

MP [1] = 1

This is an internal variable required to be set before starting the cable analyzer. Set this bit to a 1.

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Pass [9:8]

These bits are 11b when reading the results of the cable analyzer.

Error [7:6]

These bits must be 00b when reading the results of the cable analyzer.

Table 13: Shadow Register 0x26-1 (Pages A0h-B7h, Address 26h)

Address	15–8	7–0	Default
0x26-1	Pair-B length	Pair-A length	0x0000

Pair-B Length [15:8]

These bits indicate the length of pair-Bonce the cable analyzer is completed. To convert this value to meters, multiply the value by 0.8. This value should be used in combination with the result posted on the condition of pair-B in bits [13:12] of shadow register 0x26-0.

Table 14: Pair-B Cable Diagnostics Result

Pair-B state [13:12] (shadow register 0x26-0)	Pair-B length [15:8] (shadow register 0x26-1)
01b	Distance at which an open is detected in pair-B
10b	Distance at which a short is detected in pair-B

Pair-A Length [7:0]

These bits indicate the length of pair-A once the cable analyzer is completed. To obtain the value in meters, multiply this value by 0.8. This value should be used in combination with the result posted on the condition of pair-A in bits [11:10] of shadow register 0x26-0.

Table 15: Pair-A Cable Diagnostics Result

Pair-A state [11:10] (shadow register 0x26-0)	Pair-A length [7:0] (shadow register 0x26-1)
01b	Distance at which an open is detected in pair-A
10b	Distance at which a short is detected in pair-A

Table 16: Shadow Register 0x26-2 (Pages A0h-B7h, Address 26h)

Address	15–14	13–12	11–10	9–6	5	4–0	Default
0x26–2	GainA	Reserved	TypeA	Reserved	HP	ThresholdA	0x0000

GainA [15:14] = 01b

This is an internal variable required to be set before starting the cable analyzer. Set these bits to 01b.

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TypeA [11:10] = 10b

This is an internal variable required to be set before starting the cable analyzer. Set these bits to 10b.

HP [5] = 1

This is an internal variable required to be set before starting the cable analyzer. Set these bits to a 1.

ThresholdA [4:0] = 00100b

This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set these bits to 00100b.

Table 17: Shadow Register 0x26-3 (Pages A0h-B7h, Address 26h)

Address	*15–8*	*7–0*	*Default*
0x26-3	SourceA	Reserved	0x0000

SourceA [13:8] = 00100000b

This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set these bits to 00100000b.

Table 18: Shadow Register 0x26-4 S (Pages A0h-B7h, Address 26h)

Address	*15–11*	*10*	*9*	*8–6*	*5–0*	*Default*
0x26-4	Reserved	TypeB	Reserved	TPG	Reserved	0x0000

TypeB [10]

This is an internal variable required to be set before starting the cable analyzer. Set this bit to a 1.

TPG [8:6]

This is an internal variable required to be set before starting the cable analyzer. Set this bit to 100b.

Table 19: Shadow Register 0x26-5 (Pages A0h-B7h, Address 26h)

Address	*15–14*	*13–5*	*4–2*	*1–0*	*Default*
0x26-5	GainB	Reserved	ThresholdB	Reserved	0x0400

GainB [15:14 = 11b]

This is an internal variable required to be set before starting the cable analyzer. Set these bits to 11b.

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ThresholdB [4:2] = 001b

This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set these bits to 001b.

Table 20: Shadow Register 0x26-6 (Pages A0h-B7h, Address 26h)

Address	*15–14*	*13–8*	*7–0*	*Default*
0x26-6	Reserved	SourceB	Reserved	0x0000

SourceB [13:8] = 000001b

This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set these bits to 000001b.

Table 21: Shadow Register 0x26-7 (Pages A0h-B7h, Address 26h)

Address	*15–9*	*8–6*	*5*	*4–0*	*Default*
0x26-7	Reserved	PGWB	Reserved	AmpB	0x0000

PGWB [8:6] = 001b

This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set this bit to a 001b

AmpB [4:0] = 01100b

This is an internal variable required to be set before setting the start bit in shadow register 0x26-0 to start the cable analyzer. Set this bit to a 01100b.

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Programming Example

The following example of code shows a general flow of completing the cable analyzer in the PHY.

```
Cable Analyzer programming
-------------------------------------------------
Start
Write register (Pages A0h-B7h, address 3Eh) = 0x008BEnable shadow register
Wait1
Read (Pages A0h-B7h, address 28h) ; Wait here for at least 2 seconds of bit 6 for address 28h to be
at 0. This ensures that there is no energy from the link partner.
Write (Pages A0h-B7h, address 28h) -0x0000
End Wait1
Write register (Pages A0h-B7h, address 26h) = 0x0000
Write register (Pages A0h-B7h, address 28h) = 0x0200;Set access shadow register 26h to 0x26–2
Write (Pages A0h-B7h, address 26h) = 0x4824; 0x26–2
Write (Pages A0h-B7h, address 26h) = 0x4000; 0x26-3
Write (Pages A0h-B7h, address 26h) = 0x0500; 0x26-4
Write (Pages A0h-B7h, address 26h) = 0xC404; 0x26-5
Write (Pages A0h-B7h, address 26h) = 0x0100; 0x26-6
Write (Pages A0h-B7h, address 26h) = 0x004C; 0x26-7
Write (Pages A0h-B7h, address 26h) = 0x8006; 0x26-0 (Start cable diagnostics)
Wait2
    Write (Pages A0h-B7h, address 28h) = 0x0000; Set access to 0x26-0
    Read (Pages A0h-B7h, 1 address 26h) ; Read 0x26-0
    If register 0x26-0 bit [2] = 1 then go to Wait2
Result
Pair-A status = 0x26-0 bit [11:10]
Pair-B status = 0x26-0 bit [13:12]

Read (Pages A0h-B7h, 19h, address 26h) ; Read 0x26-1
Pair-A length = bit [7:0] X 0.8 meters
Pair-B length = bit [15:8] X 0.8 meters

Write register (Pages A0h-B7h, 1address 3Eh) = 0x000BEnable default MII register access
End
```

Note: If a port is connected to a link partner with a good cable (no short or no open on either pair) and the link partner is not powered up, then the cable status bits are valid, but the length bits are invalid.

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Cable Analyzer Flow Chart

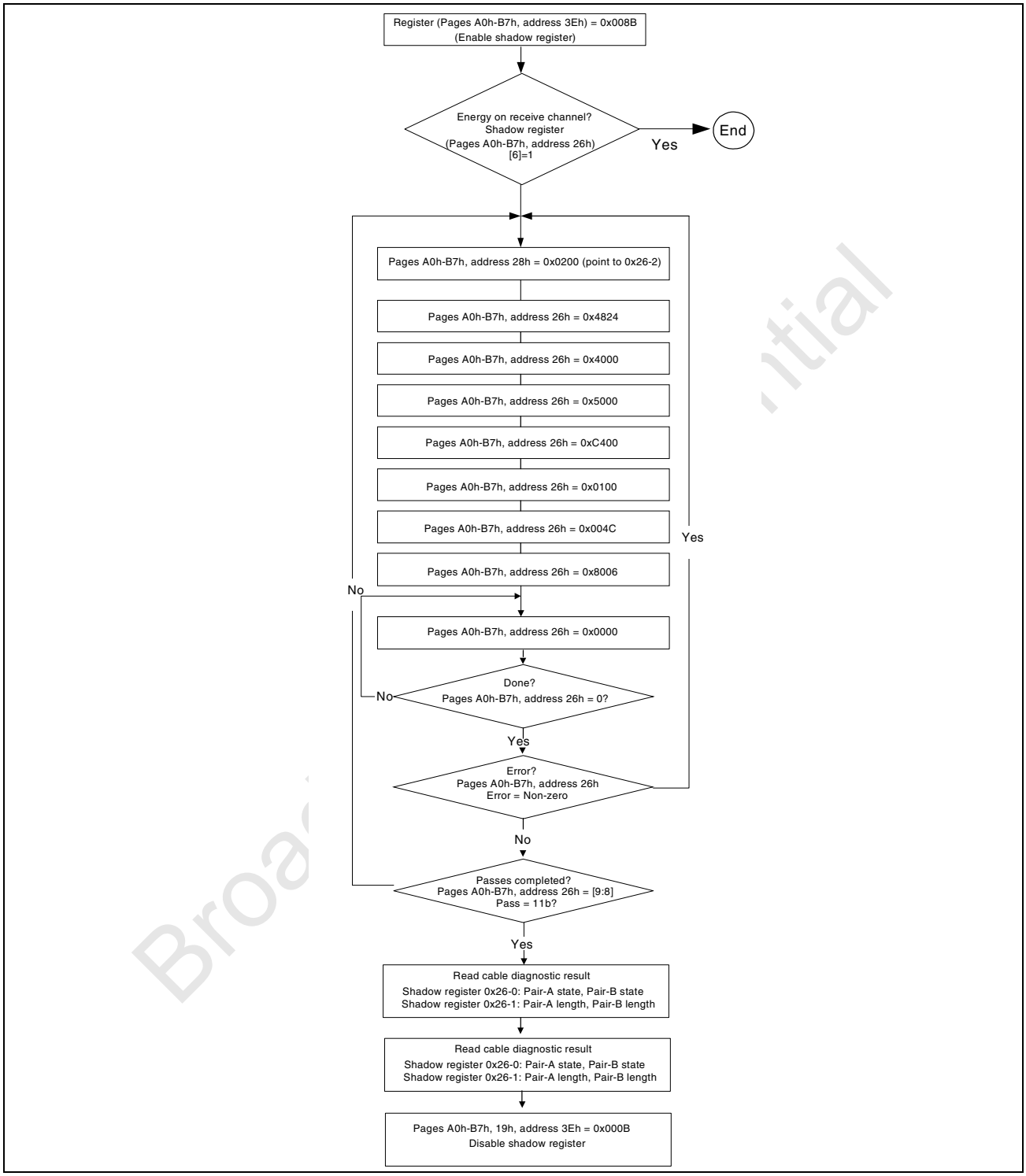

Figure 17: Cable Analyzer Flow Chart

Frame Management

The BCM53262M provides a frame management block that works in conjunction with a selectable port interface to receive forwarded management frames directed to the switch.

The frame management block is configured via the FRM_MNGT_PORT bits of the Global Management Configuration register as shown in Table 99: “Global Management Configuration Register (Page 03h: Address 00h),” on page 205.

An external CPU connects via the selected port interface to process the forwarded frames and respond appropriately. When the selected port is defined as the Frame Management Port, it is referred to as the In-band Management Port (IMP).

In Band Management Port

The IMP can be used as a full-duplex port, which can be used to forward management information to the external management agent, such as BPDUs, mirrored frames, or frames addressed to other Static address entries that have been identified as of special interest to the management system.

As IMP is defined as the Frame Management Port, normal frame data is forwarded to the port based on the state of the RX_UCST_EN, RX_MCST_EN and RX_BCST_EN bits in the associated IMP Port Control Register. If these bits are cleared, no frame data will be forwarded to the Frame Management Port, with the exception that frames meeting the Mirror Ingress/Egress Rules criteria, will always be forwarded to the designated Frame Management Port.

The BCM53262M device intrusively tags frames destined to the management entity to allow the identity of the originating ingress port of a frame to be retained. Additional header information is inserted into the original frame, between the original SA field and Type/Length fields, see Figure 18 on page 89. The tag includes the BRCM Type field and the BRCM Tag field. The Broadcom tag type is 0x8874, the alignment of the regenerated FCS may vary depending on the original frame length, and the regenerated FCS covers from the whole frame, including the BRCM Type and BRCM tag. A recalculated FCS is appended to the resultant frame, before the frame is forwarded.

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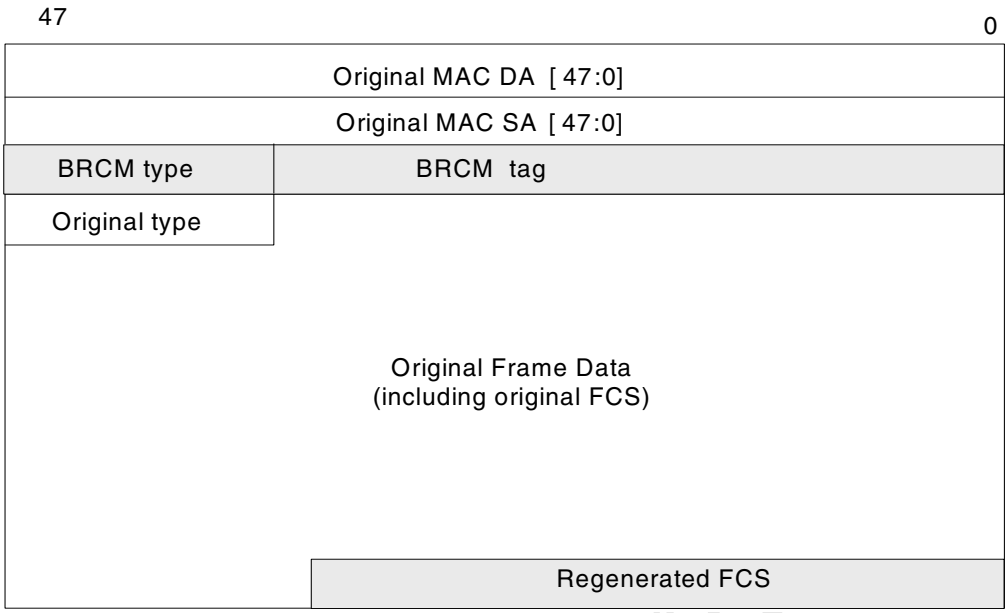

Figure 18: Broadcom-Tagged Packet Encapsulation Format

The Broadcom Tag is designed for asymmetric operation across the IMP port. The information carried from the BCM53262M to the external CPU (IMP Egress) is different from the information carried from the external CPU to BCM53262M (IMP Ingress).

Similarly, the host system must insert the BRCM Type/Length and Tag fields into frames it wishes to send into the management port, to be routed to specific egress ports. The OPCODE within the Tag field determines how the frame will be handled, and allows frames to be forwarded using the normal address lookup or via a Port ID designation within the Tag.

Note: The FCS (outer) is ignored by the BCM53262M device. However, the management entity is still intended to provide 4 bytes of any data as a place holder. Only the final outgoing FCS (inner) is required.

The BRCM Tag and BRCM Type/Length fields are transmitted with the convention of highest significant octet first, followed by next lowest significant octet, etc., and with the least significant bit of each octet transmitted out from the MAC first. So for the BRCM Type/Length field in Table 22 on page 90, the most significant octet would be transmitted first (bits 24:31), with bit 24 being the first bit transmitted.

IMP Ingress

Table 22 shows the format of the IMP Ingress BRCM Tag field. The OPCODE field slightly modifies the use and validity of some fields in the Tag. Table 23 defines the supported OPCODEs.

Table 22: BRCM Header Tag Format (CPU to IMP)

31-29	*28,27*	*26,25*	*24 - 6*	*5-0*
Opcode = (000) Unicast/Multicast/ Broadcast	TQ[1:0]	TE[1:0]	Reserved	Reserved
Opcode = (010) Egress Directed	TQ[1:0]	TE[1:0]	Reserved	Dest Portid Indicates the destination Port ID for Egress Directed frames. ***Note:*** Setting Dest Portid = 0x30 allows egress directed frame to loopback to CPU. This is for testing purpose.
Opcode = (100) Multicast Egress Directed to 10/100 Ports	TQ[1:0]	TE[1:0]	Dest Port Vector [Port 47~Port 24] Defines the destination Port IDs for Multicast Egress Directed frames. ***Note:*** Bit 24 is not used	
Opcode = (101) Multicast Egress Directed to GigaPorts	TQ[1:0]	TE[1:0]		Dest Port Vector [G3, G2, G1, G0, IMP] Defines the destination GigaPort IDs for Multicast Egress direct frames. ***Note:*** For testing purpose, setting bit[0] = 1 allows the CPU to loop back the frame at the IMP port.

Table 23: OPCODE Field in BRCM Tag for Management Port Frame

OpCodes	*Name*	*Description*
0 0 0	Unicast/Multicast	Normal unicast and multicast frames are forwarded using the address table lookup of the DA contained in the frame.
	Broadcast	Broadcast frames sent by the host management system into IMP port are forwarded based on the broadcast rule that is in effect.
0 1 0	Egress Directed	An Egress Directed frame is sent by the host management system into the IMP port, and is forwarded to the Egress Port specified in the Destination Port ID fields in the BRCM Tag.
1 0 0	Multicast Egress Directed	A Multicast Egress Directed frame is sent by the host management system into the IMP port and is forwarded to multiple 10/100 Egress Ports specified in the Dest Port Vector field in Table 22 on page 90.
1 0 1	Multicast Egress Directed	A multicast Egress Directed frame is sent by the host management system into the IMP port and is forwarded to multiple Egress ports specified in the Dest Port Vector field in Table 22 on page 90.

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Table 24: TQ and TE Fields in BRCM Tag for Management Port Frame

Field	Name	Description
TQ[1:0]	Traffic Class Queue	Uses by the host CPU to assign a traffic class queue for forwarding the packet. • 11: Highest queue • 10: 3rd queue • 01: 2nd queue • 00: Lowest queue
TE[1:0]	Tag Enforcement	Used by the host CPU to enforce the 802.1Q/1p tagging/untagging encapsulation of the packet at the egress forwarding of the packet. • 11: Reserved • 10: Enforces tagging regardless of the 802.1Q VLAN untag mask • 01: Enforces untagging regardless of the 802.1Q VLAN untag mask • 00: No enforcement. Follows the 802.1Q VLAN untag mask

IMP Egress

Table 25 shows the format of the IMP Egress BRCM Tag field. The OPCODE field slightly modifies the use and validity of some fields in the Tag. Table 26 defines the supported OPCODEs.

Table 25: BRCM Header Tag Format (IMP to CPU)

31-29	28-17	16	15-14	13 - 8	7,6	5 - 0
Opcode = (000) Unicast Multicast/ Broadcast	Frame Oct Count[11:0] This 11-bit field incorporates the Octet Count of the entire Ethernet frame octet count starting at the DA field and inclusive of CRC, but not including the BRCM Type, BRCM Tag, and recalculated FCS.	RSVD	QoS: Indicates the traffic class queue used in forwarding the packet to CPU	Reason Code[5:0]: Indicates the reason code for the packet to be forwarded to CPU.	ERMON 7: Extended RMON for Ingress 6: Extended RMON for Egress	SRC_PID: Indicates the source Port ID for ingress directed frames.

Table 26: OPCODE Field in BRCM Tag for Management Port Frame

OpCodes	Name	Description
0 0 0	Unicast/ Multicast/ Broadcast	Unicast, multicast, reserved multicast and broadcast frames from a network port destined to the host management system are forwarded using the address table lookup of the DA contained in the frames. All frames are automatically inserted a BRCM Tag that includes the Frame Oct Count and Source Port ID fields.

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Table 27: Reason Code Field in BRCM Tag for Management Port Frame

Reason Code	Name	Description
0	Mirroring	The packet is mirrored to the CPU as the capture port.
1	SA Learning	The packet is forwarded to the CPU for controlled MAC SA learning.
2	Switching/Flooding	The packet is forwarded to the CPU either because of flooding or the CPU is the intended receive host.
3	Protocol Termination	The packet is trapped by the CPU because an IEEE 802.1-defined L2 protocol must be terminated by the CPU.
4	Protocol Snooping	The packet is copied to the CPU because an L3 or application level protocol must be monitored by the CPU for network security or operation efficiency.
5	Exception Processing/Flooding	The packet is trapped and forwarded to the CPU either because of flooding or for some special processing, even though the CPU is not the intended receive host.

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Switch Controller

The core of the BCM53262M device is a cost-effective and high-performance switch controller. The controller manages packet forwarding between the MAC receive and transmit ports through the frame buffer memory with a store and forward architecture. The switch controller encompasses the functions of buffer management, memory arbitration and transmit descriptor queueing.

Buffer Management

The frame buffer memory is divided into 256 bytes per page. Each packet received may allocated more than one page, of which, six pages are required for storing maximum 1536B frame data. Frame data is stored to the memory block as the packet is received. After reception, the frame is queued to the egress port(s) transmit queue. For unicast frames, following transmission of a packet from the frame buffer memory, the block of memory for the frame is released to the free buffer pool. If the frame is destined to multiple ports, the memory block is not released until all ports complete transmission of the frame.

Memory Arbitration

Processes requesting access to the internal memory include the receive and transmit frame data handlers, address resolution, learning and aging functions, and output port queue managers. These processes are arbitrated to provide fair access to the memory and minimize latency of critical processes to provide a fully nonblocking solution.

Transmit Output Port Queues

When the Quality of Service (QoS) function is turned off, the switch controller maintains an output port queue for each port. The queue depth becomes smaller for each output port when the QoS function is on. Transmit descriptors are updated after the packet has been received and the destination port resolved. One or two transmit descriptors are assigned to each destination port queue linking the destination with the frame data. For packets which have frame sizes larger than 512 bytes, two transmit descriptors are required. In the case of multicast and broadcast packets, a transmit descriptor for the packet is assigned to the transmit descriptor queues of multiple ports.

For each port, frames are initiated for transmission with minimum IPG until the transmit descriptor queue of the port is empty.

When the QoS is turned on, the single queue is split into four different-sized priority queues. These four queues are maintained by the switch controller for each transmit port. The weighted fair scheduling is applied to the queues to select frames from all queues and prevent starvation.

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Integrated High-Performance Memory

The BCM53262M includes 4 Mb of integrated, high-performance RAM which stores all packet buffer and address table information; and eliminates the need for external memory. This allows for the implementation of extremely low-cost systems.

Clocking

The BCM53262M uses a single 25-MHz clock input to derive the device's internal clocks to operate at 100 MHz, which affect the operation of the system logic and internal RAM. This allows for the best trade-offs with respect to performance, cost, and power.

MIB Engine

The MIB Engine is responsible for processing status words received from each port. Based on whether it is a receive status or transmit status, appropriate MIB counters are updated. The BCM53262M implements 70 plus MIB counters on a per-port basis. MIB counters can be categorized into three groups:

- Receive only counters
- Transmit only counters
- Receive or transmit counters

The receive or transmit counters group can, as a group, be selectively steered to the receive or transmit process on a per-port basis. The following section describes each individual counter.

MIB Counters Per Port

Table 28: Receive Only Counters (17)

Counters	*Description*
RxDropPkts (32 bit)	The number of packets received by a port that were dropped due to security conflict when MAC address security Control is enabled.
RxOctets (64 bit)	The number of bytes of data received by a port (excluding preamble but including FCS), including bad packets.
RxBroadcastPkts (32 bit)	The number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
RxMulticastPkts (32 bit)	The number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
RxSAChanges (32 bit)	The number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater based network.

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Table 28: Receive Only Counters (17) (Cont.)

Counters	Description
RxUndersizePkts (32 bit)	The number of good packets received by a port that are less than 64 bytes long (excluding framing bits but including the FCS).
RxOversizePkts (32 bit)	The number of good packets received by a port that are greater than MAX_RX_LIMIT (excluding framing bits but including the FCS). This counter alone is incremented for packets in the range MAX_RX_LIMIT–2048 bytes inclusive, whereas both this counter and the RxExcessSizeDisc counter is incremented for packets of 2049 bytes and higher. (Revision B silicon.) See Bit 2:1 at Table 56: "New Control Register (Page 00h: Address 03h)," on page 167. The number of good packets received by a port that are greater than 1518 (excluding framing bits but including the FCS). This counter alone is incremented for packets in the range 1518–2048 bytes inclusive, whereas both this counter and the RxExcessSizeDisc counter is incremented for packets of 2049 bytes and higher. (Revision A silicon)
RxFragments (32 bit)	The number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.
RxJabbers (32 bit)	The number of packets received by a port that are longer than MAX_RX_LIMIT bytes and have either an FCS error or an alignment error (Revision B silicon). See Bit 2:1 at Table 56: "New Control Register (Page 00h: Address 03h)," on page 167. The number of packets received by a port that are longer than 1522 bytes and have either an FCS error or an alignment error (Revision A silicon).
RxUnicastPkts (32 bit)	The number of good packets received by a port that are addressed to a unicast address.
RxAlignmentErrors (32 bit)	The number of packets received by a port that have a length (excluding framing bits but including FCS) between 64 and 1522 bytes, inclusive, and have a bad FCS with a nonintegral number of bytes.
RxFCSErrors (32 bit)	The number of packets received by a port that have a length (excluding framing bits but including FCS) between 64 and 1522 bytes inclusive, and have a bad FCS with an integral number of bytes.
RxGoodOctets (64 bit)	The total number of bytes in all good packets received by a port (excluding framing bits, but including FCS).
RxExcessSizeDisc (32 bit)	The number of good packets received by a port that are greater than 2048 bytes (excluding framing bits but including the FCS) and were discarded due to excessive length.
RxPausePkts (32 bit)	The number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC Control Frame EtherType field (88-08h), have a destination MAC address of either the MAC Control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE Opcode (00-01), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an 802.3-compliant MAC is only permitted to transmit PAUSE frames when in full duplex mode, with flow control enabled, and with the transfer of PAUSE frames determined by the result of auto-negotiation, an 802.3-MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network.

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Table 28: Receive Only Counters (17) (Cont.)

Counters	Description
RxSymbolErrors (32 bit)	The total number of times a valid length packet was received at a port and at least one invalid data symbol was detected. Counter only increment once per carrier event and does not increment on detection of collision during the carrier event.
RxDiscPkts (32 bit)	The number of good packets received by a port that are discarded by the forwarding processes. This counter increments each time a good packet received by a port is discarded due to a final egress forwarding decision produced by the following processes: • ARL DA • VLAN • Spanning tree • EAP • CFP • Protected port • WAN port • VPN port • Link down status • Rate control • Flow control This counter does not include packets dropped due to Rx-based flow control process.

Table 29: Transmit Counters Only (21)

Counters	Description
TxDropPkts (32 bit)	This counter is incremented every time a transmit packet is dropped due to lack of resources (e.g., transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters.
TxOctets (64 bit)	The total number of good bytes of data transmitted by a port (excluding preamble but including FCS).
TxBroadcastPkts (32 bit)	The number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
TxMulticastPkts (32 bit)	The number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
TxCollisions (32 bit)	The number of collisions experienced by a port during packet transmissions.
TxUnicastPkts (32 bit)	The number of good packets transmitted by a port that are addressed to a unicast address.
TxSingleCollision (32 bit)	The number of packets successfully transmitted by a port that experienced exactly one collision.
TxMultipleCollision (32 bit)	The number of packets successfully transmitted by a port that experienced more than one collision.

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Table 29: Transmit Counters Only (21) (Cont.)

Counters	Description
TxDeferredTransmit (32 bit)	The number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy.
TxLateCollision (32 bit)	The number of times that a collision is detected later than 512 bit-times into the transmission of a packet.
TxExcessiveCollision (32 bit)	The number of packets that are not transmitted from a port because the packet experienced 16 transmission attempts.
TxPausePkts (32 bit)	The number of PAUSE frames transmitted by a port. The MAC resolve to full duplex mode, with 802.3x flow control PAUSE frame exchange enabled at the completion of auto-negotiation.
TxFrameInDisc (32 bit)	The number of valid packets received which are discarded by the forwarding process due to lack of space on an output queue. Not maintained or reported in the MIB counters. Located in the Congestion Management registers (Page 0Ah). This attribute only increments if a network device is not acting in compliance with a flow control request, or the BCM53262M internal flow control/buffering scheme has been misconfigured.
TxQoS0Pkts (32 bit)	The total number of good packets transmitted on queue 0 when QoS is enabled.
TxQoS0Octets (64 bit)	The total number of good bytes transmitted on queue 0 when QoS is enabled.
TxQoS1Pkts (32 bit)	The total number of good packets transmitted on queue 1 when QoS is enabled.
TxQoS1Octets (64 bit)	The total number of good bytes transmitted on queue 1 when QoS is enabled.
TxQoS2Pkts (32 bit)	The total number of good packets transmitted on queue 2 when QoS is enabled.
TxQoS2Octets (64 bit)	The total number of good bytes transmitted on queue 2 when QoS is enabled.
TxQoS3Pkts (32 bit)	The total number of good packets transmitted on queue 3 when QoS is enabled.
TxQoS3Octets (64 bit)	The total number of good bytes transmitted on queue 3 when QoS is enabled.

Table 30: Transmit or Receive Counters (6)

Counters	Description
Pkts64Octets (32 bit)	The number of packets (including error packets) that are 64 bytes long.
Pkts65to127Octets (32 bit)	The number of packets (including error packets) that are between 65 and 127 bytes long.
Pkts128to255Octets (32 bit)	The number of packets (including error packets) that are between 128 and 255 bytes long.
Pkts256to511Octets (32 bit)	The number of packets (including error packets) that are between 256 and 511 bytes long.
Pkts512to1023Octets (32 bit)	The number of packets (including error packets) that are between 512 and 1023 bytes long.
Pkts1024toMaxOctets (32 bit) (Revision B silicon)	The number of packets (including error packets) that are between 1024 and MAX_RX_LIMIT bytes long. See Bit 2:1 at Table 56: "New Control Register (Page 00h: Address 03h)," on page 167.
Pkts1024to1522Octets (32 bit) (Revision A silicon)	The number of packets (including error packets) that are between 1024 and 1522 bytes long.

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Total Number of Counters Per Port: 35

Table 31 identifies the mapping of the BCM53262M MIB counters and their generic mnemonics, to the specific counters and mnemonics for each of the key IETF MIBs which are supported (this is defined where there is a direct mapping). However, there are several additional statistics counters that are indirectly supported, which make up the full complement of the counters required to fully support each MIB. These are shown in Table 32 on page 100. Finally, Table 33 on page 100 identifies the additional counters supported by the BCM53262M, and references the specific standard or reason for the inclusion of the counter.

Table 31: Directly Supported MIB Counters

BCM53262M MIB	*Ethernet-Like MIB RFC 1643*	*Bridge MIB RFC 1493*	*MIB II Interface RFC 1213/1573*	*RMON MIB RFC 1757*
RxDropPkts	dot3StatsInternalMAC ReceiveErrors	dot1dTpPortInDiscards	ifInDiscards	–
RxOctets	–	–	ifInOctets	etherStatsOctets
RxBroadcastPkts	–	–	ifInBroadcastPkts	etherStatsBroadcastPkts
RxMulticastPkts	–	–	ifInMulticastPkts	etherStatsMulticastPkts
RxSAChanges	Note 2	Note 2	Note 2	Note 2
RxUndersizePkts	–	–	–	etherStatsUndersizePkts
RxOversizePkts	dot3StatsFrameToo Longs	–	–	etherStatsOverrsizePkts
RxFragments	–	–	–	eytherStatsFragments
RxJabbers	–	–	–	etherStatsJabbers
RxUnicastPkts	–	–	ifInUcastPkts	–
RxAlignmentErrors	dot3StatsAlignmentErrors	–	–	–
RxFCSErrors	dot3StatsFCSErrors	–	–	–
RxGoodOctets	–	–	–	–
RxExcessSizeDisc	Note 2	Note 2	Note 2	Note 2
RxPausePkts	Note 2	Note 2	Note 2	Note 2
RxSymbolErrors	Note 2	Note 2	Note 2	Note 2
Note 1	–	–	ifInErrors	–
Note 1	–	–	ifInUnknownProtos	–
Note 1	–	dot1dTpPortInFrames	–	–
TxDropPkts	dot3StatsInternalMAC TransmitErrors	–	ifOutDiscards	–
TxOctets	–	–	ifOutOctets Note 3	–
Note 1	–	dot1dTpPortOutFrames	–	–
TxBroadcastPkts	–	–	ifOutBroadcastPkts	–
TxMulticastPkts	–	–	ifOutMulticastPkts	–
TxCollisions	–	–	–	etherStatsCollisions
TxUnicastPkts	–	–	ifOutUcastPkts	–
TxSingleCollision	dot3StatsSingleCollision Frames	–	–	–
TxMultipleCollision	dot3StatsMultipleCollisio n Frames	–	–	–

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Table 31: Directly Supported MIB Counters (Cont.)

BCM53262M MIB	Ethernet-Like MIB RFC 1643	Bridge MIB RFC 1493	MIB II Interface RFC 1213/1573	RMON MIB RFC 1757
TxDeferredTransmit	dot3StatsDeferred Transmissions	–	–	–
TxLateCollision	dot3StatsLateCollision	–	–	–
TxExcessiveCollision	dot3StatsExcessive Collision	–	–	–
TxFrameInDisc	Note 2	Note 2	Note 2	Note 2
TxPausePkts	Note 2	Note 2	Note 2	Note 2
Note 4	dot3StatsCarrierSense Errors	–	–	–
Note 1	–	–	ifOutErrors	–
Pkts64Octets	–	–	–	etherStatsPkt64Octets
Pkts65to127Octets	–	–	–	etherStatsPkt65to127 Octets
Pkts128to255Octets	–	–	–	etherStatsPkt128to255 Octets
Pkts256to511Octets	–	–	–	etherStatsPkt256to511 Octets
Pkts512to1023Octets	–	–	–	etherStatsPkt512to1023 Octets
Pkts1024toMaxOctets (Revision B silicon)	–	–	–	etherStatsPkt1024toMax Octets
Pkts1024to1522Octets (Revision A silicon)	–	–	–	etherStatsPkt1024to1522 Octets
Note 1	–	–	–	etherStatsDropEvents
Note 1	–	–	–	etherStatsPkts
Note 1	–	–	–	etherStatsCRCAlignErrors
Note 4	dot3StatsSQETestErrors	–	–	–

Note 1: Derived by summing two or more of the supported counters. See Table 32 on page 100 for specific details.
Note 2: Extensions required by recent Standards developments or BCM53262M operation specifics.
Note 3: The MIB II Interfaces specification for if OutOctets includes preamble/SFD and errored bytes. Because 802.3 compliant MACs have no requirement to keep track of the number of transmit bytes in an errored frame, this count is impossible to maintain. The TxOctets maintained by the BCM53262M is consistent with good bytes transmitted, excluding preamble but including FCS. The count can be adjusted to more closely match the if OutOctets definition by adding the preamble for TxGoodPkts, and possibly an estimate of the octets involved in TxCollisions and TxLateCollision.
Note 4: The attributes TxCarrierSenseErrors and TxSQETestErrors are not supported in the BCM53262M. These attributes were originally defined to support coax based AUI transceivers. The BCM53262M's integrated transceiver design means these error conditions are eliminated. MIBs intending to support such counters should return a value of 0 or not supported.

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Table 32: Indirectly Supported MIB Counters

BCM53262M MIB	*Ethernet-Like MIB RFC 1643*	*Bridge MIB RFC 1493*	*MIB II Interface RFC 1213/1573*	*RMON MIB RFC 1757*
RxErrorPkts = RxAlignmentErrors + RxFCSErrors + RxFragments + RxOversizePkts + RxJabbers	–	–	ifInErrors	–
–	–	–	ifInUnknownProtos	–
RxGoodPkts = RxUnicastPkts + RxMulticastPkts + RxBroadcastPkts	–	dot1dTpPortIn Frames	–	–
DropEvents = RxDropPkts + TxDropPkts	–	–	–	etherStatsDrop Events
RxTotalPkts = RxGoodPkts + RxErrorPkts	–	–	–	etherStatsPkts
RxCRCAlignErrors = RxCRCErrors + RxAlignmentErrors	–	–	–	etherStatsCRCAlign Errors
NA—BCM53262M cannot experience this error—return as 0	dot3StatsSQETest Errors	–	–	–
RxFramesTooLong = RxOversizePkts + RxJabber	dot3StatsFrameToo Longs	–	–	–
TxGoodPkts = TxUnicastPkts + TxMulticastPkts + TxBroadcastPkts	–	dot1dTpPortOut Frames	–	–
TxErrorPkts = TxExcessiveCollision + TxLateCollision Note 1	–	–	ifOutErrors	–

Note 1: The number of packets transmitted from a port which experienced late collision, or excessive collision. While for some media types in half-duplex operation, frames which experience carrier sense errors are also summed in this counter, the BCM53262M's integrated design means this error condition is eliminated.

Table 33: Supported MIB Extensions

MIB	*Appropriate Standards Reference*
RxSAChanges	IEEE 802.3u Clause 30—Repeater Port Managed Object Class, aSourceAddressChanges

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Table 33: Supported MIB Extensions (Cont.)

MIB	*Appropriate Standards Reference*
RxExcessSizeDisc	The BCM53262M cannot store packets in excess of 1536 bytes (excluding preamble/SFD but inclusive of FCS). This counter indicates packets that were discarded by the BCM53262M due to excessive length.
RxPausePkts	IEEE 802.3x Clause 30—Pause Entity Managed Object Class, PAUSEMACCtrlFramesReceived
RxSymbolErrors	IEEE 802.3u Clause 30—Repeater Port Managed Object Class, aSymbolErrorDuringPacket
TxFrameInDisc	Internal diagnostic use for optimization of flow control and buffer allocation algorithm.
TxPausePkts	IEEE 802.3x Clause 30—Pause Entity Managed Object Class, aPAUSEMACCtrlFramesTransmitted

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Section 4: System Interfaces

Overview

The BCM53262M includes the following interfaces.

Each of these is discussed in more detail in the following sections.

- "MII Port" on page 102
- "10/100 Mbps Copper Interface" on page 106
- "Configuration Pins" on page 107
- "Programming Interfaces" on page 107
- "EEPROM Interface" on page 112
- "Extended Bus Interface" on page 113
- "MDC/MDIO Interface" on page 118
- "LED Interfaces" on page 127
- "JTAG Interface" on page 136

MII Port

The BCM53262M provides a fully 802.3u compatible MII interface as a twenty-fifth network port (port 48). The port can be configured to operate differently dependent on the programming of the internal registers.

Network Port

In unmanaged mode after power-up, the MII operates as a normal MAC-based MII port, capable of interfacing directly to an external TX or FX transceiver. The port incorporates an internal MAC, and functions identically to the integrated 10/100 ports. Frames are forwarded to the port under control of the forwarding model.

Predecessors of the BCM53262M device allowed the MII management signals (MDC/MDIO) to interrogate the internal MII registers associated with the integrated 10/100 Mbps PHYs. The BCM53262M can still support this mode, in which case, configuration of the integrated PHYs requires the 2.5-MHz clock to be supplied to the BCM53262M MDC pin and any external MII-connected transceiver, and the external management device controls MDIO to select and configure all the PHYs appropriately. To operate in this mode, the external transceiver needs to support some signals in addition to the standard MII signals, so that the state of the external transceiver can be monitored by the BCM53262M. Individual active-low Link, Speed (100 Mbps), Duplex, and link partner Flow Control mode signals from the transceiver should be provided. An MII-based single 10/100 Mbps PHY, such as the BCM5202, provides these additional signals. With these additional signals, the BCM53262M generates port LEDs for the external MII-based PHY, equivalent to the LEDs of the internal transceivers.

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The more typical use of the MII in a BCM53262M implementation is that the device is accessed via the SPI. In this case, on sensing activity of the SPI, the BCM53262M takes control of the MII management pins, and sources the 2.5-MHz clock signal for MDC. The external PHY can be accessed by the management entity, since its MII registers are aliased to the Port 48 (Table 327: “External Port MII Registers Page Versus PHY,” on page 374). Access to MII registers in this page in the register map automatically generates an MDIO/MDC request to the external MII-based transceiver, allowing configuration control and status monitoring of the off-chip PHY port.The MII port uses the unique PHY address of 18h. The external PHY must be programmed/ strapped to respond to the PHY address of 18h. See “MDC/MDIO Interface” on page 118 for additional detail on internal and external PHY address values.

When an external transceiver is connected to the BCM53262M MII port and managed by the MDC/MDIO lines, the state of the link, speed, full/half-duplex and link partner flow control capabilities (among many others) can all be accessed via software, and need not be provided as hardware pins. In order to preserve LED display capabilities for the MII port, an additional alias register is provided in the Control registers (Page 0h), All the specific register information is temporary and subject to be change in the final version of the data sheet. This allows the state of the aforementioned status bits to be read from the external PHY and then written to this register, so that consistent LED status information for all 10/100 ports can be preserved.

If no MII-based external transceiver is present, page 28h of the register space is not present, and returns indeterminate data when read.

Reverse MII Port

BCM53262M device includes an enhanced MII mode that supports direct MAC-to-MAC connectivity. The BCM53262M device supports a strap option selectable Reverse MII (RvMII) mode, which makes the BCM53262M MII interface appear as a 100-Mbps full-duplex PHY MII, as seen by the external MAC.

To support this RvMII mode, the clock-to-data timing has been modified. The TXC/RXC input clocks become 25-MHz clock outputs (identical to those of a PHY MII) that only support a 100-Mbps MII interface.

Rv MII mode is enabled by selecting the strap pin RvMII.

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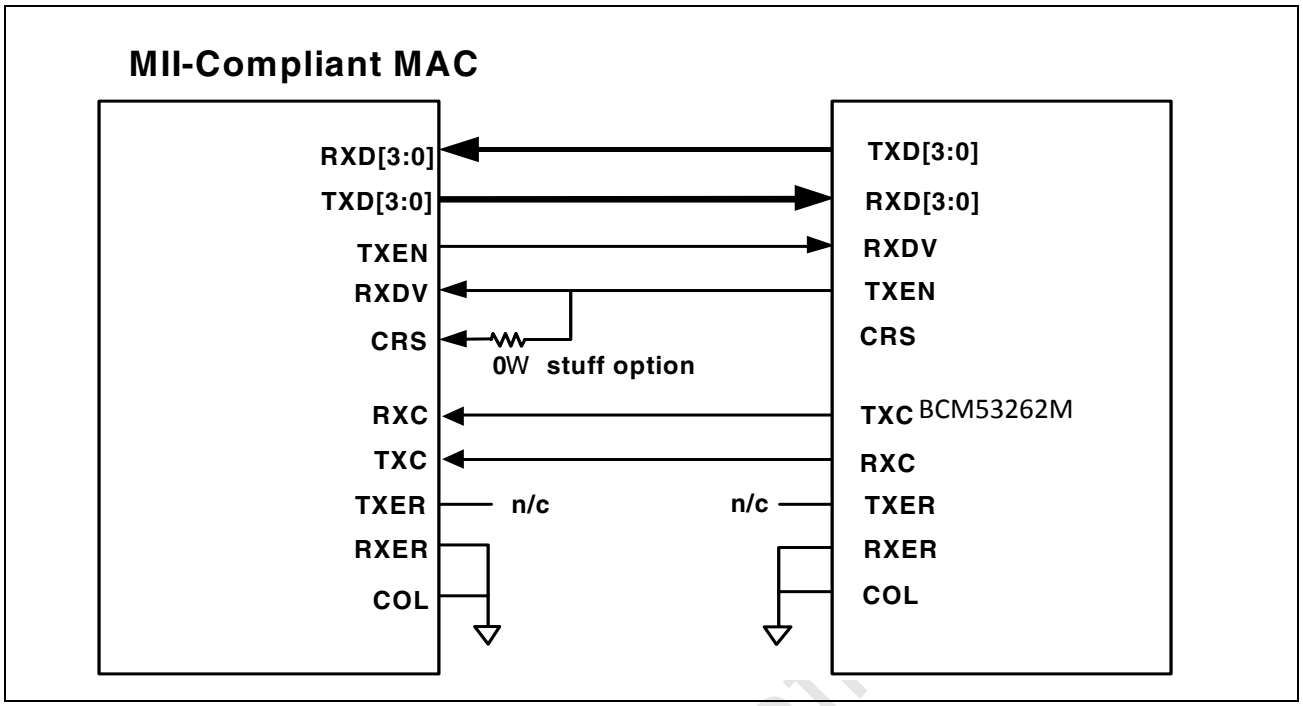

Figure 19: MAC-to-MAC MII Connection

Management Port (IMP)

The dedicated port can be used as a high-speed connection to transfer management packets to the external management agent. For more information, see "Frame Management" on page 88

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Serial Interface

Each LVDS-compatible serial port can be configured in SGMII or SerDes mode.

SGMII Mode

The SGMII interface transmits serial data differentially at 1.25 Gbaud via the (SD_TXDN, SD_TXDP) pins, and receives serial data differentially via the (SD_RXDN, SD_RXDP) pins. Transmit data timing is recovered from the incoming data signal and the attached link partner does so, likewise. The SGMII interface pins are shared with the SerDes interface pins.

The data signals operate at 1.25 Gbaud. Each of these signals is realized as a differential pair because of the speed of operation, providing signal integrity while minimizing system noise. The SGMII signals use LVDS voltage levels. Both the data and clock signals are DC-balanced; therefore, implementations that meet the AC parameters, but fail to meet the DC parameters, can be AC-coupled.

The 1.25-Gbaud transfer rate of the SGMII is greater than required for the BCM53262M transceiver operating at 10 Mbps or 100 Mbps. When these situations occur, the BCM53262M elongates the frame by replicating each frame byte 10 times for 100 Mbps and 100 times for 10 Mbps. This frame elongation takes place above the IEEE Standard 802.3z PCS layer, making the start-frame delimiter appear only once per frame.

When the device operates at 10 Mbps or 100 Mbps, the SGMII differential pair replicates the data 100 and 10 times, respectively.

SerDes Mode

The SerDes interface operates via 1000Base-X and complies with IEEE 802.3, Clauses 36 and 37. The interface shares differential data pins with the SGMII interface. The BCM53262M SerDes can be used in various applications as listed below.

- The SerDes interface can be connected to SerDes fiber modules creating switched fiber ports.
- The SerDes interface and be connected to a SerDes-to-copper PHY creating switched copper ports.
- The SerDes interface can be connected to a SerDes MAC or switch for a SerDes switch-to-switch application.

The SerDes auto-negotiation is similar to the SGMII except for the link timer. Table 34 summarizes the differences between the two interfaces.The differential pair runs at 1.25 Gbps. The data is 8b/10b encoded, and the decoded data throughput is 1 Gbps.

Table 34: SGMII and SerDes Auto-Negotiation

	Link Timer	*Remote Fault*	*PAUSE Frame*	*Speed Bit*	*Link Status*	*Duplex Bit*
SGMII	1.6 ms	Not Supported	Not Supported	Supported	Supported	Supported
SerDes	10 ms	Supported	Supported	Not Supported (always 1000Base-X)	Not Supported	Supported

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SerDes/SGMII Auto-Negotiation

It is necessary to pass control information to the link partner when establishing a link. The link partner receives and decodes the sent control information and also begins auto-negotiation. The link partner acknowledges the update of the link status and visa versa. Upon receiving proper acknowledgement, the BCM53262M completes auto-negotiation and returns to normal data mode. The included control information for SerDes and SGMII is compared in Table 34.

10/100 Mbps Copper Interface

The internal PHYs transmit and receive data via the digiPHY. This section discusses the following topics:

- "Auto-Negotiation"
- "Automatic MDI Crossover"
- "10/100Base-T Forced Mode Auto-MDIX"

For more information on the integrated PHY block, see "Integrated PHY" on page 77.

Auto-Negotiation

The BCM53262M negotiates its mode of operation over the copper media using the auto-negotiation mechanism defined in the IEEE 802.3u specifications. When the auto-negotiation function is enabled, the BCM53262M automatically chooses the mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM53262M can be configured to advertise the following modes:

- 100Base-TX full-duplex and/or half-duplex
- 10Base-T full-duplex and/or half-duplex

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode, commonly referred to as highest common denominator (HCD).

Automatic MDI Crossover

During auto-negotiation, one end of the link needs to perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The BCM53262M internal PHY can perform an automatic media dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports.

During auto-negotiation, the BCM53262M internal PHY normally transmits on the TD± pin and receives on the RD± pin. When connecting to another device that does not perform MDI crossover, the BCM53262M internal PHY automatically switches its RD±/TD± pin pairs, when necessary, to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function. During 100Base-TX operation, pair swaps automatically occur within the device and do not require user intervention.

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10/100Base-T Forced Mode Auto-MDIX

The Forced Mode Auto-MDIX feature allows the copper auto-negotiation to be disabled in either 10Base-T or 100Base-T and still take advantage of the automatic MDI crossover function. Whenever the forced link is down for at least four seconds, then auto-negotiation is internally enabled with its automatic MDI crossover function until link pulses or 100Base-Tx idles are detected. Once detected, the internal PHY returns to forced mode operation.

Configuration Pins

Initial configuration of the BCM53262M takes place during power-on/reset by loading internal control values from hardware strap pins. The value of the pin is loaded when the reset sequence completes and the pin transitions to normal operation. Pull-up or pull-down resistors can be added to these pins to control the device configuration. If the pins are left floating, the default value is determined based on the internal pull-up or pull-down configuration.

Programming Interfaces

The BCM53262M can be programmed via the SPI Interface, EEPROM Interface, or Extended Bus. The SPI interface provides access for a general purpose microcontroller, allowing read and write access to the internal BCM53262M register space. It is configured to be compatible with the Motorola® Serial Peripheral Interface (SPI) protocol. Alternatively, the EEPROM interface can be connected to an external EEPROM for writing register values upon power-up initialization.

A 16-bit or 8-bit extended bus interface on the BCM53262M is designed to provide connection to an external processor, allowing read and write accesses to the internal BCM53262M registers.

The internal address space of the BCM53262M device is broken into a number of pages. Each page groups a logical set of registers associated with a specific function. Each page provides a logical address space of 256 bytes, although, in general, only a small portion of the address space in each page is utilized.

SPI Interface

The BCM53262M can be controlled over a serial interface that is compatible with a subset of the Motorola Synchronous Serial Peripheral Interconnect (SPI) bus. The microcontroller interface consists of four signals: serial clock (SCK), slave select (SS/CS), master-in/slave-out (MISO/DO) and master-out/slave-in (MOSI/DI). The BCM53262M always operates as an SPI slave device, in that it never initiates a transfer on the SPI and only responds to the read and write requests issued from a master device.

A layer of protocol is added to the basic SPI definition to facilitate transfers from the BCM53262M. This protocol establishes the definition of the first two bytes issued by the master to the BCM53262M slave during an SPI transfer. The first byte issued from the SPI master in any transaction is defined as a command byte, which is always followed by a register address byte, and any additional bytes are data bytes.

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The SPI mode supports normal SPI determined by the content of the command byte. Table 35 shows the normal SPI command byte.

Table 35: Normal SPI Command Byte

0	1	1	MODE = 0	CHIP ID 2 (MSB)	CHIP ID 1	CHIP ID 0 (LSB)	Read/ Write (0/1)

The MODE bit (bit 4) of the command byte determines the meaning of bits 7:5. If bit 4 is a 0, it is a normal SPI command byte, and bits 7:5 should be defined as 011b.

In command bytes, bits[3:1] indicate the CHIP ID to be accessed. Because the BCM53262M operates as a single-chip system, the CHIP ID will be 000. Note that the SS# signal must also be active for any BCM53262M device to recognize that it is being accessed.

Bit 0 of the command byte is the R/W signal (0 = Read, 1 = Write) and determines the transmission direction of the data.

The byte following the command byte is an 8-bit register address. Initially, this sets the page address, followed by another command byte that contains the register base address in that page, which is used as the location to store the next byte of data received in the case of a write operation, or the next address from which to retrieve data in the case of a read operation. This base address increments as each byte of data is transmitted/ received, allowing a contiguous block data from a register to be stored/read in a single transmission.

Noncontiguous blocks are also stored/read through the use of multiple transmissions, which allow a new command byte and register base address to be specified. The $\overline{SS}$ signal must remain low for the entire read or write transaction, as shown in Figure 20 on page 108 and Figure 21 on page 108, with the transaction terminated by the deassertion of the $\overline{SS}$ line by the master.

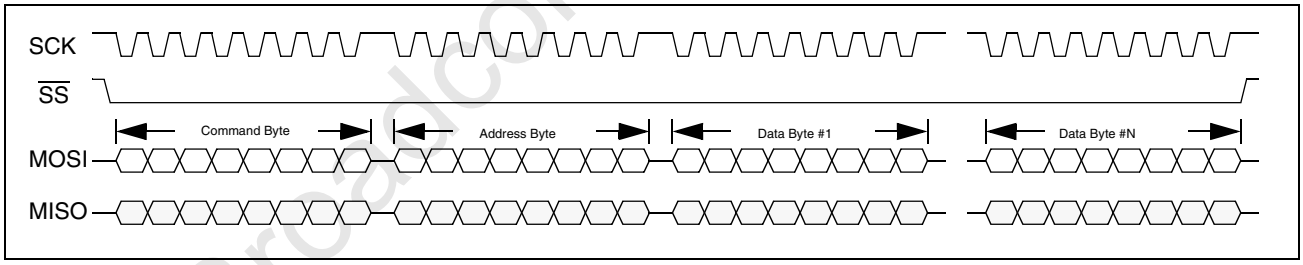

Figure 20: SPI Serial Interface Write Operation

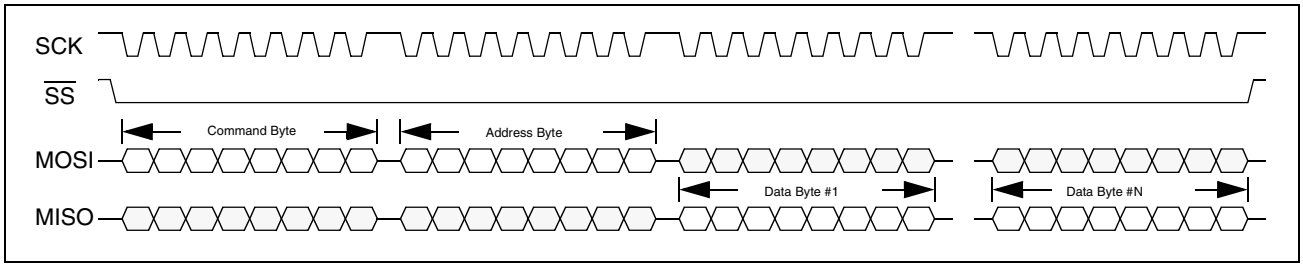

Figure 21: SPI Serial Interface Read Operation

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The Serial Interface supports operation up to 2 MHz in SPI mode.

Normal SPI Mode

Normal SPI mode allows single-byte read and multibyte string write operations, with the CPU polling to monitor progress. Read operations are performed using the SPI Status Register and SPI Data I/O Register. All read operations take the form:

<CMD, CHIP ID, R><REG ADDR>

where the first byte is the command byte with the appropriate CHIP ID and Read bits set, and the second byte is the register address.

All write operations are of the form:

<CMD, CHIP ID, W><REG ADDR><DATA0>...<DATAn>

where the first byte is the command byte with the appropriate CHIP ID and Write bits set, the second byte is the register address, and the remaining bytes are the exact number of data bytes appropriate for the selected register follow. Failure to provide the correct number of data bytes means the register write operation does not occur.

A simple flow chart for the read process is shown in Figure 22 on page 110.

To read a register, first the Page Register is written (<CMD, CHIP ID, W><REG ADDR = FFh><DATA = NEW PAGE>). It is only necessary to write the page register when moving to a new page. Once in the correct page, a read operation is performed on the appropriate register (<CMD, CHIP ID, R><REG ADDR>). Once the SPI Status Register indicates that the data is available (RACK = 1), the data can be read. Data is read from the SPI Data I/O Register, located at F0h–F7h on every page (so no page swap is necessary to read the data on any page). A read operation can access any or all of the bytes on a specific register, including the ability to start at any offset. For instance, reading from SPI Data I/O Register [0], reads the least significant byte of the register, and successive reads to SPI Data I/O Register [0] read the remaining bytes. However, reading the first byte from SPI Data I/O Register [2] reads the third byte of the register, and successive reads to SPI Data I/O Register [2] reads the remaining bytes of the register up to the most significant byte of the register. It is not necessary to read all bytes of a registers, only the bytes of interest. The SPI master can then move on to perform another read or write operation.

A flow chart for the write process is shown in Figure 23 on page 111. To write a register, the Page Register is written if necessary (<CMD, CHIP ID, W><REG ADDR = FFh><DATA = NEW PAGE>), then data is written to the selected register (<CMD, CHIP ID, W><REG ADDR><DATA0>...<DATAn>), where DATA0 is the least significant byte of the register, and DATAn is the most significant byte of the register, and the exact number of bytes is present as defined by the register width. No byte offset is provided for write operations, and all bytes must be present to activate the write process internal to the BCM53262M.

The following simple rules apply to the normal SPI mode:

- A write to the page register at any time causes the SPI state machine to reset.
- A read operation can access any number of bytes at any offset using the SPI Data I/O Register.
- A write operation must write the exact number of bytes to the register being accessed.
- The RXRDY/TXRDY flags in SPI Status Register must be checked after each 8-byte string has been read/written to ensure the next string is ready and can be accepted (since the largest internal register is 8

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bytes, this restriction only applies to reading and writing frames via the SPI).

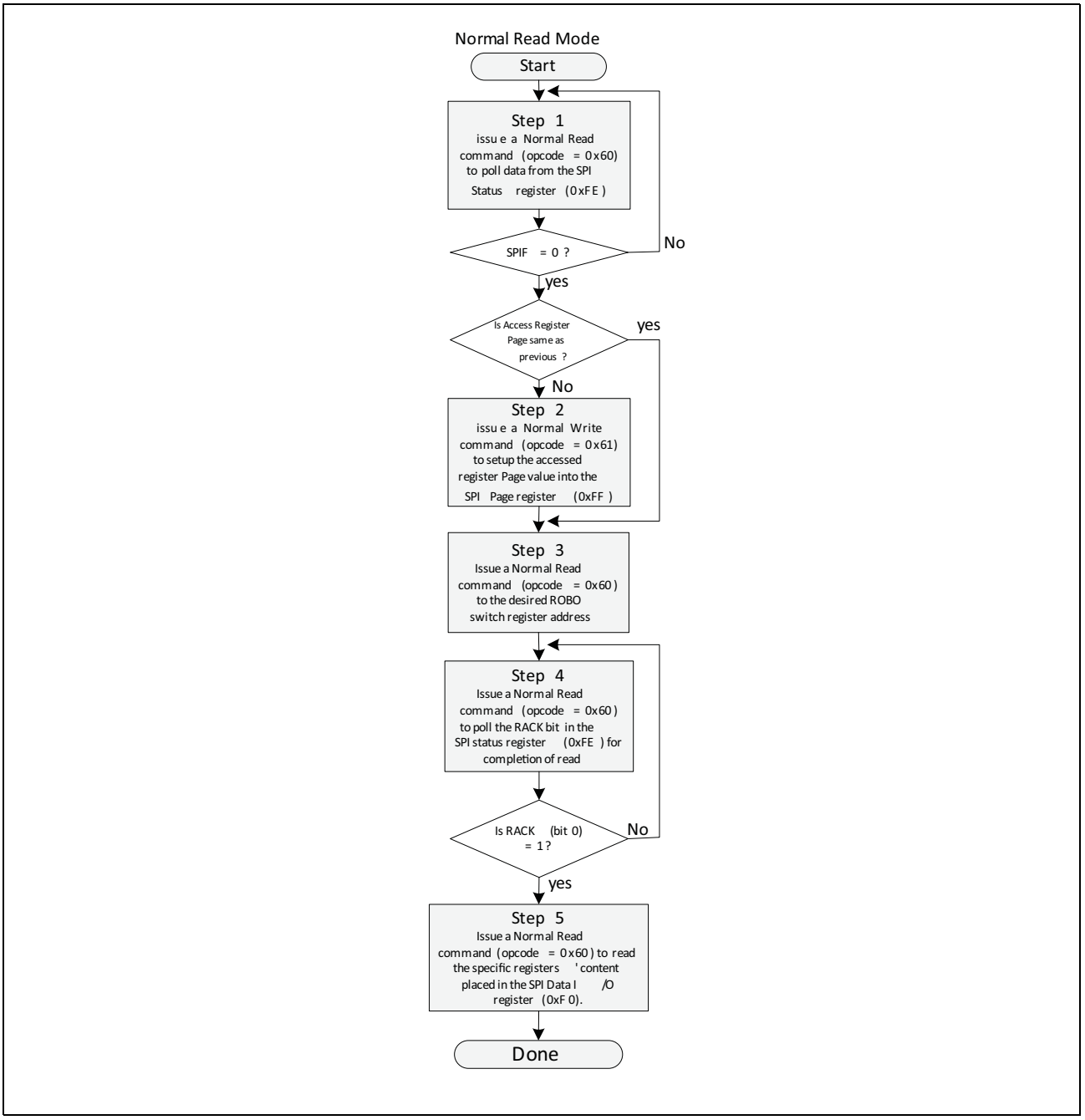

Figure 22: Normal SPI Mode Read Flow Chrt

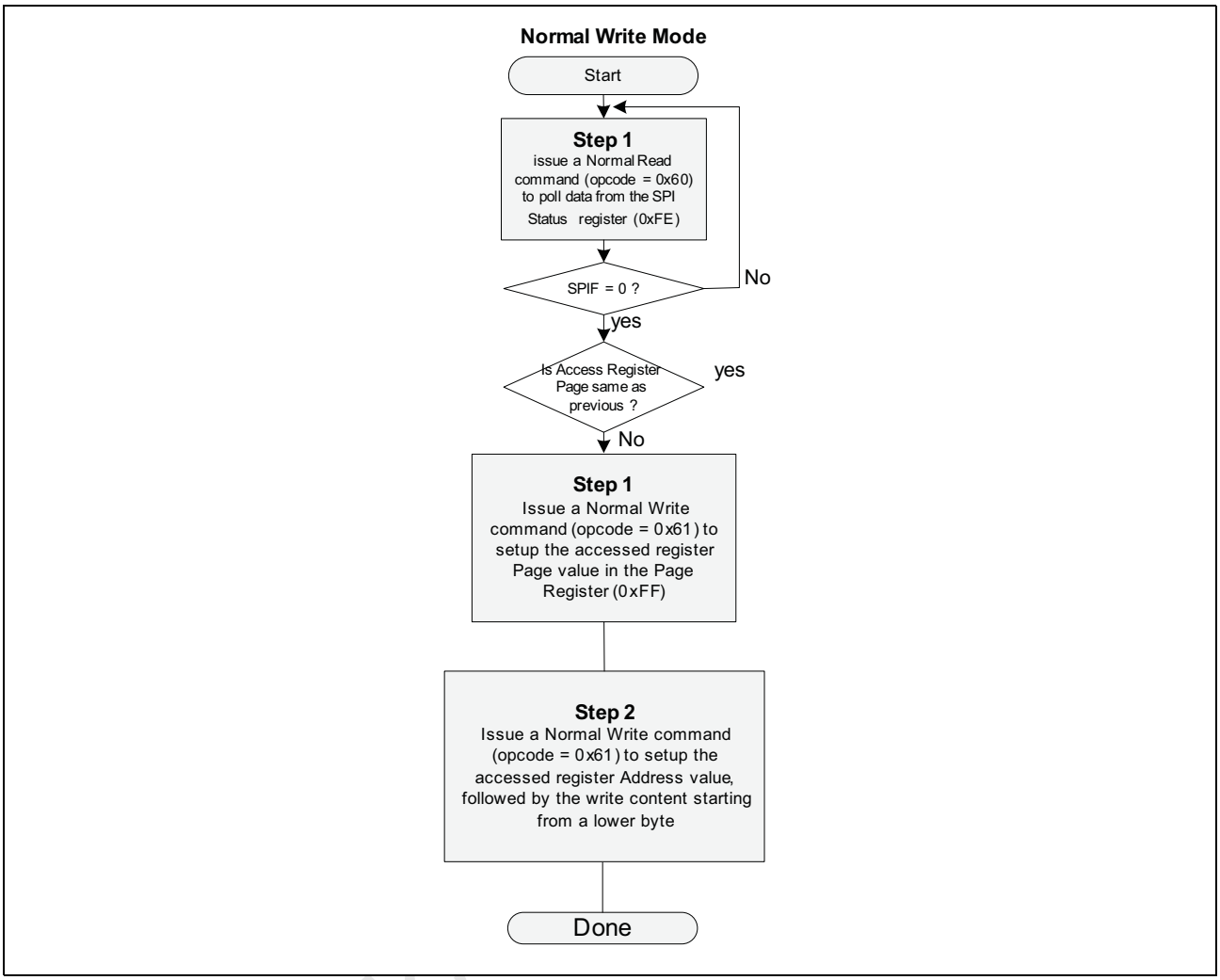

Figure 23: Normal SPI Mode Write Flow Chart

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EEPROM Interface

The BCM53262M can be connected via the Serial Interface to a low-cost external serial EEPROM, enabling it to download register programming instructions during power-on initialization.For each programming instruction fetched from the EEPROM, the instruction executes immediately and affects the register file.

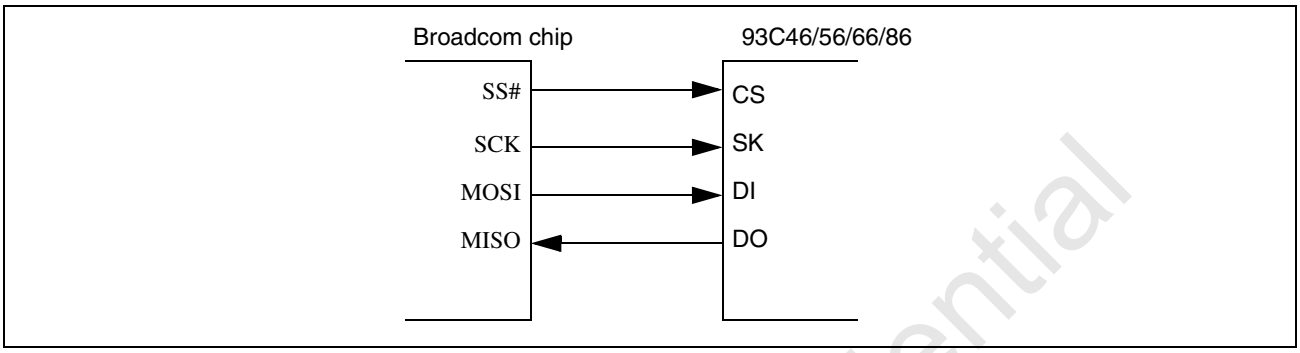

Figure 24: Serial EEPROM Connection

During the chip initialization phase, the data is sequentially read-in from the EEPROM after the internal memory has been cleared. The first data read-in is the HEADER and matches a predefined magic code. In the case where the HEADER data does not match the instruction fetch, the process stops, and the EEPROM controller treats it as if no EEPROM exists. If the magic code matches, the fetch instruction process continues until it reaches the instruction length defined in the HEADER.

The BCM53262M supports EEPROMs with varying capacities. These include the 93C46, 93C56, 93C66 and 93C86. The BCM53262M implements the automatic detection of EEPROM types. The two EEPROM_TYPE[1:0] strap pins are designated as “don't cares” and “can be ignored”.

EEPROM Format

The EEPROM should be configured to x16 word format. The header contains a key and length information as in Table 36.

- Upper 5 bits are magic code 15h, which indicates valid data follows.
- Bit 10 is for speed indication. A 0 means normal speed. A 1 indicates speed up. The default is 0.
- Lower 10 bits indicate the total length of all entries. For example:
  - 93C46 up to 64 words
  - 93C56 up to 128 words
  - 93C66 up to 256 words
  - 93C86 up to 1024 words

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Table 36: EEPROM Header Format

15:11	*10*	*9:0*
Magic code, 15h	Speed	Total Entry Number • 93C46: 0–63 • 93C56: 0–127 • 93C66: 0–255 • 93C86: 0–1023

After chip initialization, the header is read from the EEPROM and used to compare to the pre-defined magic code. When the fetched data does not match the predefined magic code, the EEPROM instruction fetch process is stopped. If the magic code is matched, fetching instructions continues until the instruction length as defined in the HEADER.

The EEPROM Port shares pins with the SPI port. Either the SPI port or the EEPROM can be selected by using the strap pin, CPU_EEPROM_SEL. The register space for the EEPROM port is the same as for the SPI port.

Contact your local Broadcom FAE for EEPROM Programming Guide for more details on EEPROM data format.

Extended Bus Interface

The Extended Bus (EB) interface is an asynchronous bus designed for the host CPU to access the internal BCM53262M register space indirectly through a register map. The EB interface operates based on 100 MHz internal system clock. The EB interface consists of: Address bus (EB_ADDR[3:0]), Data bus (EB_DATA[15:0]), Chip Select (EB_CS), Output Enable (EB_OE), Write Enable (EB_WE). The data bus can be configured as 8-bit or 16-bit modes and is selected by strap pin EB_16BITMODE. In 8-bit mode, address is byte-aligned. In 16-bit mode, address is 2-byte aligned.

Table 37: Interface Signals

Signal Name	*Direction*	*Description*
EB_ADDR[3:0]	I	Address of register to be accessed in the register map.
EB_DATA[15:0]	I/O	Data value to be written into the register specified by EB_ADDR for a write operation or data read from the register specified by EB_ADDR for a read operation.
$\overline{\text{EB_CS}}$	I	**Chip Select.** Selects the EB Bus operation.
$\overline{\text{EB_OE}}$	I	**Output Enable.** Enables the output drivers of the EB_DATA bus.
$\overline{\text{EB_WE}}$	I	**Write Enable.** Enables the register write function.
EB_16BITMODE	I	**Strap pin.** • 1 = Indicates the EB Bus operates in 16-bit mode. • 0 = Indicates the EB Bus operates in 8-bit mode.

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Register Map

All read and write accesses to the internal BCM53262M register space are conducted indirectly through a set of registers as outlined in the following maps.

Table 38: Register Map In 8-bit Mode

Address	*Bit*	*Register Name*	*Description*
0000	[7:0]	Data Byte 0	Store data read from or write to byte 0
0001	[7:0]	Data Byte 1	Store data read from or write to byte 1
0010	[7:0]	Data Byte 2	Store data read from or write to byte 2
0011	[7:0]	Data Byte 3	Store data read from or write to byte 3
0100	[7:0]	Data Byte 4	Store data read from or write to byte 4
0101	[7:0]	Data Byte 5	Store data read from or write to byte 5
0110	[7:0]	Data Byte 6	Store data read from or write to byte 6
0111	[7:0]	Data Byte 7	Store data read from or write to byte 7
1000	[7:0]	Page Address	Store BCM53262M internal register page address to be accessed
1001	[7:0]	Offset Address	Store BCM53262M internal register offset address to be accessed
1010	[7:0]	Command	• Bits[7:2]: Reserved. • Bit[1]: Write Command. When set, enable write operation. • Bit[0]: Read Command. When set, enable read operation. ***Note:*** Either bit [1] or bit [0] should be set, but not simultaneously. These bits are self-clear after the operation is completed.
1011	[7:0]	Status	• Bits[7:1]: Reserved. • Bit[0]: When set, indicating a read or write operation is still busy. This bit is self-clear after the operation is complete. ***Note:*** When accidentally accessing to the reserved addresses, this bit will always be asserted, due to no register acknowledgement.
1100	[7:0]	Byte Count	This register records the byte count that had been successfully read from or write to the accessed register. • Bit[7] = 1: 8 bytes. • Bit[6] = 1: 7 bytes. • Bit[5] = 1: 6 bytes. • Bit[4] = 1: 5 bytes. • Bit[3] = 1: 4 bytes. • Bit[2] = 1: 3 bytes. • Bit[1] = 1: 2 bytes. • Bit[0] = 1: 1 byte.
Others	[7:0]	Reserved	Unmapped area.

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Table 39: Register Map In 16-bit Mode

Address	Bit	Register Name	Description
0000	[15:0]	Data Bytes 1, 0	Store data read from or write to bytes 1 and 0
0010	[15:0]	Data Bytes 3, 2	Store data read from or write to bytes 3 and 2
0100	[15:0]	Data Bytes 5, 4	Store data read from or write to bytes 5 and 4
0110	[15:0]	Data Bytes 7, 6	Store data read from or write to bytes 7 and 6
1000	[15:0]	Page Address, Offset Address	Store BCM53262M internal register Page and Offset addresses to be accessed
1010	[15:0]	Status, Command	• Bits[15:9]: Reserved. • Bit[8]: When set, indicating a read or write operation is still busy. This bit is self-clear after the operation is complete. ***Note:*** When accidentally accessing to the reserved addresses, this bit will always be asserted, due to no register acknowledgement. • Bits[7:2]: Reserved. • Bit[1]: Write Command. When set, enable write operation. • Bit[0]: Read Command. When set, enable read operation. ***Note:*** Either bit [1] or bit [0] should be set, but not simultaneously. These bits are self-clear after the operation is completed.
1100	[15:0]	Byte Count	This register records the byte count that had been successfully read from or write to the accessed register. Bits[15:8] = Reserved Bit[7] = 1: 8 bytes. Bit[6] = 1: 7 bytes. Bit[5] = 1: 6 bytes. Bit[4] = 1: 5 bytes. Bit[3] = 1: 4 bytes. Bit[2] = 1: 3 bytes. Bit[1] = 1: 2 bytes. Bit[0] = 1: 1 byte.
Others	[15:0]	Reserved	Unmapped area.

EB Interface Read Cycle

The host CPU starts an EB read cycle by asserting an address on EB_ADDR followed by the chip select EB_CS. Read data is available on EB_DATA on the falling edge of EB_OE. The EB_OE signal must be active for at lease 4 internal system clock cycle, which is running at 100 Mhz. The cycle is terminated at the rising edges of both EB_OE and EB_CS.

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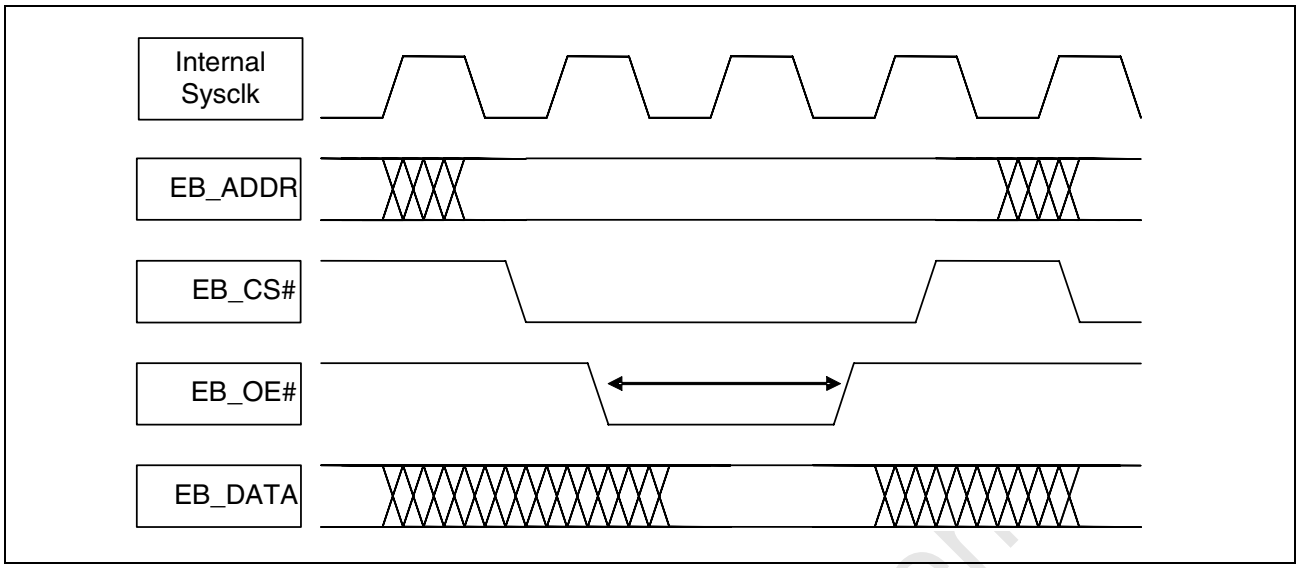

Figure 25: ED Read Cycle

EB Interface Write Cycle

The host CPU starts an EB write cycle by asserting an address on EB_ADDR followed by the chip select EB_CS. Ensure that write data is available on EB_DATA before the falling edge of EB_WE. The EB_WE signal must be active for at lease 4 internal system clock cycle, which is running at 100 MHz. The cycle is terminated at the rising edges of both EB_WE and EB_CS.

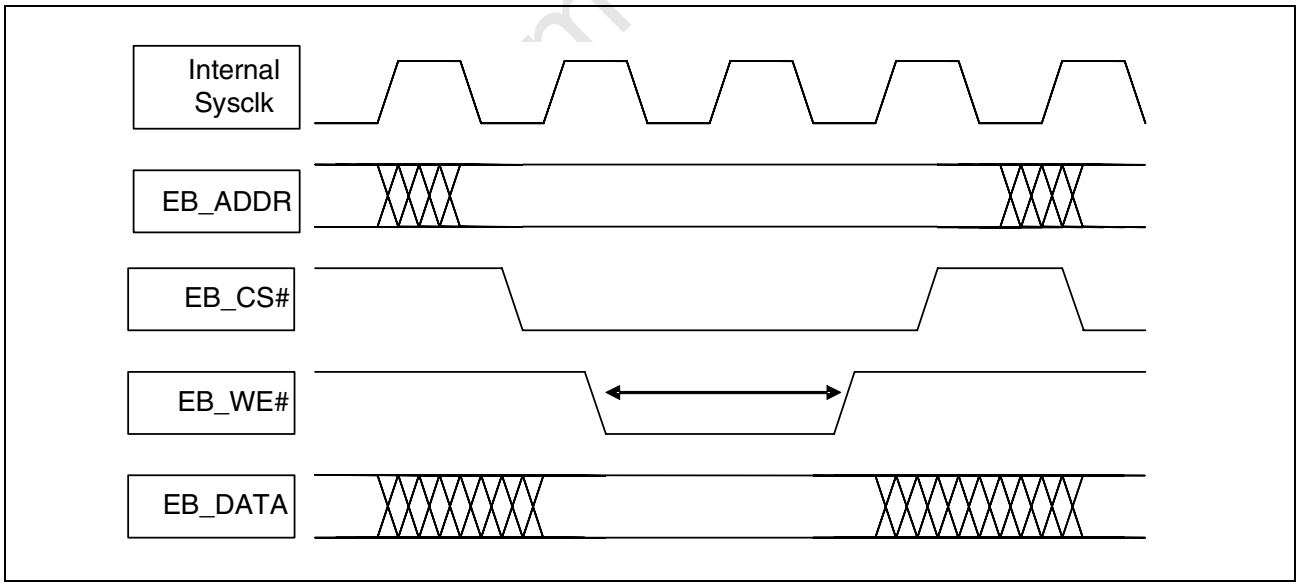

Figure 26: ED Write Cycle

Programming Sequence

Use the following sequence to read from or write to any internal BCM53262M register.

Read Operation

- Program Page Address Register and Offset Address Register to point to BCM53262M internal register
- Set bit[0] of Command Register to 1 to issue a read operation
- Polling Status Register until the Busy bit is 0, which indicates the operation is complete
- Read Byte Count Information Register to learn how many bytes are valid for this read operation (optional)
- Read Data Byte 0 ~ Data Byte 7 Register for the read data.

Write Operation

- Program Page Address Register and Offset Address Register to point to BCM53262M internal register
- Program Data Byte 0 ~ Data Byte 7 Register with the write data.
- Set bit[1] of Command Register to 1 to issue a write operation
- Polling Status Register until the Busy bit is 0, which indicates the operation is complete
- Read Byte Count Information Register to learn how many bytes are successfully written for this operation (optional)

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MDC/MDIO Interface

MDC/MDIO Master Interface

Each of the external transceivers can be daisy-chained to the MDC and MDIO pins of the BCM53262M. The BCM53262M uses the MDC/MDIO interface to read/write the register information of the external transceivers.

The BCM53262M initiates a master MII access cycle when:

- Automatically polling the external PHY MII registers, unless the PHY_POLL_DIS strap pin is deliberately pulled high
- Any SCK activity is detected on the SPI interface to access the external PHY MII registers

Each external transceiver is assigned a unique hardware PHY address for MII management. The IMP port hardware PHY address is 18h. Gigabit ports G0, G1, G2 and G3 have hardware PHY addresses 19h, ..., 1Ch respectively.

Each time a master MII write or read operation is executed, the transceiver compares the PHY address with its own PHY address definition. The operation is executed only when the addresses match.

Note: When a master MII access cycle is executed, the BCM53262M sources a 2.5 MHz clock on the MDC pin.

MDC/MDIO Slave Interface

The BCM53262M executes a MII slave access cycle, when the CPU initiates a read/write access to either the switch registers or the internal transceiver MII registers.

Switch Register Access Through Pseudo-PHY Interface

The switch registers are organized into pages, each of which contains a defined register set. To access any switch register, both the page number and register address must be specified.

The CPU can access the BCM53262M switch registers through the MDC and MDIO interface. The switch registers are accessed through a pseudo-PHY (PHY Address = 01E), which is not used by any of the physical transceivers on the BCM53262M MDC/MDIO path. Page number, register address and the read/write data are encapsulated in the MII management frame format.

The algorithm for read access to the switch registers is shown in Figure 35 on page 125. The algorithm for write access is shown in Figure 36 on page 126. The pseudo-PHY MDC/MDIO interface has an address space of 32, as shown in Figure 28 on page 122. The first 16 registers are reserved by IEEE. Only addresses 16-31 can be used to access the switch registers. The switch register page number, register address, and access type are determined by registers 16 and 17. The data read from or written to a switch register is stored in registers 24 to 27 (64 bits total).

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MDC/MDIO Slave Interface Register Programming

Each internal transceiver in the BCM53262M is assigned a unique hardware PHY address.

Transceiver 24 has address 00000. Transceivers 25-47 have addresses 1 through 17h, respectively.

Each internal PHY checks that the PHY address of the initiated command matches that of its own before executing the command.

The BCM53262M fully complies with the IEEE 802.3u Media Independent Interface (MII) specification. The MII management interface registers of each internal transceiver are serially written-to and read-from using a common set of MDIO and MDC pins. A single clock must be provided to the BCM53262M at a rate of 0-12.5 MHz through the MDC pin.

The serial data is communicated on the MDIO pin. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock. MDC may be stopped between frames provided no timing requirements are violated. MDC must be active during each valid bit of every frame, including preamble, instruction, address, data, and at least one idle bit. Every MII read or write instruction frame contains the fields shown in Table 40.

Table 40: MII Management Frame Format

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*DATA*	*IDle*	*Direction*
Read	1 ... 1	01	10	AAAAA	RRRRR	ZZ	Z ... Z	Z	Driven to BCM53262M
						Z0	D ... D	Z	Driven by BCM53262M
Write	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Z	Driven to BCM53262M

Preamble (PRE)

32 consecutive 1 bits must be sent through the MDIO pin to the BCM53262M to signal the beginning of an MII instruction. Fewer than 32 1 bits will cause the remainder of the instruction to be ignored. In preamble suppression mode, only two preamble bits are required between frames.

Start of Frame (ST)

A 01 pattern indicates that the start of the instruction follows.

Operation Code (OP)

A read instruction is indicated by 10, while a WRITE instruction is indicated by 01.

PHY Address (PHYAD)

A 5-bit PHY address follows next, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.

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Register Address (REGAD)

A 5-bit Register Address follows, with the MSB transmitted first. The register map of the BCM53262M, containing register addresses and bit definitions, are provided on the following pages.

Turnaround (TA)

The next two bit times are used to avoid contention on the MDIO pin when a read operation is performed. For a Write operation, 10 must be sent to the BCM53262M chip during these two bit times. For a read operation, the MDIO pin must be placed into high-impedance during these two bit times. The chip drives the MDIO pin to 0 during the second bit time.

Data

The last 16 bits of the frame are the actual data bits. For a write operation, these bits are sent to the BCM53262M, whereas, for a read operation, these bits are driven by the BCM53262M. In either case, the MSB is transmitted first. When writing to the BCM53262M, the data field bits must be stable during the rising edge of MDC. When reading from the BCM53262M, the data field bits are valid after the rising-edge of MDC until the next rising-edge of MDC.

Idle

A high impedance state of the MDIO line. All tri-state drivers are disabled and an external pull-up resistor pulls the MDIO line to logic 1. At least one or more clocked idle states are required between frames.

Following are two examples of MII write and read instructions:

To put a transceiver with PHY address 00001 into Loopback mode, the following MII write instruction must be issued:

- 1111 1111 1111 1111 1111 1111 1111 1111 0101 00001 00000 10 0100 0000 0000 0000

To determine if a PHY is in the link pass state, the following MII read instruction must be issued:

- 1111 1111 1111 1111 1111 1111 1111 1111 0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ

For the MII read operation, the BCM53262M will drive the MDIO line during the second half of the TA field and the Data field (the last 17 bit times).

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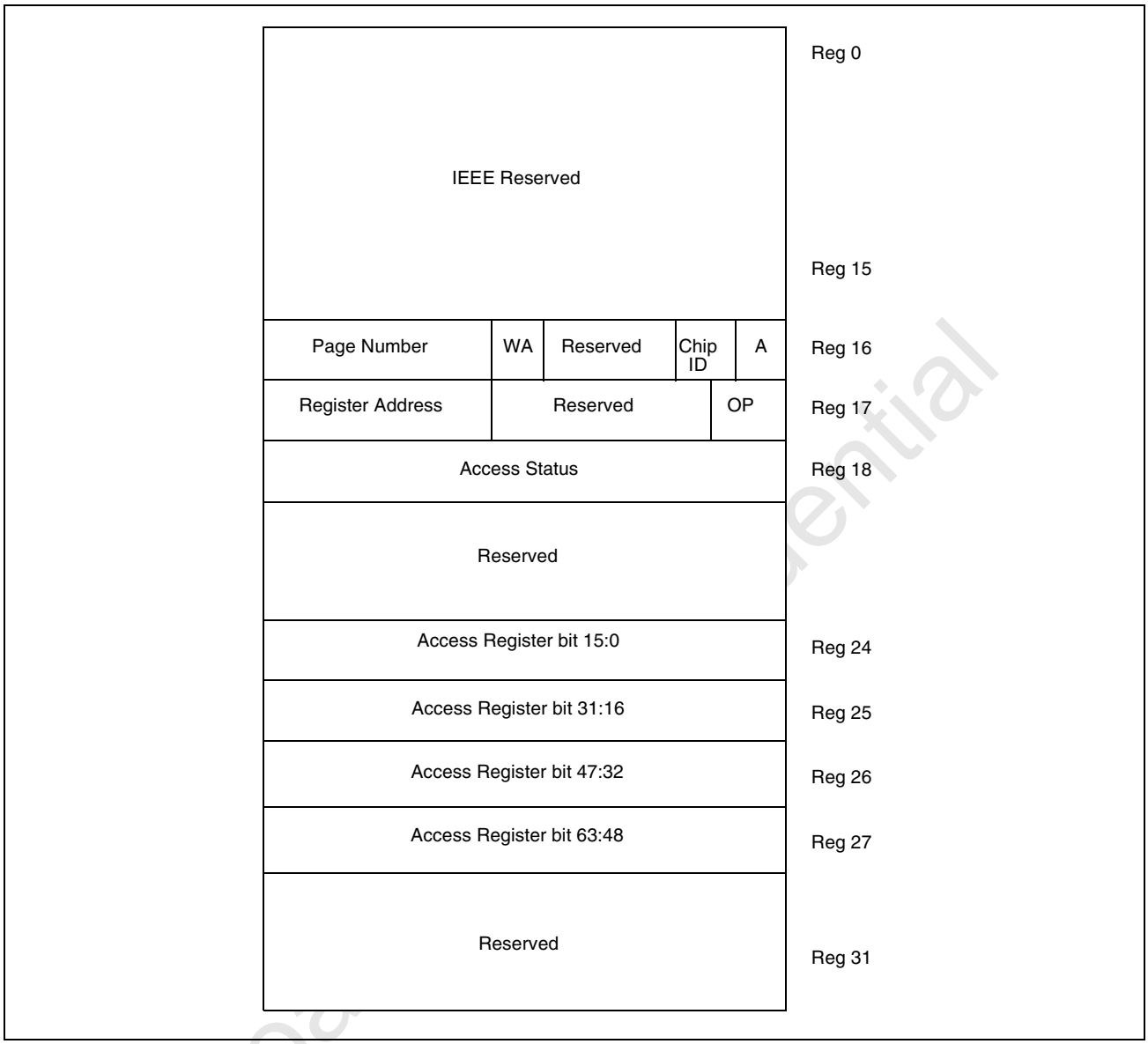

Figure 27: Pseudo PHY MII Register Definitions

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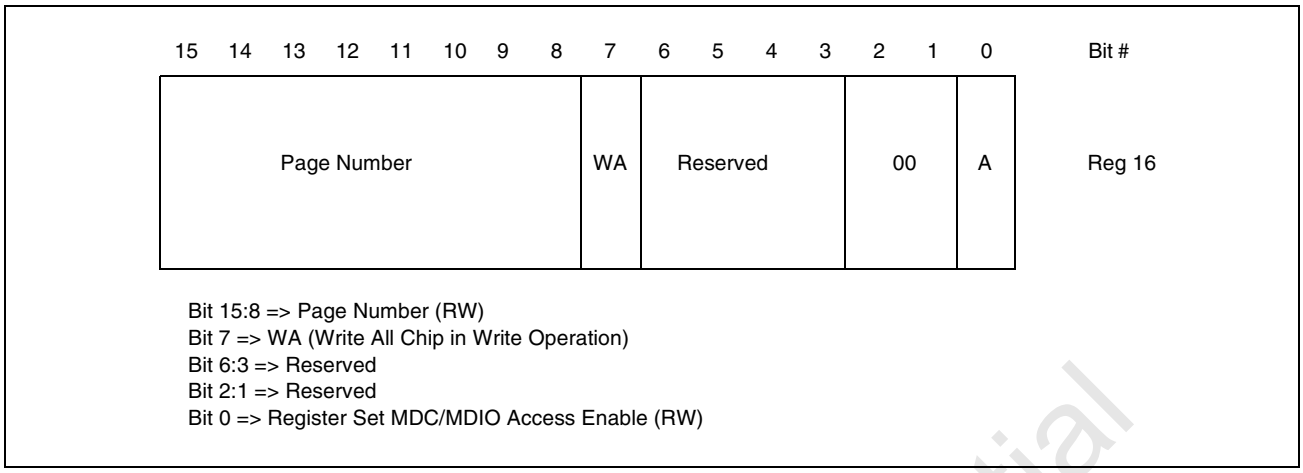

Figure 28: Pseudo PHY MII Register 16: Register Set Access Control Bit Definition

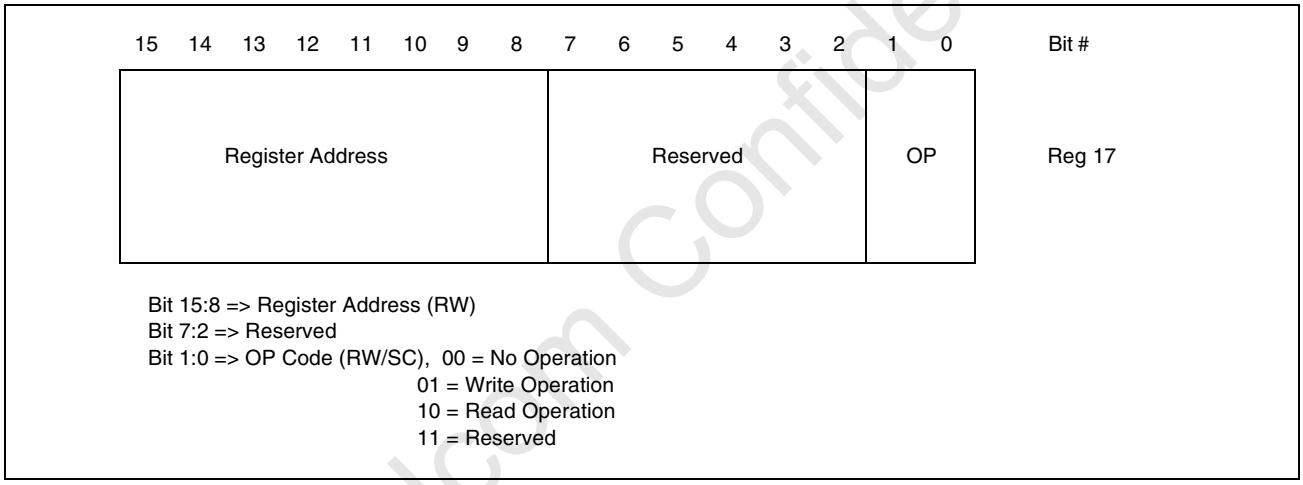

Figure 29: Pseudo PHY MII Register 17: Register Set Read/Write Control Bit Definition

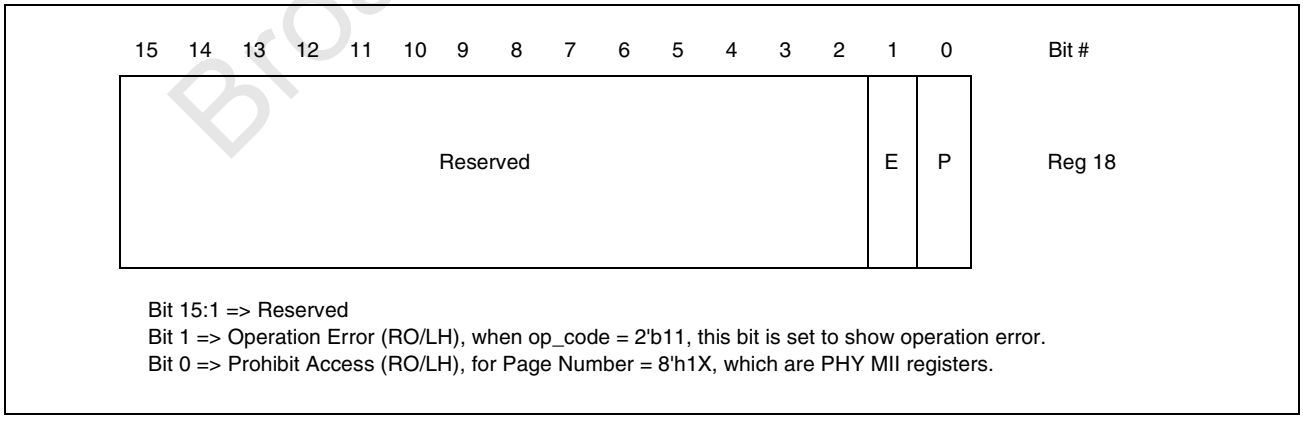

Figure 30: Pseudo PHY MII Register 18: Register Access Status Bit Definition

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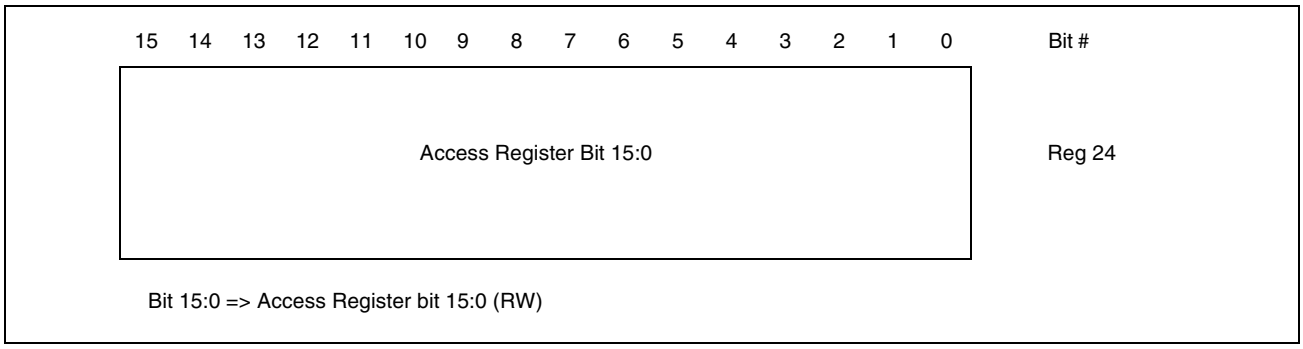

Figure 31: Pseudo PHY MII Register 24: Access Register Bit Definition

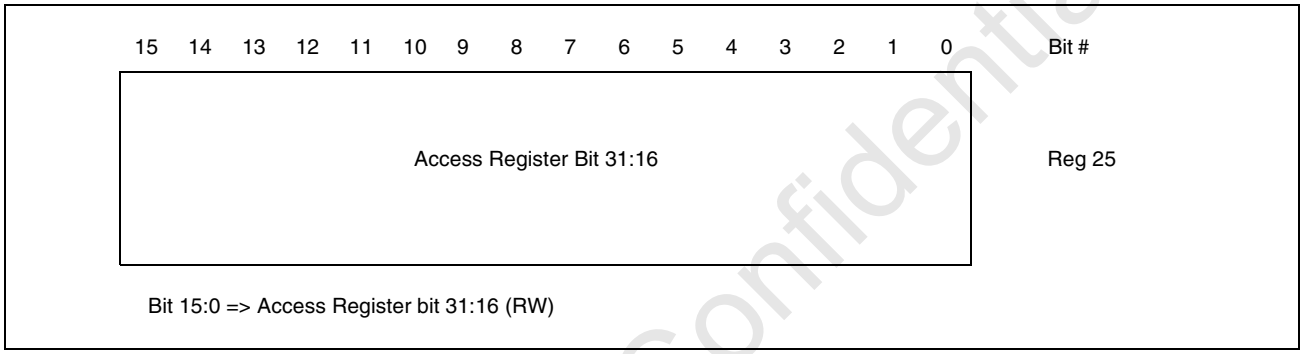

Figure 32: Pseudo PHY MII Register 25: Access Register Bit Definition

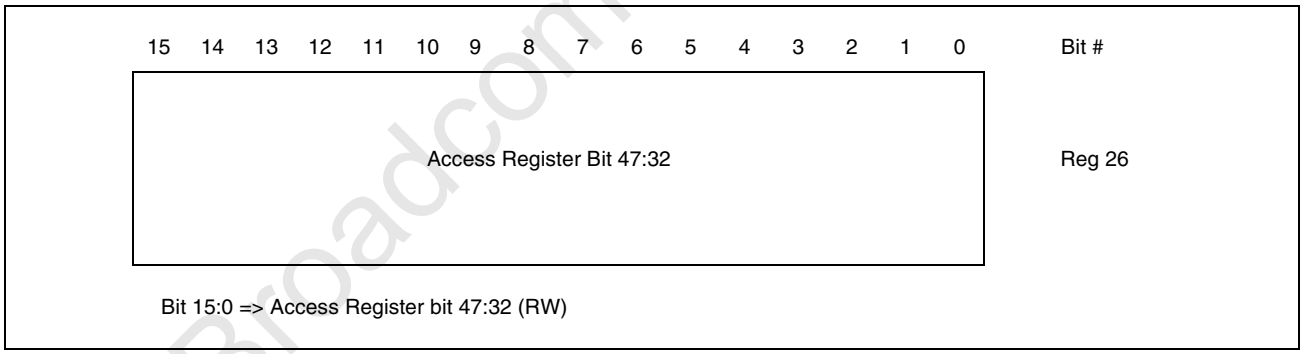

Figure 33: Pseudo PHY MII Register 26: Access Register Bit Definition

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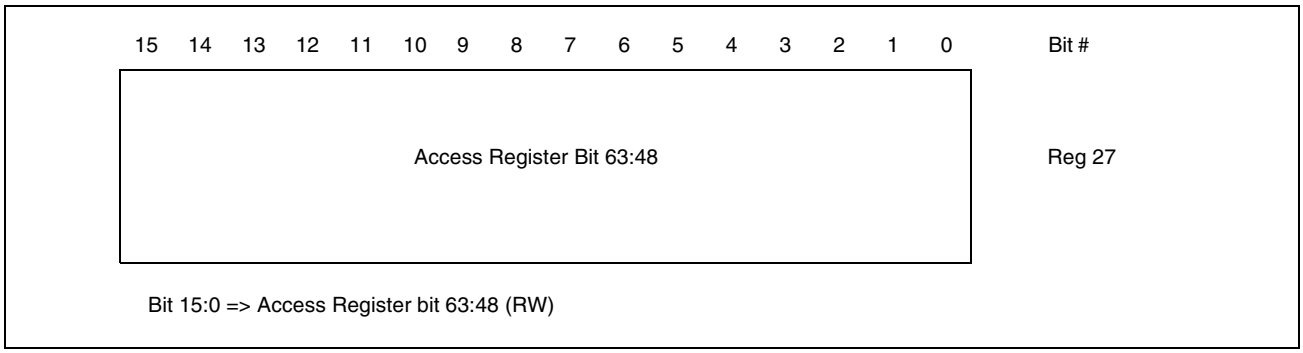

Figure 34: Pseudo PHY MII Register 27: Access Register Bit Definition

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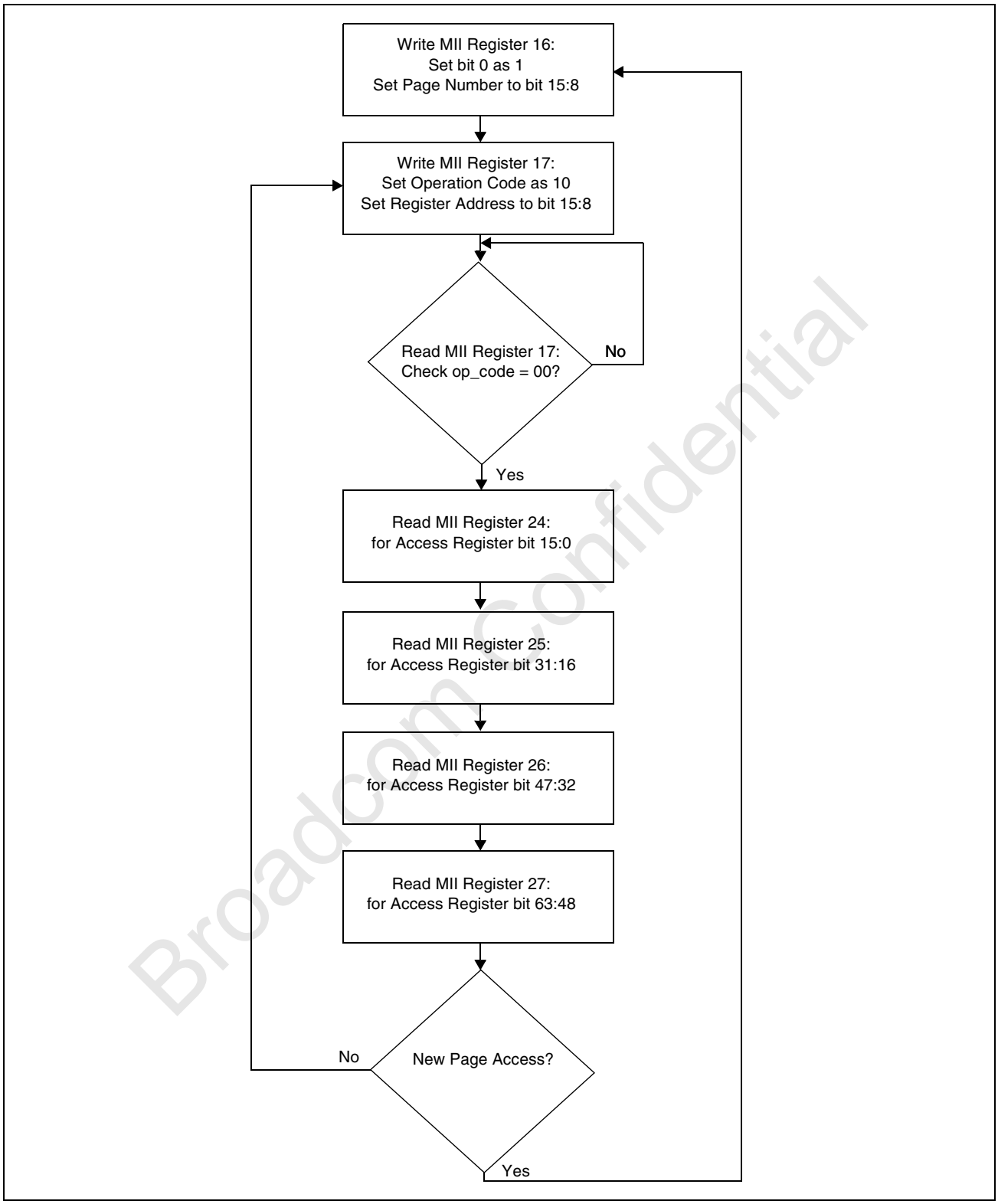

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Figure 35: Read Access to the Register Set Via the Pseudo PHY (Phyad = 11110) MDC/MDIO Path

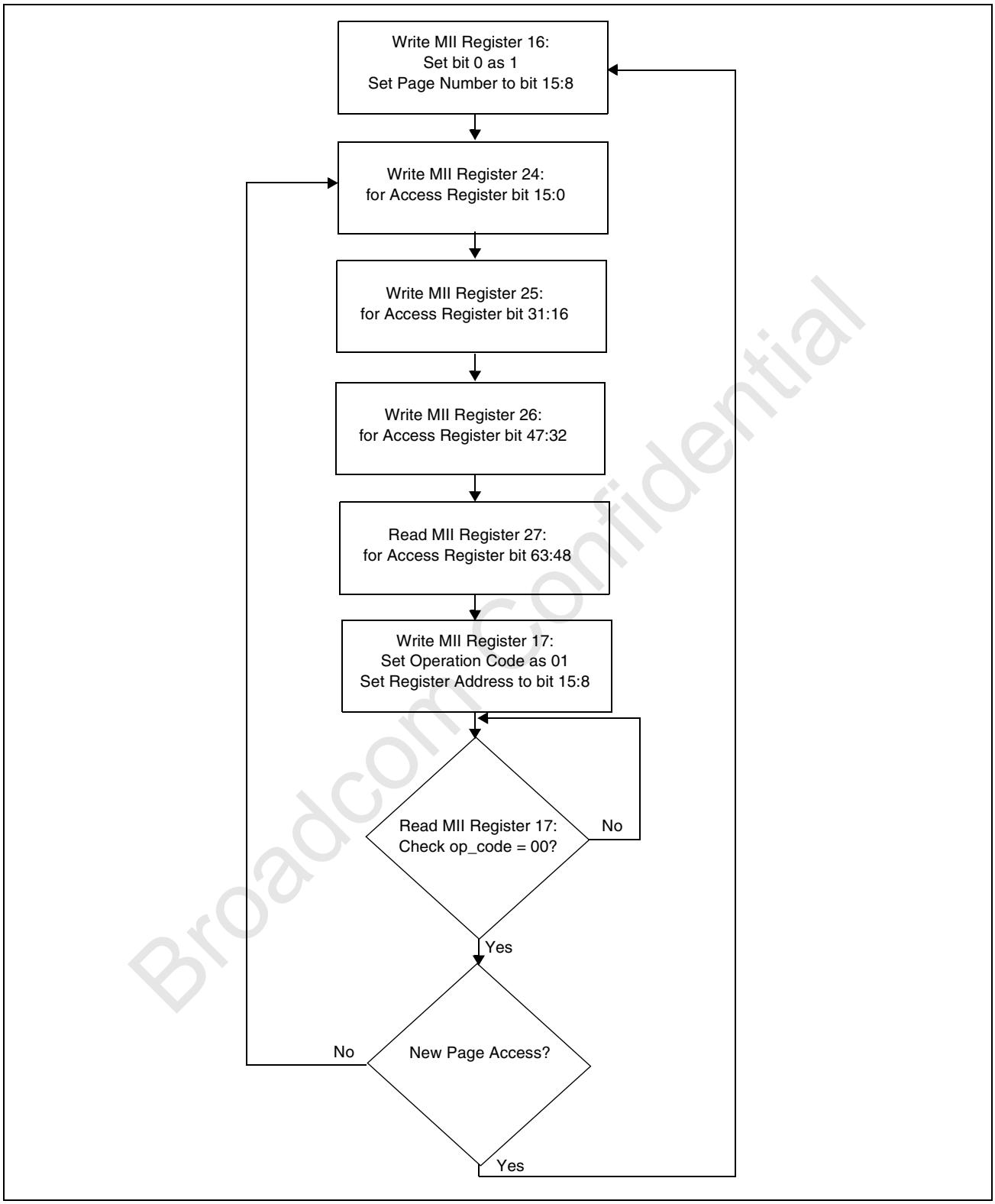

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Figure 36: Write Access to the Register Set Via the Pseudo PHY (Phyad = 11110) MDC/MDIO Path

LED Interfaces

The BCM53262M provides visibility for up to four status indications per port. Both serial and matrix interfaces are supplied to drive the status to the LEDs. The matrix interface provides a cost effective solution for implementing LED in a high port count system. Both interfaces provide per port of link status, port speed, duplex mode, combined transmit and receive activity, and collision. During power-on and reset, the serial interface shifts a continuous low value for 1.34s.

Serial LED Interface

A two-pin serial interface, LEDDATA and LEDCLK, provides data and clock to enable external shift registers to capture the LED status indications from the BCM53262M for each port. The status encapsulated within the shift sequence is configured by the LEDMODE configuration signals. The configuration signals select both the number of status bits per port and the status type of each bit. Refer to Table 42 on page 129 for LED mode shift sequence.

The LEDCLK is generated by dividing the 25 MHz input clock by 8, providing a 320 ns clock period. The LEDDATA outputs are generated on the falling edge of the LEDCLK, and have adequate setup and hold time to be clocked externally on the rising edge of LEDCLK.

The shift sequence is per port status words. Each port status word contains up to 4-bit for the designated LED status type as mentioned above. Port G3 status word is shifted out first, followed by Port G2, ..., Port IMP and Port 47, ..., and Port 24 status words, where Port IMP is configured as a regular network port with the PHY connected. When the Port IMP is configured as a management port connected to the host CPU, there is no LED status to be reported. The shift sequence is repeated every 42 ms.

See Figure 37 for an illustration of the serial LED shift sequence, and Table 41: “LED Status Types,” on page 128 for LED status Type.

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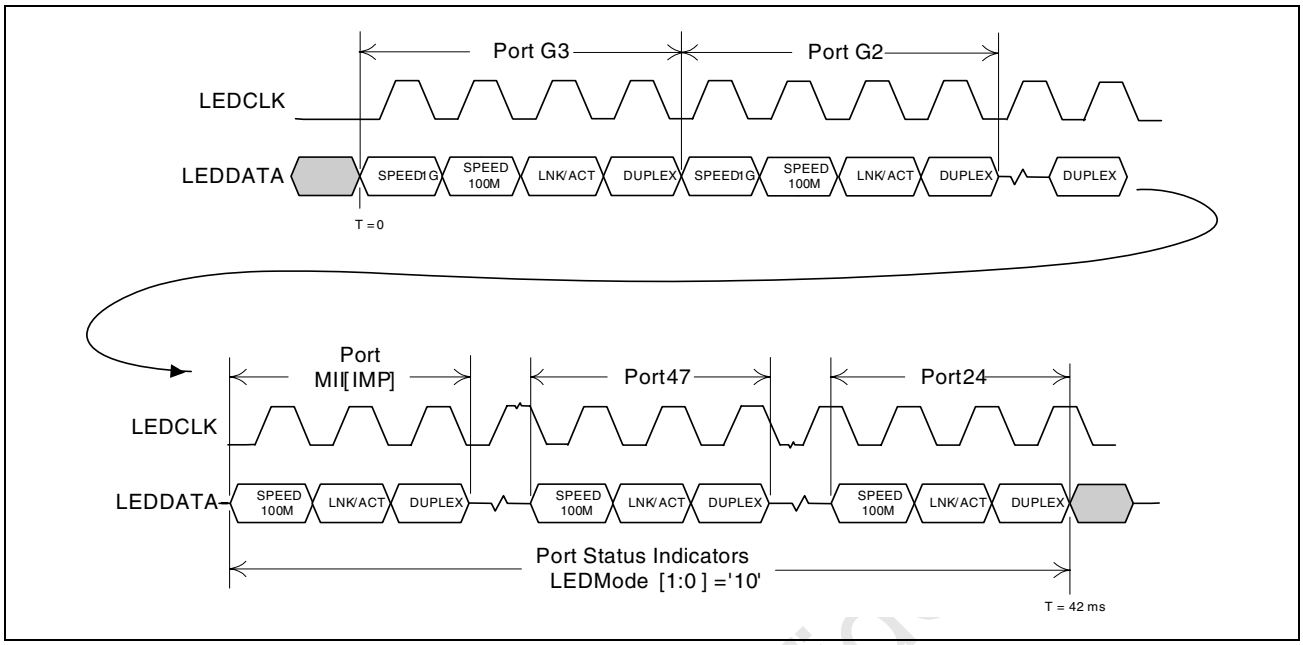

Figure 37: Serial LED Shift Sequence LEDMODE[1:0] = '10'

Note: LED status is only reported for the MII port when that port is connected to the external PHY with polling enabled.

Table 41: LED Status Types

Name	*Description*
LNK	**Link status indicator.** Low when link is established.High when link is off.
DUPLEX	**Duplex mode indicator.** High for half-duplex or no link, and low for full-duplex and link.
LNK/ACT	**Link and Activity status indicator.** Low when link is established. Blinking at 12 Hz when link is up and port is transmitting and receiving.
SPEED100M	**Speed indicator and Activity.** High for 10 Mbps or no link. Low for 100 Mbps and link
SPEED1G	**Speed indicator.** Low for link at 1000 Mbps. High for all other conditions.
DUPLEX/COL	**Duplex and Collision indicator.** Blinking when collision is detected. Low for full-duplex and link.
SPEED1G/ACT	**Speed 1G and Activity Indicator.** Low when linked at 1000 Mbps. Blinking at 12 Hz when link is up and port is transmitting and receiving.
SPEED100M/ACT	**Speed 100M and Activity Indicator.** Low when linked at 100 Mbps. Blinking at 12 Hz when link is up and port is transmitting and receiving.
SPEED10M/ACT	**Speed 10M and Activity Indicator.** Low when linked at 10 Mbps. Blinking at 12 Hz when link is up and port is transmitting and receiving.
SPEED10M/ SPEED100M/ACT	**Speed 10M, Speed 100M and Activity Indicator.** Low when linked at 10 Mbps/100 Mbps. Blinking at 12 Hz when link is up and port is transmitting and receiving.

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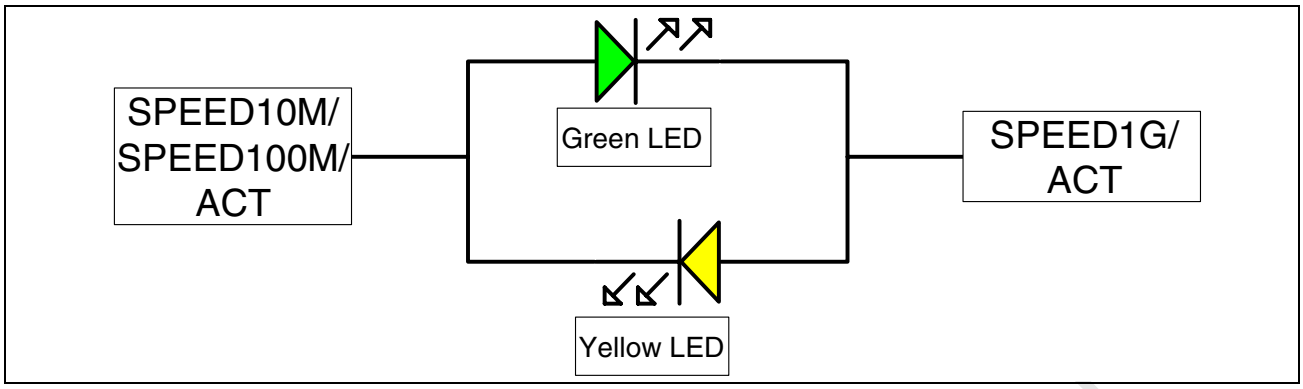

Figure 38: Bicolor SPEED/ACT LED Scheme

Table 42: LED Mode Shift Sequence

LED Mode [1:0]	*Port 24 Status*	*Port 25 Status*	*Port 26-46*	*Port 47 Status*	*Port MII (IMP) Status*[a]	*Port G0 Status*	*Port G1-G2*	*Port G3 Status*
00	SPEED100M LNK/ACT	SPEED100M LNK/ACT	....	SPEED100M LNK/ACT	SPEED100M LNK/ACT	SPEED1G SPEED100M LNK/ACT	....	SPEED1G SPEED100M LNK/ACT
01	SPEED100M/ ACT SPEED10M/ ACT DUPLEX/COL	SPEED100M/ ACT SPEED10M/ ACT DUPLEX/COL	....	SPEED100M/ ACT SPEED10M/ ACT DUPLEX/COL	SPEED100M/ ACT SPEED10M/ ACT DUPLEX/COL	SPEED1G/ACT SPEED10M/ SPEED100M/ ACT DUPLEX/COL	....	SPEED1G/ACT SPEED10M/ SPEED100M/ ACT DUPLEX/COL
10	SPEED100M LNK/ACT DUPLEX	SPEED100M LNK/ACT DUPLEX	....	SPEED100M LNK/ACT DUPLEX	SPEED100M LNK/ACT DUPLEX	SPEED1G SPEED100M LNK/ACT DUPLEX	....	SPEED1G SPEED100M LNK/ACT DUPLEX
11	SPEED100M/ ACT SPEED10M/ ACT DUPLEX	SPEED100M/ ACT SPEED10M/ ACT DUPLEX	....	SPEED100M/ ACT SPEED10M/ ACT DUPLEX	SPEED100M/ ACT SPEED10M/ ACT DUPLEX	SPEED1G/ACT SPEED100M/ ACT SPEED10M/ ACT DUPLEX	....	SPEED1G/ACT SPEED100M/ ACT SPEED10M/ ACT DUPLEX

a. Port MII(IMP) Status is the status of external PHY when the port is configured as a regular network port.

Programming LED Registers

The BCM53262M implements a versatile LED scheme. To obtain the shift sequence as outlined in Table 42: “LED Mode Shift Sequence,” on page 129, program the LED register using Table 43.

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Table 43: BCM53262M ***Legacy LED Shift Sequence Register Programming***

LED_Mode[2:0]	***00***	***01***	***10***	***11***
LED Control Register	0x0083	0x0083	0x0083	0x0083
LED Function 0 Control Register	0x0120	0x0C40	0x0124	0x0C04
LED Function 1 Control Register	0x0320	0x3040	0x0324	0x2C04
LED Function Map Register	0x001E_0000_0000_0000			
LED Enable Map Register	0x001E_FFFF_FF00_0000			
LED Mode Map 0 Register	0x001F_FFFF_FFFF_FFFF			
LED Mode Map 1 Register	0x001F_FFFF_FFFF_FFFF			

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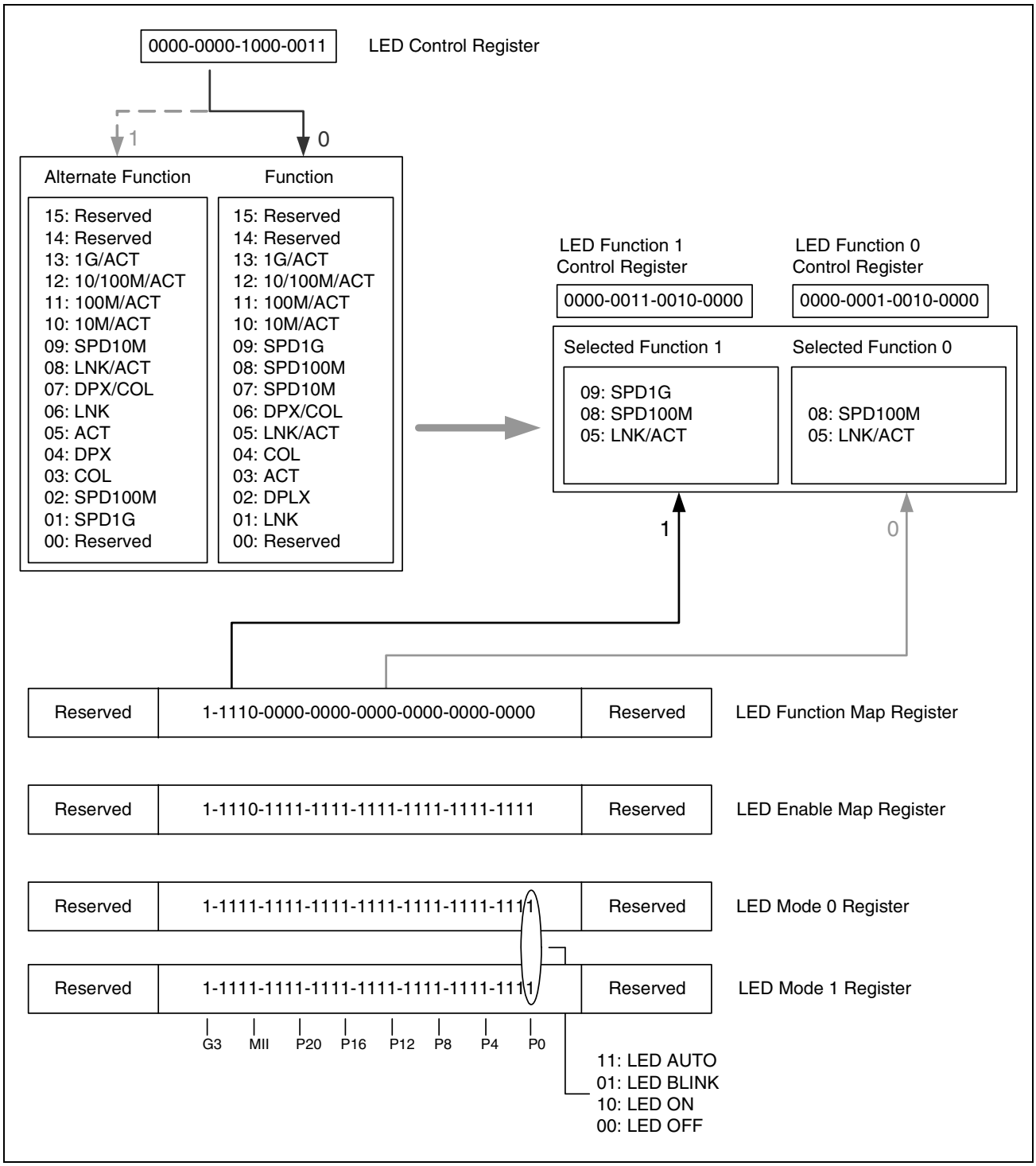

Figure 39: BCM53262 LED Register Structure Diagram

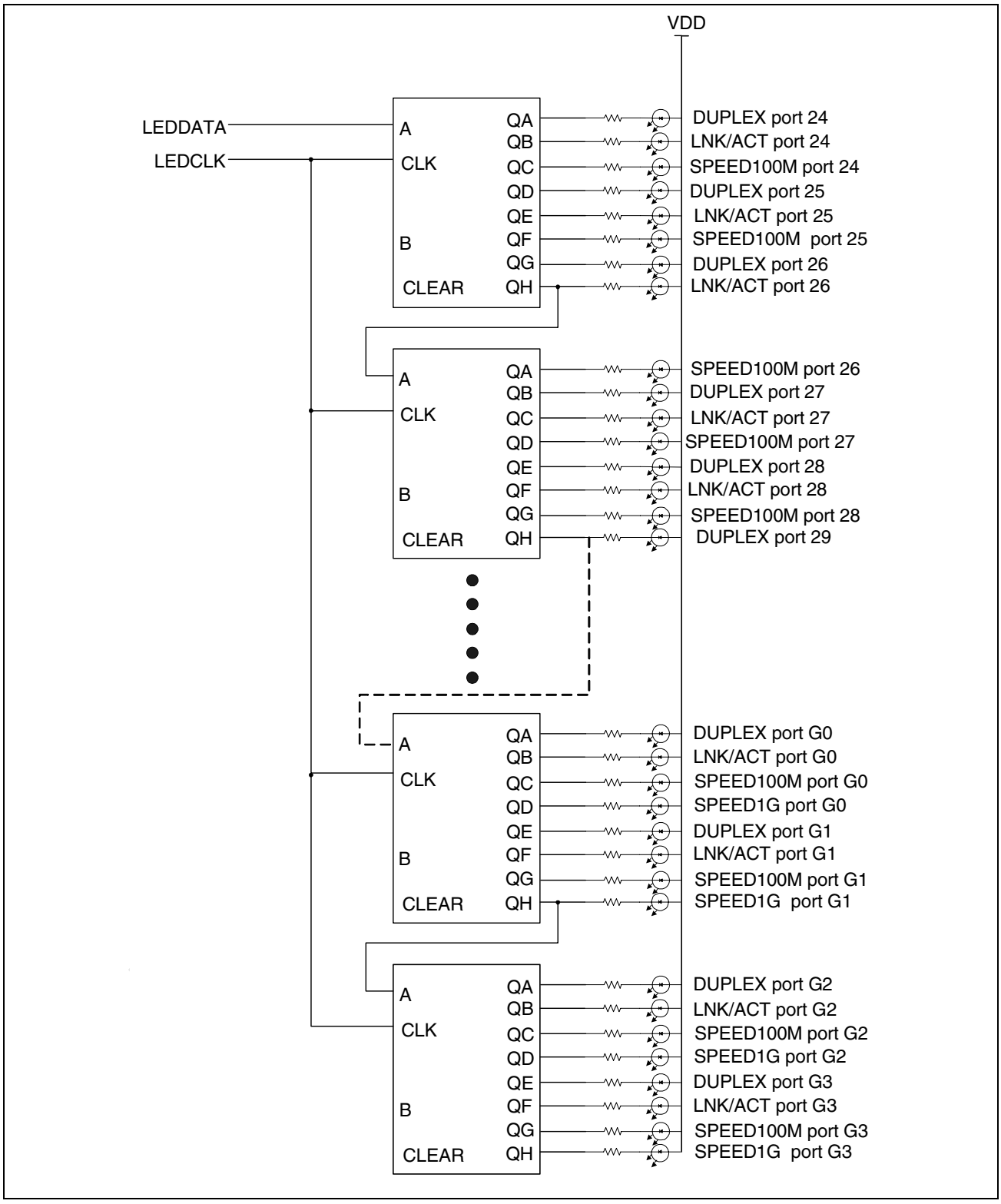

Figure 40: Partial Example External Circuit for Serial LED Mode (LEDMODE[1:0]='00')

Matrix LED Interface

A three-pin matrix interface, MLEDCOL, MLEDROW and MLEDCLK enable external shift registers to form a 32 by 8 matrix to capture the LED status indications for each port of the BCM53262M. The status encapsulated within the shift sequence is configured by the LEDMODE configuration signals. The configuration signals select both the number of status bits per port and the status type of each bit. Refer to Table 42 on page 129 for LED mode shift sequence.

The MLEDCLK is generated by dividing the 25 MHz input clock by 8, providing a 320 ns clock period. The MLEDCOL and MLEDROW outputs are generated on the falling edge of the MLEDCLK, and have adequate setup and hold time to be clocked externally on the rising edge of MLEDCLK. Refer to Figure 41 for an illustration of a typical Matrix LED circuit for a column.

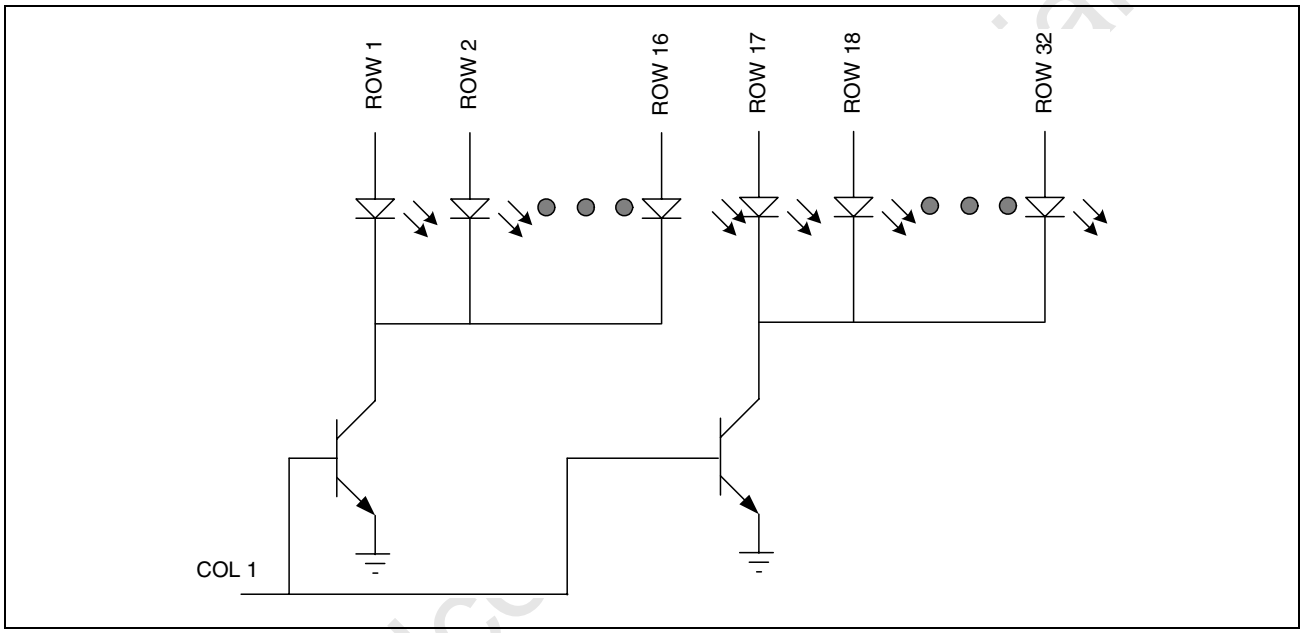

Figure 41: Typical Matrix LED Circuit

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Figure 42 shows the decoding of the column and row for the matrix shift sequences.

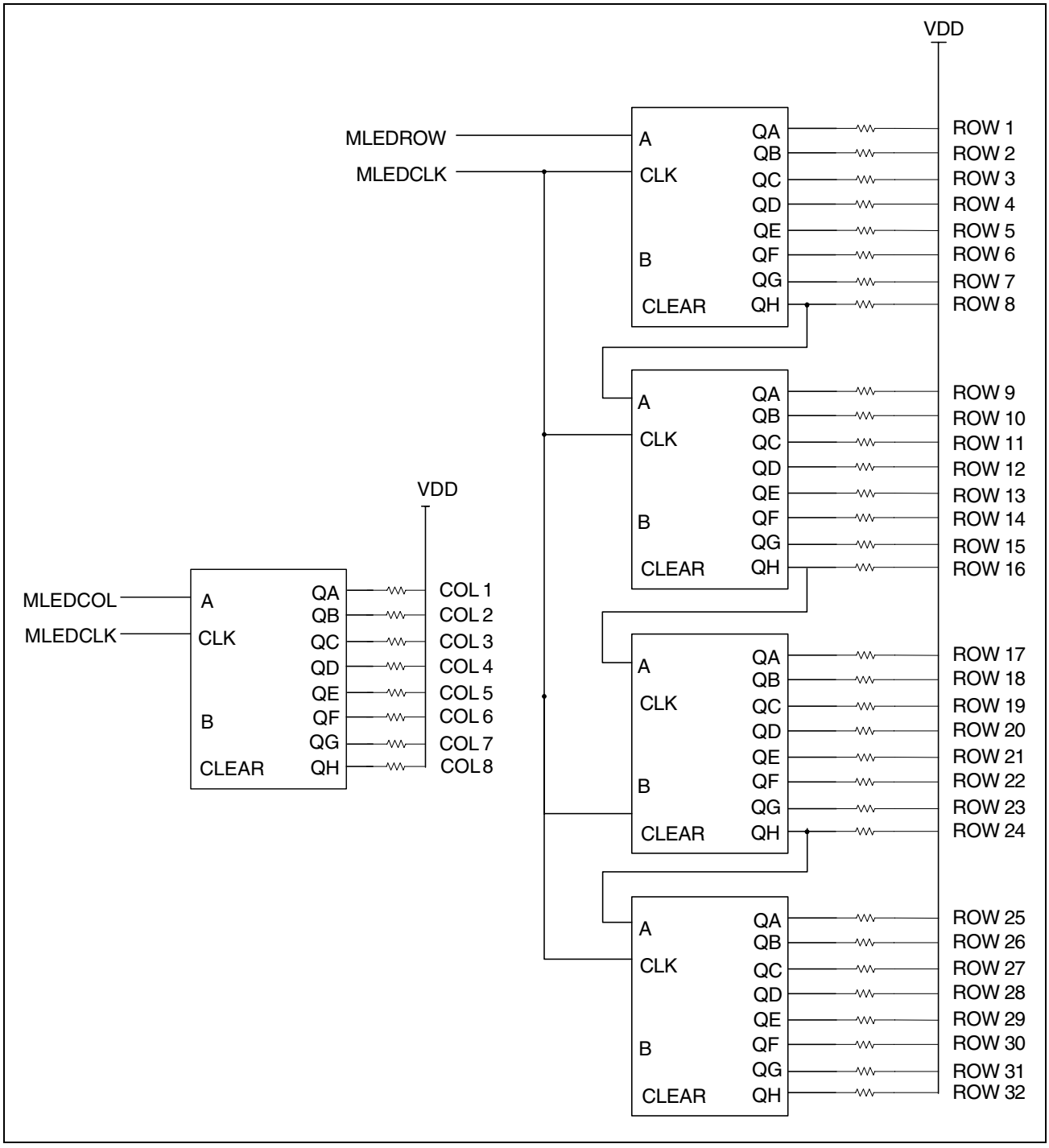

Figure 42: Matrix Row And Column Shift Sequences

Table 44 shows the relative location of per port Matrix LED status. Each port has up to 4 status words. Each status word is designated as Px-1, Px-2, Px-3 and Px-4, where x is the port number.

Table 44: Matrix Port LED Status And Sequence Map

Row	*Col 1*	*Col 2*	*Col 3*	*Col 4*	*Col 5*	*Col 6*	*Col 7*	*Col 8*
Row1	–	–	–	–	–	–	–	–
Row2	–	–	–	–	–	–	–	–
Row3	–	–	–	–	–	–	–	–
Row4	–	–	–	–	–	–	–	–
Row5	–	–	–	–	–	–	–	–
Row6	–	–	–	–	–	–	–	–
Row7	–	–	–	–	–	–	–	–
Row8	–	–	–	–	–	–	–	–
Row9	–	–	–	–	–	–	–	–
Row10	–	–	–	–	–	–	–	–
Row11	–	–	–	–	–	–	–	–
Row12	–	–	–	–	–	–	–	–
Row13	P24-4	P24-3	P24-2	P24-1	P25-4	P25-3	P25-2	P25-1
Row14	P26-4	P26-3	P26-2	P26-1	P27-4	P27-3	P27-2	P27-1
Row15	P28-4	P28-3	P28-2	P28-1	P29-4	P29-3	P29-2	P29-1
Row16	P30-4	P30-3	P30-2	P30-1	P31-4	P31-3	P31-2	P31-1
Row17	P32-4	P32-3	P32-2	P32-1	P33-4	P33-3	P33-2	P33-1
Row18	P34-4	P34-3	P34-2	P34-1	P35-4	P35-3	P35-2	P35-1
Row19	P36-4	P36-3	P36-2	P36-1	P37-4	P37-3	P37-2	P37-1
Row20	P38-4	P38-3	P38-2	P38-1	P39-4	P39-3	P39-2	P39-1
Row21	P40-4	P40-3	P40-2	P40-1	P41-4	P41-3	P41-2	P41-1
Row22	P42-4	P42-3	P42-2	P42-1	P43-4	P43-3	P43-2	P43-1
Row23	P44-4	P44-3	P44-2	P44-1	P45-4	P45-3	P45-2	P45-1
Row24	P46-4	P46-3	P46-2	P46-1	P47-4	P47-3	P47-2	P47-1
Row25	P48-4	P48-3	P48-2	P48-1	P49-4	P49-3	P49-2	P49-1
Row26	P50-4	P50-3	P50-2	P50-1	P51-4	P51-3	P51-2	P51-1
Row27	P52-4	P52-3	P52-2	P52-1	-	-	-	-
Row28	–	–	–	–	–	–	–	–
Row29	–	–	–	–	–	–	–	–
Row30	–	–	–	–	–	–	–	–
Row31	–	–	–	–	–	–	–	–
Row32	–	–	–	–	–	–	–	–

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Table 45 and Table 46 show the per port Matrix LED Mode Shift Sequence.

Table 45: Matrix LED Mode Shift Sequence For 10/100 Ports

LED Mode[1:0]	*Port x–1 Status*	*Port x–2 Status*	*Port x–3 Status*	*Port x–4 Status*
00	SPEED100M	LNK/ACT	Null	Null
01	SPEED100M/ACT	SPEED10M/ACT	DUPLEX/COL	Null
10	SPEED100M	LNK/ACT	Null	Null
11	SPEED100M/ACT	SPEED10M/ACT	DUPLEX	Null

Table 46: Matrix LED Mode Shift Sequence For 10/100/1000 Ports

LED Mode[1:0]	*Port x–1 Status*	*Port x–2 Status*	*Port x–3 Status*	*Port x–4 Status*
00	SPEED1G	SPEED100M	LNK/ACT	Null
01	SPEED1G/ACT	SPEED10M/ SPEED100M/ACT	DUPLEX/COL	Null
10	SPEED1G	SPEED100M	LNK/ACT	Null
11	SPEED1G/ACT	SPEED100M/ACT	SPEED10M/ACT	DUPLEX

JTAG Interface

A standard JTAG interface is provided for boundary scan operations. This interface uses the standard five-pin interface, and supports operation at speeds up to 20 MHz.

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Section 5: BCM53262M Hardware Signal Definitions

Table 47 lists the conventions are used to identify the I/O types in Table 48.

Table 47: I/O Signal Type Definitions

Type	*Description*	*Type*	*Description*
I	Input	O	Output
I/O	Bi-directional	O_{OD}	Open drain output
I_{PD}	Input with internal pull-down	O_{ODPM}	Open drain power management output
I_{PU}	Input with internal pull-up	O_{3S}	Tristated signal
I_S	Input with Schmidt Trigger	B	Bias
GND	Ground	A	Analog
PWR	Power supply	$\overline{\text{OVERLINE}}$	Active low signal

Pin number in *Italic* font indicates pin is shared with multiple functions.

Configuration of the BCM53262M takes place during reset by loading device control values from hardware strapping pins. Some of the strapping pin are I/O pins and have secondary function during normal device operation. They should be configured with external pull-up or pull-down resistors. The strapping value is loaded during the reset sequence and the I/O pin returns to output operation after the completion of reset. Installing a pull-up or pull-down resistor to these pins other than the intended default value can have adverse affect on the function of the device.

Table 48: Hardware Signal Descriptions

Signal Name	*Ball #*	*Type*	*Drive (mA)*	*Description*
Media Connections				

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	*Ball #*	*Type*	*Drive (mA)*	*Description*
RDN_24/RDP_24	AF6/AE6	I/O_A	–	**Receive Pair.** Differential data from the media is received on the RDN/RDP signal pair.
RDN_25/RDP_25	AC7/AC8			
RDN_26/RDP_26	AB10/AB9			
RDN_27/RDP_27	AE9/AE10			
RDN_28/RDP_28	AF10/AF9			
RDN_29/RDP_29	AF11/AF12			
RDN_30/RDP_30	AB13/AB12			
RDN_31/RDP_31	AF13/AF14			
RDN_32/RDP_32	AF16/AF15			
RDN_33/RDP_33	AF17/AF18			
RDN_34/RDP_34	AE18/AE17			
RDN_35/RDP_35	AF19/AF20			
RDN_36/RDP_36	AD20/AD19			
RDN_37/RDP_37	AE21/AE22			
RDN_38/RDP_38	AB19/AB18			
RDN_39/RDP_39	AD21/AD22			

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	*Ball #*	*Type*	*Drive (mA)*	*Description*
RDN_40/RDP_40	AC23/AD23	I/O_A	–	–
RDN_41/RDP_41	AB23/AA23			
RDN_42/RDP_42	AD26/AE26			
RDN_43/RDP_43	AA24/Y24			
RDN_44/RDP_44	Y26/AA26			
RDN_45/RDP_45	W25/V25			
RDN_46/RDP_46	V26/W26			
RDN_47/RDP_47	U26/T26			
TDN_24/TDP_24	AB7/AB8	I/O_A	–	**Transmit Pair.** Differential data is transmitted to the media on the TDN/TDP signal pair.
TDN_25/TDP_25	AD8/AD7			
TDN_26/TDP_26	AF8/AF7			
TDN_27/TDP_27	AC9/AC10			
TDN_28/TDP_28	AC12/AC11			
TDN_29/TDP_29	AD11/AD12			
TDN_30/TDP_30	AE14/AE13			
TDN_31/TDP_31	AC13/AC14			
TDN_32/TDP_32	AD16/AD15			
TDN_33/TDP_33	AC15/AC16			
TDN_34/TDP_34	AC18/AC17			
TDN_35/TDP_35	AB16/AB17			
TDN_36/TDP_36	AF22/AF21			
TDN_37/TDP_37	AC19/AC20			
TDN_38/TDP_38	AF24/AF23			
TDN_39/TDP_39	AE23/AE24			
TDN_40/TDP_40	AC24/AD24			
TDN_41/TDP_41	AF26/AF25			
TDN_42/TDP_42	AB25/AC25			
TDN_43/TDP_43	AC26/AB26			
TDN_44/TDP_44	W23/Y23			
TDN_45/TDP_45	W22/V22			
TDN_46/TDP_46	U24/V24			
TDN_47/TDP_47	U25/T25			

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	Ball #	Type	Drive (mA)	Description
Clock/Reset				
$\overline{\text{RESET}}$	D10	$I_{S,PU}$	–	**Reset.** Active-low. Resets the BCM53262M.
XTALI XTALO	P21 P22	I	–	**25-MHz Crystal/Clock Input.** For a single-ended clock signal input, connect a 25.000 (±50 ppm) MHz reference clock to the XTALI pin. This pin must be driven with a continuous clock. Leave XTALO unconnected for this mode of operation. Alternatively, a 25.000 MHz parallel-resonant crystal can be connected between the XTALI/XTALO pins, with a 22 pF capacitor from each pin to GND.
XTALI_CK25 XTALO_CK25	AA20 AB21	I	–	**Additional 25-MHz Crystal/Clock.** The signal pins when selected, CK25_SRC_SEL = 0, provide a 25 MHz clock to on-chip integrated PHY. Similarly, these inputs can be driven by a single-ended clock or connected to parallel-resonant crystal. • For a single-ended clock signal input, connect a 25.000 (±50 ppm) MHz reference clock to the XTALI_CK25 pin. This pin must be driven with a continuous clock. Leave XTALO_CK25 unconnected for this mode of operation. • Alternatively, a 25.000 MHz parallel-resonant crystal can be connected between the XTALI_CK25/ XTALO_CK25 pins, with a 27 pF capacitor from each pin to GND.
CK25_SRC_SEL	Y7	I_{PU}	–	**EPHY Clock Source Select** • 1 = Select clock source derived from internal to the device. • 0 = Select clock source from XTALI_CK25/ XTALO_CK25.
CLK25_OUT	E22	O		**25-MHz Clock Output.** A single-ended 25 MHz clock output for use to connect to external GPHY.
SGMII/SerDes Interface				
SD_TXDN_G0 SD_TXDP_G0	N23 N24	O	–	**G0 SerDes Transmit pairs.** Differential SerDes output data pairs.
SD_TXDN_G1 SD_TXDP_G1	L23 L24	O	–	**G1 SerDes Transmit pairs.** Differential SerDes output data pairs.
SD_TXDN_G2 SD_TXDP_G2	J23 J24	O	–	**G2 SerDes Transmit pairs.** Differential SerDes output data pairs.
SD_TXDN_G3 SD_TXDP_G3	G23 G24	O	–	**G3 SerDes Transmit pairs.** Differential SerDes output data pairs.
SD_RXDN_G0 SD_RXDP_G0	M25 M26	I	–	**G0 SerDes Receive pairs.** Differential SerDes input data pairs.

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	Ball #	Type	Drive (mA)	Description
SD_RXDN_G1 SD_RXDP_G1	K25 K26	I	–	**G1 SerDes Receive pairs.** Differential SerDes input data pairs.
SD_RXDN_G2 SD_RXDP_G2	H25 H26	I	–	**G2 SerDes Receive pairs.** Differential SerDes input data pairs.
SD_RXDN_G3 SD_RXDP_G3	F25 F26	I	–	**G3 SerDes Receive pairs.** Differential SerDes input data pairs.
SD_G0 SD_G1 SD_G2 SD_G3	C23 B24 A24 E23	I	–	**Fiber Signal Detect.** Single-ended input reference signal from fiber optic module.
IMP Interface				
IMP_GTXCLK (Revision B only)	C20	0	–	**IMP GMII Transmit Clock.** 125 MHz clock is driven to synchronize the data in GMII mode. ***Note:*** When the IMP Interface is configured to GMII mode, IMP_TXCLK must also be connected to a clock source (such as 25 MHz) for this port to receive/transmit packets.
IMP_TXCLK	C22	I	–	**IMP MII Receive Clock.** Synchronizes the TXD[3:0] in MII mode. In 100-Mbps mode, this input is 25 MHz. In 10-Mbps mode this input is 2.5 MHz.
		O	–	**IMP RvMII Receive Clock.** Synchronizes the TXD[3:0] in RvMII mode and connects to the MAC/management entity RXC. In 100-Mbps mode, this output is 25 MHz. In 10-Mbps mode this output is 2.5 MHz.
IMP_TXD[7:4] (Revision B only)	A23, D21, A22, E20	O	–	**IMP GMII Transmit Data Output.** Data bits TXD[7:0] are clocked on the rising edge of GTXCLK. TXD[7] is the most significant bit.
IMP_TXD[3:0]	D20, B21, A21, D19	O	–	**IMP MII Transmit Data Output.** Data bits TXD[3:0] are clocked on the rising edge of TXCLK supplied by MAC/ management entity. TXD[3] is the most significant bit. **IMP RvMII Receive Data Output.** Data bits TXD[3:0] are clocked on the rising edge of TXCLK and connected to the RXD pins of the external MAC/management entity.
IMP_TXEN	E21	O	–	**IMP GMII/MII Transmit Enable.** Active-high. TXEN indicates the data is valid on TXD pins. **IMP RvMII Receive Data Valid.** Active high. Connected to RXDV pin of MAC/ management entity. Indicates that a receive frame is in progress, and the data present on the TXD output pins is valid.
IMP_TXER	D22	O	–	**IMP GMII/MII Transmit Error.** Active-high. Asserts TXER when TXEN is high to force a bad code into the transmit data stream.

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	Ball #	Type	Drive (mA)	Description
IMP_RXCLK	C18	I	–	**IMP GMII Receive Clock.** (Revision B only) 125 MHz for 1000-Mbps operation.
		I	–	**IMP MII Receive Clock.** 25 MHz for 100-Mbps operation, and 2.5 MHz for 10-Mbps operation.
		O	–	**IMP RvMII Receive Clock.** RvMII Transmit Clock. Synchronizes the RXD[3:0] in RvMII mode and connects to the MAC/management entity TXC. 25 MHz for 100-Mbps mode.
IMP_RXD[7:4] (Revision B only)	A20, D18, E19, B19	I	–	**IMP GMII Receive Data Input.** Data bits RXD[7:0] are clocked on the rising edge of RXCLK. RXD[7] is the most significant bit.
IMP_RXD[3:0]	E18, D17, A19, A18	I	–	**IMP MII Receive Data Input.** Data bits RXD[3:0] are clocked on the rising edge of RXCLK. RXD[3] is the most significant bit. **IMP RvMII Transmit Data Input.** Clocked on the rising edge of RXCLK and connected to the TXD pins of the external MAC/management entity.
IMP_RXDV	B17	I	–	**IMP GMII/MII Receive Data Valid.** Active high. RXDV indicates that a receive frame is in progress, and the data present on the RXD output pins is valid. **IMP RvMII Transmit Enable.** Active-high. Indicates the data on the RXD[3:0] pins is encoded and transmitted. Connects to the TXEN of the external MAC/ management entity.
IMP_RXER	E17	I	–	**IMP GMII/MII Receive Error.** Indicates an error during the receive frame.
IMP_COL	E16	I_{PD}	–	**Collision Detect.** In half-duplex mode, active-high input indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous input signal.
IMP_CRS	A17	I_{PD}	–	**Carrier Sense.** Active-high. Indicates traffic on link.
EB Bus Interface				
EB_ADDR[3:0]	E15, A16, C16, D16	I		**Extended Bus Address.** Specify address of register to be accessed. EB_ADDR3 is the MSB. EB_ADDR0 is shared with SPI's MISO and EEPROM's DO.
EB_DATA[15:0]	E11, A12, C12, D12, E12, A13, B13, D13, E13, A14, C14, D14, E14, A15, B15, D15	I/O		**Extended Bus Data.** Data value to be written into EB_ADDR for a write operation or data read from the register specified by EB_ADDR for a read operation. Depending on the EB_16BITMODE setting, this will either be an 8 or 16 bit operation EB_DATA0 is Shared with SPI's MOSI and EEPROM's DI

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	Ball #	Type	Drive (mA)	Description
EB_CS	D11	I		**Extended Bus Chip Select.** Selects the BCM53262M for an EB Bus operation Shared with SPI's SS and EEPROM's CS.
EB_OE	B11	I		**Extended Bus Output Enable.** Used to enable the output drivers within the BCM53262M for the EB_DATA bus.
EB_WE	A11	I		**Expansion Bus Write Enable.** Used to write a register within the BCM53262M Shared with SPI's SCK and EEPROM's CK
EB_16BITMODE	D5	I_{PU}		**Strap Pin.** • 1 = Indicates the EB Bus operates in 16 bit mode. EB_DATA15 is the MSB. (Default) • 0 = Indicates the EB Bus operates in 16 bit mode. EB_DATA7 is the MSB.
MII Interface				
MDIO	C10	I/O_{PD}	8	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers of both the internal and external transceivers. The input data value on the MDIO pin is valid and latched on the rising edge of MDC.
MDC	A10	I/O_{PD}	8	**Management Data Clock.** For a slave-driven access, MDC must be provided to the BCM53262M as an input to allow MII management functions. Clock frequencies up to 12.5 MHz are supported. During master mode access. As in auto-polling or when any SCK activity is detected on the SPI Interface, the BCM53262M sources a 2.5-MHz clock to the external PHY device.
Bias				
RDAC2 RDAC1 RDAC0	AA22 Y21 AB14	B	–	**DAC Bias Resistor.** Adjusts the drive level of the transmit DAC. Three separate 1percent precision resistors must be connected between the RDAC pins and GND. See "Recommended Operating Conditions" on page 377 for the required value.
LEDs				
LEDMODE1 LEDMODE0	D24 B26	I_{PD} I_{PD}	–	**LED Mode.** See Table 42: "LED Mode Shift Sequence," on page 129 for details.
LEDCLK	D9	O	8	**LED Shift Clock.** Periodically active to enable the shift of LEDDATA into external registers.

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	Ball #	Type	Drive (mA)	Description
LEDDATA	A9	O	8	**LED Data Output.** Serial LED data is shifted out when LEDCLK is active. Refer to Table 41: "LED Status Types," on page 128 and Table 42: "LED Mode Shift Sequence," on page 129 for a functional description of these signals.
MLEDCLK	B9	O		**Matrix LED Shift Clock.** Periodically active to enable the shift of both MLEDCOL and MLEDROW data into external registers.
MLEDCOL	E10	O		**Matrix LED Column Data Output.** Serial LED data is shifted out when MLEDCLK is active.
MLEDROW	A8	O		**Matrix LED Row Data Output.** Serial LED data is shifted out when MLEDCLK is active.
SPI				
MISO	D16	O_{3S}	8	**Master-In/Slave-Out.** Output signal from the BCM53262M driven with serial data during a Serial Management Port Read operation. Shared with EEPROM's DO and EB_ADDR0.
MOSI	D15	I_{PU}	–	**Master-Out/Slave-In.** Input signal which receives control and address information for the Serial Management Port, as well as serial data during Write operations. Shared with EEPROM's DI and EB_DATA0.
SCK	A11	I/O_{PD}	8	**Serial Clock.** Clock input to the Serial Management Port supplied by the SPI master. Supports up to 2 MHz. Shared with EEPROM's CK and $\overline{EB_WE}$.
$\overline{SS}$	D11	I/O_{PU}	8	**Slave Select.** Active-low signal which enables a Serial Management Port Read or Write operation. Shared with EEPROM's CS and $\overline{EB_CS}$.
EEPROM				
CS	D11	O_{PU}	8	**Chip Select.** Active-high signal which enables an EEPROM read operation. Shared with SPI's $\overline{SS}$ and $\overline{EB_CS}$.
DI	D15	O_{PU}	8	**Data In.** Serial data input to the external EEPROM. Shared with SPI's MOSI and EB_DATA0.
DO	D16	I_{PU}	–	**Data Out.** Serial data output from the external EEPROM. Shared with SPI's MISO and EB_ADDR0.
CK	A11	O_{PD}	8	**Serial Data Clock.** Clock output to the EEPROM supplied by the BCM53262M. Shared with SPI's SCK and $\overline{EB_WE}$.

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	Ball #	Type	Drive (mA)	Description
Test Interface				
TCK	E5	I_{PU}	–	**JTAG Test Clock Input.** Clock input used to synchronize JTAG control and data transfers. If unused, may be left unconnected.
TDI	F5	I_{PU}	–	**JTAG Test Data Input.** Serial data input to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.
TDO	C2	O_{3S}	8	**JTAG Test Data Output.** Serial data output from the JTAG TAP Controller. Updated on the falling edge of TCK. Actively driven both high and low when enabled; high impedance otherwise.
TMS	A1	I_{PU}	–	**JTAG Mode Select Input.** Single control input to the JTAG TAP Controller used to traverse the test-logic state machine. Sampled on the rising edge of TCK. If unused, may be left unconnected.
$\overline{\text{TRST}}$	B2	I_{PU}	–	**JTAG Test Reset.** Asynchronous active-low reset input to the JTAG TAP Controller. The TRST input must be driven low to insure the TAP controller initializes to the proper state. ***Note:*** A 4.7K external pull-down resistor is required on this pin to ensure proper initialization.
Strap Configuration				
CPU_EEPROM_SEL1 CPU_EEPROM_SEL0	F10 B8	I/O_{PD} I/O_{PU}	–	**CPU Interface Selection.** • CPU_EEPROM_SEL[1:0] = 00: EEPROM interface. • CPU_EEPROM_SEL[1:0] = 01: SPI interface. (Default) • CPU_EEPROM_SEL[1:0] = 10: Reserved. • CPU_EEPROM_SEL[1:0] = 11: EB Bus interface.
EEPROM_TYPE1 EEPROM_TYPE0	C24 G21	I/O_{PD} I/O_{PD}	–	EEPROM Type Select. The EEPROM type is automatically detected by the BCM53262M. These two strap pins are essentially don't cares and can be ignored.See "EEPROM Interface" on page 112 for more information.
ENFDXFLOW	D26	I/O_{PU}	–	**Enable Automatic Full Duplex Flow Control.** In combination with the results of auto-negotiation, sets the flow control mode. Refer to Table 8: "Flow Control Modes," on page 77 for more information.
ENHDXFLOW	D25	I/O_{PU}	–	**Enable Automatic Backpressure.** • ENHDXFLOW =0: 10/100 ports half-duplex flow control is disabled. • ENHDXFLOW =1: 10/100 ports half-duplex flow control is enabled. See Table 8: "Flow Control Modes," on page 77 for more information.

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	*Ball #*	*Type*	*Drive (mA)*	*Description*
EN_GRX_FLOW	B25	I/O_{PU}	–	**Enable Gigabit Receive Flow Control.** • EN_GRX_FLOW = 0: Gigabit ports Half-duplex flow control is disabled. • EN_GRX_FLOW = 1: Gigabit ports Half-duplex flow control is enabled.
HW_FWDG_EN	C25	I/O_{PU}	–	**Forwarding Enable.** • HW_FWDG_EN = 0: Frame forwarding is disabled at power-up. Typically implemented to support compliant 802.1 Spanning Tree Protocol in a managed application. • HW_FWDG_EN = 1: Frame forwarding is enabled (typical for unmanaged applications).
MDIX_DIS	AF1	I/O_{PD}	–	**HP Auto-MDIX Disable.** • MDIX_DIS = 0: Automatic TX cable swap detection enabled. • MDIX_DIS = 1: Automatic TX cable swap detection disabled.
GIGA_IMP_IFSEL1 GIGA_IMP_IFSEL0	E9 A7	I_{PD}	–	**IMP-Port Interface Select.** • GIGA_IMP_IFSEL[1:0] = 11: Reserved (Revision A) • GIGA_IMP_IFSEL[1:0] = 11: GMII (Revision B) • GIGA_IMP_IFSEL[1:0] = 10: RvMII (Recommended) • GIGA_IMP_IFSEL[1:0] = 01: MII • GIGA_IMP_IFSEL[1:0] = 00: Reserved (Default). ***Note:*** RvMII when selected enables the interface to appear as a 100 Mbps full duplex PHY MII, as seen by external MAC. Under this mode the TXCLK/RXCLK become 25 MHz clock outputs.
PHY_POLL_DIS	C9	I_{PD}	–	**PHY Polling Disable.** • 1 = Disable External EPHY/EGPHY Polling • 0 = Enable External EPHY/EGPHY Polling
CFP_ENABLE	F6	I_{PD}	–	**CFP Function Enable.** • 1 = Enable. • 0 = Disable.
Power				
AVDD	AA19	PWR	–	**2.5V Internal 25-MHz Clock VDD.**
AVDD2	R20	PWR	–	1.2V XTALI_CK25 and XTALO_CK25 Circuit VDD.

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	*Ball #*	*Type*	*Drive (mA)*	*Description*
AVDDL	AA7, AA9, AA11, AA13, AA15, AA17, AA25, AB11, AC21, AD6, AD9, AD13, AD18, AD25, AE7, AE11, AE16, AE20, AF5, T20, U20, U21, V20, V21, W19, W20, W21, W24, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19	PWR	–	**1.2V Analog VDD.**
AVSS	AA8, AA10, AA112, AA14, AA16, AA18, AA21, AB6, AB20, AB24, AC6, AC22, AD10, AD14, AD17, AE5, AE8, AE12, AE15, AE19, AE25, P18, T19, U19, U22, U23, V19, V23, W10, W11, W12, W13, W14, W15, W16, W18, Y20, Y25	GND	–	**Analog GND.**
DVDD	H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, J8, J19, K8, K19, L8, L19, M8, M19, N8, P8, R8, R19, T8, U8, V8, V14, W9, W17	PWR	–	**1.2V Digital Core VDD.**

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	*Ball #*	*Type*	*Drive (mA)*	*Description*
OVDD	AB1, AB3, C4, C7, C11, C13, F12, F14, G8, G9, G10, G11, G12, G13, G14, H1, H3, H6, H7, H8, H20, H21, J6, J7, J20, J21, K6, K7, K20, K21, L6, L7, L20, L21, M6, M7, N6, N7, P6, P7, R1, R3, R6, R7, T6, T7, U6, U7, V6, V7, W6, W7, W8, Y8, Y9	PWR	–	**2.5V**
OVDD2	B18, B20, B22, C15, C17, F15, F17, F19, F21, G15, G16, G17, G18, G19, G20	PWR	–	**2.5V/3.3V** • GMII = 3.3V • MII = 2.5V or 3.3V • RvMII 2.5V or 3.3V
SAVDD	E25, F23, G25, H23, J25, K23, L25, M23, N19, N25, P19, P23, R25, T23	PWR	–	**1.2V SerDes VDD**
BIASVDD0 BIASVDD1 BIASVDD2	AB15 AB22 Y22	PWR	–	**2.5V Bias Circuit VDD.**
XTALVDD	N21	PWR	–	**2.5V XTAL Circuit VDD.**
SAVSS	E26, F24, G22, G26, H24, J22, J26, K22, K24, L22, L26, M20, M24, N20, N22, N26, P20, P24, R26, T24	PWR	–	**Ground**
PLLAVDD	M21, M22	PWR	–	**1.2V PLL**
PLL2AVDD	H22	PWR	–	**1.2V PLL**
PLLAVSS	R21, R22, T22	PWR	–	**Ground**
PLL2AVSS	F22	PWR	–	**Ground**

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	*Ball #*	*Type*	*Drive (mA)*	*Description*
DVSS	A26, AA5, AB5, AC2, AC4, AD1, AD3, B4, B6, B10, B12, B14, B16, B23, C1, C19, C21, D23, E2, E4, F9, F11, F13, F16, F18, F20, G5, H5, J2, J4, J5, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, K1, K3, K5, K9, K10, K11, K12, K13, K14, K15, K16, K17, K18, L5, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18, M2, M4, M5, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, N5, N9, N10, N11, N12, N13, N14, N15, N16, N17, N18, P5, P9, P10, P11, P12, P13, P14, P15, P16, P17, R5, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, T2, T4, T5, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, U1, U3, U5, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, V5, V9, V10, V11, V12, V13, V15, V16, V17, V18, W2, W4, W5, Y5	GND	–	**Digital GND.**

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Table 48: Hardware Signal Descriptions (Cont.)

Signal Name	*Ball #*	*Type*	*Drive (mA)*	*Description*
DNC	AD5, AE3, AF2, AE4, AF4, C3 B1, AC5, AF3, AA6, Y6, AE1, AE2, T21	DNC	–	**Do Not Connect.** The pins listed in this block are for test purposes only and should not be connected (float). Do not connect these pins together.
DNC	A4, AA1, AA2, AC1, A25, AB2, AD2, D1, D2, E1, F1, F2, G1, G2, H2, J1, K2, L1, L2, M1, N1, N2, P1, P2, P25, P26, R2, R23, R24, T1, U2, V1, V2, Y1, Y2, W1	DNC	–	**Do Not Connect.** The pins listed in this block are for test purposes only and should not be connected (float). Do not connect these pins together
	A23, D21, A22, E20			A23, D21, A22, E20 are DNC in Revision A silicon.
INC	D6, C5, B5, A2, F7, B3, E7, A3, F8, E6, C6, G7, D7, G6, B7, C8, D8, A6, A5, E8	NC	–	**Internally Not Connect.** The pins listed in this block are internally not connected (float).
Pull Down				
PDN	J3, T3, AC3, H4, G3, G4, F3, F4, E3, D4, D3, R4, P3, P4, N3, N4, M3, L4, L3, AB4, AA3, AA4, Y3, Y4, W3, V4, V3, K4, U4, AD4	–	–	**Pull Down.** The pins listed in this block should be connected to digital ground through a 4.7K resistor.
	C20, A20, D18, E19, B19			C20, A20, D18, E19, B19 Are PDN in Revision A silicon.

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Section 6: BCM53262M Pin Assignments

Ball List by Ball Number

Table 49: Pin Assignment (Sorted by Ball Number)

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
A1	TMS	AA13	AVDDL	AB19	RDN_38	AC24	TDN_40
A10	MDC	AA14	AVSS	AB2	DNC	AC25	TDP_42
A11	$\overline{\text{EB_WE}}$	AA15	AVDDL	AB20	AVSS	AC26	TDN_43
A12	EB_DATA14	AA16	AVSS	AB21	XTALO_CK25	AC3	PDN
A13	EB_DATA10	AA17	AVDDL	AB22	BIASVDD1	AC4	DVSS
A14	EB_DATA6	AA18	AVSS	AB23	RDN_41	AC5	DNC
A15	EB_DATA2	AA19	AVDD	AB24	AVSS	AC6	AVSS
A16	EB_ADDR2	AA2	DNC	AB25	TDN_42	AC7	RDN_25
A17	IMP_CRS	AA20	XTALI_CK25	AB26	TDP_43	AC8	RDP_25
A18	IMP_RXD0	AA21	AVSS	AB3	OVDD	AC9	TDN_27
A19	IMP_RXD1	AA22	RDAC2	AB4	PDN	AD1	DVSS
A2	INC	AA23	RDP_41	AB5	DVSS	AD10	AVSS
A20	PDN (Rev.A) IMP_RXD7 (Rev. B)	AA24	RDN_43	AB6	AVSS	AD11	TDN_29
A21	IMP_TXD1	AA25	AVDDL	AB7	TDN_24	AD12	TDP_29
A22	DNC (Rev. A) IMP_TXD5 (Rev. B)	AA26	RDP_44	AB8	TDP_24	AD13	AVDDL
A23	DNC (Rev. A) IMP_TXD7 (Rev. B)	AA3	PDN	AB9	RDP_26	AD14	AVSS
A24	SD_G2	AA4	PDN	AC1	DNC	AD15	TDP_32
A25	DNC	AA5	DVSS	AC10	TDP_27	AD16	TDN_32
A26	DVSS	AA6	DNC	AC11	TDP_28	AD17	AVSS
A3	INC	AA7	AVDDL	AC12	TDN_28	AD18	AVDDL
A4	DNC	AA8	AVSS	AC13	TDN_31	AD19	RDP_36
A5	INC	AA9	AVDDL	AC14	TDP_31	AD2	DNC
A6	INC	AB1	OVDD	AC15	TDN_33	AD20	RDN_36
A7	GIGA_IMP_IFSEL0	AB10	RDN_26	AC16	TDP_33	AD21	RDN_39
A8	MLEDROW	AB11	AVDDL	AC17	TDP_34	AD22	RDP_39
A9	LEDDATA	AB12	RDP_30	AC18	TDN_34	AD23	RDP_40
AA1	DNC	AB13	RDN_30	AC19	TDN_37	AD24	TDP_40
AA10	AVSS	AB14	RDAC0	AC2	DVSS	AD25	AVDDL
AA11	AVDDL	AB15	BIASVDD0	AC20	TDP_37	AD26	RDN_42
AA12	AVSS	AB16	TDN_35	AC21	AVDDL	AD3	DVSS
		AB17	TDP_35	AC22	AVSS	AD4	PDN
		AB18	RDP_38	AC23	RDN_40	AD5	DNC

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Ball #	Signal Name
AD6	AVDDL
AD7	TDP_25
AD8	TDN_25
AD9	AVDDL
AE1	DNC
AE10	RDP_27
AE11	AVDDL
AE12	AVSS
AE13	TDP_30
AE14	TDN_30
AE15	AVSS
AE16	AVDDL
AE17	RDP_34
AE18	RDN_34
AE19	AVSS
AE20	AVDDL
AE21	RDN_37
AE22	RDP_37
AE23	TDN_39
AE24	TDP_39
AE25	AVSS
AE26	RDP_42
AE2	DNC
AE3	DNC
AE4	DNC
AE5	AVSS
AE6	RDP_24
AE7	AVDDL
AE8	AVSS
AE9	RDN_27
AF1	MDIX_DIS
AF10	RDN_28
AF11	RDN_29
AF12	RDP_29
AF13	RDN_31
AF14	RDP_31
AF15	RDP_32
AF16	RDN_32
AF17	RDN_33
AF18	RDP_33
AF19	RDN_35
AF20	RDP_35
AF21	TDP_36
AF22	TDN_36
AF23	TDP_38
AF24	TDN_38
AF25	TDP_41
AF26	TDN_41
AF2	DNC
AF3	DNC
AF4	DNC
AF5	AVDDL
AF6	RDN_24
AF7	TDP_26
AF8	TDN_26
AF9	RDP_28
B1	DNC
B10	DVSS
B11	$\overline{\text{EB_OE}}$
B12	DVSS
B13	EB_DATA9
B14	DVSS
B15	EB_DATA1
B16	DVSS
B17	IMP_RXDV
B18	OVDD2
B19	PDN (Rev. A) IMP_RXD4 (Rev. B)
B2	$\overline{\text{TRST}}$
B20	OVDD2
B21	IMP_TXD2
B22	OVDD2
B23	DVSS
B24	SD_G1
B25	EN_GRX_FLOW
B26	LEDMODE0
B3	INC
B4	DVSS
B5	INC
B6	DVSS
B7	INC
B8	CPU_EEPROM_SEL0
B9	MLEDCLK
C1	DVSS
C10	MDIO
C11	OVDD
C12	EB_DATA13
C13	OVDD
C14	EB_DATA5
C15	OVDD2
C16	EB_ADDR1
C17	OVDD2
C18	IMP_RXCLK
C19	DVSS
C2	TDO
C20	PDN (Rev. A) IMP_GTXCLK (Rev. B)
C21	DVSS
C22	IMP_TXCLK
C23	SD_G0
C24	EEPROM_TYPE1
C25	HW_FWDG_EN
C26	SYSFREQ1
C3	DNC
C4	OVDD
C5	INC
C6	INC
C7	OVDD
C8	INC
C9	PHY_POLL_DIS
D1	DNC
D10	$\overline{\text{RESET}}$
D11	$\overline{\text{EB_CS}}$
D12	EB_DATA12
D13	EB_DATA8
D14	EB_DATA4
D15	EB_DATA0
D16	EB_ADDR0
D17	IMP_RXD2
D18	PDN (Rev. A) IMP_RXD6 (Rev. B)
D19	IMP_TXD0
D2	DNC
D20	IMP_TXD3
D21	DNC (Rev. A) IMP_TXD6 (Rev. B)
D22	IMP_TXER
D23	DVSS
D24	LEDMODE1
D25	ENHDXFLOW
D26	ENFDXFLOW
D3	PDN
D4	PDN
D5	EB_16BITMODE
D6	INC
D7	INC
D8	INC
D9	LEDCLK
E1	DNC
E10	MLEDCOL
E11	EB_DATA15
E12	EB_DATA11
E13	EB_DATA7
E14	EB_DATA3
E15	EB_ADDR3
E16	IMP_COL
E17	IMP_RXER
E18	IMP_RXD3
E19	PDN (Rev. A) IMP_RXD5 (Rev. B)
E2	DVSS
E20	DNC (Rev. A) IMP_TXD4 (Rev. B)
E21	IMP_TXEN
E22	CLK25_OUT
E23	SD_G3
E24	SYSFREQ0
E25	SAVDD
E26	SAVSS
E3	PDN

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Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
E4	DVSS	G16	OVDD2	H4	PDN	K16	DVSS
E5	TCK	G17	OVDD2	H5	DVSS	K17	DVSS
E6	INC	G18	OVDD2	H6	OVDD	K18	DVSS
E7	INC	G19	OVDD2	H7	OVDD	K19	DVDD
E8	INC	G2	DNC	H8	OVDD	K2	DNC
E9	GIGA_IMP_IFSEL1	G20	OVDD2	H9	DVDD	K20	OVDD
F1	DNC	G21	EEPROM_TYPE0	J1	DNC	K21	OVDD
F10	CPU_EEPROM_SEL1	G22	SAVSS	J10	DVSS	K22	SAVSS
F11	DVSS	G23	SD_TXDN_G3	J11	DVSS	K23	SAVDD
F12	OVDD	G24	SD_TXDP_G3	J12	DVSS	K24	SAVSS
F13	DVSS	G25	SAVDD	J13	DVSS	K25	SD_RXDN_G1
F14	OVDD	G26	SAVSS	J14	DVSS	K26	SD_RXDP_G1
F15	OVDD2	G3	PDN	J15	DVSS	K3	DVSS
F16	DVSS	G4	PDN	J16	DVSS	K4	PDN
F17	OVDD2	G5	DVSS	J17	DVSS	K5	DVSS
F18	DVSS	G6	INC	J18	DVSS	K6	OVDD
F19	OVDD2	G7	INC	J19	DVDD	K7	OVDD
F2	DNC	G8	OVDD	J2	DVSS	K8	DVDD
F20	DVSS	G9	OVDD	J20	OVDD	K9	DVSS
F21	OVDD2	H1	OVDD	J21	OVDD	L1	DNC
F22	PLL2AVSS	H10	DVDD	J22	SAVSS	L10	DVSS
F23	SAVDD	H11	DVDD	J23	SD_TXDN_G2	L11	DVSS
F24	SAVSS	H12	DVDD	J24	SD_TXDP_G2	L12	DVSS
F25	SD_RXDN_G3	H13	DVDD	J25	SAVDD	L13	DVSS
F26	SD_RXDP_G3	H14	DVDD	J26	SAVSS	L14	DVSS
F3	PDN	H15	DVDD	J3	PDN	L15	DVSS
F4	PDN	H16	DVDD	J4	DVSS	L16	DVSS
F5	TDI	H17	DVDD	J5	DVSS	L17	DVSS
F6	CFP_ENABLE	H18	DVDD	J6	OVDD	L18	DVSS
F7	INC	H19	DVDD	J7	OVDD	L19	DVDD
F8	INC	H2	DNC	J8	DVDD	L2	DNC
F9	DVSS	H20	OVDD	J9	DVSS	L20	OVDD
G1	DNC	H21	OVDD	K1	DVSS	L21	OVDD
G10	OVDD	H22	PLL2AVDD	K10	DVSS	L22	SAVSS
G11	OVDD	H23	SAVDD	K11	DVSS	L23	SD_TXDN_G1
G12	OVDD	H24	SAVSS	K12	DVSS	L24	SD_TXDP_G1
G13	OVDD	H25	SD_RXDN_G2	K13	DVSS	L25	SAVDD
G14	OVDD	H26	SD_RXDP_G2	K14	DVSS	L26	SAVSS
G15	OVDD2	H3	OVDD	K15	DVSS	L3	PDN

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Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
L4	PDN	N16	DVSS	P4	PDN	T16	DVSS
L5	DVSS	N17	DVSS	P5	DVSS	T17	DVSS
L6	OVDD	N18	DVSS	P6	OVDD	T18	DVSS
L7	OVDD	N19	SAVDD	P7	OVDD	T19	AVSS
L8	DVDD	N2	DNC	P8	DVDD	T2	DVSS
L9	DVSS	N20	SAVSS	P9	DVSS	T20	AVDDL
M1	DNC	N21	XTALVDD	R1	OVDD	T21	DNC
M10	DVSS	N22	SAVSS	R10	DVSS	T22	PLLAVSS
M11	DVSS	N23	SD_TXDN_G0	R11	DVSS	T23	SAVDD
M12	DVSS	N24	SD_TXDP_G0	R12	DVSS	T24	SAVSS
M13	DVSS	N25	SAVDD	R13	DVSS	T25	TDP_47
M14	DVSS	N26	SAVSS	R14	DVSS	T26	RDP_47
M15	DVSS	N3	PDN	R15	DVSS	T3	PDN
M16	DVSS	N4	PDN	R16	DVSS	T4	DVSS
M17	DVSS	N5	DVSS	R17	DVSS	T5	DVSS
M18	DVSS	N6	OVDD	R18	DVSS	T6	OVDD
M19	DVDD	N7	OVDD	R19	DVDD	T7	OVDD
M2	DVSS	N8	DVDD	R2	DNC	T8	DVDD
M20	SAVSS	N9	DVSS	R20	AVDD2	T9	DVSS
M21	PLLAVDD	P1	DNC	R21	PLLAVSS	U1	DVSS
M22	PLLAVDD	P10	DVSS	R22	PLLAVSS	U10	DVSS
M23	SAVDD	P11	DVSS	R23	DNC	U11	DVSS
M24	SAVSS	P12	DVSS	R24	DNC	U12	DVSS
M25	SD_RXDN_G0	P13	DVSS	R25	SAVDD	U13	DVSS
M26	SD_RXDP_G0	P14	DVSS	R26	SAVSS	U14	DVSS
M3	PDN	P15	DVSS	R3	OVDD	U15	DVSS
M4	DVSS	P16	DVSS	R4	PDN	U16	DVSS
M5	DVSS	P17	DVSS	R5	DVSS	U17	DVSS
M6	OVDD	P18	AVSS	R6	OVDD	U18	DVSS
M7	OVDD	P19	SAVDD	R7	OVDD	U19	AVSS
M8	DVDD	P2	DNC	R8	DVDD	U2	DNC
M9	DVSS	P20	SAVSS	R9	DVSS	U20	AVDDL
N1	DNC	P21	XTALI	T1	DNC	U21	AVDDL
N10	DVSS	P22	XTALO	T10	DVSS	U22	AVSS
N11	DVSS	P23	SAVDD	T11	DVSS	U23	AVSS
N12	DVSS	P24	SAVSS	T12	DVSS	U24	TDN_46
N13	DVSS	P25	DNC	T13	DVSS	U25	TDN_47
N14	DVSS	P26	DNC	T14	DVSS	U26	RDN_47
N15	DVSS	P3	PDN	T15	DVSS	U3	DVSS

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Ball #	Signal Name
U4	PDN
U5	DVSS
U6	OVDD
U7	OVDD
U8	DVDD
U9	DVSS
V1	DNC
V10	DVSS
V11	DVSS
V12	DVSS
V13	DVSS
V14	DVDD
V15	DVSS
V16	DVSS
V17	DVSS
V18	DVSS
V19	AVSS
V2	DNC
V20	AVDDL
V21	AVDDL
V22	TDP_45
V23	AVSS
V24	TDP_46
V25	RDP_45
V26	RDN_46
V3	PDN
V4	PDN
V5	DVSS
V6	OVDD
V7	OVDD
V8	DVDD
V9	DVSS
W1	DNC
W10	AVSS
W11	AVSS
W12	AVSS
W13	AVSS
W14	AVSS
W15	AVSS
W16	AVSS
W17	DVDD
W18	AVSS
W19	AVDDL
W2	DVSS
W20	AVDDL
W21	AVDDL
W22	TDN_45
W23	TDN_44
W24	AVDDL
W25	RDN_45
W26	RDP_46
W3	PDN
W4	DVSS
W5	DVSS
W6	OVDD
W7	OVDD
W8	OVDD
W9	DVDD
Y1	DNC
Y10	AVDDL
Y11	AVDDL
Y12	AVDDL
Y13	AVDDL
Y14	AVDDL
Y15	AVDDL
Y16	AVDDL
Y17	AVDDL
Y18	AVDDL
Y19	AVDDL
Y2	DNC
Y20	AVSS
Y21	RDAC1
Y22	BIASVDD2
Y23	TDP_44
Y24	RDP_43
Y25	AVSS
Y26	RDN_44
Y3	PDN
Y4	PDN
Y5	DVSS
Y6	DNC
Y7	CK25_SRC_SEL
Y8	OVDD
Y9	OVDD

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Ball List by Signal Name

Table 50: Pin Assignment (Sorted by Signal Name)

Signal Name	Ball #
AVDD	AA19
AVDD2	R20
AVDDL	AA11
AVDDL	AA13
AVDDL	AA15
AVDDL	AA17
AVDDL	AA25
AVDDL	AA7
AVDDL	AA9
AVDDL	AB11
AVDDL	AC21
AVDDL	AD13
AVDDL	AD18
AVDDL	AD25
AVDDL	AD6
AVDDL	AD9
AVDDL	AE11
AVDDL	AE16
AVDDL	AE20
AVDDL	AE7
AVDDL	AF5
AVDDL	T20
AVDDL	U20
AVDDL	U21
AVDDL	V20
AVDDL	V21
AVDDL	W19
AVDDL	W20
AVDDL	W21
AVDDL	W24
AVDDL	Y10
AVDDL	Y11
AVDDL	Y12
AVDDL	Y13
AVDDL	Y14
AVDDL	Y15
AVDDL	Y16
AVDDL	Y17
AVDDL	Y18
AVDDL	Y19
AVSS	AA10
AVSS	AA12
AVSS	AA14
AVSS	AA16
AVSS	AA18
AVSS	AA21
AVSS	AA8
AVSS	AB20
AVSS	AB24
AVSS	AB6
AVSS	AC22
AVSS	AC6
AVSS	AD10
AVSS	AD14
AVSS	AD17
AVSS	AE12
AVSS	AE15
AVSS	AE19
AVSS	AE25
AVSS	AE5
AVSS	AE8
AVSS	P18
AVSS	T19
AVSS	U19
AVSS	U22
AVSS	U23
AVSS	V19
AVSS	V23
AVSS	W10
AVSS	W11
AVSS	W12
AVSS	W13
AVSS	W14
AVSS	W15
AVSS	W16
AVSS	W18
AVSS	Y20
AVSS	Y25
BIASVDD0	AB15
BIASVDD1	AB22
BIASVDD2	Y22
CFP_ENABLE	F6
CK25_SRC_SEL	Y7
CLK25_OUT	E22
CPU_EEPROM_SEL0	B8
CPU_EEPROM_SEL1	F10
INC	A2
DNC (Rev. A) IMP_TXD5 (Rev. B)	A22
DNC (Rev. A) IMP_TXD7 (Rev. B)	A23
DNC	A25
DNC	A4
INC	A5
INC	A6
DNC	AA1
DNC	AA2
DNC	AA6
DNC	AB2
DNC	AC1
DNC	AC5
DNC	AD2
DNC	AD5
DNC	AE1
DNC	AE2
DNC	AE3
DNC	AE4
DNC	AF2
DNC	AF3
DNC	AF4
DNC	B1
INC	B3
INC	B5
INC	B7
DNC	C3
INC	C5
INC	C6
INC	C8
DNC	D1
DNC	D2
DNC (Rev. A) IMP_TXD6 (Rev. B)	D21
INC	D6
INC	D7
INC	D8
DNC	E1
DNC (Rev. A) IMP_TXD4 (Rev. B)	E20
INC	E6
INC	E7
INC	E8
DNC	F1
DNC	F2
INC	F7
INC	F8
DNC	G1
DNC	G2
INC	G6
INC	G7
DNC	H2
DNC	J1
DNC	K2
DNC	L1

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Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
DNC	L2	DVDD	N8	DVSS	J11	DVSS	M13
DNC	M1	DVDD	P8	DVSS	J12	DVSS	M14
DNC	N1	DVDD	R19	DVSS	J13	DVSS	M15
DNC	N2	DVDD	R8	DVSS	J14	DVSS	M16
DNC	P1	DVDD	T8	DVSS	J15	DVSS	M17
DNC	P2	DVDD	U8	DVSS	J16	DVSS	M18
DNC	P25	DVDD	V14	DVSS	J17	DVSS	M2
DNC	P26	DVDD	V8	DVSS	J18	DVSS	M4
DNC	R2	DVDD	W17	DVSS	J2	DVSS	M5
DNC	R23	DVDD	W9	DVSS	J4	DVSS	M9
DNC	R24	DVSS	A26	DVSS	J5	DVSS	N10
DNC	T1	DVSS	AA5	DVSS	J9	DVSS	N11
DNC	T21	DVSS	AB5	DVSS	K1	DVSS	N12
DNC	U2	DVSS	AC2	DVSS	K10	DVSS	N13
DNC	V1	DVSS	AC4	DVSS	K11	DVSS	N14
DNC	V2	DVSS	AD1	DVSS	K12	DVSS	N15
DNC	W1	DVSS	AD3	DVSS	K13	DVSS	N16
DNC	Y1	DVSS	B10	DVSS	K14	DVSS	N17
DNC	Y2	DVSS	B12	DVSS	K15	DVSS	N18
DNC	Y6	DVSS	B14	DVSS	K16	DVSS	N5
DVDD	H10	DVSS	B16	DVSS	K17	DVSS	N9
DVDD	H11	DVSS	B23	DVSS	K18	DVSS	P10
DVDD	H12	DVSS	B4	DVSS	K3	DVSS	P11
DVDD	H13	DVSS	B6	DVSS	K5	DVSS	P12
DVDD	H14	DVSS	C1	DVSS	K9	DVSS	P13
DVDD	H15	DVSS	C19	DVSS	L10	DVSS	P14
DVDD	H16	DVSS	C21	DVSS	L11	DVSS	P15
DVDD	H17	DVSS	D23	DVSS	L12	DVSS	P16
DVDD	H18	DVSS	E2	DVSS	L13	DVSS	P17
DVDD	H19	DVSS	E4	DVSS	L14	DVSS	P5
DVDD	H9	DVSS	F11	DVSS	L15	DVSS	P9
DVDD	J19	DVSS	F13	DVSS	L16	DVSS	R10
DVDD	J8	DVSS	F16	DVSS	L17	DVSS	R11
DVDD	K19	DVSS	F18	DVSS	L18	DVSS	R12
DVDD	K8	DVSS	F20	DVSS	L5	DVSS	R13
DVDD	L19	DVSS	F9	DVSS	L9	DVSS	R14
DVDD	L8	DVSS	G5	DVSS	M10	DVSS	R15
DVDD	M19	DVSS	H5	DVSS	M11	DVSS	R16
DVDD	M8	DVSS	J10	DVSS	M12	DVSS	R17

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Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #
DVSS	R18	DVSS	W2	IMP_RXD0	A18	OVDD	H20
DVSS	R5	DVSS	W4	IMP_RXD1	A19	OVDD	H21
DVSS	R9	DVSS	W5	IMP_RXD2	D17	OVDD	H3
DVSS	T10	DVSS	Y5	IMP_RXD3	E18	OVDD	H6
DVSS	T11	EB_16BITMODE	D5	IMP_RXDV	B17	OVDD	H7
DVSS	T12	EB_ADDR0	D16	IMP_RXER	E17	OVDD	H8
DVSS	T13	EB_ADDR1	C16	IMP_TXCLK	C22	OVDD	J20
DVSS	T14	EB_ADDR2	A16	IMP_TXD0	D19	OVDD	J21
DVSS	T15	EB_ADDR3	E15	IMP_TXD1	A21	OVDD	J6
DVSS	T16	$\overline{\text{EB_CS}}$	D11	IMP_TXD2	B21	OVDD	J7
DVSS	T17	EB_DATA0	D15	IMP_TXD3	D20	OVDD	K20
DVSS	T18	EB_DATA1	B15	IMP_TXEN	E21	OVDD	K21
DVSS	T2	EB_DATA10	A13	IMP_TXER	D22	OVDD	K6
DVSS	T4	EB_DATA11	E12	LEDCLK	D9	OVDD	K7
DVSS	T5	EB_DATA12	D12	LEDDATA	A9	OVDD	L20
DVSS	T9	EB_DATA13	C12	LEDMODE0	B26	OVDD	L21
DVSS	U1	EB_DATA14	A12	LEDMODE1	D24	OVDD	L6
DVSS	U10	EB_DATA15	E11	MDC	A10	OVDD	L7
DVSS	U11	EB_DATA2	A15	MDIO	C10	OVDD	M6
DVSS	U12	EB_DATA3	E14	MDIX_DIS	AF1	OVDD	M7
DVSS	U13	EB_DATA4	D14	MLEDCLK	B9	OVDD	N6
DVSS	U14	EB_DATA5	C14	MLEDCOL	E10	OVDD	N7
DVSS	U15	EB_DATA6	A14	MLEDROW	A8	OVDD	P6
DVSS	U16	EB_DATA7	E13	OVDD	AB1	OVDD	P7
DVSS	U17	EB_DATA8	D13	OVDD	AB3	OVDD	R1
DVSS	U18	EB_DATA9	B13	OVDD	C11	OVDD	R3
DVSS	U3	$\overline{\text{EB_OE}}$	B11	OVDD	C13	OVDD	R6
DVSS	U5	$\overline{\text{EB_WE}}$	A11	OVDD	C4	OVDD	R7
DVSS	U9	EEPROM_TYPE0	G21	OVDD	C7	OVDD	T6
DVSS	V10	EEPROM_TYPE1	C24	OVDD	F12	OVDD	T7
DVSS	V11	EN_GRX_FLOW	B25	OVDD	F14	OVDD	U6
DVSS	V12	ENFDXFLOW	D26	OVDD	G10	OVDD	U7
DVSS	V13	ENHDXFLOW	D25	OVDD	G11	OVDD	V6
DVSS	V15	GIGA_IMP_IFSEL0	A7	OVDD	G12	OVDD	V7
DVSS	V16	GIGA_IMP_IFSEL1	E9	OVDD	G13	OVDD	W6
DVSS	V17	HW_FWDG_EN	C25	OVDD	G14	OVDD	W7
DVSS	V18	IMP_COL	E16	OVDD	G8	OVDD	W8
DVSS	V5	IMP_CRS	A17	OVDD	G9	OVDD	Y8
DVSS	V9	IMP_RXCLK	C18	OVDD	H1	OVDD	Y9

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Signal Name	Ball #
OVDD2	B18
OVDD2	B20
OVDD2	B22
OVDD2	C15
OVDD2	C17
OVDD2	F15
OVDD2	F17
OVDD2	F19
OVDD2	F21
OVDD2	G15
OVDD2	G16
OVDD2	G17
OVDD2	G18
OVDD2	G19
OVDD2	G20
PDN (Rev.A) IMP_RXD7 (Rev. B)	A20
PDN	AA3
PDN	AA4
PDN	AB4
PDN	AC3
PDN	AD4
PDN (Rev. A) IMP_RXD4 (Rev. B)	B19
PDN (Rev. A) IMP_GTXCLK (Rev. B)	C20
PDN (Rev. A) IMP_RXD6 (Rev. B)	D18
PDN	D3
PDN	D4
PDN (Rev. A) IMP_RXD5 (Rev. B)	E19
PDN	E3
PDN	F3
PDN	F4
PDN	G3
PDN	G4
PDN	H4
PDN	J3
PDN	K4
PDN	L3

Signal Name	Ball #
PDN	L4
PDN	M3
PDN	N3
PDN	N4
PDN	P3
PDN	P4
PDN	R4
PDN	T3
PDN	U4
PDN	V3
PDN	V4
PDN	W3
PDN	Y3
PDN	Y4
PHY_POLL_DIS	C9
PLL2AVDD	H22
PLL2AVSS	F22
PLLAVDD	M21
PLLAVDD	M22
PLLAVSS	R21
PLLAVSS	R22
PLLAVSS	T22
RDAC0	AB14
RDAC1	Y21
RDAC2	AA22
RDN_24	AF6
RDN_25	AC7
RDN_26	AB10
RDN_27	AE9
RDN_28	AF10
RDN_29	AF11
RDN_30	AB13
RDN_31	AF13
RDN_32	AF16
RDN_33	AF17
RDN_34	AE18
RDN_35	AF19
RDN_36	AD20
RDN_37	AE21

Signal Name	Ball #
RDN_38	AB19
RDN_39	AD21
RDN_40	AC23
RDN_41	AB23
RDN_42	AD26
RDN_43	AA24
RDN_44	Y26
RDN_45	W25
RDN_46	V26
RDN_47	U26
RDP_24	AE6
RDP_25	AC8
RDP_26	AB9
RDP_27	AE10
RDP_28	AF9
RDP_29	AF12
RDP_30	AB12
RDP_31	AF14
RDP_32	AF15
RDP_33	AF18
RDP_34	AE17
RDP_35	AF20
RDP_36	AD19
RDP_37	AE22
RDP_38	AB18
RDP_39	AD22
RDP_40	AD23
RDP_41	AA23
RDP_42	AE26
RDP_43	Y24
RDP_44	AA26
RDP_45	V25
RDP_46	W26
RDP_47	T26
$\overline{\text{RESET}}$	D10
SAVDD	E25
SAVDD	F23
SAVDD	G25
SAVDD	H23

Signal Name	Ball #
SAVDD	J25
SAVDD	K23
SAVDD	L25
SAVDD	M23
SAVDD	N19
SAVDD	N25
SAVDD	P19
SAVDD	P23
SAVDD	R25
SAVDD	T23
SAVSS	E26
SAVSS	F24
SAVSS	G22
SAVSS	G26
SAVSS	H24
SAVSS	J22
SAVSS	J26
SAVSS	K22
SAVSS	K24
SAVSS	L22
SAVSS	L26
SAVSS	M20
SAVSS	M24
SAVSS	N20
SAVSS	N22
SAVSS	N26
SAVSS	P20
SAVSS	P24
SAVSS	R26
SAVSS	T24
SD_G0	C23
SD_G1	B24
SD_G2	A24
SD_G3	E23
SD_RXDN_G0	M25
SD_RXDN_G1	K25
SD_RXDN_G2	H25
SD_RXDN_G3	F25
SD_RXDP_G0	M26

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Signal Name	Ball #
SD_RXDP_G1	K26
SD_RXDP_G2	H26
SD_RXDP_G3	F26
SD_TXDN_G0	N23
SD_TXDN_G1	L23
SD_TXDN_G2	J23
SD_TXDN_G3	G23
SD_TXDP_G0	N24
SD_TXDP_G1	L24
SD_TXDP_G2	J24
SD_TXDP_G3	G24
SYSFREQ0	E24
SYSFREQ1	C26
TCK	E5
TDI	F5
TDN_24	AB7
TDN_25	AD8
TDN_26	AF8
TDN_27	AC9
TDN_28	AC12
TDN_29	AD11
TDN_30	AE14
TDN_31	AC13
TDN_32	AD16
TDN_33	AC15
TDN_34	AC18
TDN_35	AB16
TDN_36	AF22
TDN_37	AC19
TDN_38	AF24
TDN_39	AE23
TDN_40	AC24
TDN_41	AF26
TDN_42	AB25
TDN_43	AC26
TDN_44	W23
TDN_45	W22
TDN_46	U24
TDN_47	U25

Signal Name	Ball #
TDO	C2
TDP_24	AB8
TDP_25	AD7
TDP_26	AF7
TDP_27	AC10
TDP_28	AC11
TDP_29	AD12
TDP_30	AE13
TDP_31	AC14
TDP_32	AD15
TDP_33	AC16
TDP_34	AC17
TDP_35	AB17
TDP_36	AF21
TDP_37	AC20
TDP_38	AF23
TDP_39	AE24
TDP_40	AD24
TDP_41	AF25
TDP_42	AC25
TDP_43	AB26
TDP_44	Y23
TDP_45	V22
TDP_46	V24
TDP_47	T25
TMS	A1
$\overline{\text{TRST}}$	B2
INC	A3
XTALI	P21
XTALI_CK25	AA20
XTALO	P22
XTALO_CK25	AB21
XTALVDD	N21

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Section 7: BCM53262M Ball Locations

676-PBGA Ball Location Diagram

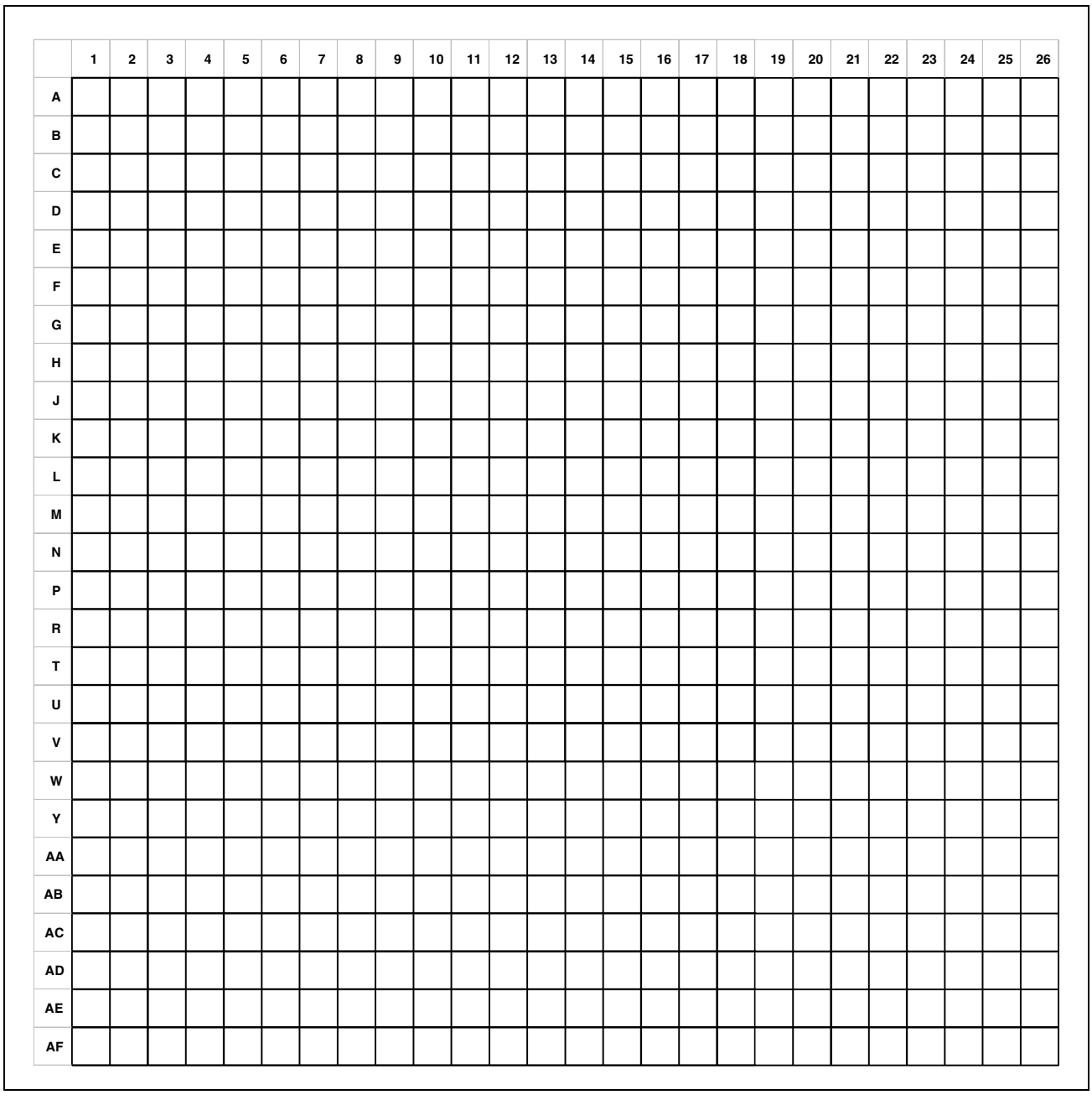

Figure 43: 676-PBGA Ball Location Diagram (Top View)

Section 8: Register Definitions

Register Notations

In the register description tables, the following notation in the R/W column is used to describe the ability to read or write:

- R/W = Read or write
- RO = Read only
- LH = Latched high. Clear after read operation
- LL = Latched low. Clear after read operation
- H = Fixed high
- L = Fixed low
- SC = Self clear after read

Reserved bits must be written as the default value and ignored when read.

Register Definition

The BCM53262 series consists of several devices with differing port configurations. Except as noted in Table 51, all switching features are identical within each of the devices. The register definition described hereunder is in the highest port count configuration. Refer to Table 51 for the valid port configuration and feature difference for the specific device.

Table 51: Valid Port Map and Feature Difference

Device	*FE Ports*	*GE Ports*	*CFP Rules*	*MAC-Based QoS/VLAN*	*Protocol-Based QoS/VLAN*	*QinQ*	*VLAN Translation*
BCM53262M	P24 ~ P47	G0, G1, G2, G3	1K	Y	Y	Y	Y
BCM53262S	P24 ~ P47	G0, G1, G2, G3	512	N	N	N	N

The BCM53262M's registers set can be accessed through the SPI Port or EB bus. The register space is organized into pages, each contains a certain set of registers. The following table lists the pages defined in the BCM53262M. In addition to access via the SPI port, registers can be accessed via the MDC/MDIO path via pseudo MII mode. The per-port MII registers are still accessible via the MDC/MDIO path of the external MII, compatible with the BCM53xx device mode.

To access a page, the page register (0xFF) is written with the page value. The registers contained in the page can then be accessed by their address.

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Table 52: Global Page Register Map

Page	*Description*
00h	"Page 00h: Control Registers" on page 165.
01h	"Page 01h: Control 1 Registers" on page 185
02h	"Page 02h: Status Registers" on page 196.
03h	"Page 03h: Management Mode Registers" on page 203.
04h	"Page 04h: ARL Control Register" on page 218.
05h	"Page 05h: ARL Access Registers" on page 221.
06h-09h	Reserved
0Ah	"Page 0Ah: Priority Queue Control Registers" on page 240
10h	"Page 10h: PHY Info Registers" on page 257
20h	"Page 20h: CFP Registers" on page 258
21h	"Page 21h: CFP Control Registers" on page 269
22h	"Page 22h: CFP UDF Control Registers" on page 274
30h	"Page 30h: QoS Registers" on page 286.
31h	"Page 31h: MAC-Based Aggregation Registers" on page 293
33h	"Page 33h: Port Egress Control Registers" on page 296
34h	"Page 34h: 802.1Q VLAN Registers" on page 299.
40h	"Page 40h: 802.1x Registers" on page 315.
41h	"Page 41h: 802.1x_1 Registers" on page 321
43h	"Page 43h: Rate Control Registers" on page 328
44h	Reserved
45h	"Page 45h: 802.1s Multiple Spanning Tree Registers" on page 334
68h-84h	"Page 68h–84h: Port MIB Registers" on page 336
85h	"Page 85h: Snapshot Port MIB Registers" on page 338
A0h–B7h	"Page A0h–B7h: FE Ports 24-47 MII Registers" on page 340
B8h	Reserved
B9h-BCh	"Page B9h-BCh: Internal SerDes Port (P49~P52) MII Registers" on page 353
BDh-D7h	Reserved
D8h-DCh	"Page D8h–DCh: External PHY Registers" on page 373
F0h	SPI Data I/O 0—Table 329: "Global Registers (Maps to All Pages)," on page 375.
F1h	SPI Data I/O 1—Table 329: "Global Registers (Maps to All Pages)," on page 375.
F2h	SPI Data I/O 2—Table 329: "Global Registers (Maps to All Pages)," on page 375.
F3h	SPI Data I/O 3—Table 329: "Global Registers (Maps to All Pages)," on page 375.
F4h	SPI Data I/O 4—Table 329: "Global Registers (Maps to All Pages)," on page 375.
F5h	SPI Data I/O 5—Table 329: "Global Registers (Maps to All Pages)," on page 375.
F6h	SPI Data I/O 6—Table 329: "Global Registers (Maps to All Pages)," on page 375.
F7h	SPI Data I/O 7–0.

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Table 52: Global Page Register Map (Cont.)

Page	*Description*
F8h–FDh	Reserved
FEh	"Global Registers" on page 375.
FFh	Page Register

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Page 00h: Control Registers

Table 53: Control Registers (Page 00h)

Address	*Bits*	*Register Name*
00h	8	“Switch Mode Register (Page 00h/Addr 00h)” on page 166
01h	Reserved	
02h	8	“PHY Scan Control Register (Page 00h/Addr 02h)” on page 166
03h	8	“New Control Register (Page 00h/Addr 03h)” on page 167
05h-1Fh	–	Reserved
20h	8	“Broadcast Forward Map Register (Page 00h/Addr 20h)” on page 168
28h	64	“IPMC Lookup Fail Forward Map Register (Page 00h/Addr 28h)” on page 169
30h	64	“Unicast Lookup Fail Forward Map Register (Page 00h/Addr 30h)” on page 169
38h	64	“Multicast Lookup Fail Forward Map Register (Page 00h/Addr 38h)” on page 170
40h	64	“Protected Port Select Register (Page 00h/Addr 40h)” on page 171
48h	64	“Software Flow Control Registers (Page 00h/Addr 48h)” on page 172
50h	32	“Strap Pins Status Register (Page 00h/Addr 50h)” on page 173
54h-59h	Reserved	
5Ah	16	“LED Control Register (Page 00h/Addr 5Ah)” on page 175
5Ch	16	“LED Function 0 Control Register (Page 00h/Addr 5Ch–5Dh)” on page 177
5Eh	16	“LED Function 1 Control Register (Page 00h/Addr 5Eh–5Fh)” on page 177
60h	64	“LED Function Map Register (Page 00h/Addr 60h–67h)” on page 179
68h	64	“LED Enable Map Register (Page 00h/Addr 68h–6Fh)” on page 180
70h	64	“LED Mode Map 0 Register (Page 00h/Addr 70h–77h)” on page 181
78h	64	“LED Mode Map 1 Register (Page 00h/Addr 78h–7Fh)” on page 182
90h	64	“RX PAUSE PASS Register (Page 00h/Addr 90h–97h)” on page 183
98h	64	“TX PAUSE PASS Register (Page 00h/Addr 98h–9Fh)” on page 184
A0h–EFh	Reserved	
F0h–F7h	–	SPI Data I/O[0:7]
FEh	–	SPI Status
FFh	8	Page Register

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Switch Mode Register (Page 00h/Addr 00h)

Table 54: Switch Mode Register (Page 00h: Address 00h)

Bit	Name	R/W	Description	Default
7:6	RSVD	–	Reserved. Write as default. Ignore on read.	10
5:4	IPG	R/W	Programmable Inter-Packet-Gap. For 10/100 speed: • 11 = 96-bit time • 10 = 92-bit time • 0x = Reserved	11
3	NOBLKCD	R/W	When the bit is set, it does not block the carrier detected signal. • 1 = Does not block, and txport always defers to CRS. • 0 = Block CD	0
2	RSVD	R/W	Reserved. Write as default. Ignore on read.	1
1	SW_FWDG_EN	R/W	Software Forwarding Enable. • SW_FWDG_EN=1: Frame forwarding is enabled. • SW_FWDG_EN=0: Frame forwarding is disabled. Read from HW_FWDG_EN pin on power-on. Can be overwritten subsequently. For managed switch implementations (BCM53262M mode), the switch should be configured to disable forwarding on power-on, to allow the processor to configure the internal address table and other parameters, before frame forwarding is enabled.	HW_FWDG_EN strap pin state
0	SW_FWDG_MODE	R/W	Software Forwarding Mode. Programmed from the inverse of the HW_FWDG_EN pin at power-on. Can be overwritten subsequently. • 1 = Managed Mode. • 0 = Unmanaged Mode.	inverted HW_FWDG_EN strap pin state

PHY Scan Control Register (Page 00h/Addr 02h)

Table 55: PHY Scan Control Register (Page 00h: Address 02h)

Bit	Name	R/W	Description	Default
7	RSVD	RO	Reserved. Write default. Ignore on read.	0
6:2	RSVD	RO	Reserved. Write default. Ignore on read.	0

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Table 55: PHY Scan Control Register (Page 00h: Address 02h)

Bit	Name	R/W	Description	Default
1	EN_PHY_SCAN	R/W	Enable Global External PHY Scanning Function Programmed from the inverse of the PHY_POLL_DIS pin at power-on reset. Can be overwritten subsequently. When enabled, the BCM53262M will poll externally at addresses 18h, 19h, 1Ah, 1Bh and 1Ch to read the PHY status. • 1 = Enable PHY scanning • 0 = Disable PHY scanning	1 Inverse of PHY_POLL_DIS Strap Pin State
0	EN_INIT_CFG	R/W	Enable.	1

New Control Register (Page 00h/Addr 03h)

Table 56: New Control Register (Page 00h: Address 03h)

Bit	Name	R/W	Description	Default
7:6	MLF_FM_EN	R/W	Multicast Lookup Fail Forward Map Enable. • 00: Any incoming packets with multicast DA not in ARL table are flooded. • 01: Any incoming packets with multicast DA not in ARL table are forwarded according to the "Multicast Lookup Fail Forward Map Register (Page 00h/Addr 38h)" on page 170. • 10: IPMC lookup fail packets are forwarded according to "IPMC Lookup Fail Forward Map Register (Page 00h/Addr 28h)" on page 169. • 11: Reserved.	0
5	ULF_FM_EN	R/W	Unicast Lookup Fail Forward Map Enable. When set to 1, any incoming packets with unicast DA not in ARL table are forwarded according to the "Unicast Lookup Fail Forward Map Register (Page 00h/Addr 30h)" on page 169.	0
4	CLK25	R/W	• 1 = Enable 25-MHz clock output. • 0 = Disable 25-MHz clock output.	1
3	BCAST_FWD_MAP_EN	R/W	Broadcast Traffic Forward Control • 1 = Broadcast packets are forwarded according to "Broadcast Forward Map Register (Page 00h/Addr 20h)" on page 168. • 0 = Broadcast packets are flooded to all ports.	0

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Table 56: New Control Register (Page 00h: Address 03h) (Cont.)

Bit	Name	R/W	Description	Default
2:1	MAX_RX_LIMIT	RW	Maximum Receive Packet Length Limit (Revision B Silicon only) * 00 = 2048 bytes for all packets (Default) * 01 = 1536 bytes for all packets * 10 = 1518 bytes for untagged packets or 1522 bytes for single tagged packets or 1526 bytes for doubled tagged packets * 11 = 2000 bytes for all packets	0
	RSVD	RO	Reserved (Revision A Silicon) Write default. Ignore on read.	0
0	DIS_ECC_CHK	R/W	When set to a 1, disable ECC check.	0

Broadcast Forward Map Register (Page 00h/Addr 20h)

Table 57: BCAST Forward Map Register (Page 00h: Address 20h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved. Write default. Ignore on read	0
52:24	BCST_FWD_MAP[52:24]	R/W	Broadcast Forward Map When BCAST_FWD_MAP_EN = 1 in "New Control Register (Page 00h/Addr 03h)" on page 167. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24] – 1 = Forward enable. – 0 = Forward disable.	0
23:0	RSVD	–	Reserved	–

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IPMC Lookup Fail Forward Map Register (Page 00h/Addr 28h)

Table 58: IPMC Lookup Fail Forward Map Register (Page 00h: Address 28h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved. Write default. Ignore on read	0
52:24	IPMC_LF_FWD_MAP[52:24]	R/W	IPMC Lookup Fail Forward Map, when MLF_FM_EN = 10 in "New Control Register (Page 00h/Addr 03h)" on page 167. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47 - port 24] – 1 = Forward enable – 0 = Forward disable	0
23:0	RSVD	–	Reserved	0

Unicast Lookup Fail Forward Map Register (Page 00h/Addr 30h)

Table 59: UC Lookup Fail Forward Map Register (Page 00h: Address 30h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved. Write default. Ignore on read	0
52:24	UC_LF_FWD_MAP[52:24]	R/W	Unicast Lookup Fail Forward Map, when ULF_FM_EN = 1 in "New Control Register (Page 00h/Addr 03h)" on page 167. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24] – 1 = Forward enable. – 0 = Forward disable.	0
23:0	RSVD	–	Reserved	0

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Multicast Lookup Fail Forward Map Register (Page 00h/Addr 38h)

Table 60: MC Lookup Fail Forward Map Register (Page 00h: Address 38h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved. Write default. Ignore on read	0
52:24	MC_LF_FWD_MAP[52:24]	R/W	MC Lookup Fail Forward Map, when MLF_FM_EN = 1 in "New Control Register (Page 00h/Addr 03h)" on page 167. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24] – 1 = Forward enable. – 0 = Forward disable.	0
23:0	RSVD	–	Reserved	0

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Protected Port Select Register (Page 00h/Addr 40h)

Table 61: Protected Port Select Register (Page 00h: Address 40h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved. Write default. Ignore on read	0
52:24	PROT_SEL[52:24]	R/W	Protected Port Select Map • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24] Set the assigned protected port to 1. ***Example:*** If port 24 is assigned as the protected port, set to 53'h00_0000_0100_0000. ***Note:*** The management port could not be configured as protected port.	0
23:0	RSVD	RO	Reserved	0

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Software Flow Control Registers (Page 00h/Addr 48h)

Table 62: Software Flow Control Register (Page 00h: Address 48h)

Bit	Name	R/W	Description	Default
63	SW_FLOW_CON_EN	R/W	Software Flow Control Override Enable. Any change to the SW_FLOW_CON state directly affects the "Pause Status Summary Register (Page 02h/Addr 30h–37h)" on page 203.	0
62	RSVD	–	Reserved.	0
61:58	RSVD	RO	Reserved. Write default. Ignore on read.	0
57:24	SW_FLOW_CON	R/W	Per port software override full-duplex/ half-duplex flow control. • Bit 57 for Giga TX port G3. • Bit 56 for Giga RX port G3. • Bit 55 for Giga TX port G2. • Bit 54 for Giga RX port G2. • Bit 53 for Giga TX port G1. • Bit 52 for Giga RX port G1. • Bit 51 for Giga TX port G0. • Bit 50 for Giga RX port G0. • Bit 49 for IMP TX port. • Bit 48 for IMP RX port. • Bits 47:24 = 10/100 ports [port 47-port 24] – 1 = Enable – 0 = Disable	3FF-FFFF-FF
23:0	RSVD	–	Reserved	0

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Strap Pins Status Register (Page 00h/Addr 50h)

Table 63: Strap Pins Status Register (Page 00h: Address 50h)

Bit	Name	R/W	Description	Default
31:29	RSVD	RO	Reserved	0
28	WRALLPHY	RO	Allow update to all PHYs at the same time.	0
27	RSVD	RO	Reserved. Write default. Ignore on read.	0
26	EN_SYSCLK_PROBE	RO	• 1 = Enable sysclk probe • 0 = Disable sysclk probe	0
25	EN_EXTCLK	RO	• 1 = Enable external clock • 0 = Disable external clock	0
24:22	RSVD	RO	Reserved	0
21:20	GIGA_IMP_IFSEL	RO	• 00 = Reserved • 01 = MII • 10 = RvMII • 11 = Reserved	00
19	EB_16BIT	RO	• EB Bus mode: • 1 = EB Bus in 16-bit mode • 0 = EB Bus in 8-bit mode.	0
18:17	RSVD	RO	Reserved	0
16:15	CPU_EEPROM_SEL	RO	• 11 = EB_Bus interface enable. • 10 = Reserved • 01 = SPI interface is enabled to CPU port • 00: Disables SPI interface and enables EEPROM interface	1
14	PHY_POLL_DIS	RO	• 1 = Disable external EPHY/EGPHY polling • 0 = Enable external EPHY/EGPHY polling	0
13:12	RSVD	RO	Reserved	0
11	BIST_CLR_RAM	RO	• 0 = Select Memory Clear function • 1 = Select BIST function	1
10	SKIP_SRAM_BIST		Disable BIST/Memory clear function	0
9	MDIX_DIS	RO	Disable PHY MDIX Function	0
8	RSVD	RO	Reserved	1
7:6	LEDMODE	RO	LEDMODE[1:0].	0
5	EN_GRX_FLOW	RO	Full-duplex GigaPort RX Flow Control Enable	1
4	HW_FWDG_EN	RO	• 1 = Forwarding process enable. • 0 = Turn off forwarding process. Default is assertion for unmanaged switch.	1

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Table 63: Strap Pins Status Register (Page 00h: Address 50h) (Cont.)

Bit	Name	R/W	Description	Default
3:2	SYSFREQ	RO	System Clock Status • 00 = 100 MHz • 01 = 111 MHz • 10 = 111 MHz • 11 = 125 MHz	00
1	ENHDXFLOW	RO	Half-duplex port Flow Control Enable.	1
0	ENFDXFLOW	RO	Full-duplex port Flow Control Enable and GigaPort TX Flow Control Enable.	1

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LED Control Register (Page 00h/Addr 5Ah)

Table 64: LED Control Register (Page 00h: Address 5Ah)

Bit	Name	R/W	Description	Default
15:11	RSVD	R/W	Reserved Write as default. Ignore on read.	0
10	EN_Alt_SEQ	R/W	New Bit Stream Enable • 0 = Keep original LED Function Map 0/1 bit sequence • 1 = Enable alternate LED bit sequence for both LED Function Map 0/1 as follows: – 15: reserved – 14: reserved – 13: 1G/ACT – 12: 10/100M/ACT – 11: 100M/ACT – 10: 10M/ACT – 9: SPD10M – 8: LNK/ACT – 7: DPX/COL – 6: LNK – 5: ACT – 4: DPX – 3: COL – 2: SPD100M – 1: SPD1G – 0: reserved	0
9	ACT Blink Rate	R/W	Change Blinking Rate for Different Link Speed. When set to **1**, changes the blinking rate for: • 10M = LED Frequency/4 • 100M = LED Frequency/2 • 1G = LED Frequency/1	0
8	LED Bit Stream Order	R/W	Bit Stream from Low Port Number First. When set to **1**, enables LED bit stream from the low port number to be shifted out first.	1
7	LED_EN	R/W	LED Function Enable. Program from HW_FWDG_EN pin on power-on. Can be overwritten subsequenly. Default is assertion for unmanaged switch. • 1 = Enable LED function • 0 = Disable LED function	HW_FWDG_EN pin
6	RSVD	R/W	Reserved Write as default. Ignore on read.	0
5	LED_PSCAN_EN	R/W	Write to enable port scan during POST period.	0

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Table 64: LED Control Register (Page 00h: Address 5Ah)

Bit	Name	R/W	Description	Default
4:3	RSVD	R/W	Reserved Write as default. Ignore on read.	0
2:0	LED_RFS_STOP	R/W	LED Flashing Rate Control • 111 : 80 ms/6 Hz. • 110 : 70 ms/7 Hz. • 101 : 60 ms/8 Hz. • 100 : 50 ms/10 Hz. • 011 : 40 ms/12 Hz. (Default) • 010 : 30 ms/16 Hz. • 001 : 20 ms/25 Hz. • 000 : Invalid.	0x03

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LED Function 0 Control Register (Page 00h/Addr 5Ch–5Dh)

Table 65: LED Function 0 Control Register (Page 00h: Address 5Ch–5Dh)

Bit	Name	R/W	Description	Default
15:0	LED_FUNC 0	R/W	LED Function 0 Control 15: RSVD 14: RSVD 13: 1G/ACT 12: 10/100/ACT 11: 100M/ACT 10: 10M/ACT 9: SPD 1G 8: SPD 100M 7: SPD 10M 6: DPX/COL 5: LNK/ACT 4: COL 3: ACT 2: DPLX 1: LNK 0: RSVD LEDMODE [00] = 0x0120 (Default) LEDMODE [01] = 0x0C40 LEDMODE [10] = 0x0124 LEDMODE [11] = 0x0C04	LEDMODE[1:0] strap pin state

LED Function 1 Control Register (Page 00h/Addr 5Eh–5Fh)

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Table 66: LED Function 1 Control Register (Page 00h: Address 5Eh–5Fh)

Bit	Name	R/W	Description	Default
15:0	LED_FUNC 1	R/W	LED Function 1 Control 15: RSVD 14: RSVD 13: 1G/ACT 12: 10/100/ACT 11: 100M/ACT 10: 10M/ACT 9: SPD 1G 8: SPD 100M 7: SPD 10M 6: DPX/COL 5: LNK/ACT 4: COL 3: ACT 2: DPLX 1: LNK 0: RSVD LEDMODE [00] = 0x0320 (Default) LEDMODE [01] = 0x3040 LEDMODE [10] = 0x0324 LEDMODE [11] = 0x2C04	LEDMODE[1:0] strap pin state

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LED Function Map Register (Page 00h/Addr 60h–67h)

Table 67: LED Function Map Register (Page 00h: Address 60h–67h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	LED_FUNC _MAP	R/W	Per Port LED Function Select Bit • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24] – 1 = Select Function 1 – 0 = Select Function 0	1E-FFFF-FF
23:0	RSVD	RO	Reserved	0

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LED Enable Map Register (Page 00h/Addr 68h–6Fh)

Table 68: LED Enable Map Register (Page 00h: Address 68h–6Fh)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	LED_EN _MAP	R/W	Per Port LED Function Enable Bit • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 =10/100 ports [port 47-port 24] – 1 = Enable Function – 0 = Disable Function	1E-FFFF-FF
23:0	RSVD	RO	Reserved	0

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LED Mode Map 0 Register (Page 00h/Addr 70h–77h)

Table 69: LED Mode Map 0 Register (Page 00h: Address 70h–77h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	LED_MODE _MAP 0	R/W	Per port LED output control • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24] LED_Mode_Map 0 is used in conjunction with LED_Mode_Map 1 to determine the LED output. • [LED_Mode_Map 1, LED_Mode_Map 0] = 11: Auto. • [LED_Mode_Map 1, LED_Mode_Map 0] = 10: Blink. • [LED_Mode_Map 1, LED_Mode_Map 0] = 01: On. • [LED_Mode_Map 1, LED_Mode_Map 0] = 00: Off.	1E-FFFF-FF
23:0	RSVD	RO	Reserved	0

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LED Mode Map 1 Register (Page 00h/Addr 78h–7Fh)

Table 70: LED Mode Map 1 Register (Page 00h: Address 78h–7Fh)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	LED_MODE _MAP 1	R/W	Per port LED output Control • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24] LED_Mode_Map 1 is used in conjunction with LED_Mode_Map 0 to determine the LED output. • [LED_Mode_Map 1, LED_Mode_Map 0] = 11: Auto. • [LED_Mode_Map 1, LED_Mode_Map 0] = 10: Blink. • [LED_Mode_Map 1, LED_Mode_Map 0] = 01: On. • [LED_Mode_Map 1, LED_Mode_Map 0] = 00: Off.	1E-FFFF-FF
23:0	RSVD	RO	Reserved	0

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RX PAUSE PASS Register (Page 00h/Addr 90h–97h)

Table 71: RX Pause Pass Register (Page 00h: Address 90h–97h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	IGNORE_RX _PAUSE	R/W	Per port RX Pause Control • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24] – 1 = Ignore incoming 802.3x pause frames. – 0 = Comply with 802.3x pause frame control.	0
23:0	RSVD	RO	Reserved	0

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TX PAUSE PASS Register (Page 00h/Addr 98h–9Fh)

Table 72: TX Pause Pass Register (Page 00h: Address 98h–9Fh)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	IGNORE_TX _PAUSE	R/W	Per port TX Pause Control • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24] – 1 = Do not transmit 802.3x pause frames. – 0 = Comply with 802.3x pause frame control.	0
23:0	RSVD	RO	Reserved	0

Configuration ID Register (Page 00h/Addr EEh)

Table 73: Configuration ID Register (Page 00h/Addr EEh)

Bit	Name	R/W	Description	Default
15:5	RSVD	RO	Reserved	0
4:0	CONF_ID	RO	Configuration ID	0x03

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Page 01h: Control 1 Registers

Table 74: Control 1 Registers (Page 01h)

Address	Bits	Register Name
00h-27h	Reserved	–
28h-3Fh	8	“MII Port 24-47 State Override Registers (Page 01h/Addr 28h–3Fh)” on page 186
40h	8	“MII Port State Override Register” on page 186
41h-44h	8	“MII GigaPort State Override Registers (Page 01h/Addr 41-44h)” on page 188
45h-67h	Reserved	–
68h	8	“IMP Port PHY Scan Result Registers (Page 01H/Addr 68h)” on page 189
69h-72h	8	“G0–G3 GigaPorts PHY Scan Result Registers (Page 01h/Addr 69h–72h)” on page 190
73h-87h	Reserved	–
88h-9Fh	8	“10/100 Ports 24-47 Control Registers (Page 01h/Addr 88h–9Fh)” on page 191
A0h	8	“IMP Port Control Register (Page 01h/Addr A0h)” on page 193
A1h-A4h	8	“GigaPorts G0-G3 Control Registers (Page 01h/Addr A1h–A4h)” on page 194
A5h-AFh	Reserved	–
B0h		“Status Control Register (Page 01h/Addr B0h)” on page 195
B1h–EFh	Reserved	
F0h–F7h		SPI Data I/O[0:7]
F8h–FDh	Reserved	–
FEh		SPI Status
FFh	8	Page Register

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MII Port 24-47 State Override Registers (Page 01h/Addr 28h–3Fh)

Table 75: MII Port 24-47 State Override Registers (Page 01h/Addr 28h–3Fh)

Address	Bits	Register Name
28h	8	Port 24 (see "MII Port State Override Register" on page 186)
29h	8	Port 25 (see "MII Port State Override Register" on page 186)
2Ah	8	Port 26 (see "MII Port State Override Register" on page 186)
2Bh	8	Port 27 (see "MII Port State Override Register" on page 186)
2Ch	8	Port 28 (see "MII Port State Override Register" on page 186)
2Dh	8	Port 29 (see "MII Port State Override Register" on page 186)
2Eh	8	Port 30 (see "MII Port State Override Register" on page 186)
2Fh	8	Port 31 (see "MII Port State Override Register" on page 186)
30h	8	Port 32 (see "MII Port State Override Register" on page 186)
31h	8	Port 33 (see "MII Port State Override Register" on page 186)
32h	8	Port 34 (see "MII Port State Override Register" on page 186)
33h	8	Port 35 (see "MII Port State Override Register" on page 186)
34h	8	Port 36 (see "MII Port State Override Register" on page 186)
35h	8	Port 37 (see "MII Port State Override Register" on page 186)
36h	8	Port 38 (see "MII Port State Override Register" on page 186)
37h	8	Port 39 (see "MII Port State Override Register" on page 186)
38h	8	Port 40 (see "MII Port State Override Register" on page 186)
39h	8	Port 41 (see "MII Port State Override Register" on page 186)
3Ah	8	Port 42 (see "MII Port State Override Register" on page 186)
3Bh	8	Port 43 (see "MII Port State Override Register" on page 186)
3Ch	8	Port 44 (see "MII Port State Override Register" on page 186)
3Dh	8	Port 45 (see "MII Port State Override Register" on page 186)
3Eh	8	Port 46 (see "MII Port State Override Register" on page 186)
3Fh	8	Port 47 (see "MII Port State Override Register" on page 186)

MII Port State Override Register

Table 76: MII Port State Override Register

Bit	Name	R/W	Description	Default
7	RSVD	–	Reserved	1
6	MII_SW_OR	R/W	MII Software Override. • 0 = Use internal MII hardware pin status. • 1 = Use contents of this register.	0
5	SW_FC_En	R/W	Software Flow Control Enable.	0

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Table 76: MII Port State Override Register (Cont.)

Bit	Name	R/W	Description	Default
4:3	RSVD	RO	Reserved Write default. Ignore on read	0
2	SPEED	R/W	Software Port Speed Setting. • 1 = 100 Mbps. • 0 = 10 Mbps.	1
1	DPLX	R/W	Software Duplex Mode Setting. • 1 = Full-duplex • 0 = Half-duplex	1
0	LINK	R/W	Link State. • 1 = Link pass (up). • 0 = Link fail.	1

IMP/MII Port State Override Registers (Page 01h/Addr 40h)

Note: This register is in Rev. A silicon only.

Table 77: IMP Port State Override Registers (Page 01h/Addr 40h)

Bit	Name	R/W	Description	Default
7	PHY_Scan Enable	R/W	PHY Scan Control on IMP(MII) port: • 0 = Use MII Software Override • 1 = PHY scan enabled.	1
6	MII_SW_OR	R/W	MII Software Override: • 0 = Use MII hardware pin status • 1 = Use contents of this register	0
5	SW_FC_En	R/W	Software Flow Control Enable	0
4:3	RSVD	RO	Reserved Write default. Ignore on read	0
2	SPEED	R/W	Software Port Speed Setting: • 1 = 100 Mbps • 0 = 10 Mbps.	1
1	FDX	R/W	Full-duplex: • 1 = Full-duplex • 0 = Half-duplex	1
0	LINK	R/W	Link State. • 1 = Link pass (up) • 0 = Link fail	1

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MII GigaPort State Override Registers (Page 01h/Addr 41-44h)

Table 78: MII GigaPort State Override Registers (Page 01h/Addr 41-44h)

Address	Bits	Register Name
40h	8	IMP Port (Rev. B silicon only) (see Table 79: "MII GigaPort State Override Registers," on page 188)
41h	8	GE port 0 (see Table 79: "MII GigaPort State Override Registers," on page 188)
42h	8	GE port 1 (see Table 79: "MII GigaPort State Override Registers," on page 188)
43h	8	GE port 2 (see Table 79: "MII GigaPort State Override Registers," on page 188)
44h	8	GE port 3 (see Table 79: "MII GigaPort State Override Registers," on page 188)

Table 79: MII GigaPort State Override Registers

Bit	Name	R/W	Description	Default
7	GPHY_Scan Enable	R/W	Allows per port control for the BCM53262M to scan the external GPHY.	1
6	MII_SW_OR	R/W	MII Software Override. • 0 = Use GMII hardware pin status. • 1 = Use contents of this register.	0
5	TX Flow Control	R/W	Software Tx Flow Control Enable. Link Partner Flow Control Capability. • 0 = Not PAUSE capable. • 1 = PAUSE capable.	0
4	RX Flow Control	R/W	Software Rx Flow Control Enable. Link Partner Flow Control Capability. • 0 = Not PAUSE capable. • 1 = PAUSE capable.	0
3:2	SPEED	R/W	Speed. • 10 = 1000 Mbps. • 01 = 100 Mbps. • 00 = 10 Mbps.	10
1	FDX	R/W	Full-duplex. • 1 = Full-duplex. • 0 = Half-duplex.	1
0	LINK	R/W	Link State. • 1 = Link pass. • 0 = Link fail.	1

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IMP Port PHY Scan Result Registers (Page 01H/Addr 68h)

Note: This register is in Rev. A silicon only.

Table 80: IMP Port PHY Scan Result Registers (Page 01H/Addr 68h)

Bit	Name	R/W	Description	Default
7	RSVD	RO	Reserved Write default. Ignore on read	0
6	TIMEOUT	RO	PHY Register Scan Timeout Error	0
5	Flow Control	RO	Software Flow Control Enable Link Partner Flow Control Capability • 0 = Not PAUSE capable • 1 = PAUSE capable	0
4:3	RSVD	RO	Reserved Write default. Ignore on read	0
2	SPEED	RO	Speed status • 1 = 100 Mbps • 0 = 10 Mbps	0
1	FDX	RO	Duplex status • 1 = Full-duplex • 0 = Half-duplex	0
0	LINK	RO	Link status • 1 = Link pass • 0 = Link fail	0

IMP GigaPort PHY Scan Result Register (Page 01h/Addr 68h)

Note: This register is in Rev. B silicon only.

Table 81: IMP GigaPort PHY Scan Result Register (Page 01h/Addr 68h)

Address	Bits	Register Name
68h	8	IMP GigaPort (see Table 83: "GigaPorts PHY Scan Result Registers," on page 190)

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G0–G3 GigaPorts PHY Scan Result Registers (Page 01h/Addr 69h–72h)

Table 82: G0–G3 GigaPorts PHY Scan Result Registers (Page 01h/Addr 69h–72h)

Address	Bits	Register Name
69h	8	GE port 0 (see Table 83: "GigaPorts PHY Scan Result Registers," on page 190)
70h	8	GE port 1 (see Table 83: "GigaPorts PHY Scan Result Registers," on page 190)
71h	8	GE port 2 (see Table 83: "GigaPorts PHY Scan Result Registers," on page 190)
72h	8	GE port 3 (see Table 83: "GigaPorts PHY Scan Result Registers," on page 190)

Table 83: GigaPorts PHY Scan Result Registers

Bit	Name	R/W	Description	Default
7	RSVD	RO	Reserved Write default. Ignore on read	0
6	TIMEOUT	RO	PHY Register Scan Timeout Error	0
5	TX Flow Control	RO	Software Tx Flow Control Enable. Link Partner Flow Control Capability. • 0 = Not PAUSE capable. • 1 = PAUSE capable.	0
4	RX Flow Control	RO	Software Rx Flow Control Enable. Link Partner Flow Control Capability. • 0 = Not PAUSE capable. • 1 = PAUSE capable.	0
3:2	SPEED	RO	Speed Status. • 10 = 1000 Mbps. • 01 = 100 Mbps. • 00 = 10 Mbps.	0
1	FDX	RO	Duplex Status. • 1 = Full-duplex. • 0 = Half-duplex.	0
0	LINK	RO	Link Status. • 1 = Link pass. • 0 = Link fail.	0

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10/100 Ports 24-47 Control Registers (Page 01h/Addr 88h–9Fh)

Table 84: 10/100 Ports 24-47 Control Registers (Page 01h/Addr 88h–9Fh)

Address	Bits	Register Name
88h	8	Port 24 (see Table 85: "10/100 Ports Control Registers," on page 192)
89h	8	Port 25 (see Table 85: "10/100 Ports Control Registers," on page 192)
8Ah	8	Port 26 (see Table 85: "10/100 Ports Control Registers," on page 192)
8Bh	8	Port 27 (see Table 85: "10/100 Ports Control Registers," on page 192)
8Ch	8	Port 28 (see Table 85: "10/100 Ports Control Registers," on page 192)
8Dh	8	Port 29 (see Table 85: "10/100 Ports Control Registers," on page 192)
8Eh	8	Port 30 (see Table 85: "10/100 Ports Control Registers," on page 192)
8Fh	8	Port 31 (see Table 85: "10/100 Ports Control Registers," on page 192)
90h	8	Port 32 (see Table 85: "10/100 Ports Control Registers," on page 192)
91h	8	Port 33 (see Table 85: "10/100 Ports Control Registers," on page 192)
92h	8	Port 34 (see Table 85: "10/100 Ports Control Registers," on page 192)
93h	8	Port 35 (see Table 85: "10/100 Ports Control Registers," on page 192)
94h	8	Port 36 (see Table 85: "10/100 Ports Control Registers," on page 192)
95h	8	Port 37 (see Table 85: "10/100 Ports Control Registers," on page 192)
96h	8	Port 38 (see Table 85: "10/100 Ports Control Registers," on page 192)
97h	8	Port 39 (see Table 85: "10/100 Ports Control Registers," on page 192)
98h	8	Port 40 (see Table 85: "10/100 Ports Control Registers," on page 192)
99h	8	Port 41 (see Table 85: "10/100 Ports Control Registers," on page 192)
9Ah	8	Port 42 (see Table 85: "10/100 Ports Control Registers," on page 192)
9Bh	8	Port 43 (see Table 85: "10/100 Ports Control Registers," on page 192)
9Ch	8	Port 44 (see Table 85: "10/100 Ports Control Registers," on page 192)
9Dh	8	Port 45 (see Table 85: "10/100 Ports Control Registers," on page 192)
9Eh	8	Port 46 (see Table 85: "10/100 Ports Control Registers," on page 192)
9Fh	8	Port 47 (see Table 85: "10/100 Ports Control Registers," on page 192)

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Table 85: 10/100 Ports Control Registers

Bit	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	Spanning Tree Protocol State. CPU writes the current computed states of its Spanning Tree Algorithm for this port. • 000 = No Spanning Tree (unmanaged mode). • 001 = Disabled State (Default for Managed mode). • 010 = Blocking State. • 011 = Listening State. • 100 = Learning State. • 101 = Forwarding State. • 110–111 = Reserved. ***Note:*** Ignored when SW_FWDG_MODE = Unmanaged.	Controlled by HW_FWDG_EN Strap Option
4:2	RSVD	RO	Reserved Write default. Ignore on read	0
1	TX_DISABLE	R/W	Disables the transmit function of the port at the MAC level. • 1 = disable • 0 = enable	0
0	RX_DISABLE	R/W	Disables the receive function of the port at the MAC level. • 1 = disable • 0 = enable	0

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IMP Port Control Register (Page 01h/Addr A0h)

Table 86: IMP Port Control Register (Page 01h: Address A0h)

Bit	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	Spanning Tree Protocol State. CPU writes the current computed states of its Spanning Tree Algorithm for this port. • 000 = No Spanning Tree (unmanaged mode). • 001 = Disabled State. • 010 = Blocking State. • 011 = Listening State. • 100 = Learning State. • 101 = Forwarding State. • 110–111 = Reserved. ***Note:*** Ignored when SW_FWDG_MODE = Unmanaged.	Controlled by HW_FWDG_EN Strap Option
4	RX_UCST_EN	R/W	Receive Unicast Enable. Enables the receipt of unicast frames on the IMP, when the IMP is configured as the Frame Management Port, and the frame was flooded due to no matching address table entry. When cleared, unicast frames that meet the Mirror Ingress/Egress Rules are still forwarded to the Frame Management Port. ***Note:*** Ignored if the IMP is not selected as the Frame Management Port.	0
3	RX_MCST_EN	R/W	Receive Multicast Enable. Enables the receipt of multicast frames on the IMP, when the IMP is configured as the Frame Management Port, and the frame was flooded due to no matching address table entry. When cleared, multicast frames that meet the Mirror Ingress/Egress Rules are still forwarded to the Frame Management Port. ***Note:*** Ignored if the IMP is not selected as the Frame Management Port.	0
2	RX_BCST_EN	R/W	Receive Broadcast Enable. Enables the receipt of broadcast frames on the IMP, when the IMP is configured as the Frame Management Port. When cleared, multicast frames that meet the Mirror Ingress/Egress Rules are still forwarded to the Frame Management Port. ***Note:*** Ignored if the IMP is not selected as the Frame Management Port.	0

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Table 86: IMP Port Control Register (Page 01h: Address A0h) (Cont.)

Bit	Name	R/W	Description	Default
1	TX_DISABLE	R/W	Disables the transmit function of the port at the MAC level. • 1 = disable • 0 = enable	0
0	RX_DISABLE	R/W	Disables the receive function of the port at the MAC level. • 1 = disable • 0 = enable	0

GigaPorts G0-G3 Control Registers (Page 01h/Addr A1h–A4h)

Table 87: GigaPorts G0-G3 Control Registers (Page 01h/Addr A1h–A4h)

Address	Bits	Register Name
A1h	8	GE port 0 (see Table 88: "GigaPorts Control Registers," on page 194)
A2h	8	GE port 1 (see Table 88: "GigaPorts Control Registers," on page 194)
A3h	8	GE port 2 (see Table 88: "GigaPorts Control Registers," on page 194)
A4h	8	GE port 3 (see Table 88: "GigaPorts Control Registers," on page 194)

Table 88: GigaPorts Control Registers

Bit	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	Spanning Tree Protocol State. CPU writes the current computed states of its Spanning Tree Algorithm for this port. • 000 = No Spanning Tree (unmanaged mode). • 001 = Disabled State. • 010 = Blocking State. • 011 = Listening State. • 100 = Learning State. • 101 = Forwarding State. • 110–111 = Reserved. ***Note:*** Ignored when SW_FWDG_MODE = Unmanaged.	Controlled by HW_FWDG_EN Strap Option
4:2	RSVD	RO	Reserved Write default. Ignore on read	0
1	TX_DISABLE	R/W	Disables the transmit function of the port at the MAC level.	0
0	RX_DISABLE	R/W	Disables the receive function of the port at the MAC level.	0

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Status Control Register (Page 01h/Addr B0h)

Table 89: Status Control Register (Page 01h: Address B0h)

Bit	Name	R/W	Description	Default
7:1	RSVD	RO	Reserved Write default. Ignore on read	0
0	EN_IMP_RX_PAUSE_NOTAG	R/W	• 1 = CPU to IMP port, standard PAUSE frame without BRCM tag. • 0 = CPU to IMP port, requires BRCM tag for PAUSE frame	1

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Page 02h: Status Registers

Table 90: Status Registers (Page 02h)

Address	Bits	Register Name
00h–07h	64	"BIST Status 0 Register (Page 02h/Addr 00h–07h)" on page 197
08h–0Fh	64	"BIST Status 1 Register (Page 02h/Addr 08h–0Fh)" on page 198
10h–13h	64	"Link Status Summary Register (Page 02h/Addr 10h–17h)" on page 199
18h–1Fh	64	"Link Status Change Register (Page 02h/Addr 18h–1Fh)" on page 200
20h–27h	64	"Port Speed Summary Register (Page 02h/Addr 20h–27h)" on page 201
28h–2Fh	64	"Duplex Status Summary Register (Page 02h/Addr 28h–2Fh)" on page 202
30h–37h	64	"Pause Status Summary Register (Page 02h/Addr 30h–37h)" on page 203
38h–4Fh	Reserved	
60h–EFh	Reserved	
F0h–F7h	–	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	–	SPI Status
FFh	8	Page Register

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BIST Status 0 Register (Page 02h/Addr 00h–07h)

Table 91: BIST Status 0 Register (Page 02h/Addr 00h–07h)

Bit	Name	R/W	Description	Default
63	MAC2VLAN_MBIST_ERR	RO	MAC-based Vlan Table Memory BIST Error	0
62	PROTOCOL2VLAN_MBIST_ERR	RO	Protocol-based Vlan Table Memory BIST Error	0
61	FLOW2VLAN_MBIST_ERR	RO	Flow-based Vlan Table Memory BIST Error	0
60	IPMC_MBIST_ERR	RO	IP Multicast Table Memory BIST Error.	0
59	MSPT_MBIST_ERR	RO	Multiple Spanning Tree Table Memory BIST Error.	0
58	CFP_TCAM_LOGIC_ERR	RO	CFP TCAM Logic Error.	0
57	CFP_CNT_MBIST_ERR	RO	CFP Counter Memory BIST Error.	0
56	CFP_ACT_MBIST_ERR	RO	CFP Action Memory BIST Error.	0
55	CFP_RM_MBIST_ERR	RO	CFP Rate Meter Memory BIST Error.	0
54:39	CFP_TCAM_MBIST_ERR[15:0]	RO	CFP TCAM BIST Error.	0
38:30	MIB_MBIST_ERR[8:0]	RO	MIB Memory BIST Error. • Bit 38: GigaPort 3 • Bit 37: GigaPort 2 • Bit 36: GigaPort 1 • Bit 35: GigaPort 0 • Bit 34: IMP • Bit 33: Reserved • Bit 32: FE Ports 47-40 • Bit 31: FE Ports 39-32 • Bit 30: FE Ports 31-24	0
29	GTXQ_MBIST_ERR	RO	Global TXQ BIST Error.	0
28:0	TXQ_MBIST_ERR[28:0]	RO	Per-port TXQ BIST Error. • Bits 28-25: GigaPorts 3-0 • Bit 24: IMP • Bits 23-0: FE Ports 47-24	0

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BIST Status 1 Register (Page 02h/Addr 08h–0Fh)

Table 92: BIST Status 1 Register (Page 02h/Addr 08h–0Fh)

Bit	Name	R/W	Description	Default
63:11	RSVD	RO	Reserved.	0
10	FT_MCOL_DEFECT	RO	Frame Buffer Memory Defect (>= 1 error).	0
9	AT_MCOL_DEFECT	RO	Address Table Defect (>= 1 error).	0
8	VT_MCOL_DEFECT	RO	VLAN Table defect (>= 1 error).	0
7	FM_MCOL_DEFECT	RO	Frame Buffer Memory Failed (>= 2 errors).	0
6	AT_MCOL_DEFECT	RO	Address Table Failed (>= 2 errors).	0
5	VT_MCOL_DEFECT	RO	VLAN Table Failed (>= 2 errors).	0
4	FM_ECC_MBIST_ERR	RO	Frame Buffer ECC Memory BIST Error.	0
3	BFC_MBIST_ERR	RO	Buffer Control Memory BIST Error.	0
2	IRC_MBIST_ERR	RO	Ingress Rate Control Configuration Table BIST Error.	0
1	ERC_MBIST_ERR	RO	Egress Rate Control Configuration Table BIST Error.	0
0	VLAN2VLAN_MBIST_ERR	RO	VLAN Translation Table Memory Error.	0

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Link Status Summary Register (Page 02h/Addr 10h–17h)

Table 93: Link Status Summary Register (Page 02h: Address 10h–17h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	LINK_STATUS[52:24]	RO	Link Status. A 29-bit field indicating the Link Status for each 10/100Base-T port, the MII port and the 4-Gbit ports. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP/MII • Bits 47:24 = 10/100 ports [port 47-port 24] – 0 = Link Fail. – 1 = Link Pass. ***Note:*** Link status for the IMP/MII port can only be reported for an external transceiver by: - Using the MII_LINK# pin to pass the transceiver's state to the BCM53262M: - Using the CPU to read the link status via the MDC/MDIO interface and write this back to the "Page 01h: Control 1 Registers" on page 185.	0
23:0	RSVD	–	Reserved	0

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Link Status Change Register (Page 02h/Addr 18h–1Fh)

Table 94: Link Status Change Register (Page 02h: Address 18h–1Fh)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	LINK_STATUS_CHANGE[52:24]	RC	Link Status Change. A 29-bit field indicating that the Link Status for each individual 10/100Base-T port, MII, or 4 gigabit ports had changed since the last read operation. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP/MII • Bits 47:24 = 10/100 ports [port 47-port 24] Upon change of link status, a bit remains set until cleared by a read operation. • 0 = Link Status Constant • 1 = Link Status Change Link status change for the IMP/MII port can only be reported for an external transceiver by using the: • MII_LINK# pin to pass the transceiver's state to the BCM53262M. • CPU to read the link status via the MDC/MDIO interface and write this back to the "Page 01h: Control 1 Registers" on page 185.	0
23:0	RSVD	–	Reserved	0

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Port Speed Summary Register (Page 02h/Addr 20h–27h)

Table 95: Port Speed Summary Register (Page 02h: Address 20h–27h)

Bit	Name	R/W	Description	Default
63:58	RSVD	RO	Reserved Write default. Ignore on read	0
57:24	PORT_SPEED[57:24]	RO	Port Speed. Bits [57:48] field indicating the operating speed for each GigaPort and IMP/MII port. • Bits[57:56] for giga port G3. • Bits[55:54] for giga port G2. • Bits [53:52] for GigaPort G1. • Bits [51:50] for GigaPort G0. • Bits [49:48] for IMP/MII port. – 00 = 10 Mbps – 01 = 100 Mbps – 10 = 1000 Mbps Bits[47:24] field indicating the operating speed for each 10/100Base-T port • Bits 47:24 = 10/100 ports [port 47-port 24] respectively. – 0 = 10 Mbps – 1 = 100 Mbps ***Note:*** Port speed for the IMP/MII port can only be reported for an external transceiver by using the: – MII_SPD# strap to pass the transceiver's default state to the BCM53262M. – CPU to read the port speed via the MCD/MDIO interface and write this back to the "Page 01h: Control 1 Registers" on page 185.	0
23:0	RSVD	–	Reserved	0

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Duplex Status Summary Register (Page 02h/Addr 28h–2Fh)

Table 96: Duplex Status Summary Register (Page 02h: Address 28h–2Fh)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	DUPLEX_STATE[50:24]	RC	Duplex State. A 29-bit field indicating that the Duplex State for each individual 10/100Base-T port, IMP/MII, or 4-Gbit ports. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP/MII • Bits 47:24 = 10/100 ports [port 47-port 24] – 0 = Half-duplex. – 1 = Full-duplex. ***Note:*** The duplex state for the IMP/MII port can only be reported for an external transceiver by: - Using the MII_DUPLX# strap option to pass the transceiver's default state to the BCM53262M. - Using the CPU to read the half/full-duplex state via the MDC/MDIO interface and write this back to the "Page 01h: Control 1 Registers" on page 185.	0
23:0	RSVD	–	Reserved	0

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Pause Status Summary Register (Page 02h/Addr 30h–37h)

Table 97: Pause Status Summary Register (Page 02h: Address 30h–37h)

Bit	Name	R/W	Description	Default
63:58	RSVD	RO	Reserved Write default. Ignore on read	0
57:56	PAUSE_STATE_G3[1:0]	RO	Pause state for GigaPort G3. • Bit 1 = for TX. • Bit 0 = for RX.	0
55:54	PAUSE_STATE_G2[1:0]	RO	Pause state for GigaPort G2. • Bit 1 = for TX. • Bit 0 = for RX.	0
53:52	PAUSE_STATE_G1[1:0]	RO	Pause state for GigaPort G1. • Bit 1 = for TX. • Bit 0 = for RX.	0
51:50	PAUSE_STATE_G0[1:0]	RO	Pause state for GigaPort G0. • Bit 1 = for TX. • Bit 0 = for RX.	0
49:48	PAUSE_STATE_IMP	RO	Pause state for IMP port • Bit 1 = for TX. • Bit 0 = for RX. ***Note:*** The pause state for the IMP port can only be reported for an external transceiver by using the CPU to read the negotiated pause state via the MCD/MDIO interface and write this back to the Port Status Override register (page 0h, Address B9h).	0
47:24	PAUSE_STATE[23:0]	RC	Pause state. A 24-bit field indicating the PAUSE state for each 10/100Base-T port. • Bits [47:24] = 10/100 ports [port 47-port 24] respectively. • 0 = No pause. • 1 = Pause.	0
23:0	RSVD	–	Reserved	0

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Page 03h: Management Mode Registers

Table 98: Management Mode Registers (Page 03h)

Address	bits	Register Name
00h	8	"Global Management Configuration Register (Page 03h/Addr 00h)" on page 205
01h	8	"Table Memory Reset Control Register (Page 03h/Addr 01h)" on page 205

Table 98: Management Mode Registers (Page 03h)

Address	*bits*	*Register Name*
02h	8	“Management Port ID Register (Page 03h/Addr 02h)” on page 206
03h	Reserved	
04h–07h	32	“Reset Table Memory Register (Page 03h: Address 03h)” on page 207
08h–0Fh	64	“RMON MIB Steering Register (Page 03h/Addr 08h–0Fh)” on page 208
10h–17h	64	“Mirror Capture Control Register (Page 03h/Addr 10h–17h)” on page 209
18h–1Fh	64	“Ingress Mirror Control Register (Page 03h/Addr 18h–1Fh)” on page 210
20h–21h	16	“Ingress Mirror Divider Register (Page 03h/Addr 20h–21h)” on page 210
22h–27h	48	“Ingress Mirror MAC Address Register (Page 03h/Addr 22h–27h)” on page 211
28h–2Fh	64	“Egress Mirror Control Register (Page 03h/Addr 28h–2Fh)” on page 212
30h–31h	16	“Egress Mirror Divider Register (Page 03h/Addr 30h–31h)” on page 213
32h–37h	48	“Egress Mirror MAC Address Register (Page 03h/Addr 32h–37h)” on page 213
38h–3Fh	Reserved	
40h	8	“Special Management Control Register (Page 03h/Addr 40h)” on page 214
41h–4Fh	Reserved	
50h	8	“MIB Snapshot Control Register (Page 03h/Addr 50h)” on page 215
51h–5Fh	Reserved	
60h–67h	64	“Ingress RMON Register (Page 03h/Addr 60h–67h)” on page 216
68h–69h	16	“Egress RMON Register (Page 03h/Addr 68h–69h)” on page 217
6Ah–7Bh	Reserved	
7Ch	8	“Chip Reset Control Register (Page 03h/Addr 7Ch)” on page 217
7Dh–87h	Reserved	
88h	–	Reserved
89h–8Fh	Reserved	
–	–	Reserved
93h–EFh	Reserved	
F0h–F7h	–	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	–	SPI Status
FFh	8	Page Register

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Global Management Configuration Register (Page 03h/Addr 00h)

Table 99: Global Management Configuration Register (Page 03h: Address 00h)

Bit	Name	R/W	Description	Default
7:6	FRM_MNGT_PORT	R/W	Frame Management Port. Defines the physical port used to forward management frames directed to the switch. • 00 = No Management Port • 01 = Reserved • 10 = IMP (In-band Management Port) • 11 = Reserved These bits are ignored when SW_FWD_MODE = 0 (unmanaged) in the Switch Mode register Page 00h, Address 00h.	00
5	RSVD	RO	Reserved Write default. Ignore on read	0
4:3	IGMP_MLD_CHK	R/W	• 11 = IGMP/MLD snooping is enabled. IGMP/MLD packet is forwarded according to its original port forwarding map from DA/VID look-up in addition to IMP port. • 01 = IGMP/MLD snooping is enabled. IGMP/MLD packet is forwarded to IMP port only. • 00 = IGMP/MLD snooping is disabled.	0
2	RSVD	RO	Reserved Write default. Ignore on read	0
1	RX_BPDU_EN	R/W	Receive BPDU Enable. Enables all ports to receive BPDUs and forward to the defined Physical Management Port. Management CPU must set this bit to globally allow BPDUs to be received.	0
0	RSVD	–	Reserved	0

Table Memory Reset Control Register (Page 03h/Addr 01h)

Table 100: Table Memory Reset Control Register (Page 03h/Addr 01h)

Bit	Name	R/W	Description	Default
7:5	RSVD	R/W	Reserved	00
4	RST_MSPT	SC	Reset Multiple Spanning Tree Table Setting bit = 1 sets the table content to zero, and the bit resets to 0 when the operation is done.	0
3	RST_IPMC	SC	Reset L2 Multicast Table Setting bit = 1 sets the table content to zero, and the bit resets to 0 when the operation is done.	0

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Table 100: Table Memory Reset Control Register (Page 03h/Addr 01h)

Bit	Name	R/W	Description	Default
2	RST_VT	SC	Reset VLAN Table Setting bit = 1 sets the table content to zero, and the bit resets to 0 when the operation is done.	0
1	RST_ARL	SC	Reset ARL Table Setting bit = 1 sets the table content to zero, and the bit resets to 0 when the operation is done.	0
0	RST_MIB_CNTR	SC	Reset MIB counters Setting bit = 1 sets the table content to zero, and the bit resets to 0 when the operation is done.	0

Management Port ID Register (Page 03h/Addr 02h)

Table 101: Management Port ID Register (Page 03h: Address 02h)

Bit	Name	R/W	Description	Default
7:6	RSVD	RO	Reserved Write default. Ignore on read	0
5:0	PORT ID	R/W	Port ID where Management Port is located. This must be programmed consistent with the Frame Management Port in the Global Management Configuration register. ***Note:*** Only IMP port (Port 48 [30h]) is legal value (i.e., not to be set to any other value).	0x30

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Reset Table Memory Register (Page 03h: Address 03h)

Table 102: Reset Table Memory Register (Page 03h: Address 03h)

Bit	Name	R/W	Description	Default
7:6	RSVD	–	Reserved	0
5:0	RST_TBL_MEM	SC	When the corresponding bit is set, the table memory is reset. • Bit 5: Resets the port-based egress rate control configuration memory • Bit 4: Resets the port-based ingress rate control configuration memory • Bit 3: Resets the Flow-based VLAN table • Bit 2: Resets the Protocol-based VLAN table • Bit 1: Resets the MAC-based VLAN table • Bit 0: Resets the VLAN-based VLAN table	0

Aging Time Control Register (Page 03h/Addr 04h–07h)

Table 103: Aging Time Control Register (Page 03h: Address 04h–07h)

Bit	Name	R/W	Description	Default
31:20	RSVD	RO	Reserved Write default. Ignore on read	0
19:0	AGE_TIME	R/W	Specifies the aging time in seconds for dynamically learned address. Maximum age time is 1,048,575s. ***Note:*** While 802.1D specifies a range of values of 10–1,000,000s, this register does not enforce this range. Setting the AGE_TIME to 0 disables the aging process.	0x12C

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RMON MIB Steering Register (Page 03h/Addr 08h–0Fh)

Table 104: RMON MIB Steering Register (Page 03h: Address 08h–0Fh)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read	–
52:24	OR_RMON_RCV[52:24]	R/W	Override RMON Receive. Forces the RMON packet size “bucket” counters from the normal default of snooping on the receive side of the MAC, to the transmit side. This allows the RMON bucket counters to snoop either transmit or receive, allowing full-duplex MAC support. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

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Mirror Capture Control Register (Page 03h/Addr 10h–17h)

Table 105: Mirror Capture Control Register (Page 03h: Address 10h–17h)

Bit	Name	R/W	Description	Default
63	MIRROR_ENABLE	R/W	Global enable/disable for all mirroring on this chip. When reset, mirroring is disabled. When set, mirroring is enabled according to ingress and egress control rules, to the port designated as MIRROR_CAPTURE_PORT.	0
62	RSVD	–	Reserved	1
61:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	MIRROR_CAPTURE_PORT	R/W	Mirror Capture Port. Bit mask which identifies the single unique port which is designated as the port to which all ingress and/or egress traffic is mirrored on this chip/system. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

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Ingress Mirror Control Register (Page 03h/Addr 18h–1Fh)

Table 106: Ingress Mirror Control Register (Page 03h: Address 18h–1Fh)

Bit	Name	R/W	Description	Default
63:62	IN_MIRROR_FILTER	R/W	Ingress Mirror Filter. Defines conditions under which frames received on a port that has been selected in the IN_MRROR_MASK[52:24], is compared to in order to determine if they should be forwarded to the MIRROR_CAPTURE_PORT. • 00 = Mirror all ingress frames • 01 = Mirror all received frames with DA = IN_MIRROR_MAC • 10 = Mirror all received frames with SA = IN_MIRROR_MAC • 11 = Reserved.	0
61	IN_DIV_EN	R/W	Ingress Divider Enable. Mirror every n^{th} received frame (n=IN_MIRROR_DIV, defined in Register Page 03h, Address 20h) that has passed through the IN_MIRROR_FILTER.	0
60:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	IN_MIRROR_MASK[52:24]	R/W	Ingress Mirror Port Mask. A 29-bit mask which selectively allows any port with its corresponding bit set, to be mirrored to the port identified by the MIRROR_CAPTURE_PORT value. ***Note:*** While multiple bits in a device may be set, severe congestion and/or frame loss may occur if excessive bandwidth from the mirrored port(s) is directed to the MIRROR_CAPTURE_PORT. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

Ingress Mirror Divider Register (Page 03h/Addr 20h–21h)

Table 107: Ingress Mirror Divider Register (Page 03h: Address 20h–21h)

Bit	Name	R/W	Description	Default
15:10	RSVD	RO	Reserved Write default. Ignore on read	0

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Table 107: Ingress Mirror Divider Register (Page 03h: Address 20h–21h)

Bit	Name	R/W	Description	Default
9:0	IN_MIRROR_DIV	R/W	Ingress Mirror Divider. Receive frames that have passed the IN_MIRROR_FILTER rule can further reduce the overall number of frames forwarded to the MIRROR_CAPTURE_PORT to avoid the congestion. When the IN_DIV_EN bit in the Ingress Mirror Control register is set, only one in n frames is mirrored. ***Note:*** Where n = IN_MIRROR_DIV and n must not be set to 0.	0

Ingress Mirror MAC Address Register (Page 03h/Addr 22h–27h)

Table 108: Ingress Mirror MAC Address Register (Page 03h: Address 22h–27h)

Bit	Name	R/W	Description	Default
47:0	IN_MIRROR_MAC	R/W	Ingress Mirror MAC Address. MAC address that is compared against ingress frames in accordance with the IN_MIRROR_FILTER rules in Register Page 03h, Address 18h.	0

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Egress Mirror Control Register (Page 03h/Addr 28h–2Fh)

Table 109: Egress Mirror Control Register (Page 03h: Address 28h–2Fh)

Bit	Name	R/W	Description	Default
63:62	OUT_MIRROR_FILTER	R/W	Egress Mirror Filter. Defines the type of Egress frames to be mirrored. • 00: Mirror all egress frames • 01: Mirror all transmitted frames with DA = OUT_MIROR_MAC • 10: Mirror all transmitted frames with SA = OUT_MIRROR_MAC • 11: Reserved.	0
61	OUT_DIV_EN	R/W	Egress Divider Enable. Mirror every nth transmitted frame (n=OUT_MIRROR_DIV) that has passed through the OUT_MIRROR_FILTER.	0
60:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	OUT_MIRROR_MASK[52:24]	R/W	Egress Mirror Port Mask is to select the port(s) Egress traffic be forwarded to the MIRROR_CAPTURE_PORT. A 29-bit mask which selectively allows any port with its corresponding bit set, to be mirrored to the port identified by the MIRROR_CAPTURE_PORT value. ***Note:*** While multiple bits in a device may be set, severe congestion and/or frame loss may occur if excessive bandwidth from the mirrored port(s) is directed to the MIRROR_CAPTURE_PORT. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	–

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Egress Mirror Divider Register (Page 03h/Addr 30h–31h)

Table 110: Egress Mirror Divider Register (Page 03h: Address 30h–31h)

Bit	Name	R/W	Description	Default
15:10	RSVD	RO	Reserved Write default. Ignore on read	0
9:0	OUT_MIRROR_DIV	R/W	Egress Mirror Divider. Transmit frames that have passed the OUT_MIRROR_FILTER rule can further reduced the overall number of frames forwarded to the MIRROR_CAPTURE_PORT to avoid the congestion. When the OUT_DIV_EN bit in the Egress Mirror Control register is set, only one in n frames is mirrored. ***Note:*** Where n = OUT_MIRROR_DIV and n must not be set to 0.	0

Egress Mirror MAC Address Register (Page 03h/Addr 32h–37h)

Table 111: Egress Mirror MAC Address Register (Page 03h: Address 32h–37h)

Bit	Name	R/W	Description	Default
47:0	OUT_MIRROR_MAC	R/W	Egress Mirror MAC Address. MAC address that is compared against egress frames in accordance with the OUT_MIRROR_FILTER rules.	0

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Special Management Control Register (Page 03h/Addr 40h)

Table 112: Special Management Control Register (Page 03h: Address 40h)

Bit	Name	R/W	Description	Default
7:6	RSVD	–	Reserved	10
5	EN_ARP_CONTROL	R/W	ARP Frame Control. • 0 = ARP frames are flooded in the defined VLAN domain, but are not forwarded to IMP if the IMP does not belong to the same VLAN. • 1 = ARP frames are flooded in the defined VLAN domain and also copied to the IMP even if the IMP is not part of the same VLAN group.	0
4	BYPASS_SPT_CHK	R/W	When this bit is set, incoming packet with DA= 01-80-c2-00-00-00 ~ 01-80-c2-00-00-10 bypasses spanning tree state checking.	0
3	En_ALL_Zero_DA_Drop	R/W	Drop All 0 MAC DA Frame Control. When set, any frame with MAC DA = 00:00:00:00:00:00 is dropped otherwise it is forwarded as is.	0
2	RSVD	R/W	Write as default. Ignore on read.	0
1	PASS_ARP_DHCP	R/W	Enable to Pass ARP and DHCP frames. When management mode is enabled, and if bit 2, RX_BCST_EN (Page 01h/Addr A0h) is disabled, set this bit to 1 to allow the receiving of ARP and DHCP packets.	0
0	PASS_BPDU/Rsvd-MCAST	R/W	Enable to Pass BPDU and Reserved Multicast Frames. Setting this bit allows any port in spanning tree Disable state to forward BPDU and reserved multicast frames within range 01:80:C2:00:00:02 through 01:80:C2:00:00:0F to the IMP port.	0

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MIB Snapshot Control Register (Page 03h/Addr 50h)

Table 113: MIB Snapshot Control Register (Page 03h: Address 50h)

Bit	Name	R/W	Description	Default
7	SNAPSHOT_START/DONE	R/W (SC)	Snapshot Start/Done Command. When enabled, this bit is self clear to indicate that the process is completed and the snapshot is ready at Table : "Page 85h: Snapshot Port MIB Registers," on page 338. • 1 = Initiate MIB Snapshot function. • 0 = Snapshot function completed.	0
6	SNAPSHOT_MIRROR	RO	1 = enable read address to port MIB from MIB snapshot memory 0 = enable to read from port MIB memory	0
5:0	SNAPSHOT_PORT	RO	MIB Snapshot Port Number. These bits specify the port number to snapshot. • 52 = Giga Port G3 • 51 = Giga Port G2 • 50 = GigaPort G1 • 49 = GigaPort G0 • 48 = IMP • 24 ~ 47 = 10/100 ports [port 24-port 47] • 0 ~ 23 = Reserved	0

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Ingress RMON Register (Page 03h/Addr 60h–67h)

Table 114: Ingress RMON Register (Page 03h: Address 60h–67h)

Bit	Name	R/W	Description	Default
63:60	INGRESS_CFG	R/W	Ingress RMON Setting. An exponential value indicating the percentage of traffic that is forwarded to CPU due to Ingress Extended RMON. Percentage = $1/(2^{\wedge INGRESS_CFG})$	Fh
59:58	INGRESS_PRI	R/W	Ingress RMON Priority Define which priority queue to use for Ingress Extended RMON. • 11 = Queue 3 • 10 = Queue 2 • 01 = Queue 1 • 00 = Queue 0	0
57:53	RSVD	RO	Reserved Write default. Ignore on read	0
52:24	EN_INGRESS_PORTMAP	R/W	Ingress RMON Enabled Port Map. A 29-bit mask which selectively allows any port with its corresponding bit set, to enable Ingress Extended RMON. ***Note:*** Bit 48 is reserved and must be set to 0. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = Reserved. Must be 0. • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

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Egress RMON Register (Page 03h/Addr 68h–69h)

Table 115: Egress RMON Register (Page 03h: Address 68h–69h)

Bit	Name	R/W	Description	Default
15:12	EGRESS_CFG	R/W	Egress RMON Setting. An exponential value indicating the percentage of traffic that is forwarded to CPU due to Ingress Extended RMON. Percentage = $1/(2^{\wedge EGRESS_CFG})$	Fh
11:10	EGRESS_PRI	R/W	Egress RMON Priority Define which priority queue to use for Egress Extended RMON. • 11 = Queue 3 • 10 = Queue 2 • 01 = Queue 1 • 00 = Queue 0	0
9:7	RSVD	RO	Reserved Write default. Ignore on read	0
6	EN_EGRESS_RMON	R/W	Enable Egress RMON • 1 = Enable • 0 = Disable	0
5:0	EGRESS_RMON_PORT	R/W	Egress RMON Port. Define which port is Egress RMON Port. • 52 = GigaPort G3 • 51 = GigaPort G2 • 50 = GigaPort G1 • 49 = GigaPort G0 • 48 = IMP • 24 ~ 47 = 10/100 ports [port 24-port 47] • 0 ~ 23 = Reserved	0

Chip Reset Control Register (Page 03h/Addr 7Ch)

Table 116: Chip Reset Control Register (Page 03h: Address 7Ch)

Bit	Name	R/W	Description	Default
7:1	RSVD	RO	Reserved Write default. Ignore on read	0
0	RST_CHIP	R/W (SC)	Reset Chip. • 1 = Reset the entire chip. • 0 = Resume normal operation ***Note:*** This bit is self clear	0

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Page 04h: ARL Control Register

Table 117: ARL Control Registers (Page 04h)

Address	Bits	Register Name
00h	8	"Global ARL Configuration Register (Page 04h/Addr 00h)" on page 218
01h–03h	Reserved	
04h–09h	48	"BPDU Multicast Address Register (Page 04h/Addr 04h–09h)" on page 219
0Ah–0Fh	Reserved	
10h–15h	48	"Multiport Address 1 Register (Page 04h/Addr 10h–15h)" on page 219
16h–17h	Reserved	
18h–1Fh	64	"Multiport Vector 1 Register (Page 04h/Addr 18h–1Fh)" on page 220
20h–25h	48	"Multiport Address 2 Register (Page 04h/Addr 20h–25h)" on page 220
26h–27h	Reserved	
28h–2Fh	64	"Multiport Vector 2 Register (Page 04h/Addr 28h–2Fh)" on page 220
30h–EFh	Reserved	
F0h–F7h	–	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	–	SPI Status
FFh	8	Page Register

Global ARL Configuration Register (Page 04h/Addr 00h)

Table 118: Global ARL Configuration Register (Page 04h: Address 00h)

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	Reserved. Write default. Ignore on read.	0
4	MPORT_ADDR_EN	R/W	Multiport Address Enable. • When bit 4 is set to 1 by the host, a frame with matching DAs to the Multiport Address 1 and/or 2 registers is forwarded to the ports defined in their associated Multiport Vector 1 and/or 2 registers. • When bit 4 is set to 0 (default): A frame with matching DAs to the Multiport Address 1 and/or 2 registers is forwarded to the IMP port. This allows for support of User defined BPDU packets. ***Note:*** If only one multiport address is required, the host should write both Multiport Address/ Vector entries to the same value.	0

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Table 118: Global ARL Configuration Register (Page 04h: Address 00h)

Bit	Name	R/W	Description	Default
3:0	RSVD	RO	Reserved. Write default. Ignore on read.	0

BPDU Multicast Address Register (Page 04h/Addr 04h–09h)

Table 119: BPDU Multicast Address Register (Page 04h: Address 04h–09h)

Bit	Name	R/W	Description	Default
47:0	BPDU_MC_ADDR	R/W	BPDU Multicast Address 1. Defaults to the 802.1 defined reserved multicast address for the Bridge Group Address. Programming to an alternate value allows support of proprietary protocols in place of the normal Spanning Tree Protocol. Frames with a matching DA to this address are forwarded to the designated management port (IMP).	01-80-C2-00-00-00h

Multiport Address 1 Register (Page 04h/Addr 10h–15h)

Table 120: Multiport Address 1 Register (Page 04h: Address 10h–15h)

Bit	Name	R/W	Description	Default
47:0	MPORT_ADDR_1	R/W	Multiport Address 1. Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 1 register. Must be enabled using the MPORT_ADDR_EN bit in the Global ARL Configuration register.	00-00-00-00-00-00h

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Multiport Vector 1 Register (Page 04h/Addr 18h–1Fh)

Table 121: Multiport Vector 1 Register (Page 04h: Address 18h–1Fh)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved. Write default. Ignore on read.	0
52:24	MPORT_VCTR_1 [52:24]	R/W	**Multiport Vector 1.** A 29-bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 1 register is forwarded to each port with a bit set in the Multiport Vector 1 bit map. • Bit 52 = GigaPort G3 • Bit 51 = GigaPort G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

Multiport Address 2 Register (Page 04h/Addr 20h–25h)

Table 122: Multiport Address 2 Register (Page 04h: Address 20h–25h)

Bit	Name	R/W	Description	Default
47:0	MPORT_ADDR_2	R/W	Multiport Address 2. Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 2 register. Must be enabled using the MPORT_ADDR_EN bit in the Global ARL Configuration register.	00-00-00-00-00-00h

Multiport Vector 2 Register (Page 04h/Addr 28h–2Fh)

Table 123: Multiport Vector 2 Register (Page 04h: Address 28h–2Fh)

Bit	Name	R/W	Description	Default
63:53	Reserved	RO	Reserved. Write default. Ignore on read.	0

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Table 123: Multiport Vector 2 Register (Page 04h: Address 28h–2Fh)

Bit	Name	R/W	Description	Default
52:24	MPORT_VCTR_2 [52:24]	R/W	Multiport Vector 2. A 29-bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 2 register is forwarded to each port with a bit set in the Multiport Vector 2 bit map. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

Page 05h: ARL Access Registers

Table 124: ARL Access Registers (Page 05h)

Address	Bits	Register Name
00h	8	“ARL Read/Write Control Register (Page 05h/Addr 00h)” on page 223
01h–0Fh	Reserved	
02h–07h	48	“MAC Address Index Register (Page 05h/Addr 02h–07h)” on page 223
08h–09h	16	“VID Table Index Register (Page 05h/Addr 08h–09h)” on page 224
0Ah–0Fh	Reserved	
10h–17h	64	“ARL Entry 0 Register, for Multicast Address (Page 05h/Addr 10h–17h)” on page 225
18h–19h	64	“ARL Entry 1 Register, for Unicast Address (Page 05h/Addr 18h–1Fh)” on page 227
1Ah–1Fh	Reserved	
20h–21h	16	“VID Entry 0 Register (Page 05h/Addr 20h–21h)” on page 228
22h–27h	Reserved	
28h–2Fh	16	“VID Entry 1 Register (Page 05h/Addr 28h–29h)” on page 229
30h–37h	16	“Multitable Index Register (Page 05h/Addr 30h–31h)” on page 229
38h–3Fh	64	“Multitable Data 0 Register (Page 05h/Addr 38h–3Fh)” on page 231
40h–47h	64	“Multitable Data 1 Register (Page 05h/Addr 40h–47h)” on page 232
48h–4Fh	64	“Multitable Data 2 Register (Page 05h/Addr 48h–4Fh)” on page 235
50h	8	“ARL Search Control Register (Page 05h/Addr 50h)” on page 236
51h	Reserved	
52h–53h	16	“ARL Search Address Register (Page 05h/Addr 52h–53h)” on page 236

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Table 124: ARL Access Registers (Page 05h)

Address	Bits	Register Name
54h–5Bh	64	"ARL Search Result MAC Register (Page 05h/Addr 54h–5Bh)" on page 237
5Ch–5Dh	16	"ARL Search Result VID Register (Page 05h/Addr 5Ch–5Dh)" on page 239
5Eh–EFh	Reserved	
F0h–F7h	–	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	–	SPI Status
FFh	8	Page Register

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ARL Read/Write Control Register (Page 05h/Addr 00h)

Table 125: ARL Read/Write Control Register (Page 05h: Address 00h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/Done Command. Write as 1 to initiate a read or write command after first loading the MAC_ADDR_INDX register with the MAC address for which the ARL entry is to be read or written. The BCM53262M resets the bit to indicate that a write or read operation has completed, and data from the bin entry is available in ARL Entry.	0
6:4	Reserved	RO	Reserved. Write default. Ignore on read.	0
3:1	TBL_INDEX	R/W	Index to Tables • 111= Flow to VLAN Table • 110 = Protocol to VLAN Table • 101 = MAC to VLAN Table • 100 = VLAN to VLAN Table • 011 = Multiple Spanning Tree Table • 010 = Multicast Table • 001 = VLAN Table • 000 = ARL Table	0
0	TBL_R/W	R/W	Table Read/Write. • 1 = Read. • 0 = Write.	0

MAC Address Index Register (Page 05h/Addr 02h–07h)

Table 126: MAC Address Index Register (Page 05h: Address 02h–07h)

Bit	Name	R/W	Description	Default
47:0	MAC_ADDR_INDX	R/W	MAC Address Index. The MAC address for which status is to be read or written. By writing the 48 bit SA or DA address, and initiating a read command, the complete ARL bin location is returned in the ARL Entry location. The entry is 64 bits wide. Initiating a write command writes the contents of ARL Entry to the specified bin location and overwrites the current contents of the bin, regardless of the Valid bit status in each entry. ***Note:*** MAC_ADDR_INDX is also used as the index to the MAC to VLAN table.	00-00-00-00-00-00h

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VID Table Index Register (Page 05h/Addr 08h–09h)

Table 127: VID Table Index Register (Page 05h: Address 08h–09h)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	Reserved. Write default. Ignore on read.	0
11:0	VID_TBL_INDX	R/W	VLAN Table Index. When 802.1Q is enabled and VID_MAC Control, bits[6:5] of 802.1Q VLAN Control 0 register are asserted (Page 34h, Addr 00h), VID_TBL_INDX is used with the MAC_ADDR_INDX, defined in the MAC Address Index register, to form the hash index for which status is to be read or written.	000h

ARL Entry 0 Register, for Unicast Address (Page 05h/Addr 10h–17h)

Table 128: ARL Entry 0 Register, for Unicast Address Register (Page 05h: Address 10h–17h)

Bit	Name	R/W	Description	Default
63	VALID	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning takes place if an address location is not valid and has not been marked as static.	0
62	STATIC	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry does not take place. When cleared, the internal learning and aging process controls the validity of the entry.	0
61:60	CON[1:0]	R/W	ARL mode control. These bits select the ARL mode, which determines the forwarding decision. • 11 = Forward to destination port specified by ARL and also send to IMP. (Suggest to also set bit 62). • 10 = Drop if MAC_SA match. (Suggest to also set bit 62). • 01 = Drop if MAC_DA match. (Suggest to also set bit 62). • 00 = Normal ARL function. Forward to destination port specified by ARL.	0

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Table 128: ARL Entry 0 Register, for Unicast Address Register (Page 05h: Address 10h–17h) (Cont.)

Bit	Name	R/W	Description	Default
59	AGE0	R/W	Age Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as Static, the entry has the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
58:54	Reserved	R/W	Write as default. Ignore on read	0
53:48	PORTID[5:0]	R/W	Port Identification (for unicast address) The port number which identifies where the station with unique MACADDR is connected. • 52 = Giga Port G3 • 51 = Giga Port G2 • 50 = GigaPort G1 • 49 = GigaPort G0 • 48 = IMP • 24 ~ 47 = 10/100 ports [port 24-port 47] • 0 ~ 23 = Reserved	0
47:0	MACADDR	R/W	MAC Address	0

ARL Entry 0 Register, for Multicast Address (Page 05h/Addr 10h–17h)

Table 129: ARL Entry, for Multicast Address Register (Page 05h: Address 10h–17h)

Bit	Name	R/W	Description	Default
63	VALID	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management\processor has invalidated the entry. Automatic learning takes place if an address location is not valid and has not been marked as static.	0
62	STATIC	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry does not take place. When cleared, the internal learning and aging process controls the validity of the entry.	0

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Table 129: ARL Entry, for Multicast Address Register (Page 05h: Address 10h–17h) (Cont.)

Bit	Name	R/W	Description	Default
61:60	CON[1:0]	R/W	ARL mode control. These bits select the ARL mode, which determines the forwarding decision. • 11 = Forward to destination port specified by ARL and also send to IMP. (Suggest to also set bit 62). • 10 = Drop if MAC_SA match. (Suggest to also set bit 62). • 01 = Drop if MAC_DA match. (Suggest to also set bit 62). • 00 = Normal ARL function. Forward to destination port specified by ARL.	0
59:48	MC_Index 0	R/W	Multicast Index 0 12-bit index to 4K entry Multicast Vector table.	0
47:0	MACADDR	R/W	MAC Address	0

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ARL Entry 1 Register, for Unicast Address (Page 05h/Addr 18h–1Fh)

Table 130: ARL Entry Register, for Unicast Address (Page 05h: Address 18h–1Fh)

Bit	Name	R/W	Description	Default
63	VALID	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning takes place if an address location is not valid and has not been marked as static.	0
62	STATIC	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry does not take place. When cleared, the internal learning and aging process controls the validity of the entry.	0
61:60	CON[1:0]	R/W	ARL mode control. These bits select the ARL mode, which determines the forwarding decision. • 11 = Forward to destination port specified by ARL and also send to IMP. (Suggest to also set bit 62). • 10 = Drop if MAC_SA match. (Suggest to also set bit 62). • 01 = Drop if MAC_DA match. (Suggest to also set bit 62). • 00 = Normal ARL function. Forward to destination port specified by ARL.	0
59	AGE0	R/W	Age. Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as Static, the entry has the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
58:54	Reserved	R/W	Write as default. Ignore on read	0
53:48	PORTID[5:0]	R/W	Port Identification. The port number which identifies where the station with unique MACADDR is connected. • 52 = Giga Port G3 • 51 = Giga Port G2 • 50 = GigaPort G1 • 49 = GigaPort G0 • 24 ~ 47 = 10/100 ports [port 24-port 47] • 0 ~ 23 = Reserved	0
47:0	MACADDR	R/W	MAC Address.	0

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ARL Entry 1 Register, for Multicast Address (Page 05h/Addr 18h–1Fh)

Table 131: ARL Entry Register, for Multicast Address (Page 05h: Address 18h–1Fh)

Bit	Name	R/W	Description	Default
63	VALID	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning takes place if an address location is not valid and has not been marked as static.	0
62	STATIC	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry does not take place. When cleared, the internal learning and aging process controls the validity of the entry.	0
61:60	CON[1:0]	R/W	ARL mode control. These bits select the ARL mode, which determines the forwarding decision. • 11 = Forward to destination port specified by ARL and also send to IMP. (Suggest to also set bit 62). • 10 = Drop if MAC_SA match. (Suggest to also set bit 62). • 01 = Drop if MAC_DA match. (Suggest to also set bit 62). • 00 = Normal ARL function. Forward to destination port specified by ARL.	0
59:48	MC_Index 1	R/W	Multicast Index 1 12-bit index to 4K entry Multicast Vector table.	0
47:0	MACADDR	R/W	MAC Address.	0

VID Entry 0 Register (Page 05h/Addr 20h–21h)

Table 132: VID Entry Register (Page 05h: Address 20h–21h)

Bit	Name	R/W	Description	Default
15	RSVD	RO	Reserved. Write default. Ignore on read.	0
14:12	USER_DEF	RO	User Defined Field These are user defined bits. These bits are also written into the ARL table along with ARL_VID_ENTRY.	0
11:0	ARL_VID_Entry	R/W	ARL VID Entry. The VID field to be either read from or written to the ARL table entry. The VID is a don't-care field when 802.1Q is disabled.	0

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VID Entry 1 Register (Page 05h/Addr 28h–29h)

Table 133: VID Entry Register (Page 05h: Address 28h–29h)

Bit	Name	R/W	Description	Default
15	RSVD	RO	Reserved. Write default. Ignore on read.	0
14:12	USER_DEF	RO	User Defined Field These are user defined bits. These bits are also written into the ARL table along with ARL_VID_ENTRY.	0
11:0	ARL_VID_Entry	R/W	ARL VID Entry. The VID field to be either read from or written to the ARL table entry. The VID is a don't-care field when 802.1Q is disabled.	0

Multitable Index Register (Page 05h/Addr 30h–31h)

Table 134: Multitable Index Register (Page 05h: Address 30h–31h)

Bit	Name	R/W	Description	Default
15:12	RSVD	RO	Reserved. Write default. Ignore on read.	0

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Table 134: Multitable Index Register (Page 05h: Address 30h–31h)

Bit	Name	R/W	Description	Default
11:0	MULTI_TBL_INDEX	R/W	Multitable Index. When TBL_INDEX, bits[3:1] of "ARL Read/Write Control Register (Page 05h/Addr 00h)" on page 223) are set. • 111 = Access to Flow to VLAN Table: – MULTI_TBL_INDEX[11:9] is ignored and should be zero. – MULTI_TBL_INDEX[8:0] is then used as the Flow to VLAN Table index and consisted of NEW_FLOW_INDX (4 bits) + Egress Port ID (5 bits). NEW_FLOW_INDX is defined as bits[28:25] in "CFP Action Policy Data Register (Page 20h/Addr 70h–75h)" on page 263). • 110 = Access to Protocol to VLAN Table: – MULTI_TBL_INDEX[11:4] is ignored and should be zero. – MULTI_TBL_INDEX[3:0] is then used as the Protocol to VLAN Table index. • 101 = Access to MAC to VLAN Table: – MULTI_TBL_INDEX[11:0] is reserved and should be ignored. • 100 = Access to VLAN to VLAN Table: – MULTI_TBL_INDEX[11:0] is then used as the VLAN to VLAN Table index. ***Note:*** MULTI_TBL_INDEX[11:0] is defined as the VID embedded in the ingress packet. • 011 = Access to Multiple Spanning Tree Table: – MULTI_TBL_INDEX[11:8] is ignored and should be zero. – MULTI_TBL_INDEX[7:0] is then used as the Multiple Spanning Tree Table index. • 010 = Access to Multicast Table: – MULTI_TBL_INDEX[11:0] is then used as the Multicast Table index. • 001 = Access to VLAN Table: – MULTI_TBL_INDEX[11:0] is then used as the VLAN Table index. • 000 = Access to ARL Table: – MULTI_TBL_INDEX[11:0] is then used as the ARL Table index.	0

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Multitable Data 0 Register (Page 05h/Addr 38h–3Fh)

Table 135: Multitable Data 0 Register (Page 05h: Address 38h–3Fh)

Bit	Name	R/W	Description	Default
63:0	TBL_DATA_0	R/W	When Flow to VLAN Table is accessed, • TBL_DATA_0 [63:12] : reserved • TBL_DATA_0 [11:0] : VID When Protocol to VLAN Table is accessed, • TBL_DATA_0 [63:32]: reserved • TBL_DATA_0 [31]: Valid • TBL_DATA_0 [30:28]: Priority for Protocol base. • TBL_DATA_0 [27:16]: VID • TBL_DATA_0 [15:0]: Ether Type When MAC to VLAN Table is accessed, • TBL_DATA_0 [63]: Valid_0 • TBL_DATA_0 [62:60]: PRI_0, Priority for MAC SA base • TBL_DATA_0 [59:48]: VID_0 • TBL_DATA_0 [47:0]: MAC address When VLAN to VLAN Table is accessed, • TBL_DATA_0 [63:13]: reserved • TBL_DATA_0 [12]: • 1: mapping mode • 0: transparent mode • TBL_DATA_0 [11:0]: New VID When Multiple Spanning Tree Table is accessed, • TBL_DATA_0 [63:0]: reserved When Multicast Table is accessed, • TBL_DATA_0 [63:53]: reserved • TBL_DATA_0 [52:24]: Multicast Forwarding vector • TBL_DATA_0 [23:0]: reserved When VLAN Table is accessed, • TBL_DATA_0 [63:53]: reserved • TBL_DATA_0 [52:24]: VLAN Table Forwarding vector • TBL_DATA_0 [23:0]: reserved	0

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Multitable Data 1 Register (Page 05h/Addr 40h–47h)

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Table 136: Multitable Data 1 Register (Page 05h: Address 40h–47h)

Bit	Name	R/W	Description	Default
63:0	TBL_DATA_1	R/W	When Flow to VLAN Table is accessed, • TBL_DATA_1 [63:0]: reserved When Protocol to VLAN Table is accessed, • TBL_DATA_1 [63:0]: reserved When MAC to VLAN Table is accessed, • TBL_DATA_1 [63]: Valid_1 • TBL_DATA_1 [62:60]: PRI_1, Priority for MAC base (SA) • TBL_DATA_1 [59:48]: VID_1 • TBL_DATA_1 [47:0]: MAC-1, MAC address When VLAN to VLAN Table is accessed, • TBL_DATA_1 [63:0]: reserved When Multiple Spanning Tree Table is accessed, • TBL_DATA_1 [63:60]: reserved • TBL_DATA_1 [59:57]: Multiple Spanning tree state for port 39 • TBL_DATA_1 [56:54]: Multiple Spanning tree state for port 38 • TBL_DATA_1 [53:51]: Multiple Spanning tree state for port 37 • ..... • TBL_DATA_1 [17:15]: Multiple Spanning tree state for port 25 • TBL_DATA_1 [14:12]: Multiple Spanning tree state for port 24 ***Note:*** TBL_DATA [3bits] – 000 = no spanning tree – 001 = disable state – 010 = blocking state – 011 = listening state – 000 = learning state – 101 = forwarding state – 110,111 = reserved When Multicast Table is accessed, • TBL_DATA_1 [63:0]: reserved When VLAN Table is accessed, • TBL_DATA_1 [63:53]: reserved • TBL_DATA_1 [52:24]: VLAN Table Untag vector • TBL_DATA_1 [23:0]: reserved	0

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Multitable Data 2 Register (Page 05h/Addr 48h–4Fh)

Table 137: Multitable Data 2 Register (Page 05h: Address 48h–4Fh)

Bit	Name	R/W	Description	Default
63:0	TBL_DATA_2	R/W	When Flow to VLAN Table is accessed, • TBL_DATA_2 [63:0]: reserved When Protocol to VLAN Table is accessed, • TBL_DATA_2 [63:0]: reserved When MAC to VLAN Table is accessed, • TBL_DATA_2 [63:0]: reserved When VLAN to VLAN Table is accessed, • TBL_DATA_2 [63:0]: reserved When Multiple Spanning Tree Table is accessed, • TBL_DATA_2 [63:39]: reserved • TBL_DATA_2 [38:36]: Multiple Spanning tree state for port 52 • TBL_DATA_2 [35:33]: Multiple Spanning tree state for port 51 • ..... • TBL_DATA_2 [2:0]: Multiple Spanning tree state for port 40 ***Note:*** TBL_DATA[3bits] – 000 = no spanning tree – 001 = disable state – 010 = blocking state – 011 = listening state – 000 = learning state – 101 = forwarding state – 110,111 = reserved When Multicast Table is accessed: • TBL_DATA_2 [63:0]: reserved When VLAN Table is accessed: • TBL_DATA_2 [63:9]: reserved • TBL_DATA_2 [8]: disable the learning process for packet that matches this VLAN • TBL_DATA_2 [7:0]: VLAN Table Spanning ID is for mapping to the MSTP table	0

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ARL Search Control Register (Page 05h/Addr 50h)

Table 138: ARL Search Control Register (Page 05h: Address 50h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/Done Command. Write as 1 to initiate a sequential search of the ARL entries, returning each entry that is currently occupied (Valid = 1 and AGE = 0) in the ARL Search Result register. Reading the ARL Search Result register causes the ARL search to continue. The BCM53262M clears this bit to indicate the entire ARL entry database has been searched.	0
6:1	RSVD	RO	Reserved. Write default. Ignore on read.	0
0	ARL_SR_VALID	RC	ARL Search Result Valid. Set by the BCM53262M to indicate that an ARL entry is available in the ARL Search Result register. Reset by a host read to the ARL Search Result register, which causes the ARL search process to continue through the ARL entries until the next entry is found with a Valid bit is set.	0

ARL Search Address Register (Page 05h/Addr 52h–53h)

Table 139: ARL Search Address Register (Page 05h: Address 52h–53h)

Bit	Name	R/W	Description	Default
15	ARL_ADDR_VALID	R/W (SC)	ARL Address Valid. Indicates the lower 15 bits of this register contain a valid internal representation of the ARL entry currently being accessed.	0
14:13	RSVD	RO	Reserved. Write default. Ignore on read.	0
12:0	ARL_ADDR	R/W	ARL Address. 15-bit internal representation of the address of the ARL entry currently being accessed by the ARL search routine. This is not a direct address of the ARL location.	0

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ARL Search Result MAC Register (Page 05h/Addr 54h–5Bh)

Table 140: ARL Search Result Register (Page 05h: Address 54h–5Bh)

Bit	Name	R/W	Description	Default
63	VALID	RO	Valid. Set to indicate that a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. All entries returned by the ARL Search process has the VALID bit set.	0
62	STATIC	RO	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry does not take place. When cleared, the internal learning and aging process controls the validity of the entry. All entries with STATIC bit set are returned by the ARL Search process.	0
61:60	CON[1:0]	RO	ARL mode control. These bits select the ARL mode, which determines the forwarding decision. • 11 = Forward to destination port specified by ARL and also send to IMP. (Suggest to also set bit 62). • 10 = Drop if MAC_SA match. (Suggest to also set bit 62). • 01 = Drop if MAC_DA match. (Suggest to also set bit 62). • 00 = Normal ARL function. Forward to destination port specified by ARL.	0
59	AGE	RO	Age. Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as Static, the entry has the AGE bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
58:54	RSVD	RO	Reserved. Write default. Ignore on read.	0
53:48	PORTID[5:0]	RO	Port Identification. The port number which identifies where the station with unique MACADDR is connected. • 52 = Giga Port G3 • 51 = Giga Port G2 • 50 = GigaPort G1 • 49 = GigaPort G0 • 48 = IMP • 24 ~ 47 = 10/100 ports [port 24-port 47] • 0 ~ 23 = Reserved	0

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Table 140: ARL Search Result Register (Page 05h: Address 54h–5Bh) (Cont.)

Bit	Name	R/W	Description	Default
47:0	MACADDR	RO	MAC Address. The unique MAC address of the station occupying this ARL entry.	0

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ARL Search Result VID Register (Page 05h/Addr 5Ch–5Dh)

Table 141: ARL Search Result VID Register (Page 05h: Address 5Ch–5Dh)

Bit	Name	R/W	Description	Default
15	RSVD	RO	Reserved. Write default. Ignore on read.	0
14:12	USER_DEF	RO	User Defined Field These are user defined bits. These bits are also written into the ARL table along with ARL_VID_ENTRY.	0
11:0	VID	RO	VID search result.	0

Note: If 802.1Q is enables, Broadcom recommends to read the ARL Search Result VID register first, then read the ARL Search Result MAC register.

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Page 0Ah: Priority Queue Control Registers

Table 142: Priority Control Registers (Page 0Ah)

Address	Bits	Description
00h-01h	16	Flow Control Diagnostic Register (PAGE 0AH/ADDR 00H-02H)
02h-05h	Reserved	
06h-07h	16	QUEUE 0 100 TX THRESHOLD CONTROL 1 REGISTER (PAGE 0AH/ADDR 06H-07H)
08h-09h	16	QUEUE 0 100 TX THRESHOLD CONTROL 2 REGISTER (PAGE 0AH/ADDR 08H-09H)
0Ah-0Dh	Reserved	
0Eh-0Fh	16	GLOBAL THRESHOLD CONTROL 1 REGISTER (PAGE 0AH/ADDR 0EH-0FH)
10h-11h	16	GLOBAL THRESHOLD CONTROL 2 REGISTER (PAGE 0AH/ADDR 10H-11H)
12h-2Fh	Reserved	
30h-31h	16	GLOBAL OPTION CONTROL REGISTER (PAGE 0AH/ADDR 30H-31H)
32h-63h	Reserved	–
64h-65h	16	QUEUE 0 TXDSC CONTROL REGISTER (PAGE 0AH/ADDR 64H-65H)
66h-69h	Reserved	
6Ah-6Bh	16	QUEUE 1 100BT THRESHOLD CONTROL 1 REGISTER (PAGE 0AH/ADDR 6AH-6BH)
6Ch-6Dh	16	QUEUE 1 100BT THRESHOLD CONTROL 2 REGISTER (PAGE 0AH/ADDR 6CH-6DH)
6Eh-71h	Reserved	–
72h-73h	16	QUEUE 1 TXDSC CONTROL REGISTER (PAGE 0AH/ADDR 72H-73H)
74h-77h	Reserved	
78h-79h	16	QUEUE 2 100TX THRESHOLD CONTROL 1 REGISTER (PAGE 0AH/ADDR 78H-79H)
7Ah-7Bh	16	QUEUE 2 100TX THRESHOLD CONTROL 2 REGISTER (PAGE 0AH/ADDR 7AH-7BH)
7Ch-7Fh	Reserved	–
80h-81h	16	QUEUE 2 TXDSC CONTROL REGISTER (PAGE 0AH/ADDR 80H-81H)
82h-85h	Reserved	–
86h-87h	16	QUEUE 3 100TX THRESHOLD CONTROL 1 REGISTER (PAGE 0AH/ADDR 86H-87H)
88h-89h	16	QUEUE 3 100TX THRESHOLD CONTROL 2 REGISTER (PAGE 0AH/ADDR 88H-89H)
8Ah-8Dh	Reserved	
8Eh-8Fh	16	QUEUE 3 TXDSC CONTROL REGISTER (PAGE 0AH/ADDR 8EH-8FH)
90h-93h	Reserved	
94h-95h	16	DLF THRESHOLD DROP REGISTER (PAGE 0AH/ADDR 94H-95H)

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Table 142: Priority Control Registers (Page 0Ah) (Cont.)

Address	*Bits*	*Description*
96h-97h	16	BROADCAST THRESHOLD DROP REGISTER (PAGE 0AH/ADDR 96H-97H)
98h-9Fh	Reserved	–
A0h-A1h	16	LAN TO IMP UNICAST CONTROL REGISTER (PAGE 0AH/ADDR A0H-A1H)
A2h-A3h	16	LAN TO IMP MULTICAST CONTROL 1 REGISTER (PAGE 0AH/ADDR A2H-A3H)
A4h-A5h	16	LAN TO IMP MULTICAST CONTROL 2 REGISTER (PAGE 0AH/ADDR A4H-A5H)
A6h-AFh	Reserved	–
B0h-B1h	16	IMP TO LAN CONTROL 1 REGISTER (PAGE 0AH/ADDR B0H-B1H)
B2h-B3h	16	IMP TO LAN CONTROL 2 REGISTER (PAGE 0AH/ADDR B2H-B3H)
B4h-BFh	Reserved	–
C0h-C1h	16	QUEUE 1 TOTAL THRESHOLD CONTROL 1 REGISTER (PAGE 0AH/ADDR C0H-C1H)
C2h-C3h	16	QUEUE 1 TOTAL THRESHOLD CONTROL 2 REGISTER (PAGE 0AH/ADDR C2H-C3H)
C4h-C5h	16	QUEUE 2 TOTAL THRESHOLD CONTROL 1 REGISTER (PAGE 0AH/ADDR C4H-C5H)
C6h-C7h	16	QUEUE 2 TOTAL THRESHOLD CONTROL 2 REGISTER (PAGE 0AH/ADDR C6H-C7H)
C8h-C9h	16	QUEUE 3 TOTAL THRESHOLD CONTROL 1 REGISTER (PAGE 0AH/ADDR C8H-C9H)
CAh-CBh	16	QUEUE 3 TOTAL THRESHOLD CONTROL 2 REGISTER (PAGE 0AH/ADDR CAH-CBH)
CCh-CFh	Reserved	–
D0h-D1h	16	QUEUE 1 TOTAL BC/DLF DROP THRESHOLD CONTROL REGISTER (PAGE 0AH/ ADDR D0HD1H
D2h-D3h	16	QUEUE 2 TOTAL BC/DLF DROP THRESHOLD CONTROL REGISTER (PAGE 0AH/ ADDR D2HD3H)
D4h-D5h	16	QUEUE 3 TOTAL BC/DLF DROP THRESHOLD CONTROL REGISTER (PAGE 0AH/ ADDR D4HD5H)

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Flow Control Diagnostic Register (Page 0Ah/Addr 00h–01h)

Table 143: Flow Control Diagnostic Register (Page 0Ah: Address 00h–01h)

Bit	Name	R/W	Description	Default
15:14	RSVD	RO	Reserved. Write default. Ignore on read.	0
13:12	DIAG_HIST_SEL	R/W	Select which histogram value to report.	0
11:8	DIAG_TXQ_SEL	R/W	Select which Tx Queue to be monitored.	0
7:6	FC_PRI-Q_SEL	R/W	• 11 = Highest Queue • 10 = 2nd Queue • 01 = 1st Queue • 00 = Lowest Queue	0
5:0	DIAG_FC_PORT	R/W	Diagnose Port Flow Control. These bits select which port to monitor. • 52 = Port number for GigaPort G3 • 51 = Port number for GigaPort G2 • 50 = Port number for GigaPort G1 • 49 = Port number for GigaPort G0 • 48 = Port number for IMP • 24 ~ 47 = Port numbers for 10/100 ports [port 24-port 47]	0x18

Queue 0 100 TX Threshold Control 1 Register (Page 0Ah/Addr 06h–07h)

Table 144: Queue 0 100 Tx Threshold Control 1 Register (Page 0Ah: Address 06h–07h)

Bit	Name	R/W	Description	Default
15:8	Q0_BT100_HYST_THRS	RO	Q0 Unpause Threshold Regulates the transmission of the TXQ based flow control unpause frame. Under mixed-speed mode, when Q0 reaches the pause condition and the number of pointers queued up in the corresponding TXQ (Q0) drops below this threshold, an unpause frame is dispatched. The effective threshold is the default value multiplied by 8.	13h
7:0	Q0_BT100_PAUS_THRS	R/W	Q0 Pause Threshold Regulates the transmission of the TXQ based flow control pause frame. Under mixed-speed mode, when the number of pointers queued up in the corresponding TXQ (Q0) exceeds this threshold, a pause frame is dispatched. The effective threshold is the default value multiplied by 8.	1Ch

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Table 144: Queue 0 100 Tx Threshold Control 1 Register (Page 0Ah: Address 06h–07h)

Bit	Name	R/W	Description	Default
Note: When QoS is disabled, this register is ignored.				

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Queue 0 100 TX Threshold Control 2 Register (Page 0Ah/Addr 08h–09h)

Table 145: Queue 0 100 Tx Threshold Control 2 Register (Page 0Ah: Address 08-09h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	Q0_BT100_DROP_THRS	RO	Q0 Unicast Drop Threshold Regulates incoming unicast frames. Under mixed-speed mode, when the number of pointers queued up in the corresponding TXQ (Q0) exceeds this threshold, all incoming unicast frames will be dropped. The effective threshold is the default value multiplied by 8.	9Fh	98
7:0	Q0_BT100_DROP_THRS	R/W	Q0 Multicast Drop Threshold Regulates incoming multicast frames. Under mixed-speed mode, when the number of pointers queued up in the corresponding TXQ (Q0) exceeds this threshold, all incoming multicast frames will be dropped. The effective threshold is the default value multiplied by 8.	9Fh	73

Note: When QoS is disabled, this register is ignored.

Global Threshold Control 1 Register (Page 0Ah/Addr 0Eh–0Fh)

Table 146: Global Threshold Control 1 Register (Page 0Ah: Address 0E-0Fh)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	FC_GLBL_HYST_THRS	RO	Flow Control Global Unpause Threshold Regulates the global transmission of the TXQ based flow control unpause frame. When the BCM53262M is in a pause condition, and the number of pointers queued up in all the corresponding TXQs drops below this threshold, an unpause frame is dispatched. The effective threshold is the default value multiplied by 8.	61h	44

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Table 146: Global Threshold Control 1 Register (Page 0Ah: Address 0E-0Fh)

Bit	Name	R/W	Description	Default	Recommended Value
7:0	FC_GLBL_PAUSE_THRD	R/W	Flow Control Global Pause Threshold Regulates the global transmission of the TXQ-based flow control pause frame. When the number of pointers queued up in all the corresponding TXQs exceeds this threshold, a pause frame is dispatched. The effective threshold is the default value multiplied by 8.	85h	7E

Global Threshold Control 2 Register (Page 0Ah/Addr 10h–11h)

Table 147: Global Threshold Control 2 Register (Page 0Ah: Address 10-11h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	FC_GLBL_DROP_THRS	RO	Flow Control Unicast Global Drop Threshold Regulates global incoming unicast frames. When the total number of pointers queued up in all the corresponding TXQs exceeds this threshold, all incoming unicast frames will be dropped. The effective threshold is the default value multiplied by 8.	B2h	9B
7:0	FC_GLBL_MC_DROP_THRD	R/W	Flow Control Multicast Global Drop Threshold Regulates global incoming multicast frames. When the total number of pointers queued up in all the corresponding TXQs exceeds this threshold, all incoming multicast frames will be dropped. The effective threshold is the default value multiplied by 8.	B2h	7E

Global Option Control Register (Page 0Ah/Addr 30h–31h)

Table 148: Global Option Control Register (Page 0Ah: Address 30h–31h)

Bit	Name	R/W	Description	Default
15	RSVD	RO	Reserved Write default. Ignore on read.	0

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Table 148: Global Option Control Register (Page 0Ah: Address 30h–31h) (Cont.)

Bit	Name	R/W	Description	Default
14	EN_DLF_BC_DROP_THRS	R/W	Enable DLF/BC Drop Threshold. Enable local port individual DLF and broadcast drop threshold.	0
13:11	RSVD	RO	Reserved	0x7
10	EN_MCAST_BLANCE	R/W	Enable multicast traffic balance • 1 = use hund_pause and hund_unpause • 0 = use mcast_drop threshold	1
9:8	RSVD	RO	Reserved. Write default. Ignore on read.	0
7	AGGRESSIVE_DROP	R/W	Aggressive Drop Mode. • 1 = Enable. • 0 = Disable.	0
6:5	RSVD	RO	Reserved. Write default. Ignore on read.	0
4	Enable Multicast Drop	R/W	Enable multicast drop feature due to RX base and TX base flow control scheme.	1
3	Enable Unicast Drop	R/W	Enable unicast drop feature due to TX base flow control scheme.	1(QOS on) / 0 (QOS off)
2	Enable TXQ Pause	R/W	Enable unicast pause frame generation due to TX base flow control scheme.	1
1	Enable RX Drop	R/W	Enable unicast drop feature due to RX base flow control scheme.	0
0	Enable RX Pause	R/W	Enable unicast pause frame generation due to RX base flow control scheme.	0

Queue 0 TxDsc Control Register (Page 0Ah/Addr 64h–65h)

Table 149: Queue 0 TxDsc Control Register (Page 0Ah: Address 64h–65h)

Bit	Name	R/W	Description	Default
15:6	RSVD	RO	Reserved. Write default. Ignore on read.	0
5:0	Q0_quota_size	R/W	The round robin weight for priority queue 0.	01h

Note: Maximum Q0_quota_size allowable is 37h.

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Queue 1 100BT Threshold Control 1 Register (Page 0Ah/Addr 6Ah–6Bh)

Table 150: Queue 1 100BT Threshold Control 1 Register (Page 0Ah: Address 6Ah–6Bh)

Bit	Name	R/W	Description	Default
15:8	Q1_BT100_HYST_THRS	R/W	Q1 Unpause Threshold Regulates the transmission of the TXQ-based flow control unpause frame. Under mixed-speed mode, when Q0 reaches a pause condition, and the number of pointers queued up in the corresponding TXQ (Q1) drops below this threshold, an unpause frame is dispatched. The effective threshold is the default value multiplied by 8.	13h
7:0	Q1_BT100_PAUS_THRS	R/W	Q1 Pause Threshold Regulates the transmission of the TXQ-based flow control pause frame. Under mixed-speed mode, when the number of pointers queued up in the corresponding TXQ (Q1) exceeds this threshold, a pause frame is dispatched. The effective threshold is the default value multiplied by 8.	1Ch

Note: When QoS is disabled, this register is ignored.

Queue 1 100BT Threshold Control 2 Register (Page 0Ah/Addr 6Ch–6Dh)

Table 151: Queue 1 100BT Threshold Control 2 Register (Page 0Ah: Address 6Ch–6Dh)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	Q1_BT100_DROP_THRS	R/W	Q1 Unicast Drop Threshold Regulates incoming unicast frames. Under mixed- speed mode, when the number of pointers queued up in the corresponding TXQ (Q1) exceeds this threshold, all incoming unicast frames will be dropped. The effective threshold is the default value multiplied by 8.	9Fh	98
7:0	Q1_BT100_MCDROP_THRS	R/W	Q1 Multicast Drop Threshold Regulates incoming multicast frames. Under mixed- speed mode, when the number of pointers queued up in the corresponding TXQ (Q1) exceeds this threshold, all incoming multicast frames will be dropped. The effective threshold is the default value multiplied by 8.	9Fh	73

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Table 151: Queue 1 100BT Threshold Control 2 Register (Page 0Ah: Address 6Ch–6Dh)

Bit	Name	R/W	Description	Default	Recommended Value
Note: When QoS is disabled, this register is ignored.					

Queue 1 TxDsc Control Register (Page 0Ah/Addr 72h–73h)

Table 152: Queue 1 TxDsc Control Register (Page 0Ah: Address 72h–73h)

Bit	Name	R/W	Description	Default
15:6	RSVD	RO	Reserved. Write default. Ignore on read.	0
5:0	Q1_quota_size	R/W	The round robin weight for priority queue 0.	02h
Note: Maximum Q1_quota_size allowable is 37h.				

Queue 2 100TX Threshold Control 1 Register (Page 0Ah/Addr 78h–79h)

Table 153: Queue 2 100TX Threshold Control 1 Register (Page 0Ah: Address 78h–79h)

Bit	Name	R/W	Description	Default
15:8	Q2_BT100_HYST_THRS	R/W	Q2 Unpause Threshold Regulates the transmission of the TXQ-based flow control unpause frame. Under mixed-speed mode, when Q0 reaches a pause condition, and the number of pointers queued up in the corresponding TXQ (Q2) drops below this threshold, an unpause frame is dispatched. The effective threshold is the default value multiplied by 8.	13h
7:0	Q2_BT100_PAUS_THRS	R/W	Q2 Pause Threshold Regulates the transmission of the TXQ-based flow control pause frame. Under mixed-speed mode, when the number of pointers queued up in the corresponding TXQ (Q2) exceeds this threshold, a pause frame is dispatched. The effective threshold is the default value multiplied by 8.	1Ch
Note: When QoS is disabled, this register is ignored.				

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Queue 2 100TX Threshold Control 2 Register (Page 0Ah/Addr 7Ah–7Bh)

Table 154: Queue 2 100TX Threshold Control 2 Register (Page 0Ah: Address 7Ah–7Bh)

Bit	Name	R/W	Description	Default	Recommend Value
15:8	Q2_BT100_DROP_THRS	R/W	Q2 Unicast Drop Threshold Regulates incoming unicast frames. Under mixed- speed mode, when the number of pointers queued up in the corresponding TXQ (Q2) exceeds this threshold, all incoming unicast frames will be dropped. The effective threshold is the default value multiplied by 8.	9Fh	98
7:0	Q2_BT100_MCDROP_THRS	R/W	Q2 Multicast Drop Threshold Regulates incoming multicast frames. Under mixed- speed mode, when the number of pointers queued up in the corresponding TXQ (Q2) exceeds this threshold, all incoming multicast frames will be dropped. The effective threshold is the default value multiplied by 8.	9Fh	73

Note: When QoS is disabled, this register is ignored.

Queue 2 TxDsc Control Register (Page 0Ah/Addr 80h–81h)

Table 155: Queue 2 TxDsc Control Register (Page 0Ah: Address 80h–81h)

Bit	Name	R/W	Description	Default
15:6	RSVD	RO	Reserved. Write default. Ignore on read.	0
5:0	Q2_quota_size	R/W	The round robin weight for priority queue 0.	04h

Note: Maximum Q2_quota_size allowable is 37h.

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Queue 3 100TX Threshold Control 1 Register (Page 0Ah/Addr 86h–87h)

Table 156: Queue 3 100TX Threshold Control 1 Register (Page 0Ah: Address 86h–87h)

Bit	Name	R/W	Description	Default
15:8	Q3_BT100_HYST_THRS	R/W	Q3 Unpause Threshold Regulates the transmission of the TXQ-based flow control unpause frame. Under mixed-speed mode, when Q0 reaches a pause condition, and the number of pointers queued up in the corresponding TXQ (Q3) drops below this threshold, an unpause frame is dispatched. The effective threshold is the default value multiplied by 8.	13h
7:0	Q3_BT100_PAUS_THRS	R/W	Q3 Pause Threshold Regulates the transmission of the TXQ-based flow control pause frame. Under mixed-speed mode, when the number of pointers queued up in the corresponding TXQ (Q3) exceeds this threshold, a pause frame is dispatched. The effective threshold is the default value multiplied by 8.	1Ch

Queue 3 100TX Threshold Control 2 Register (Page 0Ah/Addr 88h–89h)

Table 157: Queue 3 100TX Threshold Control 2 Register (Page 0Ah: Address 88h–89h)

Bit	Name	R/W	Description	Default	Recommened Value
15:8	Q3_BT100_DROP_THRS	R/W	Q3 Unicast Drop Threshold Regulates incoming unicast frames. Under mixed- speed mode, when the number of pointers queued up in the corresponding TXQ (Q3) exceeds this threshold, all incoming unicast frames will be dropped. The effective threshold is the default value multiplied by 8.	9Fh	98
7:0	Q3_BT100_MCDROP_THRS	R/W	Q3 Multicast Drop Threshold Regulates incoming multicast frames. Under mixed- speed mode, when the number of pointers queued up in the corresponding TXQ (Q3) exceeds this threshold, all incoming multicast frames will be dropped. The effective threshold is the default value multiplied by 8.	9Fh	73

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Queue 3 TxDsc Control Register (Page 0Ah/Addr 8Eh–8Fh)

Table 158: Queue 3 TxDsc Control Register (Page 0Ah: Address 8Eh–8Fh)

Bit	Name	R/W	Description	Default
15:6	RSVD	RO	Reserved Write default. Ignore on read.	0
5:0	Q3_quota_size	R/W	The round robin weight for priority queue 3.	08h
Note: Maximum Q3_quota_size allowable is 37h.				

DLF Threshold Drop Register (Page 0Ah/Addr 94h–95h)

Table 159: DLF Threshold Drop Register (Page 0Ah: Address 94h–95h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	TOTAL_INDV_DLFTH_DROP	R/W	Total individual DLF drop threshold. Regulates total incoming DLF frames. When EN_DLF_BC_DROP_THRS of "Global Option Control Register (Page 0Ah/Addr 30h–31h)" on page 245 is asserted, the total incoming DLF frames exceed this threshold are dropped. The effective threshold is the default value multiplied by 8.	B2h	7E
7:0	INDV_DLFTH_DROP	R/W	Individual DLF drop threshold. Regulates individual port incoming DLF frames. When EN_DLF_BC_DROP_THRS of "Global Option Control Register (Page 0Ah/Addr 30h–31h)" on page 245 is asserted, the incoming DLF frames at individual port exceed this threshold are dropped. The effective threshold is the default value multiplied by 8.	9Fh	–

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Broadcast Threshold Drop Register (Page 0Ah/Addr 96h–97h)

Table 160: Broadcast Threshold Drop Register (Page 0Ah: Address 96h–97h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	TOTAL_INDV_BCSTTH_DROP	R/W	Total individual broadcast drop threshold. Regulates total incoming Broadcast frames. When EN_DLF_BC_DROP_THRS of "Global Option Control Register (Page 0Ah/Addr 30h–31h)" on page 245 is asserted, the total incoming Broadcast frames exceed this threshold are dropped. The effective threshold is the default value multiplied by 8.	B2h	7E
7:0	INDV_BCSTTH_DROP	R/W	Individual broadcast drop threshold. Regulates individual port incoming Broadcast frames. When EN_DLF_BC_DROP_THRS of "Global Option Control Register (Page 0Ah/Addr 30h–31h)" on page 245 is asserted, the incoming Broadcast frames at individual port exceed this threshold are dropped. The effective threshold is the default value multiplied by 8.	9Fh	–

LAN to IMP Unicast Control Register (Page 0Ah/Addr A0h–A1h)

Table 161: LAN to IMP MC Control 1 Register (Page 0Ah: Address A0h–A1h)

Bit	Name	R/W	Description	Default
15	IMP_CONGST_REMAP_EN	R/W	Remap IMP Port Congestion Status • 1 = Remap from PAUSE to DROP	0
14:0	RSVD	–	Reserved	1

LAN to IMP Multicast Control 1 Register (Page 0Ah/Addr A2h–A3h)

Table 162: LAN to IMP MC Control 1 Register (Page 0Ah: Address A2h–A3h)

Bit	Name	R/W	Description	Default
15:1	RSVD	–	Reserved	0

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Table 162: LAN to IMP MC Control 1 Register (Page 0Ah: Address A2h–A3h)

Bit	Name	R/W	Description	Default
0	MC_IMP_DROP_EN	R/W	When this bit is set, activates the MC_IMP_DROP_THRSHLD in "LAN to IMP Multicast Control 2 Register (Page 0Ah/Addr A4h–A5h)" on page 253.	0

LAN to IMP Multicast Control 2 Register (Page 0Ah/Addr A4h–A5h)

Table 163: LAN to IMP MC Control 2 Register (Page 0Ah: Address A4h–A5h)

Bit	Name	R/W	Description	Default
15:8	RSVD	RO	Reserved	0
7:0	MC_IMP_DROP_THRSHLD	R/W	Total use threshold for MC traffic from LAN to IMP.	6Ch

IMP to LAN Control 1 Register (Page 0Ah/Addr B0h–B1h)

Table 164: IMP to LAN Control 1 Register (Page 0Ah: Address B0h–B1h)

Bit	Name	R/W	Description	Default
15:1	RSVD	RO	Reserved	0
0	High_Rate_IMP_PAUSE_EN	R/W	• 1 = Remap LAN-ports congestion status observed by IMP port from Drop/Pause to Pause/Hysteresis	0

IMP to LAN Control 2 Register (Page 0Ah/Addr B2h–B3h)

Table 165: LAN to IMP MC Control 2 Register (Page 0Ah: Address B2h–B3h)

Bit	Name	R/W	Description	Default
15:8	DROP_IMP_THRSHLD	RO	If the total buffer use exceeds this threshold, the drop congestion status observed by the IMP port does not remap to pause.	BCh
7:0	PAUSE_IMP_THRSHLD	R/W	If the total buffer use exceeds this threshold, the pause congestion status observed by the IMP port does not remap to hysteresis.	AAh

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Queue 1 Total Threshold Control 1 Register (Page 0Ah/Addr C0h–C1h)

Table 166: Queue 1 Total Threshold Control 1 Register (Page 0Ah: Address C0h–C1h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	HYST_THRSHLD_Q1	RO	–	61h	46
7:0	PAUSE_THRSHLD_Q1	R/W	Total pause threshold for Q1	8Ch	80

Queue 1 Total Threshold Control 2 Register (Page 0Ah/Addr C2h–C3h)

Table 167: Queue 1 Total Threshold Control 2 Register (Page 0Ah: Address C2h–C3h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	Total_Drop_THRSHLD_Q1	R/W	Total drop threshold for Q1	B4h	9D
7:0	RSVD	RO	Reserved	0	7E

Queue 2 Total Threshold Control 1 Register (Page 0Ah/Addr C4h–C5h)

Table 168: Queue 2 Total Threshold Control 1 Register (Page 0Ah: Address C4h–C5h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	HYST_THRSHLD_Q2	RO	–	61h	48
7:0	PAUSE_THRSHLD_Q2	R/W	Total pause threshold for Q2	93h	82

Queue 2 Total Threshold Control 2 Register (Page 0Ah/Addr C6h–C7h)

Table 169: Queue 2 Total Threshold Control 2 Register (Page 0Ah: Address C6h–C7h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	Total_Drop_THRSHLD_Q2	R/W	Total drop threshold for Q2	B6h	9F
7:0	RSVD	RO	Reserved	0	7E

Queue 3 Total Threshold Control 1 Register (Page 0Ah/Addr C8h–C9h)

Table 170: Queue 3 Total Threshold Control 1 Register (Page 0Ah: Address C8h–C9h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	HYST_THRSHLD_Q3	RO	–	61h	4A

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Table 170: Queue 3 Total Threshold Control 1 Register (Page 0Ah: Address C8h–C9h)

Bit	Name	R/W	Description	Default	Recommended Value
7:0	PAUSE_THRSHLD_Q3	R/W	Total pause threshold for Q3	9Bh	84

Queue 3 Total Threshold Control 2 Register (Page 0Ah/Addr CAh–CBh)

Table 171: Queue 3 Total Threshold Control 2 Register (Page 0Ah: Address CAh–CBh)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	Total_Drop_THRSHLD_Q3	R/W	Total drop threshold for Q3	B8h	A1
7:0	RSVD	RO	Reserved	0	7E

Queue 1 Total BC/DLF Drop Threshold Control Register (Page 0Ah/Addr D0h-D1h

Table 172: Queue 1 Total BC/DLF Drop Threshold Control Register (Page 0Ah/Addr D0h-D1h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	Total_DLF_DROP_THRESH_Q1	R/W	Total DLF drop threshold for Q1	B4h	7E
7:0	TOTAL_BC_DROP_THRESH_Q1	R/W	Total BC drop threshold for Q1.	B4h	7E

Queue 2 Total BC/DLF Drop Threshold Control Register (Page 0Ah/Addr D2h-D3h)

Table 173: Queue 2 Total BC/DLF Drop Threshold Control Register (Page 0Ah/Addr D2h-D3h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	Total_DLF_DROP_THRESH_Q2	R/W	Total DLF drop threshold for Q2	B6h	7E
7:0	TOTAL_BC_DROP_THRESH_Q2	R/W	Total BC drop threshold for Q2	B6h	7E

Queue 3 Total BC/DLF Drop Threshold Control Register (Page 0Ah/Addr D4h-D5h)

Table 174: Queue 3 Total BC/DLF Drop Threshold Control Register (Page 0Ah/Addr D4h-D5h)

Bit	Name	R/W	Description	Default	Recommended Value
15:8	Total_DLF_DROP_THRESH_Q3	R/W	Total DLF drop threshold for Q3	B8h	7E

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Table 174: Queue 3 Total BC/DLF Drop Threshold Control Register (Page 0Ah/Addr D4h-D5h)

Bit	Name	R/W	Description	Default	Recommended Value
7:0	TOTAL_BC_DROP_THRESH_Q3	R/W	Total BC drop threshold for Q3	B8h	7E

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Page 10h: PHY Info Registers

Table 175: PHY Info Registers (Page 10h)

Address	Bits	Register Name
00h–03h	Reserved	
04h–05h	16	"PHY ID High Register (Page 10h/Addr 04h)" on page 257
06h–07h	16	"PHY ID Low Register (Page 10h/Addr 06h)" on page 257
08h–EFh	Reserved	
F0h–F7h	–	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	–	SPI Status
FFh	8	Page Register

PHY ID High Register (Page 10h/Addr 04h)

Table 176: PHY ID High Register (Page 10h: Address 04h)

Bit	Name	R/W	Description	Default
15:0	MII_ADDR	RO	PHYID HIGH	0143h

PHY ID Low Register (Page 10h/Addr 06h)

Table 177: PHY ID Low Register (Page 10h: Address 06h)

Bit	Name	R/W	Description	Default
15:0	MII_ADDR	RO	PHY ID LOW	BF2Nh

Where N[3:2], the upper 2 bits of the nibble denote the revision and the lower 2 bits, N[1:0] denote the stepping.

Table 178: Chip Revision

N		Revision	Stepping
00	00	A	0
	01		1
	10		2
	11		3
01	00	B	0
	01		1
	10		2
	11		3

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Table 178: Chip Revision

N		Revision	Stepping
10	00	C	0
	01		1
	10		2
	11		3
11	00	D	0
	01		1
	10		2
	11		3

Page 20h: CFP Registers

Table 179: CFP Registers (Page 20h)

Address	*Bits*	*Register Name*
00h–03h	32	“CFP Access Register (Page 20h/Addr 00h–03h)” on page 260
04h–0Fh	Reserved	
10h–17h	64	“CFP TCAM Data 0 Register (Page 20h/Addr 10h–17h)” on page 260
18h–1Fh	64	“CFP TCAM Data 1 Register (Page 20h/Addr 18h–1Fh)” on page 261
20h–27h	64	“CFP TCAM Data 2 Register (Page 20h/Addr 20h–27h)” on page 261
28h–2Fh	64	“CFP TCAM Data 3 Register (Page 20h/Addr 28h–2Fh)” on page 261
30h–37h	64	“CFP TCAM Data 4 Register (Page 20h/Addr 30h–37h)” on page 261
38h–3Fh	64	“CFP TCAM Data 5 Register (Page 20h/Addr 38h–3Fh)” on page 262
40h–47h	64	“CFP TCAM Mask 0 Register (Page 20h/Addr 40h–47h)” on page 262
48h–4Fh	64	“CFP TCAM Mask 1 Register (Page 20h/Addr 48h–4Fh)” on page 262
50h–57h	64	“CFP TCAM Mask 2 Register (Page 20h/Addr 50h–57h)” on page 262
58h–5Fh	64	“CFP TCAM Mask 3 Register (Page 20h/Addr 58h–5Fh)” on page 263
60h–67h	64	“CFP TCAM Mask 4 Register (Page 20h/Addr 60h–67h)” on page 263
68h–6Fh	64	“CFP TCAM Mask 5 Register (Page 20h/Addr 68h–6Fh)” on page 263
70h–75h	48	“CFP Action Policy Data Register (Page 20h/Addr 70h–75h)” on page 263
74h–7Fh	Reserved	
80h–83h	32	“CFP Rate Meter Configuration Register (Page 20h/Addr 80h–83h)” on page 268
88h–8Fh	Reserved	
90h–93h	32	“CFP Rate Inband Statistic Register (Page 20h/Addr 90h–93h)” on page 268
94h–97h	32	“CFP Rate Outband Statistic Register (Page 20h/Addr 94h–97h)” on page 268

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Table 179: CFP Registers (Page 20h) (Cont.)

Address	Bits	Register Name
F0h–F7h	–	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	–	SPI Status
FFh	8	Page Register

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CFP Access Register (Page 20h/Addr 00h–03h)

Table 180: CFP Access Register (Page 20h: Address 00h–03h)

Bit	Name	R/W	Description	Default
31	RATE_MTR_EN	R/W	Rate Meter Enable This bit enables the hardware for Rate Meter function. Software should set this bit after the Rate Meter Memory has been initialized.	0
30:19	RSVD	R/W	Reserved	0
18:9	ACCESS_ADDR	R/W	Indicates the address offset of the RAM blocks for the operation. For a Read and Write operation, this is the target address for the TCAM and RAM blocks.	0
8:4	MEM_SEL	R/W	RAM Selection. A single bit field selects the target of the operation. • 10000 = Out-band Statistic RAM • 01000 = In-band Statistic RAM • 00100 = Rate Meter RAM • 00010 = Action/Policy RAM • 00001 = TCAM • 00000 = No Operation • Others = Reserved	0
3:0	OP_CODE	R/W	Operation Select • 0011: Memory Fill operation.Software runs the operation to fill data to the memory assigned by MEM_SEL. • 0010: Write operation (for TCAM and RAM) • 0001: Read operation (for TCAM and RAM) • 0000: No operation • Others: Reserved	0

CFP TCAM Data 0 Register (Page 20h/Addr 10h–17h)

Table 181: CFP TCAM Data 0 Register (Page 20h: Address 10h–17h)

Bit	Name	R/W	Description	Default
63:0	TCAM_DATA0[63:0]	R/W	TCAM Data for different Opcode For Opcode = 4’b0001 • The output of TCAM data [63:0] For Opcode = 4’b0010 • The input of TCAM data [63:0]	0

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CFP TCAM Data 1 Register (Page 20h/Addr 18h–1Fh)

Table 182: CFP TCAM Data 1 Register (Page 20h: Address 18h–1Fh)

Bit	Name	R/W	Description	Default
63:0	TCAM_DATA1[127:64]	R/W	TCAM Data for different Opcode For Opcode = 4'b0001 • The output of TCAM data [127:64] For Opcode = 4'b0010 • The input of TCAM data [127:64]	0

CFP TCAM Data 2 Register (Page 20h/Addr 20h–27h)

Table 183: CFP TCAM Data 2 Register (Page 20h: Address 20h–27h)

Bit	Name	R/W	Description	Default
63:0	TCAM_DATA2[191:128]	R/W	TCAM Data for different Opcode For Opcode = 4'b0001 • The output of TCAM data [191:128] For Opcode = 4'b0010 • The input of TCAM data [191:128]	0

CFP TCAM Data 3 Register (Page 20h/Addr 28h–2Fh)

Table 184: CFP TCAM Data 3 Register (Page 20h: Address 28h–2Fh)

Bit	Name	R/W	Description	Default
63:0	TCAM_DATA3[255:192]	R/W	TCAM Data for different Opcode For Opcode = 4'b0001 • The output of TCAM data [255:192] For Opcode = 4'b0010 • The input of TCAM data [255:192]	0

CFP TCAM Data 4 Register (Page 20h/Addr 30h–37h)

Table 185: CFP TCAM Data 4 Register (Page 20h: Address 30h–37h)

Bit	Name	R/W	Description	Default
63:0	TCAM_DATA3[319:256]	R/W	TCAM Data for different Opcode For Opcode = 4'b0001 • The output of TCAM data [319:256] For Opcode = 4'b0010 • The input of TCAM data [319:256]	0

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CFP TCAM Data 5 Register (Page 20h/Addr 38h–3Fh)

Table 186: CFP TCAM Data 5 Register (Page 20h: Address 38h–3Fh)

Bit	Name	R/W	Description	Default
63:0	TCAM_DATA3[383:320]	R/W	TCAM Data for different Opcode For Opcode = 4'b0001 • The output of TCAM data [383:320] For Opcode = 4'b0010 • The input of TCAM data [383:320]	0

CFP TCAM Mask 0 Register (Page 20h/Addr 40h–47h)

Table 187: CFP TCAM Mask 0 Register (Page 20h: Address 40h–47h)

Bit	Name	R/W	Description	Default
63:0	TCAM_MASK0[63:0]	R/W	TCAM Mask for different Opcode For Opcode = 4'b0001 • The output of TCAM mask [63:0] For Opcode = 4'b0010 • The input of TCAM mask [63:0]	0

CFP TCAM Mask 1 Register (Page 20h/Addr 48h–4Fh)

Table 188: CFP TCAM Mask 1 Register (Page 20h: Address 48h–4Fh)

Bit	Name	R/W	Description	Default
63:0	TCAM_MASK1[127:64]	R/W	TCAM Mask for different Opcode For Opcode = 4'b0001 • The output of TCAM mask [127:64] For Opcode = 4'b0010 • The input of TCAM mask [127:64]	0

CFP TCAM Mask 2 Register (Page 20h/Addr 50h–57h)

Table 189: CFP TCAM Mask 2 Register (Page 20h: Address 50h–57h)

Bit	Name	R/W	Description	Default
63:0	TCAM_MASK2[191:128]	R/W	TCAM Mask for different Opcode For Opcode = 4'b0001 • The output of TCAM mask [191:128] For Opcode = 4'b0010 • The input of TCAM mask [191:128]	0

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CFP TCAM Mask 3 Register (Page 20h/Addr 58h–5Fh)

Table 190: CFP TCAM Mask 3 Register (Page 20h: Address 58h–5Fh)

Bit	Name	R/W	Description	Default
63:0	TCAM_MASK3[255:192]	R/W	TCAM Mask for different Opcode For Opcode = 4'b0001 • The output of TCAM mask [255:192] For Opcode = 4'b0010 • The input of TCAM mask [255:192]	0

CFP TCAM Mask 4 Register (Page 20h/Addr 60h–67h)

Table 191: CFP TCAM Mask 4 Register (Page 20h: Address 60h–67h)

Bit	Name	R/W	Description	Default
63:0	TCAM_MASK4[319:256]	R/W	TCAM Mask for different Opcode For Opcode = 4'b0001 • The output of TCAM mask [319:256] For Opcode = 4'b0010 • The input of TCAM mask [319:256]	0

CFP TCAM Mask 5 Register (Page 20h/Addr 68h–6Fh)

Table 192: CFP TCAM Mask 5 Register (Page 20h: Address 68h–6Fh)

Bit	Name	R/W	Description	Default
63:0	TCAM_MASK5[371:320]	R/W	TCAM Mask for different Opcode For Opcode = 4'b0001 • The output of TCAM mask [371:320] For Opcode = 4'b0010 • The input of TCAM mask [371:320]	0

CFP Action Policy Data Register (Page 20h/Addr 70h–75h)

Table 193: CFP Action Policy Data Register (Page 20h: Address 70h–75h)

Bit	Name	R/W	Description	Default
47:46	RSVD	RO	Reserved. Write default. Ignore on read.	0

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Table 193: CFP Action Policy Data Register (Page 20h: Address 70h–75h) (Cont.)

Bit	Name	R/W	Description	Default
45	CHNG_DSCP_OB	R/W	Change DSCP for Out-Band: • 1 = Replace DSCP field of the corresponding packet with New_DSCP_OB • 0 = Ignore New_DSCP_OB content for this policy	0
44:39	NEW_DSCP_OB	R/W	New DSCP value for Out-Band • The value will replace the original DSCP value if CHNG_DSCP_OB is set	0
38:37	CHNG_FWD_OB[1:0]	R/W	Change Forward Map for Out-Band • 00: No change. Forward based on ARL forward map. • 01: Use NEW_FWD_OB[5:0] as final forward map • 10: ARL forward map is ORed with NEW_FWD_OB[5:0] to get the final forward map • 11: Explicit actions (such as switching drop, copy CPU, mirror) are defined by NEW_FWD_OB[5:0]	0

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Table 193: CFP Action Policy Data Register (Page 20h: Address 70h–75h) (Cont.)

Bit	Name	R/W	Description	Default
36:31	NEW_FWD_OB[5:0]	R/W	New Destination Port Number for Out-Band. • When bits[38:37] = 01 or 10, NEW_FWD_OB[5:0] is defined as: – 0~23 = Reserved – 24 = Port 24 – ... – 47 = Port 47 – 48 = IMP – 49 = Giga Port G0 – 50 = Giga Port G1 – 51 = Giga Port G2 – 52 = Giga Port G3 – 53 ~ 62 = Reserved – 63 = Flood to all linked-up ports. • When bits[38:37] = 11, NEW_FWD_OB[5:0] defines the new actions: – 0~55 = Reserved – 56 = Forward packet based on ARL forward map – 57 = Forward packet based on ARL and copy to Mirror Capture port – 58 = Forward packet based on ARL and copy to IMP port – 59 = Forward packet based on ARL and to both IMP and Mirror Capture ports – 60 = Drop the packet – 61 = Forward packet to Mirror Capture port only – 62 = Forward packet to IMP port only – 63 = Forward packet to both IMP and Mirror Capture ports.	0
30:29	CHNG_FLOW		change flow (VID) for In/Out-Band (modify packet) • 11 = use NEW_FLOW_INDX to get VID value on Egress side to swap CVID/SPVID at UNI/NNI port. • 10 = use NEW_FLOW_INDX to get VID value on Egress side to swap SPVID at NNI port • 01 = use NEW_FLOW_INDX to get VID value on Egress side to swap CVID at UNI port • 00 = do not care NEW_FLOW_INDX content for this policy	0
28:25	NEW_FLOW_INDX		New Flow (VID) index for In/Out-Band	0

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Table 193: CFP Action Policy Data Register (Page 20h: Address 70h–75h) (Cont.)

Bit	Name	R/W	Description	Default
24	CHNG_DSCP_IB		Change DSCP for In-Band.(modify packet) • 1 = will change DSCP field of the corresponding packet • 0 = Don't care New_DSCP_IB content for this policy	0
23:18	NEW_DSCP_IB		New DSCP value for In-Band The value will replace the original DSCP value if CHNG_DSCP_IB is set	0
17	CHNG_PCP		Change 802.1p header for In/Out-Band • 1 = Replace 802.1p field of the corresponding packet with NEW_PCP • 0 = Ignore New_PCP content for this policy	0
16:14	NEW_PCP	RO	New 802.1p header for In/Out-Band This value will replace the original 802.1p tag if CHNG_PCP is set.	0
13	CHNG_QOS	R/W	Update Priority for In/Out-Band. • 1 = Replace the priority of the corresponding frame with NEW_QOS. • 0 = Ignore NEW_QOS content for this policy.	0
12:11	NEW_QOS	RO	Priority map for In/Out-Band (Ethernet port only) The priority to be changed to if CHNG_QOS is set	0
10	CHNG_QOS_IMP	R/W	Change QoS for In/Out-Band (IMP port only, do not modify packet) • 1 = Replace the priority of the corresponding frame with NEW_QOS_IMP. • 0 = Ignore NEW_QOS_IMP content for this policy.	0
9:8	NEW_QOS_IMP	R/W	Priority Map for In/Out-Band (IMP port only) The priority to be changed to if CHG_QOS_IMP is asserted.	0
7:6	CHNG_FWD_IB[1:0]	R/W	Change Forward Map for In-Band • 00: Forward based on ARL forward map with no change • 01: Use NEW_FWD_IB[5:0] as final forward map. • 10: ARL forward map is ORed with NEW_FWD_IB[5:0] to get the final forward map • 11: Explicit actions (such as switching drop, copy CPU, mirror) are defined by NEW_FWD_IB[5:0]	0

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Table 193: CFP Action Policy Data Register (Page 20h: Address 70h–75h) (Cont.)

Bit	Name	R/W	Description	Default
5:0	NEW_FWD_IB[5:0]	R/W	New Destination Port Number for In-Band. • When bits[38:37] = 01 or 10, NEW_FWD_IB[5:0] is defined as: – 0~23 = Reserved – 24 = Port 24 – ... – 47 = Port 47 – 48 = IMP – 49 = Giga Port G0 – 50 = Giga Port G1 – 51 = Giga Port G2 – 52 = Giga Port G3 – 53 ~ 62 = Reserved – 63 = Flood to all linked-up ports. • When bits[38:37] = 11, NEW_FWD_IB[5:0] defines the new actions: – 0~55 = Reserved – 56 = Forward packet based on ARL forward map – 57 = Forward packet based on ARL and copy to Mirror Capture port – 58 = Forward packet based on ARL and copy to IMP port – 59 = Forward packet based on ARL and to both IMP and Mirror Capture ports – 60 = Drop the packet – 61 = Forward packet to Mirror Capture port only – 62 = Forward packet to IMP port only – 63 = Forward packet to both IMP and Mirror Capture ports.	0

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CFP Rate Meter Configuration Register (Page 20h/Addr 80h–83h)

Table 194: CFP Rate Meter Configuration Register (Page 20h: Address 80h–83h)

Bit	Name	R/W	Description	Default
31:22	RSVD	RO	Reserved. Write default. Ignore on read.	0
21:15	BKT_SIZE	R/W	Bucket Size Unit = 8KB Bucket size = 8KB x BKT_SIZE • 000 = 0000 KB • 001 = 0008 KB • 002 = 0016 KB • ..... • 127 = 1016 KB	0
14	RFRSH_UNIT	R/W	Refresh Unit • 1 = 1 Mbps • 0 = 62.5 Kbps	0
13:0	RFRSH_CNT	R/W	Refresh count • 1: Rate = 1 Mbps x RFRSH_CNT • 0: Rate = 62.5Kbps x RFRSH_CNT	0

CFP Rate Inband Statistic Register (Page 20h/Addr 90h–93h)

Table 195: CFP Rate Inband Statistic Register (Page 20h: Address 90h–93h)

Bit	Name	R/W	Description	Default
31:0	INBAND_CNTR	R/W	Inband Counter. Data to be read from or written to the Inband rate counter.	0

CFP Rate Outband Statistic Register (Page 20h/Addr 94h–97h)

Table 196: CFP Rate Outband Statistic Register (Page 20h: Address 94h–97h)

Bit	Name	R/W	Description	Default
31:0	OUTBAND_CNTR	R/W	Outband Counter. Data to be read from or written to the Outband rate counter.	0

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Page 21h: CFP Control Registers

Table 197: CFP Control Registers (Page 21h)

Address	Bits	Register Name
00h–07h	8	“CFP Global Control Register (Page 21h/Addr 00h)” on page 270
08h–09h	8	“Range Checker Control Register (Page 21h/Addr 08h)” on page 270
0Ah–0Fh	Reserved	
10h–11h	16	“Global CFP Control1 Register (Page 21h/Addr 10h)” on page 272
20h–23h	64	“CFP Enable Control Register (Page 21h/Addr 20h–27h)” on page 272
30h–33h	32	“VID Range Checker 0 Register (Page 21h/Addr 30h)” on page 272
34h–37h	32	“VID Range Checker 1 Register (Page 21h/Addr 34h)” on page 272
38h–3Bh	32	“VID Range Checker 2 Register (Page 21h/Addr 38h)” on page 273
3Ch–3Fh	32	“VID Range Checker 3 Register (Page 21h/Addr 3Ch)” on page 273
40h–43h	32	“L4 Port Range Checker 0 Register (Page 21h/Addr 40h)” on page 273
44h–47h	32	“L4 Port Range Checker 1 Register (Page 21h/Addr 44h)” on page 273
48h–4Bh	32	“L4 Port Range Checker 2 Register (Page 21h/Addr 48h)” on page 274
4Ch–4Fh	32	“L4 Port Range Checker 3 Register (Page 21h/Addr 4Ch)” on page 274
50h	16	“Other Checker Register (Page 21h/Addr 50h)” on page 274
58h–EFh	Reserved	
F0h–F7h	–	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	–	SPI Status
FFh	8	Page Register

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CFP Global Control Register (Page 21h/Addr 00h)

Table 198: CFP Global Control Register (Page 21h: Address 00h)

Bit	Name	R/W	Description	Default
7:6	SLICE2_PRI	R/W	Slice 2 priority	0
5:4	SLICE1_PRI	R/W	Slice 1 priority	0
3:2	SLICE0_PRI	R/W	Slice 0 priority	0
1	AGGREGATION_CTRL	R/W	CFP Aggregation control • 1 = if the action is flood, will flood to all the ports. So Aggregation ports will have multiple copies. • 0 = if the action is flood, will only forward one copy in each aggregation group. ***Note:*** In this mode it will not do the load balancing, it is up to the user to designate the ports to send the frame.	0
0	VLAN_CTRL	R/W	CFP VLAN control • 1 = if the action is flood, will flood to all the ports. it does not care VLAN security. • 0 = if the action is flood, will only forward to member set which the packet belong to.	0

Range Checker Control Register (Page 21h/Addr 08h)

Table 199: Range Checker Control Register (Page 21h/Addr 08h)

Bit	Name	R/W	Description	Default
7:5	RSVD	–	Reserved	00h
4	CHG_VID_FFF_CTRL	R/W	Change VID Control bit. This bit is used when the entries of FLOW2VLAN are set to 12'hfff. • 0 = when the new VID reading from FLOW2VLAN is 12'hfff, it will maintain the original VID. (i.e., does not change VID). • 1 = when the new VID reading from FLOW2VLAN is 12'hfff, it will change VID to 12'hfff.	0
3	RNG_CHKR_CTRL_3	R/W	Range Check Control 3 • 1 = L4 Destination port • 0 = L4 Source port	0
2	RNG_CHKR_CTRL_2	R/W	Range Check Control 2 • 1 = L4 Destination port • 0 = L4 Source port	0
1	RNG_CHKR_CTRL_1	R/W	Range Check Control 1 • 1 = L4 Destination port • 0 = L4 Source port	0

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Table 199: Range Checker Control Register (Page 21h/Addr 08h)

Bit	Name	R/W	Description	Default
0	RNG_CHKR_CTRL_0	R/W	Range Check Control 0 • 1 = L4 Destination port • 0 = L4 Source port	0

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Global CFP Control1 Register (Page 21h/Addr 10h)

Table 200: CFP Global Control 1 Register (Page 21h: Address 10h–11h)

Bit	Name	R/W	Description	Default
15:0	ISP_VLAN_DELIMITER	R/W	Delimiter of ISP Tagged frame. ***Note:*** The Delimiter of .1Q tagged frame is 0x8100	0x9100

CFP Enable Control Register (Page 21h/Addr 20h–27h)

Table 201: CFP Enable Control Register (Page 21h: Address 20h–27h)

Bit	Name	R/W	Description	Default
63:53	RSVD	–	Reserved	0
52:24	CFP_CTRL_EN	R/W	CFP Enable Control Register bits When a bit is set to '1', enable the CFP feature of the corresponding port. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

VID Range Checker 0 Register (Page 21h/Addr 30h)

Table 202: VID Range Checker 0 Register (Page 21h: Address 30h–33h)

Bit	Name	R/W	Description	Default
31:28	RSVD	–	Reserved	0
27:16	UPPR_LMT	R/W	Upper limit value	0
15:12	RSVD	–	Reserved	0
11:0	LOWR_LMT	R/W	Lower limit value	0

VID Range Checker 1 Register (Page 21h/Addr 34h)

Table 203: VID Range Checker 1 Register (Page 21h: Address 34h–37h)

Bit	Name	R/W	Description	Default
31:28	RSVD	–	Reserved	0
27:16	UPPR_LMT	R/W	Upper limit value	0
15:12	RSVD	–	Reserved	0

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Table 203: VID Range Checker 1 Register (Page 21h: Address 34h–37h)

Bit	Name	R/W	Description	Default
11:0	LOWR_LMT	R/W	Lower limit value	0

VID Range Checker 2 Register (Page 21h/Addr 38h)

Table 204: VID Range Checker 2 Register (Page 21h: Address 38h–3Bh)

Bit	Name	R/W	Description	Default
31:28	RSVD	–	Reserved	0
27:16	UPPR_LMT	R/W	Upper limit value	0
15:12	RSVD	–	Reserved	0
11:0	LOWR_LMT	R/W	Lower limit value	0

VID Range Checker 3 Register (Page 21h/Addr 3Ch)

Table 205: VID Range Checker 3 Register (Page 21h: Address 3Ch–3Fh)

Bit	Name	R/W	Description	Default
31:28	RSVD	–	Reserved	0
27:16	UPPR_LMT	R/W	Upper limit value	0
15:12	RSVD	–	Reserved	0
11:0	LOWR_LMT	R/W	Lower limit value	0

L4 Port Range Checker 0 Register (Page 21h/Addr 40h)

Table 206: L4 Port Range Checker 0 Register (Page 21h: Address 40h–43h)

Bit	Name	R/W	Description	Default
31:16	UPPR_LMT	R/W	Upper limit value	0
15:0	LOWR_LMT	R/W	Lower limit value	0

L4 Port Range Checker 1 Register (Page 21h/Addr 44h)

Table 207: L4 Port Range Checker 1 Register (Page 21h: Address 44h–47h)

Bit	Name	R/W	Description	Default
31:16	UPPR_LMT	R/W	Upper limit value	0
15:0	LOWR_LMT	R/W	Lower limit value	0

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L4 Port Range Checker 2 Register (Page 21h/Addr 48h)

Table 208: L4 Port Range Checker 2 Register (Page 21h: Address 48h–4Bh)

Bit	Name	R/W	Description	Default
31:16	UPPR_LMT	R/W	Upper limit value	0
15:0	LOWR_LMT	R/W	Lower limit value	0

L4 Port Range Checker 3 Register (Page 21h/Addr 4Ch)

Table 209: L4 Port Range Checker 3 Register (Page 21h: Address 4Ch–4Fh)

Bit	Name	R/W	Description	Default
31:16	UPPR_LMT	R/W	Upper limit value	0
15:0	LOWR_LMT	R/W	Lower limit value	0

Other Checker Register (Page 21h/Addr 50h)

Table 210: Other Checker Register (Page 21h: Address 50h–51h)

Bit	Name	R/W	Description	Default
15:14	RSVD	–	Reserved	
13:10	TCP_HDR_LNGTH	R/W	TCP Header Length	0
9:0	BIG_ICMP	R/W	Big ICMP	0

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Page 22h: CFP UDF Control Registers

Table 211: CFP UDF Control Registers (Page 22h)

Address	Bits	Register Name
00h	8	“CFP UDF A0 Control Register (Page 22h/Addr 00h)” on page 276
01h	8	“CFP UDF A1 Control Register (Page 22h/Addr 01h)” on page 276
02h	8	“CFP UDF A2 Control Register (Page 22h/Addr 02h)” on page 276
10h	8	“CFP UDF B0 Control Register (Page 22h/Addr 10h)” on page 277
11h	8	“CFP UDF B1 Control Register (Page 22h/Addr 11h)” on page 277
12h	8	“CFP UDF B2 Control Register (Page 22h/Addr 12h)” on page 277
13h	8	“CFP UDF B3 Control Register (Page 22h/Addr 13h)” on page 278
14h	8	“CFP UDF B4 Control Register (Page 22h/Addr 14h)” on page 278

Table 211: CFP UDF Control Registers (Page 22h) (Cont.)

Address	Bits	Register Name
15h	8	"CFP UDF B5 Control Register (Page 22h/Addr 15h)" on page 279
16h	8	"CFP UDF B6 Control Register (Page 22h/Addr 16h)" on page 279
17h	8	"CFP UDF B7 Control Register (Page 22h/Addr 17h)" on page 279
18h	8	"CFP UDF B8 Control Register (Page 22h/Addr 18h)" on page 280
19h	8	"CFP UDF B9 Control Register (Page 22h/Addr 19h)" on page 280
1Ah	8	"CFP UDF B10 Control Register (Page 22h/Addr 1Ah)" on page 281
20h	8	"CFP UDF C0 Control Register (Page 22h/Addr 20h)" on page 281
21h	8	"CFP UDF C1 Control Register (Page 22h/Addr 21h)" on page 281
22h	8	"CFP UDF C2 Control Register (Page 22h/Addr 22h)" on page 282
30h	8	"CFP UDF D0 Control Register (Page 22h/Addr 30h)" on page 282
31h	8	"CFP UDF D1 Control Register (Page 22h/Addr 31h)" on page 283
32h	8	"CFP UDF D2 Control Register (Page 22h/Addr 32h)" on page 283
33h	8	"CFP UDF D3 Control Register (Page 22h/Addr 33h)" on page 283
34h	8	"CFP UDF D4 Control Register (Page 22h/Addr 34h)" on page 284
35h	8	"CFP UDF D5 Control Register (Page 22h/Addr 35h)" on page 284
36h	8	"CFP UDF D6 Control Register (Page 22h/Addr 36h)" on page 285
37h	8	"CFP UDF D7 Control Register (Page 22h/Addr 37h)" on page 285
F0h–F7h	–	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	–	SPI Status
FFh	8	Page Register

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CFP UDF A0 Control Register (Page 22h/Addr 00h)

Table 212: CFP UDF A0 Control Register (Page 22h: Address 00h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_A0	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_A0	R/W	The offset used for UDF_A0 which is used in Slice 0. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF A1 Control Register (Page 22h/Addr 01h)

Table 213: CFP UDF A1 Control Register (Page 22h: Address 01h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_A1	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_A1	R/W	The offset used for UDF_A1 which is used in Slice 0. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF A2 Control Register (Page 22h/Addr 02h)

Table 214: CFP UDF A2 Control Register (Page 22h: Address 02h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_A2	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_A2	R/W	The offset used for UDF_A2 which is used in Slice 0. The number counts from the reference port of frame. Rx port extracts 16 bits data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

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CFP UDF B0 Control Register (Page 22h/Addr 10h)

Table 215: CFP UDF B0 Control Register (Page 22h: Address 10h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_B0	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_B0	R/W	The offset used for UDF_B0 which is used in Slice 1. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF B1 Control Register (Page 22h/Addr 11h)

Table 216: CFP UDF B1 Control Register (Page 22h: Address 11h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_B1	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_B1	R/W	The offset used for UDF_B1 which is used in Slice 1. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF B2 Control Register (Page 22h/Addr 12h)

Table 217: CFP UDF B2 Control Register (Page 22h: Address 12h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_B2	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0

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Table 217: CFP UDF B2 Control Register (Page 22h: Address 12h)

Bit	Name	R/W	Description	Default
5:0	UDF_OFFSET_B2	R/W	The offset used for UDF_B2 which is used in Slice 1. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF B3 Control Register (Page 22h/Addr 13h)

Table 218: CFP UDF B3 Control Register (Page 22h: Address 13h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_B3	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_B3	R/W	The offset used for UDF_B3 which is used in Slice 1. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF B4 Control Register (Page 22h/Addr 14h)

Table 219: CFP UDF B4 Control Register (Page 22h: Address 14h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_B4	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_B4	R/W	The offset used for UDF_B4 which is used in Slice 1. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

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CFP UDF B5 Control Register (Page 22h/Addr 15h)

Table 220: CFP UDF B5 Control Register (Page 22h: Address 15h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_B5	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_B5	R/W	The offset used for UDF_B5 which is used in Slice 1. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF B6 Control Register (Page 22h/Addr 16h)

Table 221: CFP UDF B6 Control Register (Page 22h: Address 16h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_B6	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_B6	R/W	The offset used for UDF_B6 which is used in Slice 1. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF B7 Control Register (Page 22h/Addr 17h)

Table 222: CFP UDF B7 Control Register (Page 22h: Address 17h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_B7	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0

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Table 222: CFP UDF B7 Control Register (Page 22h: Address 17h)

Bit	Name	R/W	Description	Default
5:0	UDF_OFFSET_B7	R/W	The offset used for UDF_B7 which is used in Slice 1. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF B8 Control Register (Page 22h/Addr 18h)

Table 223: CFP UDF B8 Control Register (Page 22h: Address 18h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_B8	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_B8	R/W	The offset used for UDF_B8 which is used in Slice1. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF B9 Control Register (Page 22h/Addr 19h)

Table 224: CFP UDF B9 Control Register (Page 22h: Address 19h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_B9	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_B9	R/W	The offset used for UDF_B9 which is used in Slice 1. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

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CFP UDF B10 Control Register (Page 22h/Addr 1Ah)

Table 225: CFP UDF B10 Control Register (Page 22h: Address 1Ah)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_B10	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_B10	R/W	The offset used for UDF_B10 which is used in Slice 1. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF C0 Control Register (Page 22h/Addr 20h)

Table 226: CFP UDF C0 Control Register (Page 22h: Address 20h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_C0	R/W	Flag indicating the type of field for starting address • 11 = start of packet (Revision B silicon) • 11 = reserved (Revision A silicon) • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_C0	R/W	The offset used for UDF_C0 which is used in Slice 2. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF C1 Control Register (Page 22h/Addr 21h)

Table 227: CFP UDF C1 Control Register (Page 22h: Address 21h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_C1	R/W	Flag indicating the type of field for starting address • 11 = start of packet (Revision B silicon) • 11 = reserved (Revision A silicon) • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0

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Table 227: CFP UDF C1 Control Register (Page 22h: Address 21h)

Bit	Name	R/W	Description	Default
5:0	UDF_OFFSET_C1	R/W	The offset used for UDF_C1 which is used in Slice 2. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF C2 Control Register (Page 22h/Addr 22h)

Table 228: CFP UDF C2 Control Register (Page 22h: Address 22h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_C2	R/W	Flag indicating the type of field for starting address • 11 = start of packet (Revision B silicon) • 11 = reserved (Revision A silicon) • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_C2	R/W	The offset used for UDF_C2 which is used in Slice 2. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 16 bits (2-bytes)	0

CFP UDF D0 Control Register (Page 22h/Addr 30h)

Table 229: CFP UDF D0 Control Register (Page 22h: Address 30h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_D0	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_D0	R/W	The offset used for UDF_D0 which is used in Slice 2. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 32 bits (4-bytes)	0

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CFP UDF D1 Control Register (Page 22h/Addr 31h)

Table 230: CFP UDF D1 Control Register (Page 22h: Address 31h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_D1	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_D1	R/W	The offset used for UDF_D1 which is used in Slice 2. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 32 bits (4-bytes)	0

CFP UDF D2 Control Register (Page 22h/Addr 32h)

Table 231: CFP UDF D2 Control Register (Page 22h: Address 32h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_D2	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_D2	R/W	The offset used for UDF_D2 which is used in Slice 2. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 32 bits (4-bytes)	0

CFP UDF D3 Control Register (Page 22h/Addr 33h)

Table 232: CFP UDF D3 Control Register (Page 22h: Address 33h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_D3	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0

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Table 232: CFP UDF D3 Control Register (Page 22h: Address 33h)

Bit	Name	R/W	Description	Default
5:0	UDF_OFFSET_D3	R/W	The offset used for UDF_D3 which is used in Slice 2. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 32 bits (4-bytes)	0

CFP UDF D4 Control Register (Page 22h/Addr 34h)

Table 233: CFP UDF D4 Control Register (Page 22h: Address 34h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_D4	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_D4	R/W	The offset used for UDF_D4 which is used in Slice 2. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 32 bits (4-bytes)	0

CFP UDF D5 Control Register (Page 22h/Addr 35h)

Table 234: CFP UDF D5 Control Register (Page 22h: Address 35h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_D5	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_D5	R/W	The offset used for UDF_D5 which is used in Slice 2. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 32 bits (4-bytes)	0

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CFP UDF D6 Control Register (Page 22h/Addr 36h)

Table 235: CFP UDF D6 Control Register (Page 22h: Address 36h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_D6	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_D6	R/W	The offset used for UDF_D6 which is used in Slice 2. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 32 bits (4-bytes)	0

CFP UDF D7 Control Register (Page 22h/Addr 37h)

Table 236: CFP UDF D7 Control Register (Page 22h: Address 37h)

Bit	Name	R/W	Description	Default
7:6	UDF_REF_D7	R/W	Flag indicating the type of field for starting address • 11 = reserved • 10 = end of IP header (including IPv4 option) • 01 = end of Ether Type • 00 = end of Tag	0
5:0	UDF_OFFSET_D7	R/W	The offset used for UDF_D7 which is used in Slice 2. The number counts from the reference port of frame. Rx port extracts 16 bits of data from the corresponding location for CFP lookup. Unit: 32 bits (4-bytes)	0

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Page 30h: QoS Registers

Table 237: QoS Registers (Page 30h)

Address	Bits	Description
00h–0Fh	Reserved	
10h–17h	64	“QoS Control Register (Page 30h/Addr 10h–17h)” on page 287
18h–1Fh	64	“QoS 802.1p Enable Register (Page 30h/Addr 18h–1Fh)” on page 288
20h–27h	64	“QoS DiffServ Enable Register (Page 30h/Addr 20h–27h)” on page 289
28h–2Fh	64	“QoS Pause Enable Register (Page 30h/Addr 28h–2Fh)” on page 290
30h–31h	16	“Priority Threshold Register (Page 30h/Addr 30h–31h)” on page 290
–	Reserved	
40h–47h	64	“DiffServ DSCP Priority Register (Page 30h/Addr 40h–4Fh)” on page 291
48h–4Fh	64	DiffServ DSCP Priority register 2
58h–5Fh	16	“QoS Reason Code Enable Register (Page 30h/Addr 58h–59h)” on page 292
60h	Reserved	
F0h–F7h	64	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	8	SPI Status
FFh	8	Page Register

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QoS Control Register (Page 30h/Addr 10h–17h)

Table 238: QoS Control Register (Pages: 30h, Address 10h–17h)

Bit	Name	R/W	Description	Default
63	CPU Control Enable	R/W	• 1 = Register values control the port-based priority settings. This includes: – QOS_Enable setting (bit 59:58 of this register). – Flow control enable/disable is controlled on a per- port basis in the "QoS Pause Enable Register (Page 30h/Addr 28h–2Fh)" on page 290. • 0 = Reserved.	1
62:60	RSVD	RO	Reserved Write default. Ignore on read.	0
59:58	QOS_Enable	R/W	Select the number of priority queues. • 11 = When CPU Control Enable (bit 63) is asserted, setting these bits to 11 enables the four-queue QoS function. • 10 = Reserved • 01 = Reserved • 00 = When CPU Control Enable (bit 63) is asserted, setting these bits to 00 disables QoS and enables the single-queue function.	00
57:2	RSVD	RO	Reserved Write default. Ignore on read.	0
1:0	PRI_SEL	R/W	Priority Scheduling • 00: 4 WRR (Default) • 01: 1 SP - 3 WRR • 10: 2 SP - 2 WRR • 11: 4 SP	00

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QoS 802.1p Enable Register (Page 30h/Addr 18h–1Fh)

Table 239: QoS 802.1p Enable Register (Page 30h: Address 18h–1Fh)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read.	0
52:24	QOS_1P_EN	R/W	802.1p QoS enable bit for per-port. A 29-bit mask which selectively allows any port with its corresponding bit set, to enable 802.1p QoS. • Bit 52 = Giga Port G3 • Bit 51 = Giga Port G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	1E-FFFF-FF
23:0	RSVD	–	Reserved	0

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QoS DiffServ Enable Register (Page 30h/Addr 20h–27h)

Table 240: QoS DiffServ Enable Register (Page 30h: Address 20h–27h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read.	0
52:24	QoS_Diff_EN	R/W	DiffServ QoS enable bit for per-port. A 29-bit mask which selectively allows any port with its corresponding bit set, to enable DiffServ QoS. • Bit 52 = GigaPort G3 • Bit 51 = GigaPort G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

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QoS Pause Enable Register (Page 30h/Addr 28h–2Fh)

Table 241: QoS Pause Enable Register (Page 30h: Address 28h–2Fh)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read.	0
52:49	GE_PAUSE_EN	R/W	Per port QoS PAUSE Enable bit. • Bit 52 = GigaPort G3 • Bit 41 = GigaPort G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0	0
48	IMP_PAUSE_EN	R/W	Per port QoS PAUSE Enable bit. • Bit 48 = IMP or as a network port.	0
47:24	FE_PAUSE_EN	R/W	Per port QoS PAUSE Enable bit. A 24-bit mask which selectively allows any port with its corresponding bit set, to enable PAUSE. • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

Note: When software control of QoS is enabled by asserting the QOS_Enable, bits[59:58] of the "QoS Control Register (Page 30h/Addr 10h–17h)" on page 287, the QoS PAUSE Enable of individual port is controlled by setting:

- 0 = Half-duplex back pressure and full-duplex flow control are disabled. Only dropping of frames is supported on the given port.
- 1 = Individual port supports half-duplex back pressure and full-duplex flow control.

However, the per port PAUSE_EN state (if enabled) allows transmission of the Pause frame only from the switch when buffers are near capacity. When the link partner sends Pause frame, the switch does not pause transmission. Any change of state on PAUSE_EN has neither effect on the "Pause Status Summary Register (Page 02h/Addr 30h–37h)" on page 203.

Priority Threshold Register (Page 30h/Addr 30h–31h)

Table 242: Priority Threshold Register (Page 30h: Address 30h–31h)

Bit	Name	R/W	Description	Default
15:14	802.1p Priority Tag 111	R/W	These two bits are used to assign priority queue of tag 111.	3h
13:12	802.1p Priority Tag 110	R/W	These two bits are used to assign priority queue of tag 110.	3h
11:10	802.1p Priority Tag 101	R/W	These two bits are used to assign priority queue of tag 101.	2h
9:8	802.1p Priority Tag 100	R/W	These two bits are used to assign priority queue of tag 100.	2h
7:6	802.1p Priority Tag 011	R/W	These two bits are used to assign priority queue of tag 011.	1h

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Table 242: Priority Threshold Register (Page 30h: Address 30h–31h)

Bit	Name	R/W	Description	Default
5:4	802.1p Priority Tag 010	R/W	These two bits are used to assign priority queue of tag 010.	1h
3:2	802.1p Priority Tag 001	R/W	These two bits are used to assign priority queue of tag 001.	0h
1:0	802.1p Priority Tag 000	R/W	These two bits are used to assign priority queue of tag 000.	0h

DiffServ DSCP Priority Register (Page 30h/Addr 40h–4Fh)

Register 40h to register 4Fh are used to assign priority to different Differentiated Service. To provides 4 priority queues and 64 different traffic classes, a 64x2 table is needed. Each entry represents one traffic class. Two bits in an entry represents the priority of that traffic.

Table 243 and Table 244 define four entries: the remaining 60 traffic classes have the same format (they are not represented in this document).

Table 243: DiffServ DSCP Priority Register 1 (Page 30h: Address 40h–47h)

Bit	Name	R/W	Description	Default
63:62	Priority of DSCP=011111	R/W	See detail description above.	0
…..	……..	R/W		
7:6	Priority of DSCP=000011	R/W	See detail description above.	0
5:4	Priority of DSCP=000010	R/W	See detail description above.	0
3:2	Priority of DSCP=000001	R/W	See detail description above.	0
1:0	Priority of DSCP=000000	R/W	See detail description above.	0

Table 244: DiffServ DSCP Priority Register 2 (Page 30h: Address 48h–4Fh)

Bit	Name	R/W	Description	Default
63:62	Priority of DSCP=111111	R/W	See detail description above.	0
…..	……..	R/W		
7:6	Priority of DSCP=100011	R/W	See detail description above.	0
5:4	Priority of DSCP=100010	R/W	See detail description above.	0
3:2	Priority of DSCP=100001	R/W	See detail description above.	0
1:0	Priority of DSCP=100000	R/W	See detail description above.	0

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QoS Reason Code Enable Register (Page 30h/Addr 58h–59h)

Table 245: QoS Reason Code Enable Register (Page 30h: Address 58h–59h)

Bit	Name	R/W	Description	Default
15:12	RSVD	–	Reserved	0
11:10	PRI_EXCEPT	R/W	To assign priority queue of Reason Code = EXCEPTION / FLOODING packets	01
9:8	PRI_PROTOCOL_SNOOP	R/W	To assign priority queue of Reason Code = PROTOCOL SNOOPING packets	10
7:6	PRI_PROTOCOL_TERM	R/W	To assign priority queue of Reason Code = PROTOCOL TERMINATION packets	11
5:4	PRI_SWITCH	R/W	To assign priority queue of Reason Code = SWITCH packets	10
3:2	PRI_SA_LEARN	R/W	To assign priority queue of Reason Code = SA LEARNING packets	0
1:0	PRI_MIRROR	R/W	To assign priority queue of Reason Code = MIRROR packets	0

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Page 31h: MAC-Based Aggregation Registers

Table 246: MAC-Based Aggregation Registers (Page 31h)

Addr	Bits	Description
00h	8	"Global Aggregation Control Register (Page 31h/Addr 00h)" on page 294
01h–0Fh	Reserved	
10h–17h	64	Group n=1, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
18h–1Fh	64	Group n=2, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
20h–27h	64	Group n=3, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
28h–2Fh	64	Group n=4, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
30h–37h	64	Group n=5, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
38h–3Fh	64	Group n=6, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
40h–47h	64	Group n=7, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
48h–4Fh	64	Group n=8, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
50h–57h	64	Group n=9, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
58h–5Fh	64	Group n=10, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
60h–67h	64	Group n=11, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
68h–6Fh	64	Group n=12, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
70h–77h	64	Group n=13, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
78h–7Fh	64	Group n=14, "Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)" on page 295
80h–EFh	Reserved	
F0h–F7h	64	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	8	SPI Status
FFh	8	Page Register

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Global Aggregation Control Register (Page 31h/Addr 00h)

Table 247: Global Aggregation Control Register (Page 31h, Address 00h)

Bit	Name	R/W	Description	Default
7:4	TRKG_SEED	R/W	Aggregation hash index selection. • bit 7: IPv4_SIP • bit 6: IPv4_DIP • bit 5: MAC_SA • bit 4: MAC_DA	0x03
3:2	RSVD	RO	Reserved. Write default. Ignore on read.	0
1	EN_AGGR	R/W	Enable Aggregation. • 1: Enable. • 0: Disable.	0
0	RSVD	RO	Reserved. Write default. Ignore on read.	0

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Aggregation Control Group n Register (Page 31h/Addr 10h–7Fh)

Table 248: Aggregation Control Group n Register

Bit	Name	R/W	Description	Default
63:54	RSVD	RO	Reserved Write default. Ignore on read.	0
53	En_TRNK_GRP	R/W	Enable Aggregation Group n. Set this bit and TRNK_PORT_MAP to enable Aggregation Group Vector.	0
52:24	TRNK_PORT_MAP	R/W	Aggregation Group n Vector. A bit mask corresponding to the physical ports on the chip. For physical ports which belong to the same aggregation, the corresponding bit should be set to 1. • Bit 52 = GigaPort G3 • Bit 51 = GigaPort G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP port • Bits 47:24 = 10/100 ports [port 47-port 24] ***Note:*** – Each port can belong to only one aggregation group. – Up to 8 ports can be assigned to an aggregation group. – All ports in an aggregation group must be from the same speed. – When En_TRNK_GRP is not set, no bits can be set in the TRNK_PORT_MAP.	0
23:0	RSVD	–	Reserved	0

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Page 33h: Port Egress Control Registers

Table 249: Port Egress Control Registers (Page 33h)

Address	Bits	Description
00h–07h	64	Port 24 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
08h–0Fh	64	Port 25 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
10h–17h	64	Port 26 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
18h–1Fh	64	Port 27 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
20h–27h	64	Port 28 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
28h–2Fh	64	Port 29 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
30h–37h	64	Port 30 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
38h–3Fh	64	Port 31 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
40h–47h	64	Port 32 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
48h–4Fh	64	Port 33 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
50h–57h	64	Port 34 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
58h–5Fh	64	Port 35 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
60h–67h	64	Port 36 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
68h–6Fh	64	Port 37 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
70h–77h	64	Port 38 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
78h–7Fh	64	Port 39 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
80h–87h	64	Port 40 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
88h–8Fh	64	Port 41 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
90h–97h	64	Port 42 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
98h–9Fh	64	Port 43 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297

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Table 249: Port Egress Control Registers (Cont.)(Page 33h)

Address	Bits	Description
A0h–A7h	64	Port 44 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
A8h–AFh	64	Port 45 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
B0h–B7h	64	Port 46 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
B8h–BFh	64	Port 47 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
C0h–C7h	64	IMP Port "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
C8h–CFh	64	Gigabit Port 0 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
D0h–D7h	64	Gigabit Port 1 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
D8h-DFh	64	Gigabit Port 2 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
E0h-E7h	64	Gigabit Port 3 "Port Egress Control Register (Page 33h/Addr 00h–D7h)" on page 297
E8h–EFh	Reserved	
F0h–F7h	64	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	8	SPI Status
FFh	8	Page Register

Port Egress Control Register (Page 33h/Addr 00h–D7h)

Table 250: Port Egress Control Register (Pages: 33h, Address 00h–D7h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved. Write default. Ignore on read.	0
52:24	PORT_EGRESS_En[52:24]	R/W	Port Egress Enable vector. A bit mask corresponding to the physical ports on the chip. Set corresponding bit to 1 to enable port egress forwarding. Set bit to 0 inhibits the port egress forwarding. • Bit 52 = GigaPort G3 • Bit 51 = GigaPort G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	1F-FFFF-FF

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Table 250: Port Egress Control Register (Pages: 33h, Address 00h–D7h)

Bit	*Name*	*R/W*	*Description*	*Default*
23:0	RSVD	–	Reserved	–

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Page 34h: 802.1Q VLAN Registers

Table 251: 802.1Q VLAN Registers (Page 34h)

Address	Bits	Description
00h	8	“802.1Q Control 0 Register (Page 34h/Addr 00h)” on page 300
01h	8	“802.1Q Control 1 Register (Page 34h/Addr 01h)” on page 300
02h	8	“802.1Q Control 2 Register (Page 34h/Addr 02h)” on page 303
03h	8	“802.1Q Control 4 Register (Page 34h/Addr 03h)” on page 305
04h	8	“802.1Q Control 5 Register (Page 34h/Addr 04h)” on page 306
05h-07h	Reserved	–
08h–0Fh	64	“802.1Q Control 3 Register (Page 34h/Addr 08h–0Fh)” on page 304
10h–3Fh	Reserved	
40h–79h	16	“802.1Q Default Port Tag Register (Page 34h/Addr 40h–79h)” on page 307
7Ah–8Fh	Reserved	
90h	8	“Global Double Tagging Control Register (Page 34h/Addr 90h)” on page 309
91h-97h	Reserved	
98h–9Fh	64	“SP Portmap Selection Register (Page 34h/Addr 98h–9Fh)” on page 310
A0h–A7h	64	“VLAN to VLAN Control Register (Page 34h/Addr A0h–A7h)” on page 311
A8h–AFh	64	“MAC to VLAN Control Register (Page 34h/Addr A8h–AFh)” on page 312
B0h–B7h	64	“Protocol to VLAN Control Register (Page 34h/Addr B0h–B7h)” on page 313
B8h–BFh	64	“Trusted Customer VLAN Register (Page 34h: Address B8h–BFh)” on page 314
F0h–F7h	64	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	8	SPI Status
FFh	8	Page Register

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802.1Q Control 0 Register (Page 34h/Addr 00h)

Table 252: 802.1Q Control 0 Register (Pages: 34h, Address 00h)

Bit	Name	R/W	Description	Default
7	EN_1QVLAN	R/W	Enable 802.1Q VLAN. When set to 1, enable 802.1Q VLAN function.	0
6:5	VID_MAC Control	R/W	ARL Table Hashing Control. When 802.1Q VLAN is enabled, these bits determine the ARL Table hashing scheme. • 11: Use both [VID, MAC]. • 10: Reserved. • 01: Reserved. • 00: Use only [MAC].	11
4	EN_DROP_VID_MISS	R/W	Enable Drop VID Miss Frames When asserted, any incoming frames with a matching DA, but not VLAN ID, are dropped.	0
3:0	RSVD	–	Reserved	0x2

802.1Q Control 1 Register (Page 34h/Addr 01h)

Table 253: 802.1Q Control 1Register (Pages: 34h, Address 01h)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0
6	IPMC_UntagMap_Chk	R/W	Bypass IP MultiCast VLAN Untag_Map Check. • 1: Enables checking IPMC frame against VLAN Untag_Map. • 0: When asserted disables checking IPMC frame against VLAN Untag_Map.	0
5	IPMC_FwdMap_Chk	R/W	Bypass IP MultiCast VLAN Fwd_Map Check. • 1: Enables checking IPMC frame against VLAN Fwd_Map. • 0: When asserted disables checking IPMC frame against VLAN Fwd_Map.	0
4	RSVD	RO	Reserved Write default. Ignore on read.	0

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Table 253: 802.1Q Control 1Register (Pages: 34h, Address 01h) (Cont.)

Bit	Name	R/W	Description	Default
3	Rsvd MC_ UntagMap_Chk	R/W	Reserved MultiCast (except GMRP and GVRP) VLAN Untag_Map Check. • 1: When asserted enables checking reserved MC frame against VLAN Untag_Map. – For untagged incoming packets, check against VLAN Untag_Map from the port default tag. • 0: Disables checking reserved MC frame against VLAN Untag_Map. – When incoming packet is untagged, port default tag is stripped on egress. – A tagged incoming packet is tagged on egress.	0
2	Rsvd MC_FwdMap_Chk	R/W	Reserved MultiCast (except GMRP and GVRP) VLAN Fwd_Map Check. • 1: When asserted enables checking reserved MC frame against VLAN Fwd_Map. – For untagged incoming packets, check against VLAN Fwd_Map from the port default tag. • 0: Disables checking reserved MC frame against VLAN Fwd_Map. – For untagged incoming packets, use VLAN Fwd_Map from the port default tag.	0
1	Special Entry MC_UntagMap_Chk	R/W	Special Entry MAC Untag Map Check. When an ingress MAC DA matches what is defined in either Multiport Address 1 or Multiport Address 2 register, the frame bypasses ARL checking. The forwarding vector for this frame is determined by either Multi Vector 1 or Multi Vector 2 register respectively. • 1: When asserted enables checking reserved MC frame against VLAN Untag_Map. – For untagged incoming packets, check against VLAN Untag_Map from the port default tag. • 0: Disables checking reserved MC frame against VLAN Untag_Map. – When incoming packet is untagged, port default tag is stripped on egress. – A tagged incoming packet is tagged on egress.	0

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Table 253: 802.1Q Control 1Register (Pages: 34h, Address 01h) (Cont.)

Bit	Name	R/W	Description	Default
0	Special Entry MC_FwdMap_Chk	R/W	Special Entry MAC Forward Map Check. When an ingress MAC DA matches what is defined in either Multiport Address 1 or Multiport Address 2 register, the frame bypasses ARL checking. The forwarding vector for this frame is determined by either Multi Vector 1 or Multi Vector 2 register respectively. • 1: When asserted enables checking reserved MC frame against VLAN Fwd_Map. – For untagged incoming packets, check against VLAN Fwd_Map from the port default tag. • 0: Disables checking reserved MC frame against VLAN Fwd_Map. – For untagged incoming packets, use VLAN Fwd_Map from the port default tag.	0

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802.1Q Control 2 Register (Page 34h/Addr 02h)

Table 254: 802.1Q Control 2 Register (Pages: 34h, Address 02h)

Bit	Name	R/W	Description	Default
7	RSVD	R/W	Reserved Write as default. Ignore on read.	0
6	GMRP/GVRP_ UntagMap_Chk	R/W	GMRP or GVRP Untag_Map Check • 1: When asserted enables checking GMRP and GVRP frame against Untag_Map. • 0: Disables checking GMRP and GVRP frame against Untag_Map. ***Note:*** This feature does not apply to IMP configured as a management port.	0
5	GMRP/ GVRP_FwdMap_Chk	R/W	GMRP or GVRP VLAN Fwd_Map Check • 1: When asserted enables checking GMRP or GVRP frame against VLAN Fwd_Map. • 0: Disables checking GMRP or GVRP frame against VLAN Fwd_Map. ***Note:*** This feature does not apply to IMP configured as a management port.	0
4	RSVD	R/W	Reserved Write as default. Ignore on read.	0
3	RSVD	RO	Reserved. Write as default. Ignore on read.	0
2	IMP Mngt Frm_FwdMap_Chk	R/W	MII Management Frame VLAN Fwd_Map Check • 1: When asserted disables checking frames received at IMP management port against VLAN Fwd_Map. • 0: Enables checking frame received at IMP management port against VLAN Fwd_Map. ***Note:*** An untagged frame received by the IMP management port is never tagged.	0
1:0	RSVD	RO	Reserved. Write as default. Ignore on read.	0

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802.1Q Control 3 Register (Page 34h/Addr 08h–0Fh)

Note: The offset address for this register is out of sequence.

Table 255: 802.1Q Control 3 Register (Pages: 34h, Address 08h–0Fh)

Bit	Name	R/W	Description	Default
63	VID_FFF	R/W	VID Special Handling Any frame with VID = FFF is treated 1 = As normal frame. 0 = As VID violation frame. (Default)	0
62:53	RSVD	RO	Reserved. Write default. Ignore on read.	0
52:24	Enable Drop Non 1Q Frame	R/W	Enable Drop Non 1Q Frames. A 29-bit mask corresponds to the physical ports on the chip. Setting any bit to 1 enables non_1Q (untagged or priority tagged) ingress frame to be dropped by the corresponding port. • Bit 52 = GigaPort G3 • Bit 51 = GigaPort G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP. • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

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802.1Q Control 4 Register (Page 34h/Addr 03h)

Table 256: 802.1Q Control 4 Register (Pages: 34h, Address 03h)

Bit	Name	R/W	Description	Default
7:6	Ingress_VID_check	R/W	Perform ingress VLAN source port membership check. Ingress VID violation is detected when the source port is not found in the VLAN Fwd_Map that is referred to by the ingress VID. • 00: Forward ingress VID violation frame but do not learn SA into ARL table. • 01: Drop frame if ingress VID violation is detected. • 10: Bypass checking for ingress VID violation but SA is learned into ARL table. ***Note:*** Ingress_VID_check does not apply to the IMP configured as management port.	10
5	Mngt_Rcv_GVRP	R/W	Forward GVRP frame to management port When set this bit to 1, forward GVRP frames to management port.	0
4	Mngt_Rcv_GMRP	R/W	Forward GMRP frame to management port When set this bit to 1, forward GMRP frames to management port.	0
3:2	RSVD	RO	Reserved. Write default. Ignore on read.	0
1	VLAN_VLAN_OPT	R/W	VLAN to VLAN Table Optional Control (Revision B Silicon only). This bit selects the index used to search the VLAN to VLAN table. ***Note:*** PORTID is referred to as the physical port ID. The logical port ID starts from 0, 1, 2, ... The physical port ID starts from 24, 25, 26..... The logical to physical port ID mapping is as follows: Logical Port ID — PORTID 0 — 24 1 — 25 2 — 26 ... — ... 23 — 47 IMP — 48 GigaPort G0 — 49 Gigaport G1 — 50 • 0 = Select VID[11:0] as the index • 1 = Select {(PORTID-24)[4:0], VID[6:0]} as the index	0
0	RSVD	RO	Reserved. Write default. Ignore on read.	0

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802.1Q Control 5 Register (Page 34h/Addr 04h)

Table 257: 802.1Q Control 5 Register (Pages: 34h, Address 04h)

Bit	Name	R/W	Description	Default
7	RSVD	–	Reserved	0
6	Preserve_non_1Q	R/W	Egress non_1Q frame control. • 1 = Preserve ingress non_1Q frames. • 0 = Apply VLAN rules if enabled to ingress non_1Q frames.	0
5	Dis_Egress_Dir_Bypass_Trunking	R/W	Disable Egress Direct Frame Trunking Rule Check. • 1 = Egress direct frames from the host management system do not bypass trunking rule check. • 0 = Allow egress direct frames from the host management system to bypass.	0
4	RSVD	RO	Reserved. Write as default. Ignore on read.	1
3	drop_Vtable_miss	R/W	Ingress VID is pointing to a nonvalid entry in the VLAN table. When set to: • 1, a frame with VLAN table miss is dropped. • 0, a frame with VLAN table miss is trapped to IMP.	0
2	RSVD	RO	Reserved. Write default. Ignore on read.	0
1	Bypass_Mngt_Rx_CRC_Chk	R/W	Bypass CRC Check at Management port. • 1 = The management port with CPU on it ignores any CRC from BRCM tagged frame or Ethernet frame. • 0 = The management port checks both CRCs. ***Note:*** With this option, CPU does not need to calculate CRC for BRCM tagged frame. However it is still required to include a place holder for the BRCM tag CRC.	0
0	RSVD	R/W	Write default. Ignore on read.	0

Note: For normal operation, Broadcom recommends to set bits 3, 1, and 0 of this register to 1.

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802.1Q Default Port Tag Register (Page 34h/Addr 40h–79h)

See Table 259: “Default 802.1Q Tag,” on page 308.

Table 258: 802.1Q Default Port Tag Register (Page: 34h, Address 40h–79h)

Bit	Name	R/W	Description	Default
Addr 40h–41h bit [15:0]	Default Tag Port 24	R/W	Default 802.1Q tag assigned to port 24.	0018h
Addr 42h–43h bit [15:0]	Default Tag Port 25	R/W	Default 802.1Q tag assigned to port 25.	0019h
Addr 44h–45h bit [15:0]	Default Tag Port 26	R/W	Default 802.1Q tag assigned to port 26.	001Ah
Addr 46h–47h bit [15:0]	Default Tag Port 27	R/W	Default 802.1Q tag assigned to port 27.	001Bh
Addr 48h–49h bit [15:0]	Default Tag Port 28	R/W	Default 802.1Q tag assigned to port 28.	001Ch
Addr 4Ah–4Bh bit [15:0]	Default Tag Port 29	R/W	Default 802.1Q tag assigned to port 29.	001Dh
Addr 4Ch–4Dh bit [15:0]	Default Tag Port 30	R/W	Default 802.1Q tag assigned to port 30.	001Eh
Addr 4Eh–4Fh bit [15:0]	Default Tag Port 31	R/W	Default 802.1Q tag assigned to port 31.	001Fh
Addr 50h–51h bit [15:0]	Default Tag Port 32	R/W	Default 802.1Q tag assigned to port 32.	0020h
Addr 52h–53h bit [15:0]	Default Tag Port 33	R/W	Default 802.1Q tag assigned to port 33.	0021h
Addr 54h–55h bit [15:0]	Default Tag Port 34	R/W	Default 802.1Q tag assigned to port 34.	0022h
Addr 56h–57h bit [15:0]	Default Tag Port 35	R/W	Default 802.1Q tag assigned to port 35.	0023h
Addr 58h–59h bit [15:0]	Default Tag Port 36	R/W	Default 802.1Q tag assigned to port 36.	0024h
Addr 5Ah–5Bh bit [15:0]	Default Tag Port 37	R/W	Default 802.1Q tag assigned to port 37.	0025h
Addr 5Ch–5Dh bit [15:0]	Default Tag Port 38	R/W	Default 802.1Q tag assigned to port 38.	0026h
Addr 5Eh–5Fh bit [15:0]	Default Tag Port 39	R/W	Default 802.1Q tag assigned to port 39.	0027h
Addr 60h–61h bit [15:0]	Default Tag Port 40	R/W	Default 802.1Q tag assigned to port 40.	0028h
Addr 62h–63h bit [15:0]	Default Tag Port 41	R/W	Default 802.1Q tag assigned to port 41.	0029h
Addr 64h–65h bit [15:0]	Default Tag Port 42	R/W	Default 802.1Q tag assigned to port 42.	002Ah
Addr 66h–67h bit [15:0]	Default Tag Port 43	R/W	Default 802.1Q tag assigned to port 43.	002Bh

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Table 258: 802.1Q Default Port Tag Register (Page: 34h, Address 40h–79h) (Cont.)

Bit	Name	R/W	Description	Default
Addr 68h–69h bit [15:0]	Default Tag Port 44	R/W	Default 802.1Q tag assigned to port 44.	002Ch
Addr 6Ah–6Bh bit [15:0]	Default Tag Port 45	R/W	Default 802.1Q tag assigned to port 45.	002Dh
Addr 6Ch–6Dh bit [15:0]	Default Tag Port 46	R/W	Default 802.1Q tag assigned to port 46.	002Eh
Addr 6Eh–6Fh bit [15:0]	Default Tag Port 47	R/W	Default 802.1Q tag assigned to port 47.	002Fh
Addr 70h–71h bit [15:0]	Default tag IMP Port	R/W	Default 802.1Q tag assigned to IMP port.	0030h
Addr 72h–73h bit [15:0]	Default Tag G0 Port	R/W	Default 802.1Q tag assigned to Gigabit port G0.	0031h
Addr 74h–75h bit [15:0]	Default Tag G1 Port	R/W	Default 802.1Q tag assigned to Gigabit port G1.	0032h
Addr 76h–77h bit [15:0]	Default Tag G2 Port	R/W	Default 802.1Q tag assigned to Gigabit port G2.	0033h
Addr 78h–79h bit [15:0]	Default Tag G3 Port	R/W	Default 802.1Q tag assigned to Gigabit port G3.	0034h

Table 259: Default 802.1Q Tag

Bit	Name	R/W	Description	Default
15:13	Pri	R/W	802.1p Priority bits.	0h
12	CFI	RO	Reserved. Write default. Ignore on read.	0
11:0	Default VID	R/W	Default 802.1Q VID for port n. • n = 52: GigaPort G3 • n = 51: GigaPort G2 • n = 50: GigaPort G1 • n = 49: GigaPort G0 • n = 48: IMP • n = 47–24: 10/100 ports (47:24) respectively.	n

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Global Double Tagging Control Register (Page 34h/Addr 90h)

Table 260: Global Double Tagging Control Register (Pages: 34h, Address 90h)

Bit	Name	R/W	Description	Default
7:2	RSVD	RO	Reserved Write default. Ignore on read.	0
1	EN_DBL_ISP_TAG	R/W	Enable Double ISP Tag.	0

Table 260: Global Double Tagging Control Register (Pages: 34h, Address 90h)

Bit	Name	R/W	Description	Default
0	Rsvd_MC_Flood	R/W	Enable Reserved Multicast Flood Mode. When BCM53262M is configured as management mode and double tagging is enabled: • 1 = Reserved multicast frame is flooded per VLAN rules. • 0 = Reserved multicast frames is trapped to IMP management port. ***Note:*** Reserved multicast frames exclude pause frame. Pause frame is treated as MAC Control Frame.	0

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SP Portmap Selection Register (Page 34h/Addr 98h–9Fh)

Table 261: SP Portmap Selection Register (Pages: 34h, Address 98h–9Fh)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read.	0
52:24	SP_PORTMAP	R/W	Enable Service Provider (SP) Port Map A 29-bit mask which selectively allows any port with its corresponding bit set, to enable as the ISP port. • Bit 52 = GigaPort G3 • Bit 51 = GigaPort G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

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VLAN to VLAN Control Register (Page 34h/Addr A0h–A7h)

Table 262: VLAN To VLAN Control Register (Pages: 34h, Address A0h–A7h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved. Write default. Ignore on read.	0
52:24	VLAN_VLAN_PORTMAP	R/W	Enable VLAN to VLAN table look up A 29-bit mask which selectively allows any port with its corresponding bit set, to enable VLAN translation. • Bit 52 = GigaPort G3 • Bit 51 = GigaPort G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

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MAC to VLAN Control Register (Page 34h/Addr A8h–AFh)

Table 263: MAC To VLAN Control Register (Pages: 34h, Address A8h–AFh)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read.	0
52:24	MAC_VLAN_PORTMAP	R/W	Enable MAC to VLAN table look up A 29-bit mask which selectively allows any port with its corresponding bit set, to enable MAC-based VLAN. • Bit 52 = GigaPort G3 • Bit 51 = GigaPort G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

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Protocol to VLAN Control Register (Page 34h/Addr B0h–B7h)

Table 264: Protocol To VLAN Control Register (Pages: 34h, Address B0h–B7h)

Bit	Name	R/W	Description	Default
63:53	RSVD	RO	Reserved Write default. Ignore on read.	0
52:24	PROT_VLAN_PORTMAP	R/W	Enable Protocol to VLAN table look up A 29-bit mask which selectively allows any port with its corresponding bit set, to enable Protocol-based VLAN. • Bit 52 = GigaPort G3 • Bit 51 = GigaPort G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	0
23:0	RSVD	–	Reserved	0

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Trusted Customer VLAN Register (Page 34h: Address B8h–BFh)

Table 265: Trusted Customer VLAN Register (Page 34h: Address B8h–BFh)

Bit	Name	R/W	Description	Default
63:53	RSVD	–	Reserved	0
52:24	TRUSTED_CVLAN_PORTMAP	R/W	Enable Trusted Customer VLAN table look up when the corresponding bit is set, port to use the trusted VID of the incoming 802.1Q tag. • Bit 52 = GigaPort G3 • Bit 51 = GigaPort G2 • Bit 50 = GigaPort G1 • Bit 49 = GigaPort G0 • Bit 48 = IMP • Bits 47:24 = 10/100 ports [port 47-port 24]	1F-FFFF-FF
23:0	RSVD	–	Reserved	0

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Page 40h: 802.1x Registers

Table 266: 802.1x Registers (Page 40h)

Addr	Bits	Description
00h–1Fh	8	"Port EAP Configuration Register (Page 40h/Addr 00h–1Ch)" on page 316
20h–CFh	48	"Port EAP Destination Address Register (Page 40h/Addr 20h–C8h)" on page 319
E0h–EFh	Reserved	
F0h–F7h	64	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	8	SPI Status
FFh	8	Page Register

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Port EAP Configuration Register (Page 40h/Addr 00h–1Ch)

See Table 268: “EAP Configuration Register,” on page 317.

Table 267: Port EAP Configuration Register (Page: 40h, Address 00h–1Ch)

Bit	Name	R/W	Description	Default
Addr 00h bit [7:0]	Port 24’s	R/W	EAP Configuration	0
Addr 01h bit [7:0]	Port 25’s	R/W	EAP Configuration	0
Addr 02h bit [7:0]	Port 26’s	R/W	EAP Configuration	0
Addr 03h bit [7:0]	Port 27’s	R/W	EAP Configuration	0
Addr 04h bit [7:0]	Port 28’s	R/W	EAP Configuration	0
Addr 05h bit [7:0]	Port 29’s	R/W	EAP Configuration	0
Addr 06h bit [7:0]	Port 30’s	R/W	EAP Configuration	0
Addr 07h bit [7:0]	Port 31’s	R/W	EAP Configuration	0
Addr 08h bit [7:0]	Port 32’s	R/W	EAP Configuration	0
Addr 09h bit [7:0]	Port 33’s	R/W	EAP Configuration	0
Addr 0Ah bit [7:0]	Port 34’s	R/W	EAP Configuration	0
Addr 0Bh bit [7:0]	Port 35’s	R/W	EAP Configuration	0
Addr 0Ch bit [7:0]	Port 36’s	R/W	EAP Configuration	0
Addr 0Dh bit [7:0]	Port 37’s	R/W	EAP Configuration	0
Addr 0Eh bit [7:0]	Port 38’s	R/W	EAP Configuration	0
Addr 0Fh bit [7:0]	Port 39’s	R/W	EAP Configuration	0
Addr 10h bit [7:0]	Port 40’s	R/W	EAP Configuration	0
Addr 11h bit [7:0]	Port 41’s	R/W	EAP Configuration	0
Addr 12h bit [7:0]	Port 42s	R/W	EAP Configuration	0
Addr 13h bit [7:0]	Port 43’s	R/W	EAP Configuration	0
Addr 14h bit [7:0]	Port 44’s	R/W	EAP Configuration	0
Addr 15h bit [7:0]	Port 45’s	R/W	EAP Configuration	0
Addr 16h bit [7:0]	Port 46’s	R/W	EAP Configuration	0
Addr 17h bit [7:0]	Port 47’s	R/W	EAP Configuration	0
Addr 18h bit [7:0]	IMP Port	R/W	EAP Configuration	0
Addr 19h bit [7:0]	GE port 0	R/W	EAP Configuration	0
Addr 1Ah bit [7:0]	GE port 1	R/W	EAP Configuration	0
Addr 1Bh bit [7:0]	GE port 2	R/W	EAP Configuration	0
Addr 1Ch bit [7:0]	GE port 3	R/W	EAP Configuration	0

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Table 268: EAP Configuration Register

Bit	Name	R/W	Description	Default
7	ROAMING_OPTION	R/W	Address Roaming Support This bit is used when EAP_MODE = 2'b10. When a SA is learned at a port and subsequently moved to anther port. The learned SA count is different depended on how this bit is set • 0 = does not support Roaming. The same SA is thus learned twice. The learned SA count is set to 2 • 1 = support address roaming. The learned SA count is set to 1	0
6	SA_VIOLATION	R/W	This bit is used when EAP_MODE = 2'b01 or 2'b10 and incoming packet with SA violation (i.e., not in ARL table or exceeding learning limitation) • 0 = drop • 1 = forward to IMP port	0
5	DIS_LEARING	R/W	• 0 = learning enabled • 1 = learning disabled.	0
4	EAP_EN_USER_DA	R/W	Enable EAP frame with user (unicast or multicast) DA. This is to change the definition of "special frame" defined under EAP_PORT_BLOCK • 0 = do not support user DA EAP frame • 1 = support user DA EAP frame	0
3:2	EAP_PORT_BLOCK	R/W	set local port to block mode (do not need this bit for management port) • 00 = local port is not blocked • 01 = local port is blocked in ingress side • 10 = local port is blocked in both ingress and egress side. only 802.1x packet and special frame will be received. • 11 = Reserved	0

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Table 268: EAP Configuration Register

Bit	Name	R/W	Description	Default
1:0	EAP_MODE	R/W	Extend Mode • 00 = Basic mode, SA will not be checked. • 01 = EAP Extended mode for unknown SA handling. For all nonEAP frame and nonEAP special frame only, check SA and port number. If unknown SA, drop or forward frame to IMP, and this unknown SA is not learned in ARL. • 10 = EAP Extended mode for SA limited learning handling. For all nonEAP frame and nonEAP special frame only, check SA learning limit. If current SA count exceeds max learn limit, drop or forward frame to IMP, and this violated SA is not learned in ARL. • 11 = Reserved	0

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Port EAP Destination Address Register (Page 40h/Addr 20h–C8h)

See Table 270: “EAP Unicast Destination Address,” on page 320.

Table 269: Port EAP Destination Address Register (Page: 40h, Address 20h–C8h)

Bit	Name	R/W	Description	Default
Addr 20h bit [47:0]	Port 24’s	R/W	EAP Unicast Destination Address Register	0
Addr 26h bit [47:0]	Port 25’s	R/W	EAP Unicast Destination Address Register	0
Addr 2Ch bit [47:0]	Port 26’s	R/W	EAP Unicast Destination Address Register	0
Addr 32h bit [47:0]	Port 27’s	R/W	EAP Unicast Destination Address Register	0
Addr 38h bit [47:0]	Port 28’s	R/W	EAP Unicast Destination Address Register	0
Addr 3Eh bit [47:0]	Port 29’s	R/W	EAP Unicast Destination Address Register	0
Addr 44h bit [47:0]	Port 30’s	R/W	EAP Unicast Destination Address Register	0
Addr 4Ah bit [47:0]	Port 31’s	R/W	EAP Unicast Destination Address Register	0
Addr 50h bit [47:0]	Port 32’s	R/W	EAP Unicast Destination Address Register	0
Addr 56h bit [47:0]	Port 33’s	R/W	EAP Unicast Destination Address Register	0
Addr 5Ch bit [47:0]	Port 34’s	R/W	EAP Unicast Destination Address Register	0
Addr 62h bit [47:0]	Port 35’s	R/W	EAP Unicast Destination Address Register	0
Addr 68h bit [47:0]	Port 36’s	R/W	EAP Unicast Destination Address Register	0
Addr 6Eh bit [47:0]	Port 37’s	R/W	EAP Unicast Destination Address Register	0
Addr 74h bit [47:0]	Port 38’s	R/W	EAP Unicast Destination Address Register	0
Addr 7Ah bit [47:0]	Port 39’s	R/W	EAP Unicast Destination Address Register	0
Addr 80h bit [47:0]	Port 40’s	R/W	EAP Unicast Destination Address Register	0
Addr 86h bit [47:0]	Port 41’s	R/W	EAP Unicast Destination Address Register	0
Addr 8Ch bit [47:0]	Port 42’s	R/W	EAP Unicast Destination Address Register	0
Addr 92h bit [47:0]	Port 43’s	R/W	EAP Unicast Destination Address Register	0
Addr 98h bit [47:0]	Port 44’s	R/W	EAP Unicast Destination Address Register	0
Addr 9Eh bit [47:0]	Port 45’s	R/W	EAP Unicast Destination Address Register	0
Addr A4h bit [47:0]	Port 46’s	R/W	EAP Unicast Destination Address Register	0
Addr AAh bit [47:0]	Port 47’s	R/W	EAP Unicast Destination Address Register	0
Addr B0h bit [47:0]	IMP Port	R/W	EAP Unicast Destination Address Register	0
Addr B6h bit [47:0]	GE port 0	R/W	EAP Unicast Destination Address Register	0
Addr BCh bit [47:0]	GE port 1	R/W	EAP Unicast Destination Address Register	0
Addr C2h bit [47:0]	GE port 2	R/W	EAP Unicast Destination Address Register	0
Addr C8h bit [47:0]	GE port 3	R/W	EAP Unicast Destination Address Register	0

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Table 270: EAP Unicast Destination Address

Bit	Name	R/W	Description	Default
63:48	RSVD	–	Reserved	0
47:0	EAP_UNI_DA	R/W	EAP unicast DA	0

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Page 41h: 802.1x_1 Registers

Table 271: 802.1x_1 Registers

Addr	Bits	Description
00h–07h	64	"EAP Destination IP Register 0 (Page 41h/Addr 00h–07h)"
08h–1Fh	64	"EAP Destination IP Register 1 (Page 41h/Addr 08h–0Fh)" on page 321
10h	16	"EAP Global Configuration Register (Page 41h/Addr 10h–11h)" on page 321
18h	16	"Learning Counter Control Register (Page 41h/Addr 18h–19h)" on page 322
20h	16	"Port Max Learn Register (Page 41h/Addr 20h–5Fh)" on page 324
60h	16	"Port SA Count Register (Page 41h/Addr 60h–98h)" on page 326

EAP Destination IP Register 0 (Page 41h/Addr 00h–07h)

Table 272: EAP Destination IP Register 0 (Page 41h, Address 00h–07h)

Bit	Name	R/W	Description	Default
63:32	DIP_SUB_REG_0	R/W	EAP Destination IP Subnet register 0	FFFFFFFF
31:0	DIP_MASK_REG_0	R/W	EAP Destination IP Mask register 0	FFFFFFFF

EAP Destination IP Register 1 (Page 41h/Addr 08h–0Fh)

Table 273: EAP Destination IP Register 1 (Page 41h, Address 08h–0Fh)

Bit	Name	R/W	Description	Default
63:32	DIP_SUB_REG_1	R/W	EAP Destination IP Subnet register 1	FFFFFFFF
31:0	DIP_MASK_REG_1	R/W	EAP Destination IP Mask register 1	FFFFFFFF

EAP Global Configuration Register (Page 41h/Addr 10h–11h)

Table 274: EAP Global Configuration Register (Page 41h, Address 10h–11h)

Bit	Name	R/W	Description	Default
15:13	RSVD	RO	Reserved Write default. Ignore on read.	0

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Table 274: EAP Global Configuration Register (Page 41h, Address 10h–11h) (Cont.)

Bit	Name	R/W	Description	Default
12	EN_DHCP	R/W	DHCP Frame Control. When EAP_MODE is set, setting this bit to accept DHCP frames otherwise reject DHCP frames [Default]. • 1 = Accept DHCP frames. • 0 = Reject DHCP frames.	0
11	EN_DIP_1	R/W	Enable Destination IP Address when EAP_MODE is set. When set, IPv4 packet with destination IP address matched with EAP Destination IP register 1 passes.	0
10	EN_DIP_0	R/W	Enable Destination IP Address when EAP_MODE is set. When set, IPv4 packet with destination IP address matched with EAP Destination IP register 0 passes.	0
9	EN_ARP	R/W	Enable ARP frame when EAP_MODE is set. When set, ARP frame (DA = FF-FF-FF-FF-FF-FF and LT = 08-06) passes.	0
8	EN_MAC_22-2F	R/W	Enable (DA = 01-80-c2-00-00-22 ~ 01-80-c2-00-00-2F) frames passed when EAP_MODE is set.	0
7	EN_MAC_21	R/W	Enable (DA = 01-80-c2-00-00-21) frame passed when EAP_MODE is set.	0
6	EN_MAC_20	R/W	Enable (DA = 01-80-c2-00-00-20) frame passed when EAP_MODE is set.	0
5	EN_MAC_11-1F	R/W	Enable (DA = 01-80-c2-00-00-11 ~ 01-80-c2-00-00-1F) frames passed when EAP_MODE is set.	0
4	EN_MAC_10	R/W	Enable (DA = 01-80-c2-00-00-10) frame passed when EAP_MODE is set.	0
3	EN_MAC_02_04-0F	R/W	Enable (DA = 01-80-c2-00-00-02) or (DA = 01-80-c2-00-00-04 ~ 01-80-c2-00-00-040F) frame passed when EAP_MODE is set.	0
2	EN_MAC_BPDU	R/W	Enable BPDU frame passed when EAP_MODE is set.	0
1	RSVD	–	Reserved	0
0	EN_EAP_PT_CHK	R/W	Enable EAP Frame Packet Type Check.	0

Learning Counter Control Register (Page 41h/Addr 18h–19h)

Table 275: Learning counter Control Register (Page 40h, Address 18h–19h)

Bit	Name	R/W	Description	Default
15	START/DONE	R/W	Start/Done command. Write 1 to initiate software learning counter control.	0

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Table 275: Learning counter Control Register (Page 40h, Address 18h–19h) (Cont.)

Bit	Name	R/W	Description	Default
14:13	ACC_CTRL	R/W	Access Control 11 = Reset to 0 in corresponding port 10 = decrease by 1 in corresponding port 01 = increase by 1 in corresponding port 00 = no operation	0
12:6	RSVD	–	Reserved	0
5:0	PORT_NUMBER	R/W	Port Number	0

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Port Max Learn Register (Page 41h/Addr 20h–5Fh)

Table 276: Port Max Learn Register (Page 41h/Addr 20h–5Fh)

Address	Port	R/W	Description	Default
Addr 20h–21h bit [15:0]	Port 24	R/W	Max Learn Number of Addresses	0x1fff
Addr 22h–23h bit [15:0]	Port 25	R/W	Max Learn Number of Addresses	0x1fff
Addr 24h–25h bit [15:0]	Port 26	R/W	Max Learn Number of Addresses	0x1fff
Addr 26h–27h bit [15:0]	Port 27	R/W	Max Learn Number of Addresses	0x1fff
Addr 28h–29h bit [15:0]	Port 28	R/W	Max Learn Number of Addresses	0x1fff
Addr 2Ah–2Bh bit [15:0]	Port 29	R/W	Max Learn Number of Addresses	0x1fff
Addr 2Ch–2Dh bit [15:0]	Port 30	R/W	Max Learn Number of Addresses	0x1fff
Addr 2Eh–2Fh bit [15:0]	Port 31	R/W	Max Learn Number of Addresses	0x1fff
Addr 30h–31h bit [15:0]	Port 32	R/W	Max Learn Number of Addresses	0x1fff
Addr 32h–33h bit [15:0]	Port 33	R/W	Max Learn Number of Addresses	0x1fff
Addr 34h–35h bit [15:0]	Port 34	R/W	Max Learn Number of Addresses	0x1fff
Addr 36h–37h bit [15:0]	Port 35	R/W	Max Learn Number of Addresses	0x1fff
Addr 38h–39h bit [15:0]	Port 36	R/W	Max Learn Number of Addresses	0x1fff
Addr 3Ah–3Bh bit [15:0]	Port 37	R/W	Max Learn Number of Addresses	0x1fff
Addr 3Ch–3Dh bit [15:0]	Port 38	R/W	Max Learn Number of Addresses	0x1fff
Addr 3Eh–3Fh bit [15:0]	Port 39	R/W	Max Learn Number of Addresses	0x1fff
Addr 40h–41h bit [15:0]	Port 40	R/W	Max Learn Number of Addresses	0x1fff
Addr 42h–43h bit [15:0]	Port 41	R/W	Max Learn Number of Addresses	0x1fff
Addr 44h–45h bit [15:0]	Port 42	R/W	Max Learn Number of Addresses	0x1fff
Addr 46h–47h bit [15:0]	Port 43	R/W	Max Learn Number of Addresses	0x1fff
Addr 48h–49h bit [15:0]	Port 44	R/W	Max Learn Number of Addresses	0x1fff
Addr 4Ah–4Bh bit [15:0]	Port 45	R/W	Max Learn Number of Addresses	0x1fff
Addr 4Ch–4Dh bit [15:0]	Port 46	R/W	Max Learn Number of Addresses	0x1fff
Addr 4Eh–4Fh bit [15:0]	Port 47	R/W	Max Learn Number of Addresses	0x1fff
Addr 50h–51h bit [15:0]	IMP Port	R/W	Max Learn Number of Addresses	0x1fff
Addr 52h–53h bit [15:0]	GigaPort G0	R/W	Max Learn Number of Addresses	0x1fff
Addr 54h–55h bit [15:0]	GigaPort G1	R/W	Max Learn Number of Addresses	0x1fff
Addr 56h–57h bit [15:0]	GigaPort G2	R/W	Max Learn Number of Addresses	0x1fff
Addr 58h–59h bit [15:0]	GigaPort G3	R/W	Max Learn Number of Addresses	0x1fff

Table 277: Max Learn Number of Address Register

Bit	Name	R/W	Description	Default
15:13	RSVD	RO	Reserved Write default. Ignore on read.	0

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Table 277: Max Learn Number of Address Register

Bit	Name	R/W	Description	Default
12:0	MAX_MAC_NUMBER	R/W	Dynamic Mode Maximum Number of MAC for each port.	0x1fff

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Port SA Count Register (Page 41h/Addr 60h–98h)

Table 278: Port SA Count Register (Page: 41h, Address 60h–98h)

Address	Port	R/W	Description	Default
Addr 60h–61h bit [15:0]	Port 24	R/W	SA count per port	0
Addr 62h–63h bit [15:0]	Port 25	R/W	SA count per port	0
Addr 64h–65h bit [15:0]	Port 26	R/W	SA count per port	0
Addr 66h–67h bit [15:0]	Port 27	R/W	SA count per port	0
Addr 68h–69h bit [15:0]	Port 28	R/W	SA count per port	0
Addr 6Ah–6Bh bit [15:0]	Port 29	R/W	SA count per port	0
Addr 6Ch–6Dh bit [15:0]	Port 30	R/W	SA count per port	0
Addr 6Eh–6Fh bit [15:0]	Port 31	R/W	SA count per port	0
Addr 70h–71h bit [15:0]	Port 32	R/W	SA count per port	0
Addr 72h–73h bit [15:0]	Port 33	R/W	SA count per port	0
Addr 74h–75h bit [15:0]	Port 34	R/W	SA count per port	0
Addr 76h–77h bit [15:0]	Port 35	R/W	SA count per port	0
Addr 78h–79h bit [15:0]	Port 36	R/W	SA count per port	0
Addr 7Ah–7Bh bit [15:0]	Port 37	R/W	SA count per port	0
Addr 7Ch–7Dh bit [15:0]	Port 38	R/W	SA count per port	0
Addr 7Eh–7Fh bit [15:0]	Port 39	R/W	SA count per port	0
Addr 80h–81h bit [15:0]	Port 40	R/W	SA count per port	0
Addr 82h–83h bit [15:0]	Port 41	R/W	SA count per port	0
Addr 84h–85h bit [15:0]	Port 42	R/W	SA count per port	0
Addr 86h–87h bit [15:0]	Port 43	R/W	SA count per port	0
Addr 88h–89h bit [15:0]	Port 44	R/W	SA count per port	0
Addr 8Ah–8Bh bit [15:0]	Port 45	R/W	SA count per port	0
Addr 8Ch–8Dh bit [15:0]	Port 46	R/W	SA count per port	0
Addr 8Eh–8Fh bit [15:0]	Port 47	R/W	SA count per port	0
Addr 90h–91h bit [15:0]	IMP Port	R/W	SA count per port	0
Addr 92h–93h bit [15:0]	GigaPort G0	R/W	SA count per port	0
Addr 94h–95h bit [15:0]	GigaPort G1	R/W	SA count per port	0
Addr 96h–97h bit [63:0]	GigaPort G2	R/W	SA count per port	0
Addr 98h–99h bit [63:0]	GigaPort G3	R/W	SA count per port	0

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Table 279: Port SA Count register

Bit	Name	R/W	Description	Default
15:13	RSVD	RO	Reserved. Write default. Ignore on read.	0
12:0	CUR_SA_CNT	RO	Current SA count	0

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Page 43h: Rate Control Registers

Table 280: Rate Control Registers (Page 43h)

Addr	Bits	Description
00h	8	"Rate Control Memory Access Register (Page 43h/Addr 00h)" on page 328
01h	8	"Rate Control Memory Port Register (Page 43h/Addr 01h)" on page 329
10h–13h	32	"Rate Control Memory Data Register 0 (Page 43h/Addr 10h–13h)" on page 330
14h–17h	32	"Rate Control Memory Data Register 1 (Page 43h/Addr 14h–17h)" on page 331
18h–1Bh	32	"Rate Control Memory Data Register 2 (Page 43h/Addr 18h–1Bh)" on page 332
1Ch–1Fh	32	"Rate Control Memory Data Register 3 (Page 43h/Addr 1Ch–1Fh)" on page 333
20h–23h	32	"Rate Control Memory Data Register 4 (Page 43h/Addr 20h–23h)" on page 333
F0h–F7h	64	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	8	SPI Status
FFh	8	Page Register

Rate Control Memory Access Register (Page 43h/Addr 00h)

Table 281: Rate Control Memory Access Register (Page: 43h, Address 00h)

Bit	Name	R/W	Description	Default
7	MEM_RW_START_DONE	R/W	Start/Done Command bit Write 1 to initiate a read or write process for a rate control memory. It will reset itself when the operation is completed.	0
6:3	RSVD	RO	• Reserved	0
2	EXTR_LNGTH_EN	R/W	Extra length calculate enable (only used for Ingress Rate Control) • 0 = disable • 1 = enable	0
1	INGRESS_EGRESS_IND	R/W	Ingress or Egress Indication • 0 = Ingress Rate Control Memory Access • 1 = Egress Rate Control Memory Access	0
0	READ_WRITE	R/W	Rate Control Memory Read/ Write • 0 = Write • 1 = Read	0

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Rate Control Memory Port Register (Page 43h/Addr 01h)

Table 282: Rate Control Memory Port Register (Page: 43h, Address 01h)

Bit	Name	R/W	Description	Default
7:6	RSVD	–	Reserved	0
5:0	RCM_PORT	R/W	Rate Control Memory Port Number • 53~63: Reserved • 52: Giga Port G3 • 51: Giga Port G2 • 50: Giga Port G1 • 49: Giga Port G0 • 48: IMP Port • 24~47: 10/100 Ports [port 24-port 47] • 0~23: Reserved	0

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Rate Control Memory Data Register 0 (Page 43h/Addr 10h–13h)

Table 283: Rate Control Memory Data Register 0 (Page: 43h, Address 10h)

Bit	Name	R/W	Description	Default
31	ING_EG_RC_EN	R/W	Ingress and/or Egress Rate Control Enable • 0 = Disable both Ingress and/or Egress Rate Control • 1 = Enable both Ingress and/or Egress Rate Control	0
30	ING_RC_DROP_EN	R/W	This bit only applies to Ingress • 0 = when over rate, pause. • 1 = when over rate, drop	0
29	RSVD	–	Reserved	0
28:22	ING_RC_PKT_MASK_B0	R/W	This field is only applicable to Ingress Rate Control. Traffic correspond to the bit set will be masked from bucket. • Bit 28 = Unknown SA • Bit 27 = Unicast Destination Lookup Failed Frame • Bit 26 = Multicast Destination Lookup Failed Frame • Bit 25 = Broadcast • Bit 24 = Multicast Reserved Frame • DA = 01-80-c2-00-00-00 ~ 2F • Bit 23 = Multicast Destination Lookup Hit Frame • Bit 22 = Unicast Destination Lookup Hit Frame	0
21:15	BUCKET_SIZE	R/W	For Ingress Rate Control: Bucket size, unit 8 KB (per bucket B0) For Egress Rate Control: Bucket size, unit 8 KB (total per port) ***Note:*** When rate control is enabled, BUCKET_SIZE cannot be set to 0.	0
14	REFRESH_UNIT	R/W	• 0 = 62.5 Kbps • 1 = 1 Mbps For Ingress Rate Control: per bucket B0 For Egress Rate Control: total per port	0
13:0	REFRESH_CNT	R/W	Refresh Count For Ingress Rate Control: per bucket B0 For Egress Rate Control: total per port ***Note:*** When rate control is enabled, REFRESH_CNT cannot be set to 0.	0

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Rate Control Memory Data Register 1 (Page 43h/Addr 14h–17h)

Table 284: Rate Control Memory Data Register 1 (Page: 43h, Address 14h)

Bit	Name	R/W	Description	Default
31	EG_RC_EN	R/W	Per Queue Egress Rate Control Enable • 0 = Per Queue Egress Rate Control disable • 1 = Per Queue Egress Rate Control enable	0
30:29	RSVD	–	Reserved	0
28:22	ING_RC_PKT_MASK_B1	R/W	This field is only applicable to Ingress Rate Control. Traffic correspond to the bit set will be masked from bucket. • Bit 28 = Unknown SA • Bit 27 = Unicast Destination Lookup Failed Frame • Bit 26 = Multicast Destination Lookup Failed Frame • Bit 25 = Broadcast • Bit 24 = Multicast Reserved Frame • DA = 01-80-c2-00-00-00 ~ 2F • Bit 23 = Multicast Destination Lookup Hit Frame • Bit 22 = Unicast Destination Lookup Hit Frame	0
21:15	BUCKET_SIZE	R/W	For Ingress Rate Control: Bucket size, unit 8 KB (per bucket B1) For Egress Rate Control: Bucket size, unit 8 KB (for Queue 0) ***Note:*** When rate control is enabled, BUCKET_SIZE cannot be set to 0.	0
14	REFRESH_UNIT	R/W	• 0 = 62.5 Kbps • 1 = 1 Mbps For Ingress Rate Control: per bucket B1 For Egress Rate Control: for Queue 0	0
13:0	REFRESH_CNT	R/W	Refresh Count, For Ingress Rate Control: per bucket B1 For Egress Rate Control: for Queue 0 ***Note:*** When rate control is enabled, REFRESH_CNT cannot be set to 0.	0

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Rate Control Memory Data Register 2 (Page 43h/Addr 18h–1Bh)

Table 285: Rate Control Memory Data Register 2 (Page: 43h, Address 18h)

Bit	Name	R/W	Description	Default
31:29	RSVD	–	Reserved	0
28:22	ING_RC_PKT_MASK_B2	R/W	This field is only applicable to Ingress Rate Control. Traffic correspond to the bit set will be masked from bucket. • Bit 28 = Unknown SA • Bit 27 = Unicast Destination Lookup Failed Frame • Bit 26 = Multicast Destination Lookup Failed Frame • Bit 25 = Broadcast • Bit 24 = Multicast Reserved Frame • DA = 01-80-c2-00-00-00–2F • Bit 23 = Multicast Destination Lookup Hit Frame • Bit 22 = Unicast Destination Lookup Hit Frame	0
21:15	BUCKET_SIZE	R/W	For Ingress Rate Control: Bucket size, unit 8 KB (per bucket B2) For Egress Rate Control: Bucket size, unit 8 KB (for Queue 1) ***Note:*** When rate control is enabled, BUCKET_SIZE cannot be set to 0.	0
14	REFRESH_UNIT	R/W	• 0 = 62.5 Kbps • 1 = 1 Mbps For Ingress Rate Control: per bucket B2 For Egress Rate Control: for Queue 1	0
13:0	REFRESH_CNT	R/W	Refresh Count, For Ingress Rate Control: per bucket B2 For Egress Rate Control: for Queue 1 ***Note:*** When rate control is enabled, REFRESH_CNT cannot be set to 0.	0

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Rate Control Memory Data Register 3 (Page 43h/Addr 1Ch–1Fh)

Table 286: Rate Control Memory Data Register 3 (Page: 43h, Address 1Ch)

Bit	Name	R/W	Description	Default
31:22	RSVD	–	Reserved	0
21:15	BUCKET_SIZE	R/W	For Egress Rate Control: Bucket size, unit 8 KB (for Queue 2) ***Note:*** When rate control is enabled, BUCKET_SIZE cannot be set to 0.	0
14	REFRESH_UNIT	R/W	• 0 = 62.5 Kbps • 1 = 1 Mbps For Egress Rate Control: for Queue 2	0
13:0	REFRESH_CNT	R/W	Refresh Count for Egress Rate Control: for Queue 2 ***Note:*** When rate control is enabled, REFRESH_CNT cannot be set to 0.	0

Rate Control Memory Data Register 4 (Page 43h/Addr 20h–23h)

Table 287: Rate Control Memory Data Register 4 (Page: 43h, Address 20h)

Bit	Name	R/W	Description	Default
31:22	RSVD	–	Reserved	0
21:15	BUCKET_SIZE	R/W	For Egress Rate Control: Bucket size, unit 8 KB (for Queue 3) ***Note:*** When rate control is enabled, BUCKET_SIZE cannot be set to 0.	0
14	REFRESH_UNIT	R/W	• 0 = 62.5 Kbps • 1 = 1 Mbps For Egress Rate Control: for Queue 3	0
13:0	REFRESH_CNT	R/W	Refresh Count for Egress Rate Control: for Queue 3 ***Note:*** When rate control is enabled, REFRESH_CNT cannot be set to 0.	0

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Page 45h: 802.1s Multiple Spanning Tree Registers

Table 288: 802.1s Multiple Spanning Tree Registers (Page 45h)

Addr	Bits	Description
00h	8	Multiple Spanning Trees "MST Control Register (Page 45h/Addr 00h)" on page 334
01h–03h	Reserved	
04h–07h	32	"Age-out Control Register (Page 45h/Addr 04h–07h)" on page 335
08h–EFh	Reserved	
F0h–F7h	64	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	8	SPI Status
FFh	8	Page Register

MST Control Register (Page 45h/Addr 00h)

Table 289: MST Control Register (Page 45h, Address 00h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W	Fast Ageing Start/Done Command. Write as 1 to initiate the fast ageing process following the AGE_MODE setting. When fast ageing process is done, this bit clears to 0.	0
6	RSVD	RO	Reserved. Write default. Ignore on read.	0
5	UPD_STATIC_EN	R/W	1 = AGE bit in static entry will be updated 0 = AGE bit in static entry will not be updated (default)	0
4	AGE_STATIC_EN	R/W	Static Entry Ageing Enable. 1 = Allow ageing static entries in ARL. 0 = Normal mode.	
3	AGE_MODE_SPT	R/W	Ageing Mode Control Per Spanning Tree. Follow the SPT_AGE_EN setting.	0
2	AGE_MODE_VLAN	R/W	Ageing Mode Control Per VLAN. Follow the AGE_EN_VID setting.	0
1	AGE_MODE_PORT	R/W	Ageing Mode Control. Per-port, follows the per-port AGE_EN_PORT setting.	0

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Table 289: MST Control Register (Page 45h, Address 00h)

Bit	Name	R/W	Description	Default
0	En_802_1s	R/W	Spanning Tree Enable. • 1 = Support 802.1s (MST); spanning tree status is fetched from MST_table. • 0 = Only one spanning tree supported. (Original mode).	0

Age-out Control Register (Page 45h/Addr 04h–07h)

Table 290: Age-Out Control Register (Page 45h, Address 04h–07h)

Bit	Name	R/W	Description	Default
31:26	RSVD	RO	Reserved. Write default. Ignore on read.	0
25:18	SPT_AGE_EN	R/W	MAC Address Ageing Control Per SPD ID. These bits specify a SPD ID. MAC Addresses that are associated with the SPD ID are age out in the auto ageing process.	0
17:6	AGE_EN_VID	R/W	MAC Address Ageing Control Per VID. These bits specify a VID. MAC Addresses that are associated with the VID are age out in the auto ageing process.	0
5:0	AGE_EN_PORT	R/W	MAC Address Ageing Control Per Port. These bits specify a port number. MAC Addresses that are associated with the port number are aged out in the auto ageing process. • 52 = Port number for GigaPort G3 • 51 = Port number for GigaPort G2 • 50 = Port number for GigaPort G1 • 49 = Port number for GigaPort G0 • 48 = Port number for IMP • 24~47 = Port numbers for 10/100 ports [port 24-port 47] • 0~ 23 = Reserved	0

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Page 68h–84h: Port MIB Registers

Per-port MIB counters reside within pages 68h through 84h. The contents of each page is listed in Table 291.

- Page 68h contains port MIB counters for port 24
- Page 69h contains port MIB counters for port 25
- ...
- Page 78h contains port MIB counters for port 40
- ...
- Page 80h contains port MIB counters for IMP port
- Page 81h contains port MIB counters for G0 port
- Page 82h contains port MIB counters for G1 port
- Page 83h contains port MIB counters for G2 port
- Page 84h contains port MIB counters for G3 port

Table 291: Port MIB Registers (Page 68h–84h)

Address	*Bits*	*Description*
00h–07h	64	TxOctets
08h–0Bh	32	TxDropPkts
0Ch–0Fh	32	TxPausePkts
10h–13h	32	TxBroadcastPkts
14h–17h	32	TxMulticastPkts
18h–1Bh	32	TxUnicastPkts
1Ch–1Fh	32	TxCollisions[a]
20h–23h	32	TxSingleCollision[a]
24h–27h	32	TxMultipleCollision[a]
2Ch–2Fh	32	TxLateCollision[a]
34h–37h	32	TxFrameInDisc
38h–3Bh	32	TxQoS0Pkts
3Ch–43h	64	TxQoS0Octets
0x44h–47h	32	TxQoS1Pkts
0x48h–4Fh	64	TxQoS1Octets
0x50h–53h	32	TxQoS2Pkts
0x54h–5Bh	64	TxQoS2Octets
0x5Ch–5Fh	32	TxQoS3Pkts
0x60h–67h	64	TxQoS3Octets
68h–6Fh	64	RxOctets
70h–73h	32	RxUndersizePkts[a]
74h–77h	32	RxPausePkts

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Table 291: Port MIB Registers (Page 68h–84h) (Cont.)

Address	*Bits*	*Description*
78h–7Bh	32	Pkts64Octets
7Ch–7Fh	32	Pkts65to127Octets
80h–83h	32	Pkts128to255Octets
84h–87h	32	Pkts256to511Octets
88h–8Bh	32	Pkts512to1023Octets
8Ch–8Fh	32	Pkts1024toMaxOctets (Revision B silicon)
		Pkts1024to1522Octets (Revision A silicon)
90h–93h	32	RxOversizePkts
94–97h	32	RxJabbers
98h–9Bh	32	RxAlignmentErrors
9Ch–9Fh	32	RxFCSErrors
A0h–A7h	64	RxGoodOctets
ACh–AFh	32	RxUnicastPkts
B0h–B3h	32	RxMulticastPkts
B4h–B7h	32	RxBroadcastPkts
B8h–BBh	32	RxSAChanges
BCh–BFh	32	RxFragments[a]
C0h–C3h	32	RxExcessSizeDisc
C4h–C7h	32	RXSymbolError
C8h–CBh	32	RxDiscPkts
CCh–EFh	Reserved	
F0h–F7h	64	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	8	SPI Status
FFh	32	Page Register

a = To save bandwidth, 3-bit counters are used internally to accumulate all (collision, undersize, or fragment) events at local ports. When either the 3-bit counters count to 7 or a normal packet (64-byte or longer) is received, the corresponding MIB counters update once.

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Page 85h: Snapshot Port MIB Registers

Snapshot Port MIB counters reside within pages 85h. The contents is listed in Table 292.

Table 292: Snapshot Port MIB Registers (Page 85h)

Address	*Bits*	*Description*
00h–07h	64	TxOctets
08h–0Bh	32	TxDropPkts
0Ch–0Fh	32	TxPausePkts
10h–13h	32	TxBroadcastPkts
14h–17h	32	TxMulticastPkts
18h–1Bh	32	TxUnicastPkts
1Ch–1Fh	32	TxCollisions[a]
20h–23h	32	TxSingleCollision[a]
24h–27h	32	TxMultipleCollision[a]
28h–2Bh	32	TxDeferredTransmit
2Ch–2Fh	32	TxLateCollision[a]
30h–33h	32	TxExcessiveCollision[a]
34h–37h	32	TxFrameInDisc
38h–3Bh	32	TxQoS0Pkts
3Ch–43h	64	TxQoS0Octets
0x44h–47h	32	TxQoS1Pkts
0x48h–4Fh	64	TxQoS1Octets
0x50h–53h	32	TxQoS2Pkts
0x54h–5Bh	64	TxQoS2Octets
0x5Ch–5Fh	32	TxQoS3Pkts
0x60h–67h	64	TxQoS3Octets
68h–6Fh	64	RxOctets
70h–73h	32	RxUndersizePkts[a]
74h–77h	32	RxPausePkts
78h–7Bh	32	Pkts64Octets
7Ch–7Fh	32	Pkts65to127Octets
80h–83h	32	Pkts128to255Octets
84h–87h	32	Pkts256to511Octets
88h–8Bh	32	Pkts512to1023Octets
8Ch–8Fh	32	Pkts1024toMaxOctets (Revision B silicon)
		Pkts1024to1522Octets (Revision A silicon)
90h–93h	32	RxOversizePkts

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Table 292: Snapshot Port MIB Registers (Page 85h) (Cont.)

Address	Bits	Description
94–97h	32	RxJabbers
98h–9Bh	32	RxAlignmentErrors
9Ch–9Fh	32	RxFCSErrors
A0h–A7h	64	RxGoodOctets
A8h–ABh	32	RxDropPkts
ACh–AFh	32	RxUnicastPkts
B0h–B3h	32	RxMulticastPkts
B4h–B7h	32	RxBroadcastPkts
B8h–BBh	32	RxSAChanges
BCh–BFh	32	RxFragments[a]
C0h–C3h	32	RxExcessSizeDisc
C4h–C7h	32	RXSymbolError
C8h–CBh	32	RxDiscPkts
CCh–EFh	Reserved	
F0h–F7h	64	SPI Data I/O[0:7]
F8h–FDh	Reserved	
FEh	8	SPI Status
FFh	32	Page Register

a = To save bandwidth, 3-bit counters are used internally to accumulate all (collision, undersize, or fragment) events at local ports. When either the 3-bit counters count to 7 or a normal packet (64-byte or longer) is received, the corresponding MIB counters update once.

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Page A0h–B7h: FE Ports 24-47 MII Registers

See "MDC/MDIO Interface" on page 118 for more information on PHY addressing.

Table 293: FE Port MII Registers Page Versus PHY

Page	*Port #*	*Hardware PHY address*
A0h	24	00000
A1h	25	00001
A2h	26	00010
A3h	27	00011
A4h	28	00100
A5h	29	00101
A6h	30	00110
A7h	31	00111
A8h	32	01000
A9h	33	01001
AAh	34	01010
ABh	35	01011
ACh	36	01101
ADh	37	01100
AEh	38	01101
AFh	39	01110
B0h	40	01111
B1h	41	10000
B2h	42	10001
B3h	43	10010
B4h	44	10011
B5h	45	10100
B6h	46	10101
B7h	47	10110

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Table 294: Port MII Registers (Page A0h–B7h)

Address	*Bits*	*Description*
00h–01h	16	"MII Control Register (Page A0h–B7h/Addr 00h–01h)" on page 342
02h–03h	16	"MII Status Register (Page A0h–B7h/Addr 02h–03h)" on page 344
04h–07h	32	"PHY Identifier Registers (Page A0h–B7h/Addr 04h–07h)" on page 346

Table 294: Port MII Registers (Cont.)(Page A0h–B7h)

Address	Bits	Description
08h–09h	16	"Auto-Negotiation Advertisement Register (Page A0h–B7h/Addr 08h–09h)" on page 346
0Ah–0Bh	16	"Auto-Negotiation Link Partner Ability Register (Page A0h–B7h/Addr 0Ah–0Bh)" on page 347
0Ch–0Dh	16	"Auto-Negotiation Expansion Register (Page A0h–B7h/Addr 0Ch–0Dh)" on page 349
0Eh–0Fh	16	"Auto-Negotiation Next Page Register (Page A0h–B7h/Addr 0Eh–0Fh)" on page 350
10h–11h	16	"Link Partner Next Page Register (Page A0h–B7h/Addr 10h–11h)" on page 351
12h–1Fh	Reserved	
20h–3Fh	–	Reserved

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MII Control Register (Page A0h–B7h/Addr 00h–01h)

Table 295: MII Control Register (Pages A0h–B7h, Address 00h–01h)

Bit	Name	R/W	Description	Default
15	Reset	R/W (SC)	• 1 = PHY reset. • 0 = Normal operation.	0
14	Loopback	R/W	• 1 = Loopback mode. • 0 = Normal operation.	0
13	Forced Speed Selection	R/W	• 1 = 100 Mbps. • 0 = 10 Mbps.	1
12	Auto-negotiation Enable	R/W	• 1 = Auto-negotiation enable. • 0 = Auto-negotiation disable.	1
11	Power Down	RO	• 0 = Normal operation. • The BCM53262M does not implement a low-power mode.	0
10	Isolate	R/W	• 1 = Electrically isolate PHY from MII. • 0 = Normal operation.	0
9	Restart Auto-negotiation	R/W (SC)	• 1 = Restart auto-negotiation process. • 0 = Normal operation.	0
8	Duplex Mode	R/W	• 1 = Full-duplex. • 0 = Half-duplex.	0
7:0	Reserved	RO	Ignore when read.	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation.

Reset

To reset an individual part PHY, the BCM53262M by software control, a 1 must be written to bit 15 of the Control register using an MII write operation. The bit clears itself after the reset process is complete, and need not be cleared using a second MII write. Writes to other Control register bits have no effect until the reset process is completed, which requires approximately 1 µs. Writing a 0 to this bit has no effect. Because this bit is self-clearing, after a few cycles from a write operation, it returns a 0 when read.

Loopback

An individual part of the BCM53262M can be placed into loopback mode by writing a 1 to bit 14 of the Control register. The loopback mode can be cleared by writing a 0 to bit 14 of the control register, or by resetting the chip. When this bit is read, it returns a 1 when the chip is in software-controlled loopback modes; otherwise it returns a 0.

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Forced Speed Selection

If auto-negotiation is enabled, this bit has no effect on the speed selection. However, if auto-negotiation is disabled by software control, the operating speed of the BCM53262M port can be forced by writing the appropriate value to bit 13 of the Control register. Writing a 1 to this bit forces 100Base-X operation, while writing a 0 forces 10Base-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. To read the overall state of forced speed selection, including both hardware and software control, use bit 8 of the Auxiliary Control register.

Auto-Negotiation Enable

Auto-negotiation is enabled by default. If bit 12 of the Control register is written with a value of 0, auto-negotiation is disabled by software control. Writing a 1 to the same bit of the Control register or resetting the chip re-enables auto-negotiation. When read, this bit returns the value most recently written to this location, or 1 if it has not been written since the last chip reset.

Power Down

The BCM53262M does not implement a low-power mode.

Isolate

Each individual PHY can be isolated from its Media Independent Interface by writing a 1 to bit 10 of the Control register. All MII outputs are ri-stated and all MII inputs are ignored. Because the MII management interface is still active, the isolate mode can be cleared by writing a 0 to bit 10 of the control register, or by resetting the chip. When this bit is read, it returns a 1 when the chip is in isolate mode; otherwise it returns a 0.

Restart Auto-Negotiation

Bit 9 of the Control register is a self-clearing bit that allows the auto-negotiation process to be restarted, regardless of the current status of the auto-negotiation state machine. For this bit to have an effect, auto-negotiation must be enabled. Writing a 1 to this bit restarts the auto-negotiation, while writing a 0 to this bit has no effect. Because the bit is self-clearing after only a few cycles, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Auxiliary Multiple PHY register.

Duplex Mode

By default, at reset this bit indicates BCM53262M half-duplex mode. If the Auto-negotiation is enabled, this bit has no effect on the duplex selection. The chip can be forced into full-duplex mode by writing a 1 to bit 8 of the Control register while auto-negotiation is disabled. Half-duplex mode can be resumed by writing a 0 to bit 8 of the control register, or by resetting the chip.

Reserved Bits

All reserved MII register bits must be written as 0 at all times. Ignore the BCM53262M output when these bits are read.

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MII Status Register (Page A0h–B7h/Addr 02h–03h)

Table 296: MII Status Register (Pages A0h–B7h, Address 02h–03h)

Bit	Name	R/W	Description	Default
15	100Base-T4 Capability	RO	0 = Not 100Base-T4 capable.	0
14	100Base-TX FDX Capability	RO	1 = 100Base-TX full-duplex capable.	1
13	100Base-TX Capability	RO	1 = 100Base-TX half-duplex capable.	1
12	10Base-T FDX Capability	RO	1 = 10Base-T full-duplex capable.	1
11	10Base-T Capability	RO	1 = 10Base-T half-duplex capable.	1
10:7	Reserved	RO	Ignore when read.	0
6	MF Preamble Suppression	R/W	• 1 = Preamble may be suppressed. • 0 = Preamble always required.	0
5	Auto-negotiation Complete	RO	• 1 = Auto-negotiation process completed. • 0 = Auto-negotiation process not completed.	0
4	Remote Fault	RO LH	• 1 = Remote/far-end fault condition detected. • 0 = No remote/far-end fault condition detected.	0
3	Auto-negotiation Capability	RO	• 1 = Auto-negotiation capable. • 0 = Not auto-negotiation capable.	1
2	Link Status	RO LL	• 1 = Link is up (Link Pass state). • 0 = Link is down (Link Fail state).	0
1	Jabber Detect	RO LH	• 1 = Jabber condition detected. • 0 = No jabber condition detected.	0
0	Extended Capability	RO	1 = Extended register capable.	1

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.

100Base-T4 Capability

The BCM53262M is not capable of 100Base-T4 operation, and returns a 0 when bit 15 of the status register is read.

100Base-X Full-Duplex Capability

The BCM53262M is capable of 100Base-X full-duplex operation, and returns a 1 when bit 14 of the Status register is read.

100Base-X Half-Duplex Capability

The BCM53262M is capable of 100Base-X half-duplex operation, and returns a 1 when bit 13 of the Status register is read.

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10Base-T Full-Duplex Capability

The BCM53262M is capable of 10Base-T full-duplex operation, and returns a 1 when bit 12 of the Status register is read.

10Base-T Half-Duplex Capability

The BCM53262M is capable of 10Base-T half-duplex operation, and returns a 1 when bit 11 of the Status register is read.

Reserved Bit

Ignore the BCM53262M output when these bits are read.

MF Preamble Suppression

This bit is the only writable bit in the Status register. Setting this bit to a 1 allows subsequent MII management frames to be accepted with or without the standard preamble pattern. When Preamble Suppression is enabled, only 2 preamble bits are required between successive Management Commands, instead of the normal 32.

Auto-Negotiation Complete

Bit 5 of the Status register returns a 1 if the auto-negotiation process has been completed and the contents of registers 4, 5 and 6 are valid.

Remote Fault

When set at the completion of auto-negotiation, indicates that a remote fault condition has been signaled by the link partner. When set in 100Base-FX mode, indicates that a far-end fault condition has been detected. This bit is latched high, and self-clears when read. Is immediately set once again in FX mode after clearing if the far-end fault condition remains true.

Auto-Negotiation Capability

The BCM53262M can perform IEEE auto-negotiation, and returns a 1 when bit 4 of the Status register is read, regardless of whether the auto-negotiation function has been disabled.

Link Status

The BCM53262M returns a 1 on bit 2 of the Status register when the link state machine is in Link Pass, indicating that a valid link has been established. Otherwise, it returns 0. When a link failure occurs after the Link Pass state has been entered, the Link Status bit is latched at 0 and remains so until the bit is read. After the bit is read, it becomes 1 if the Link Pass state has been entered again.

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Jabber Detect

10Base-T operation only. The BCM53262M returns a 1 on bit 1 of the Status register if a jabber condition has been detected. After the bit is read, or if the chip is reset, it reverts to 0.

Extended Capability

The BCM53262M supports extended capability registers, and returns a 1 when bit 0 of the Status register is read. Several extended registers have been implemented in the BCM53262M, and their bit functions are defined later in this section.

PHY Identifier Registers (Page A0h–B7h/Addr 04h–07h)

Table 297: PHY Identifier Registers (Pages A0h–B7h, Addresses 04h–05h and 06h–07h)

Bit	Name	R/W	Description	Default
15:0	MII Address 00010	RO	PHYID HIGH	0143h
15:0	MII Address 00011	RO	PHYID LOW	BF2Nh[a]

a. Refer to Table 178 on page 257 for the value of N and the associated chip revision.

Auto-Negotiation Advertisement Register (Page A0h–B7h/Addr 08h–09h)

Table 298: Auto-Negotiation Advertisement Register (Pages A0h–B7h, Address 08h–09h)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	• 1 = Next Page Operation supported. • 0 = Next Page Operation disabled.	0
14	Reserved	RO	Ignore when Read.	–
13	Remote Fault	R/W	1 = Transmit Remote Fault.	0
12:11	Reserved Technologies	RO	Ignore when Read.	–
10	Advertise Pause Capability	R/W	1 = Pause Operation for full-duplex.	1
9	Advertise 100Base-T4	R/W	0 = Do Not Advertise T4 Capability.	0
8	Advertise 100Base-X FDX	R/W	• 1 = Advertise 100Base-X full-duplex. • 0 = Do Not Advertise 100Base-X full-duplex.	1
7	Advertise 100Base-X	R/W	1 = Advertise 100Base-X.	1
6	Advertise 10Base-T FDX	R/W	• 1 = Advertise 10Base-T full-duplex. • 0 = Do Not Advertise 10Base-T full-duplex.	1
5	Advertise 10Base-T	R/W	1 = Advertise 10Base-T.	1
4:0	Advertise Selector Field	R/W	Fixed value: indicates 802.3.	00001

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Next Page

The BCM53262M supports the Next Page function. To enable this operation, write a 1 to this bit.

Remote Fault

Writing a 1 to bit 13 of the Advertisement register sends a Remote Fault indicator to the Link Partner during auto-negotiation. Writing a 0 to this bit or resetting the chip clears the Remote Fault transmission bit. This bit returns the value last written to it, or else 0 if no write has been completed since the last chip reset.

Reserved Bits

Ignore output when read.

Pause Operation for Full-Duplex Links

The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate Pause Capability to its Link Partner and has no effect on PHY operation.

Advertisement Bits

Use bits 9:5 of the Advertisement register to customize the ability information transmitted to the Link Partner. The default value for each bit reflects the abilities of the BCM53262M. By writing a 1 to any of the bits, the corresponding ability is transmitted to the Link Partner. Writing a 0 to any bit causes the corresponding ability to be suppressed from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset.

Selector Field

Bits 4:0 of the Advertisement register contain the value 00001, indicating that the chip belongs to the 802.3 class of PHY transceivers

Auto-Negotiation Link Partner Ability Register (Page A0h–B7h/Addr 0Ah–0Bh)

Table 299: Auto-Negotiation Link Partner Ability Register (Pages A0h–B7h, Address 0Ah–0Bh)

Bit	Name	R/W	Description	Default
15	LP Next Page	RO	Link Partner next page bit.	0
14	LP Acknowledge	RO	Link Partner acknowledge bit.	0
13	LP Remote Fault	RO	Link Partner remote fault indicator.	0
12:11	Reserved Technologies	RO	Ignore when read.	000

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Table 299: Auto-Negotiation Link Partner Ability Register (Pages A0h–B7h, Address 0Ah–0Bh)

Bit	Name	R/W	Description	Default
10	LP Advertise Pause	RO	Link Partner has Pause Capability.	0
9	LP Advertise 100Base-T4	RO	Link Partner has 100Base-T4 capability.	0
8	LP Advertise 100Base-X FDX	RO	Link Partner has 100Base-X FDX capability.	0
7	LP Advertise 100Base-X	RO	Link Partner has 100Base-X capability.	0
6	LP Advertise 10Base-T FDX	RO	Link Partner has 10Base-T FDX capability.	0
5	LP Advertise 10Base-T	RO	Link Partner has 10Base-T capability.	0
4:0	Link Partner Selector Field	RO	Link Partner selector field.	00000

The values contained in the Auto-negotiation Link Partner Ability register are only guaranteed to be valid after auto-negotiation has successfully completed, as indicated by bit 5 of the MII Status register.

Next Page

Bit 15 of the Link Partner Ability register returns a value of 1 when the Link Partner implements the Next Page function and has Next Page information to transmit.

Acknowledge

Bit 14 of the Link Partner Ability register is used by auto-negotiation to indicate that a device has successfully received its Link Partner's Link Code Word.

Remote Fault

Bit 13 of the Link Partner Ability register returns a value of 1 when the Link Partner signals that a remote fault has occurred. The BCM53262M simply copies the value to this register and does not act upon it.

Reserved Bits

Ignore when read.

Pause

Indicates that the Link Partner pause bit is set.

Advertisement Bits

Bits 9:5 of the Link Partner Ability register reflect the abilities of the Link Partner. A 1 on any of these bits indicates that the Link Partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time auto-negotiation is restarted or the BCM53262M is reset.

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Selector Field

Bits 4:0 of the Link Partner Ability register reflect the value of the Link Partner's selector field. These bits are cleared any time auto-negotiation is restarted or the chip is reset.

Auto-Negotiation Expansion Register (Page A0h–B7h/Addr 0Ch–0Dh)

Table 300: Auto-Negotiation Expansion Register (Pages A0h–B7h, Address 0Ch–0Dh)

Bit	Name	R/W	Description	Default
15:5	Reserved	RO	Ignore when read.	
4	Parallel Detection Fault	RO LH	• 1 = Parallel Detection fault. • 0 = No Parallel Detection fault.	0
3	Link Partner Next Page Able	RO	• 1 = Link Partner has Next Page capability. • 0 = Link Partner does not have Next Page capability.	0
2	Next Page Able	RO	• 1 = Next Page is enabled. • 0 = Next Page capability.	–
1	Page Received	RO	• 1 = New page has been received. • 0 = New page has not been received.	0
0	Link Partner Auto-negotiation Able	RO LH	• 1 = Link Partner has auto-negotiation capability. • 0 = Link Partner does not have auto-negotiation capability.	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation.

Parallel Detection Fault

Bit 4 of the Auto-negotiation Expansion register is a read-only bit that gets latched high when a parallel detection fault occurs in the auto-negotiation state machine. For further details, please consult the IEEE standard. The bit is reset to 0 after the register is read, or when the chip is reset.

Link Partner Next Page Able

Bit 3 of the Auto-negotiation Expansion register returns a 1 when the Link Partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability register.

Page Received

Bit 1 of the Auto-negotiation Expansion register is latched high when a new Link Code Word is received from the Link Partner, checked, and acknowledged. It remains high until the register is read, or until the chip is reset.

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Link Partner Auto-Negotiation Able

Bit 0 of the Auto-negotiation Expansion register returns a 1 when the Link Partner is known to have auto-negotiation capability. Before any auto-negotiation information is exchanged, or if the Link Partner does not comply with IEEE auto-negotiation, the bit returns a value of 0.

Auto-Negotiation Next Page Register (Page A0h–B7h/Addr 0Eh–0Fh)

Table 301: Next Page Transmit Register (Pages A0h–B7h, Address 0Eh–0Fh)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	• 1 = Additional Next Page(s) follow. • 0 = Last page.	0
14	Reserved	R/W	Ignore when Read.	0
13	Message Page	R/W	• 1= Message page. • 0 = Unformatted page.	1
12	Acknowledge 2	R/W	• 1 = Complies with the message. • 0 = Cannot comply with message.	0
11	Toggle	RO	• 1 = Previous value of the transmitted Link Code Word equalled logic 0. • 0 = Previous value of the transmitted Link Code Word equalled logic one.	0
10:0	Message/Unformatted Code Field	R/W		1

Next Page

Indicates whether this is the last Next Page to be transmitted.

Message Page

Differentiates a Message Page from an Unformatted Page.

Acknowledge 2

Indicates that a device has the ability to comply with the message.

Toggle

Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field

An 11-bit-wide field, encoding 2048 possible messages.

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Unformatted Code Field

An 11-bit-wide field, which may contain an arbitrary value.

Link Partner Next Page Register (Page A0h–B7h/Addr 10h–11h)

Table 302: Link Partner Next Page Register (Pages A0h–B7h, Address 10h–11h)

Bit	Name	R/W	Description	Default
15	Next Page	RO	• 1 = Additional Next Page(s) follow. • 0 = Last page.	0
14	Reserved	RO	Ignore when Read.	0
13	Message Page	RO	• 1 = Message page. • 0 = Unformatted page.	0
12	Acknowledge 2	RO	• 1 = Complies with the message. • 0 = Cannot comply with message.	0
11	Toggle	RO	• 1 = Previous value of the transmitted Link Code Word equalled logic 0. • 0 = Previous value of the transmitted Link Code Word equalled logic one.	0
10:0	Message/Unformatted Code Field	RO	–	0

Next Page

indicates whether this is the last Next Page.

Message Page

Differentiates a Message Page from an Unformatted Page.

Acknowledge 2

Indicates that Link Partner has the ability to comply with the message.

Toggle

Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field

An 11-bit-wide field, encoding 2048 possible messages.

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Unformatted Code Field

An 11-bit-wide field, which may contain an arbitrary value.

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Page B9h-BCh: Internal SerDes Port (P49~P52) MII Registers

Table 303: Internal SerDes Port (P49~P52) MII Registers

Page	Port #	Hardware PHY address
B9h	G0 (P49)	11001
BAh	G1 (P50)	11010
BBh	G2 (P51)	11011
BCh	G3 (P52)	11100

See "MDC/MDIO Interface" on page 118 for more information on PHY addressing.

Table 304: Internal SerDes Registers Page B9h–BCh

Address	Block Number	Bits	Description
00h–01h	0	16	Table 305: "MII Control (Page B9h–BCh: Address 00h–01h)," on page 355.
02h–03h	0	16	Table 306: "MII Status (Page B9h–BCh: Address 02h–03h)," on page 356.
04h–07h	0	–	Reserved
08h–09	0	16	Table 307: "Auto-Negotiation Advertisement (Page B9h–BCh: Address 08h–09h)," on page 357.
0Ah–0Bh	0	16	Table 308: "Auto-Negotiation Link Partner Ability (Page B9h–BCh: Address 0Ah–0Bh)," on page 358.
0Ch–0Dh	0	16	Table 309: "Auto-Negotiation Expansion (Page B9h–BCh: Address 0Ch–0Dh)," on page 359.
0Eh–1Dh	0	–	Reserved
1Eh–1Fh	0	16	Table 310: "Extended Status (Page B9h–BCh: Address 1Eh–1Fh)," on page 359.
20h–21h	0	16	* SerDes/SGMII Control 1 Register (see Table 311: "SerDes/SGMII Control1 (Page B9h–BCh: Address 20h–21h, Block 0)," on page 360) in Block 0. * Analog Transmit Register (see Table 312: "Analog Transmit register (Page B8h–BCh: Address 20h–21h, Block 1)," on page 362) in Block 1.
22h–23h	0	16	Table 313: "SerDes/SGMII Control 2 (Page B9h–BCh: Address 22h–23h)," on page 362.
24h–25h	0	16	Table 314: "SerDes/SGMII Control 3 (Page B9h–BCh: Address 24h–25h)," on page 363.
26h–27h	0	16	Table 315: "SerDes/SGMII 1000Base-X Control 4 (Page B9h–BCh: Address 26h–27h)," on page 365.
28h–29h	0	16	Table 316: "SerDes/SGMII Status 1 (Page B9h–BCh: Address 28h–29h)," on page 365.
2Ah–2Bh	0	16	Table 317: "SerDes/SGMII Status 2 (Page B9h–BCh: Address 2Ah–2Bh)," on page 367.
2Ch–2Dh	0	16	Table 318: "SerDes/SGMII Status 3 (Page B9h–BCh: Address 2Ch–2Dh)," on page 368.
2Eh–2Fh	0	16	Table 319: "BER/CRC Error Counter Register (Page B9h–BCh: Address 2Eh –2Fh)," on page 370.

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Table 304: Internal SerDes Registers Page B9h–BCh (Cont.)

Address	Block Number	Bits	Description
30h ~ 31h	0	16	Table 320: "PRBS Control Register (Page B9h–BCh: Address 30h–31h)," on page 370.
32h ~ 33H	0	16	Table 321: "PRBS Control Register (Page B9h–BCh: Address 32h–33h)," on page 370.
34h ~ 35h	0	16	Table 322: "Pattern Generator Control Register (Page B9h–BCh: Address 34h–35h)," on page 371.
36h ~ 37h	0	16	Table 323: "Pattern Generator Control Register (Page B9h–BCh: Address 36h–37h)," on page 372.
3Ah ~ 3Bh	0	16	Table 324: "Force Transmit 1 Register (Page B9h–BCh: Address 3Ah–3Bh)," on page 372.
3Ch ~ 3Dh	0	16	Table 325: "Force Transmit 2 Register (Page B9h–BCh: Address 3Ch–3Dh)," on page 373.
3Eh ~ 3Fh	1	16	Table 326: "Block Address (Pages B9h–BCh: Address 3Eh–3Fh)," on page 373.

Note: When Block 1 is selected via bits [3:0] (see BLK_NO of "Block Address (Pages B9h–BCh: Address 3Eh–3Fh)" on page 373). Address spaces 22h ~ 2Dh are Reserved.

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MII Control Register (Page B9h–BCh: Address 00h–01h)

Table 305: MII Control (Page B9h–BCh: Address 00h–01h)

Bit	Name	R/W	Description	Default
15	RST_SW	R/W	PHY reset. • 0 = normal operation. • 1 = PHY reset.	0
14	LOOPBACK	R/W	Loopback enable. • 0 = normal operation. • 1 = loopback enable.	0
13	Speed Select (LSB)	R/W	Speed Select Bits [6, 13]. • 1X = 1000 Mbps • 01 = 100 Mbps • 00 = 10 Mbps • Only used in SGMII Mode. Ignored when in SerDes Mode.	0
12	AN_EN	R/W	Auto-negotiation Enable (AN). • 0 = disable. • 1 = enable AN.	1
11	PWRDN	R/W	• 0 = normal operation. • The BCM53262M does not implement a low-power mode.	0
10	Reserved	RO	Reserved. Write 0, ignore read.	0
9	RESTART_AN	R/W	Restart AN. • 0 = normal operation. • 1 = restart the AN process.	0
8	Duplex	R/W	Full-duplex. • 0 = half-duplex • 1 = full-duplex	1
7	COL_TEST_EN	R/W	Collision test enable. • 0 = normal operation. • 1 = collision test mode enable.	0
6	Speed Select (MSB)	R/W	Speed Select Bits [6, 13]. • 1X = 1000 Mbps • 01 = 100 Mbps • 00 = 10 Mbps • Only used in SGMII Mode. Ignored when in SerDes Mode.	1
5:0	Reserved	RO	Reserved. Write 0, ignore read.	0x00

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MII Status Register (Page B9h–BCh: Address 02h–03h)

Table 306: MII Status (Page B9h–BCh: Address 02h–03h)

Bit	Name	R/W	Description	Default
15	100Base_T4	RO	0 = not capable. 1 = 100Base-T4 capable.	0
14	100BaseX_FDX	RO	0 = not capable. 1 = 100Base-X full-duplex capable.	0
13	100BaseX_HDX	RO	0 = not capable. 1 = 100Base-X half-duplex capable.	0
12	10BaseT_FDX	RO	0 = not capable. 1 = 10Base-T full-duplex capable.	0
11	10BaseT_HDX	RO	0 = not capable. 1 = 10Base-T half-duplex capable.	0
10	100BaseT2_FDX	RO	0 = not capable. 1 = 100Base-T2 full-duplex capable.	0
9	100BaseT2_HDX	RO	0 = not capable 1 = 100Base-T2 half-duplex capable.	0
8	EXT_STATUS	RO	0 = no extended status. 1 = Extended status in register 0x0F.	1
7	Reserved	RO	Reserved. Write 0, ignore read.	0
6	MF_PREAMBLE_ SUPPRESSION	RO	0 = PHY does not accept management frames with preamble suppressed. 1 = PHY accepts management frames with preamble suppressed.	1
5	AN_COMPLT	RO	Auto negotiation complete. 0 = not done. 1 = AN complete.	0
4	RF	RO	Remote fault. 0 = no fault detected. 1 = remote fault detected.	0
3	AN_ABILITY	RO	Auto negotiation ability. 0 = not capable of AN. 1 = AN capable.	1
2	LINK_STATUS	RO	Link status. 0 = link fail. 1 = good link.	0
1	JABBER_DETECT	RO	Jabber detect. 0 = not detected. 1 = jabber detected.	0
0	EXT_CAPABILITY	RO	Extended capability. 0 = supports basic register set only. 1 = extended register capabilities supported.	1

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Auto-Negotiation Advertisement (Page B9h–BCh: Address 08h–09h)

Table 307: Auto-Negotiation Advertisement (Page B9h–BCh: Address 08h–09h)

Bit	Name	R/W	Description	Default
15	NEXT_PG	RO	Next page. 1 = Next page ability supported 0 = Next page ability not supported	0
14	Reserved	RO	Reserved, write as 0, ignore read.	0
13:12	RF	R/W	Remote fault: 00 = No fault 01 = Link failure 10 = Offline 11 = An error	00
11:9	Reserved	RO	Reserved, write as 0, ignore read.	00
8:7	PAUSE	R/W	Pause 00 = No pause 01 = Symmetric pause 10 = Asymmetric pause towards link partner 11 = Both symmetric and asymmetric pause towards local device	11
6	HDX Capable	R/W	Half-duplex 0 = Do not advertise half-duplex 1 = Advertise half-duplex	1
5	FDX Capable	R/W	Full-duplex 0 = Do not advertise full-duplex 1 = Advertise full-duplex	1
4:0	Reserved	RO	Reserved, write as 0, ignore read.	00

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Auto-Negotiation Link Partner Ability (Page B9h–BCh: Address 0Ah–0Bh)

Table 308: Auto-Negotiation Link Partner Ability (Page B9h–BCh: Address 0Ah–0Bh)

Bit	Name	R/W	Description	Default
15	Next Page/Link	RO	When link partner configured to SerDes mode (bit[0] = 0): 1 = Link partner is next page capable 0 = Link partner is not next page capable When link partner configured to SGMII mode (bit[0] = 1): 1 = Link 0 = No link	0
14	ACK	RO	Reserved, write as 0, ignore read.	0
13:12	Remote Fault/ Duplex	RO	When link partner configured to SerDes mode (bit[0] = 0), these bits indicate advertised remote fault setting of link partner: 00 = No fault 01 = Link failure 10 = Offline 11 = AN error When link partner configured to SGMII mode bit[0] = 1), these bits indicate advertised duplex of link partner: x1 = Full-duplex x0 = Half-duplex	0x0
11:10	Reserved	RO	Reserved, write as 0, ignore read.	0
9	Speed	RO	When link partner configured to SerDes mode (bit[0] = 0), these bits are reserved When link partner configured to SGMII mode (bit[0] = 1), indicates advertised link speed of link partner: 1x = 1000M 01 = 100M 00 = 10M	0x0
8:7	Pause Capable	RO	When link partner configured to SerDes mode (bit[0] = 0), indicates link partner pause capabilities: 00 = No pause 01 = Symmetrical pause 10 = Asymmetrical pause towards link partner 11 = Both symmetric and asymmetric pause towards local device When link partner configured to SGMII mode (bit[0] = 1), these bits are reserved.	0x0

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Table 308: Auto-Negotiation Link Partner Ability (Page B9h–BCh: Address 0Ah–0Bh) (Cont.)

Bit	Name	R/W	Description	Default
6	HDX Capable	RO	When link partner configured to SerDes mode (bit[0] = 0), indicates link partner pause capabilities: 0 = Not half-duplex capable 1 = Half-duplex capable When link partner configured to SGMII mode (bit[0] = 1), these bits reserved	0
5	FDX (for SerDes only)	RO	When link partner configured to SerDes mode (bit[0] = 0), indicates link partner pause capabilities: 0 = Not full-duplex capable 1 = Full-duplex capable When link partner configured to SGMII mode (bit[0] = 1), these bits reserved	0
4:1	Reserved	RO	Reserved, write as 0, ignore read.	0x0
0	SGMII	RO	SGMII mode. 0 = Fiber mode 1 = SGMII mode	0

Auto-Negotiation Expansion (Page B9h-BCh: Address 0Ch–0Dh)

Table 309: Auto-Negotiation Expansion (Page B9h–BCh: Address 0Ch–0Dh)

Bit	Name	R/W	Description	Default
15:3	Reserved	RO	Reserved, write as 0, ignore read.	0x0000
2	NP_ABILITY	RO	Next page ability. 0 = local device is not next page enabled. 1 = local device is next page enabled.	0
1	PG_REC	RO	Page received. 0 = new link code word is not received. 1 = new link code word is received.	0
0	Reserved	RO	Reserved, write as 0, ignore read.	0

Extended Status Register (Page B9h–BCh: Address 1Eh–1Fh)

Table 310: Extended Status (Page B9h–BCh: Address 1Eh–1Fh)

Bit	Name	R/W	Description	Default
15	1000BaseX_FDX	RO	0 = not capable 1 = 1000Base-X full-duplex capable	1
14	1000BaseX_HDX	RO	0 = not capable 1 = 1000Base-X half-duplex capable	1
13	1000BaseT_FDX	RO	0 = not capable 1 = 1000Base-T full-duplex capable	0

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Table 310: Extended Status (Page B9h–BCh: Address 1Eh–1Fh) (Cont.)

Bit	Name	R/W	Description	Default
12	1000BaseT_HDX	RO	0 = not capable 1 = 1000Base-T half-duplex capable	0
11:0	Reserved	RO	Reserved, write as 0, ignore read.	000

SerDes/SGMII Control 1 (Page B9h–BCh: Address 20H ~ 21H, BLOCK 0)

Table 311: SerDes/SGMII Control1 (Page B9h–BCh: Address 20h–21h, Block 0)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Reserved, write as 0, ignore read.	0
14	DIS_SD_FILTER	R/W	Filtering the signal detect pin adds hysteresis to the signal to stabilize the readings near the threshold. The status of resulting signal detect, regardless of whether the filter is active, is recorded via "SerDes/SGMII Status 3 (Page B9h–BCh: Address 2Ch–2Dh)" bit[9]. 0 = filter signal detection from pin before using for synchronization. 1 = disable filter for signal detect.	0
13	Global Write	R/W	MDC/MDIO commands addressed to PHYADD 00 will affect all ports that have the Global Write enabled. 0 = Normal operation 1 = Global Write Enabled	0
12	Reserved SERDES_TX_AMP_OVR	RO R/W	Reserved.0 = normal operation (selected by SGMII or fiber mode). 1 = override SerDes transmit amplitude from register 1*10h bit 14.	0
11	Counter Select	R/W	Error Counter Register Definition Configures the type of events counted in BER/CRC Error Counter Register (Page 10h ~ 17h: Address 2Eh). 0 = Select CRC errors 1 = Select received packets	0
10	REMOTE_LPBK	R/W	Remote loopback operates in all available speeds. 0 = normal operation. 1 = enable remote loopback (operates in 10/100/1000 speed).	0
9	Reserved ZERO_CD_PHASE	RO R/W	Reserved0 = normal operation. 1 = force comma detector phase to zero.	0
8	CD_EN	R/W	0 = disable comma detection 1 = enable comma detection	1
7	CRC_DIS	R/W	0 = enable CRC checker. 1 = disable CRC checker by gating the clock to save power.	1

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Table 311: SerDes/SGMII Control1 (Page B9h–BCh: Address 20h–21h, Block 0) (Cont.)

Bit	Name	R/W	Description	Default
6	Reserved DIS_PLL_PWRDN	R/W	Reserved0 = PLL is powered down when Register 22 is set. 1 = PLL is never powered down. (Use this when the MAC/Switch uses the pll_clk125 output).	1
5	SGMII_MSTR	R/W	This bit configures the port to operate in Master mode (typical of PHY device) to allow testing link conditions between two Switch ports. 0 = normal operation. 1 = SGMII mode operates in master PHY mode. If auto-negotiation is enabled, then the local device sends out the following auto-negotiation code word: [15] = 1 [14] = ack [13] = 0 [12] = Register 0, bit 8 [11] = Register 0, bit 6 [10] = Register 0, bit 13 [9:0] = "0000000001" To disable the link, set Register 22 = 1. To enable the link, set Register 22 = 0.	0
4	AUTODET_EN	R/W	0 = disable auto-detection (fiber or SGMII mode is set according to bit 0 of this register). 1 = enable auto-detection (fiber and SGMII mode switches each time a auto-negotiation page is received with the wrong selector field in bit 0.)	1
3	INVERT_SD	R/W	0 = use signal detect from pin. 1 = invert signal detect from pin.	0
2	SD_EN	R/W	0 = ignore signal detect from pin. 1 = signal detect from pin must be set in order to achieve synchronization. In SGMII the signal detect is always ignored regardless of the setting of this bit.	0
1	RSVD	R/W	Write as default. Ignore on read.	0
0	FIBER	R/W	0 = SGMII mode. 1 = Fiber SerDes mode.	0

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Analog Transmit Register (Page B9h–BCh: Address 20H–21H Block 1)

Refer to Page 10h ~ 1Fh: Address 3E on how to select this register.

Table 312: Analog Transmit register (Page B8h–BCh: Address 20h–21h, Block 1)

BIt	Name	R/W	Description	Default
15:12	Output_Voltage_Level	R/W	Controls the Output Voltage level from 0V ~ 750V in 16 equal steps (Before any loss or variations in resistance). NOTE: This is approximate. The actual voltage swing can be determine by measuring the device on the board.	4'b1100
11:9	Reserved	–	Reserved	3'b100
8:6	Pre_Emphasis_Coeff	R/W	Allows eight possible combinations ranging from 0 percent to 50 percent. 0x7 is 50 percent and 0x0 is 0 percent. The granularity is roughly linear across the eight settings.	0h
5:0	Reserved	R/W	Reserved	6'b10-0000

SerDes/SGMII Control 2 (Page B9h–BCh: Address 22h–23h)

Table 313: SerDes/SGMII Control 2 (Page B9h–BCh: Address 22h–23h)

BIt	Name	R/W	Description	Default
15	Reserved	RO	Reserved, write as 0, ignore read.	0
14	CLEAR_BER_CNTR	R/W SC	1 = Clear bit-error-rate counter "BER/CRC Error Counter Register (Page 10h ~ 17h: Address 2E)" bit[15:8]. 0 = Normal operation.	0
13	TRANSMIT_IDLE_JAM_SEQ_TEST	R/W	This bit activates a transmit idle test sequence for testing purposes. The 16-stage, 10-bit transmit test sequence is forced regardless of link conditions. Setting Force Transmit 1/2 in addition to this bit can modify the idle test sequence. "Force Transmit 1 Register (Page 10h ~ 17h: Address 3Ch)" bit[9:0] will override D16.2 for stage 6 (289h) 1 = Enable transmit idle test sequence 0 = Normal operation	0
12:8	Reserved	RO	Reserved, write as 0, ignore read.	0
7	Reserved DIS_CARRIER_EXT	R/W	Reserved. 0 = Normal operation. 1 = Disable carrier extension in pcs receive.	0
6	Reserved	RO	Reserved, write as 0, ignore read.	0
5	FORCE_XMIT_DATA_ON_TXSIDE	R/W	1 = Allow packets to be transmitted regardless of the condition of the link or synchronization. 0 = Normal operation.	0
4	DIS_RF_SENSE	R/W	0 = Automatically detect remote faults and send remote fault status to link partner via auto-negotiation when fiber mode is selected. SGMII does not support remote faults. 1 = Disable automatic sensing of remote faults, such as auto-negotiation error.	0

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Table 313: SerDes/SGMII Control 2 (Page B9h–BCh: Address 22h–23h) (Cont.)

Bit	Name	R/W	Description	Default
3	Reserved EN_AN_ ERR_TIMER	ROR/ W	Reserved.0 = Normal operation. 1 = Enable auto-negotiation error timer. Error occurs when timer expires in ability-detect, ack-detect, or idle-detect. When the error occurs, config words of all zeros are sent until an ability match occurs; then the auto-negotiation-enable state is entered.	0
2	Stable Link Filter	R/W	This bit forces the constant sync status for 10ms before establishing link. This prevents potential false-link events in SerDes applications not using Auto-negotiation or the Signal Detect pin. 0 = Normal operation. 1 = Sync-status must be set for a solid 10 ms before a valid link is established when auto-negotiation is disabled.	0
1	DIS_FALSE_LINK	R/W	0 = Normal operation. 1 = Do not allow link to be established when auto-negotiation is disabled and receiving auto-negotiation code words. The link is only established in this case after idles are received. (This bit does not need to be set, if bit 0 is set.)	0
0	EN_PAR_DET	R/W	0 = Disable. 1 = Enable parallel detection. (This turns auto negotiation on and off as needed to properly link up with the link partner. The idles and auto-negotiation code words received from the link partner are used to make this decision.)	1

SerDes/SGMII Control 3 (Page B9h–BCh: Address 24h–25h)

Table 314: SerDes/SGMII Control 3 (Page B9h–BCh: Address 24h–25h)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Reserved, write as 0, ignore read.	0
14	Reserved RXFIFO_GMII_RST	ROR/W	Reserved, write as 0, ignore read.0 = normal operation. 1 = reset receive FIFO and data_out_1000. FIFO remains in reset until this bit is cleared with a software write.	0
13	DIS_TX_CRS	R/W	0 = Normal operation. 1 = Disable generating CRS from transmitting in half-duplex mode. Only receiving generates CRS.	0
12:7	Reserved	RO	Reserved.	0
12	INV_EXT_PHY_CR	R/W	0 = Use receive CRS from PHY pin. 1 = Invert receive CRS from PHY pin.	0
11	EXT_PHY_CRS	R/W	0 = Normal operation. 1 = Use external pin for the PHY receive only CRS output. (Useful in SGMII 10/100 half-duplex applications in order to reduce the collision domain latency. Requires a PHY that generates a receive only CRS output to a pin.)	0

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Table 314: SerDes/SGMII Control 3 (Page B9h–BCh: Address 24h–25h) (Cont.)

Bit	Name	R/W	Description	Default
10	JAM_FALSE_CRS	R/W	0 = normal operation. 1 = change false carriers received into packets with preamble only. (Not necessary if MAC uses CRS to determine collision).	0
9	BLK_TXEN	R/W	0 = normal operation. 1 = block txen when necessary to guarantee an IPG of at least 6.5 bytes in 10/100 mode, 7 bytes in 1000 mode.	0
8	FORCE_TXFIFO_ON	R/W	0 = normal operation. 1 = force transmit FIFO to free-run in gigabit mode (Requires clk_in and pll_clk125 to be frequency locked.)	0
7	BYP_TXFIFO_1000	R/W	0 = normal operation. 1 = bypass transmit FIFO in gigabit mode. (Useful for fiber or gigabit only applications where the MAC is using the pll_clk125 as the clk_in port. User must meet timing to the pll_clk125 domain).	0
6	Reserved	RO	Reserved.	1
5:3	Reserved	RO	Reserved.	0
6	FREQ_LOCK_ELAS_TX	R/W	0 = normal operation. 1 = minimum FIFO latency to properly handle a clock which is frequency locked, but out of phase. (Overrides bits [2:1] of this register.) PLL_CLK125 and CLK_IN must be using the same crystal.	1
5	FREQ_LOCK_ELAS_RX	R/W	0 = normal operation 1 = minimum FIFO latency to properly handle a clock which is frequency locked, but out of phase. (Not necessary if MAC uses CRS to determine collision; overrides bits [2:1] of this register.) MAC and PHY must be using the same crystal for this mode to be enabled.	0
4	EARLY_PRE_TX	R/W	0 = normal operation. 1 = send extra bytes of preamble to avoid FIFO latency. (Not necessary if MAC uses CRS to determine collision.)	0
3	EARLY_PRE_RX	R/W	0 = normal operation. 1 = send extra bytes of preamble to avoid FIFO latency. (Used in half-duplex applications to reduce collision domain latency. MAC must send 5 bytes of preamble or less to avoid noncompliant behavior.)	0
2:1	FIFO_ELAS_TX_RX	R/W	00 = supports packets up to 5 KB. 01 = supports packets up to 10 KB. 1X = supports packets up to 13.5 KB.	01
0	Reserved TXFIFO_RST	RO R/W	Reserved.0 = normal operation. 1 = reset transmit FIFO. FIFO remains in reset until this bit is cleared with a software write.	0

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SerDes/SGMII 1000Base-X Control 4 (Page B9h–BCh: Address 26h–27h)

Table 315: SerDes/SGMII 1000Base-X Control 4 (Page B9h–BCh: Address 26h–27h)

Bit	Name	R/W	Description	Default
15:11	Reserved	RO	Reserved, write as 0, ignore read.	0x00
10	ZERO_DATA_OUT_1000	R/W	0 = normal operation. 1 = zero data_out_1000 when speed is not 1000 Mbps.	0
9	CLEAR_LINKDN	R/W SC	0 = normal operation. 1 = clear latching of link down. Latch_linkdown status bit is register 0*16h bit[[10] enable_latch_linkdown control bit is bit[8] of this register.	0
8	EN_LATCH_LINKDN	R/W	0 = normal operation. 1 = enable latching of link when link is down. Transmit FIFO, receive FIFO and data_out_1000 to remain in reset state until bit[9] of this register is 1.	0
7	LINK_FORCE	R/W	0 = normal operation. 1 = force link on.	0
6	DIG_RESET	R/W	0 = normal operation. 1 = resets digital logic datapath, MII registers are not in reset state.	0
5	ANA_PLL_LOCK_OVR_VAL	R/W	PLL lock status bit override value.	0
4	EN_ANA_PLL_LOCK_OVR	R/W	0 = Override PLL lock status bit with bit [5] of this register. 1 = Use PLL lock status bit from analog directly in analog reset logic.	0
3	DIG_PLL_LOCK_OVR_VAL	R/W	PLL lock status bit override value.	0
2	EN_DIG_PLL_LOCK_OVR	R/W	0 = Override PLL lock status bit with bit [3] of this register. 1 = Use PLL lock status bit from analog directly in digital logic.	0
1	ANA_SD_OVR_VAL	R/W	Analog signal detect status bit override value.	0
0	EN_ANA_SD_OVR	R/W	0 = Override analog signal detect status with bit [1] of this register. 1 = Use analog signal detect.	1

SerDes/SGMII Status 1 (Page B9h–BCh: Address 28h–29h)

Table 316: SerDes/SGMII Status 1 (Page B9h–BCh: Address 28h–29h)

Bit	Name	R/W	Description	Default
15	TXFIFO_ERR	RO	0 = No transmit FIFO error detected since last read. 1 = Transmit FIFO error detected since last read.	0
14	RXFIFO_ERR	RO	0 = No receive FIFO error detected since last read. 1 = Receive FIFO error detected since last read.	0

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Table 316: SerDes/SGMII Status 1 (Page B9h–BCh: Address 28h–29h) (Cont.)

Bit	Name	R/W	Description	Default
13	FALSE_CRS	RO	0 = No false carrier detected since last read. 1 = False carrier detected since last read.	0
12	CRC_ERR	RO	0 = No CRC error detected since last read or detection is disabled via "SerDes/SGMII Control 1 Register (Page 10h ~ 1Fh: Address 20h)" bit[7]. 1 = CRC error detected since last read.	0
11	TX_ERR	RO	0 = No transmit error code detected since last read. 1 = Transmit error code detected since last read (rx_data_error state in PCS receive FSM).	0
10	RX_ERR	RO	0 = No receive error since last read. 1 = Receive error since last read (early_end state in PCS receive FSM).	0
9	CRS_EXT	RO	0 = No carrier extend error since last read. 1 = Carrier extend error since last read (extend_err in PCS receive FSM).	0
8	EARLY_END_EXT	RO	0 = No early end extension since last read. 1 = Early end extension since last read (early_end_ext in PCS receive FSM).	0
7	LINK_CHG	RO	0 = Link status has not changed since last read. 1 = Link status has changed since last read.	0
6	PAUSE_RES_RX	RO	0 = Disable pause receive. 1 = Enable pause receive.	0
5	PAUSE_RES_TX	RO	0 = Disable pause transmit. 1 = Enable pause transmit.	0
4:3	SPEED_STAT	RO	00 = 10 Mbps. 01 = 100 Mbps. 1X = 1000 Mbps.	0x0
2	DUPLEX_STAT	RO	0 = Half-duplex. 1 = Full-duplex.	0
1	LINK_STAT	RO	0 = Link is down. 1 = Link is up.	0
0	SGMII_MODE	RO	0 = SerDes mode (1000Base-X). 1 = SGMII mode.	0

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SerDes/SGMII Status 2 (Page B9h–BCh: Address 2Ah–2Bh)

Table 317: SerDes/SGMII Status 2 (Page B9h–BCh: Address 2Ah–2Bh)

Bit	Name	R/W	Description	Default
15	SGMII_MODE_CHG	RO	0 = SGMII/SerDes mode has not changed since last read (fixed in SGMII or SerDes mode). 1 = SGMII/SerDes mode has changed since last read (SGMII mode enabled or disabled). This bit is useful when the auto-detection is enabled in "SerDes/SGMII Control 1 Register (Page 10h ~ 1Fh: Address 20h bit[4])".	0
14	CONS_MISMATCH	RO	A consistency mismatch results from incompatibilities represented in the link code word of the local and remote link partners. SerDes or SGMII mode. 0 = Consistency mismatch has not been detected since last read. 1 = Consistency mismatch detected since last read.	0
13	AN_RES_ERR	RO	0 = Auto-negotiation error has not been detected since last read. 1 = Auto-negotiation error detected since last read.	0
12	SGMII_SEL_MIS	RO	A SGMII selector mismatch occurs when the auto-negotiation page received from the link partner has bit[0] = 0 while local device is in SGMII mode. 0 = SGMII selector mismatch not detected since last read. 1 = SGMII selector mismatch detected since last read.	0
11	SYNC_STAT_FAIL	RO	0 = Sync_status has not failed since last read. 1 = Sync_status has failed since last read (synchronization has been lost).	0
10	SYNC_STAT_OK	RO	0 = Sync_status ok has not been detected since last read. 1 = Sync_status ok detected since last read (synchronization has been achieved).	0
9	RUDI_C	RO	0 = Rudi_c has not been detected since last read. 1 = Rudi_c detected since last read.	0
8	RUDI_I	RO	0 = Rudi_i has not been detected since last read. 1 = Rudi_i detected since last read.	0
7	RUDI_INVALID	RO	0 = Rudi_invalid has not been detected since last read. 1 = Rudi_invalid detected since last read.	0
6	LINK_DN_SYNC_LOSS	RO	0 = Failure condition has not been detected since last read. 1 = A valid link went down due to a loss of synchronization for over 10 ms.	0
5	IDLE_DETECT	RO	0 = Idle detect state not entered since last read. 1 = Idle detect state in auto-negotiation FSM entered since last read.	0

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Table 317: SerDes/SGMII Status 2 (Page B9h–BCh: Address 2Ah–2Bh) (Cont.)

Bit	Name	R/W	Description	Default
4	CMPLT_ACK	RO	0 = Complete acknowledge state not entered since last read. 1 = Complete acknowledge state in auto-negotiation FSM entered since last read.	0
3	ACK_DETECT	RO	0 = Acknowledge detect state not entered since last read. 1 = Acknowledge detect state in auto-negotiation FSM entered since last read.	0
2	ABILITY_DETECT	RO	0 = Ability detect state not entered since last read. 1 = Ability detect state in auto-negotiation FSM entered since last read.	0
1	AN_DIS_LINK_OK	RO	0 = An_disable_link_ok not entered since last read. 1 = An_disable_link_ok state in auto-negotiation FSM entered since last read.	0
0	AN_EN_LINK_OK	RO	0 = An_enable state has not been entered since last read. 1 = An_enable state in auto-negotiation FSM entered since last read.	0

SerDes/SGMII Status 3 (Page B9h–BCh: Address 2Ch–2Dh)

Table 318: SerDes/SGMII Status 3 (Page B9h–BCh: Address 2Ch–2Dh)

Bit	Name	R/W	Description	Default
15:1011	Reserved	RO	Reserved. Write as 0, ignore read.	0x0
10	LATCH_LINKDN	RO	Reserved.	0
9	Signal Detect Filter Output	RO	This bit represents the output of the Signal Detect filter, regardless of whether the filter is active or not. This status signal is still valid when "SerDes/SGMII Control 1 Register (Page 10h ~ 1Fh: Address 20h)" bit[14] = 1. Noise pulses less than 16 ns wide are still removed whenever the filter is disabled 0 = Output of signal detect is not set. 1 = Output of signal detect filter is set. This signal is used for the PCS synchronization. When the Signal Detect signal is disabled "SerDes/SGMII Control 1 Register (Page 10h ~ 17H: Address 20h)" bit[2] = 0, then the output of the filter is forced high.	0
8	Signal Detect Inversion Output	RO	This status signal is the signal detect result when "SerDes/SGMII Control 1 Register (Page 10h ~ 1Fh: Address 20h)" bit[3] = 0; Otherwise, it is the inversion of the signal detect. 0 = Output of signal detect is not set. 1 = Output of signal detect filter is set. This is the only valid Signal Detect status bit when the port is powered down from "MII Control Register (Page 10h ~ 1Fh: Address 00h)" bit[11].	0

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Table 318: SerDes/SGMII Status 3 (Page B9h–BCh: Address 2Ch–2Dh) (Cont.)

Bit	Name	R/W	Description	Default
7	SD_FILTER_CHG	RO	0 = Signal detect has not changed since last read. 1 = Signal detect has changed since last read. The signal detect change is based on a change in bit [9] of this register.	0
6	SD	RO	Signal detect direct from pin.	0
5	ANA_SD	RO	Analog signal detect status bit. This status signal is the analog signal detect status if register 0*13h bit [0] is set; otherwise, it is the value based on register 0*13h bit [1].	0
4	Reserved ANA_SD_CHG	RO	Reserved. Write as 0, ignore read.0 = Analog signal detect has not changed since last read. 1 = Analog signal detect has changed since last read. The analog signal detect change is based on a change in bit [5] of this register.	0
3:0	Reserved	RO	Reserved. Write as 0, ignore read.	0x0

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BER/CRC Error Counter Register (Page B9h–BCh: Address 2Eh–2Fh)

Table 319: BER/CRC Error Counter Register (Page B9h–BCh: Address 2Eh –2Fh)

Bit	Name	R/W	Description	Default
15:8	Bit Error Rate (BER) Counter	RO	Number if invalid code groups detect while sync_status = 1 Freezes at FFh Write "SerDes/SGMII Control 2 Register (Page 10h ~ 17h: Address 22h)" bit[14] = 1 in order to clear.	00h
7:0	CRC Error/Receive Packet Counter	R/W CR	Number of CRC errors detected since last read. Freezes at FFh. When "SerDes/SGMII Control 1 Register (Page 10h ~ 17h: Address 20h)" bit[11] is set, the counter detects the number of received packets instead of CRC errors.	00h

PRBS Control Register (Page B9h–BCh: Address 30h–31h)

Table 320: PRBS Control Register (Page B9h–BCh: Address 30h–31h)

Bit	Name	R/W	Description	Default
15:4	Reserved	R/W	Write as 0, ignore on read.	00h
3:2	PRBS	R/W	11 = x(n) = 1 + x(28) + x(31) 10 = x(n) = 1 + x(18) + x(23) 01 = x(n) = 1 + x(14) + x(15) 00 = x(n) = 1 + x(6) + x(7)	00
1	Invert PRBS Order	R/W	1 = Invert polynomial sequence 0 = Normal operation	0
0	PRBS Enable	R/W	1 = Enable PRBS 0 = Disable PRBS	0

PRBS Control Register (Page B9h–BCh: Address 32h–33h)

Table 321: PRBS Control Register (Page B9h–BCh: Address 32h–33h)

Bit	Name	R/W	Description	Default
15:13	PRBS Error State	RO CR	Grey coded FSM: 100 = 1024 or more errors 101 = 512 ~ 1023 errors 111 = 256 ~ 511 errors 110 = 128 ~ 255 errors 010 = 64 ~ 127 errors 011 = 32 ~ 63 errors 001 = 1 ~ 31 errors 000 = No errors	000

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Table 321: PRBS Control Register (Page B9h–BCh: Address 32h–33h) (Cont.)

Bit	Name	R/W	Description	Default
12	PRBS Lost Lock	RO LH	1 = PRBS has lost lock since last read 0 = PRBS has not lost lock since last read	0
11	PRBS Locked	RO	1 = PRBS monitor is locked 0 = PRBS monitor is not locked	0
10:0	PRBS Errors	RO CR	Number of PRBS errors detected while locked. Freezes at 7FFh. ***Note:*** Counter is not synchronized to read status clock. The might increment while reading, causing inaccurate results. The PRBS should be disabled before reading the 11-bit error counter.	000h

Pattern Generator Control Register (Page B9h–BCh: Address 34h–35h)

Table 322: Pattern Generator Control Register (Page B9h–BCh: Address 34h–35h)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Write as 0, ignore on read.	0
14	TXER	R/W	1 = Set txer = 1 during CRC portion of packet 0 = Normal operation	0
13	Skip CRC	R/W	1 = Do not append 32-bit CRC to end of packet 0 = Normal operation	0
12	CRC Checker Enable	R/W	1 = Enable CRC Checker to detect CRC errors on packets of any size (1-byte or more) 0 = Normal operation (CRC checker only detects CRC errors on packets of at least 72-bytes)	0
11:9	IPG Select	R/W	000 = Invalid 001 = IPG of 6-bytes 010 = IPG of 10-bytes 011 = IPG of 14-bytes 100 = IPG of 18-bytes 101 = IPG of 22-bytes 110 = IPG of 26-bytes 111 = IPG of 30-bytes	100
8:3	Packet Size	R/W	000000 = Invalid 000001 = 256-bytes 000010 = 512-bytes 000011 = 768-bytes 000100 = 1024-bytes … … 111111 = 16,128-bytes	000100

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Table 322: Pattern Generator Control Register (Page B9h–BCh: Address 34h–35h) (Cont.)

Bit	Name	R/W	Description	Default
2	Single Pass Mode	R/W	1 = Only send 1 packet and stop 0 = Send packets while bit 1 of this register is set	0
1	Run Pattern Generator	R/W	1 = A rising edge on this bit while the pattern generator is in the idle state will start sending packets. If the single pass mode is set, then a single packet will be sent and the idle state will be entered. If the single pass mode is not set, then packets will be sent until this bit is cleared. At this point, the current packet will finish transmitting and then enter the idle state. ***Note:*** A valid link must be established prior to sending packets. 0 = Do not send packet	0
0	Select Pattern Generator Data	R/W	1 = Send idles or pattern generator data into transmit FIFO (Ignore MAC transmit data) 0 = Normal operation	0

Pattern Generator Control Register (Page B9h–BCh: Address 36h–37h)

Table 323: Pattern Generator Control Register (Page B9h–BCh: Address 36h–37h)

Bit	Name	R/W	Description	Default
15:4	Reserved	R/W	Write as 0, Ignore on read.	000h
3	Pattern Generator Active	RO	1 = Pattern generator is still sending packets 0 = Pattern generator is idle	0
2:0	Pattern Generator FSM	RO	000 = Idle 001 = Transmit preamble 011 = Transmit SFD 010 = Transmit data 110 = Transmit CRC 100 = IPG 101 = IPG 2 (allows FSM to be grey-coded	000

Force Transmit 1 Register (Page B9h–BCh: Address 3Ah–3Bh)

Table 324: Force Transmit 1 Register (Page B9h–BCh: Address 3Ah–3Bh)

Bit	Name	R/W	Description	Default
15:11	Reserved	R/W	Write as 0, ignore on read.	00h

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Table 324: Force Transmit 1 Register (Page B9h–BCh: Address 3Ah–3Bh)

Bit	Name	R/W	Description	Default
10	Force Transmit	R/W	This bit enables a test transmit mode of two alternating patterns. Additionally, can be used in conjunction with the Transmit Idle Test via "SerDes/SGMII Control 2 Register (Page 10h ~ 17h: Address 22h)" bit[13]. 1 = Provide alternating bit[9:0] from this register and "Force Transmit 2 Register (Page 10h ~ 17h: Address 3Ch)" bit[9:0] to SerDes analog register. 0 = Normal operation	0
9:0	Force Transmit Data 1	R/W	Value in this register will be provided to SerDes analog transmitter every other clock cycle when bit[10] is set.	17Ch

Force Transmit 2 Register (Page B9h–BCh: Address 3Ch–3Dh)

Table 325: Force Transmit 2 Register (Page B9h–BCh: Address 3Ch–3Dh)

Bit	Name	R/W	Description	Default
15:10	Reserved	R/W	Write as 0, ignore on read.	00h
9:0	Force Transmit Data 2	R/W	Value in this register will be provided to SerDes analog transmitter every other clock cycle when "Force Transmit 1 Register (Page 10h ~ 17h: Address 3Ah)" bit[10] is set.	

Block Address (Pages B9h–BCh: Address 3Eh–3Fh)

Table 326: Block Address (Pages B9h–BCh: Address 3Eh–3Fh)

Bit	Name	R/W	Description	Default
15:4	Reserved	RO	Reserved. Write 0, ignore read.	0x000
3:0	BLK_NO	R/W	Registers 00–0Fh and 1Fh do not use block addressing and are fixed. Block 0 and Block 1 selected via these bits. 0000 = valid (block 0). 0001 = valid (block 1). 0010–1111 = reserved for future implementation.	0x0

Page D8h–DCh: External PHY Registers

Information on the External PHY registers should be obtained from the external PHY data sheet. Data is obtained by polling the registers of the external PHY via the “MDC/MDIO Interface” on page 118. The actual values or meanings of these bits are controlled by the external PHY. Table 327 maps the external PHY register address to the BCM53262M offset address.

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Table 327: External Port MII Registers Page Versus PHY

Page	Port #	Hardware PHY address
D8h	48	11000
D9	49 (G0)	11001
DA	50 (G1)	11010
DBh	51 (G2)	11011
DCh	52 (G3)	11100

Table 328: External PHY Registers (Page D8h-DCh)

External PHY Register Address	Switch Address	bits	Description
00h	00h-01h	16	MII Control register
01h	02h-03h	16	MII Status register
02h	04h-07h	32	PHY Identifier registers
04h	08h–09h	16	Auto-negotiation Advertisement register
05h	0Ah–0Bh	16	Auto-negotiation Link Partner Ability register
06h	0Ch–0Dh	16	Auto-negotiation Expansion register
07h	0Eh–0Fh	16	Auto-negotiation Next Page register
08h	10h–11h	16	Link Partner Next Page register
09h–0Fh	12h–1Fh	Reserved	
10h	20h-21h	16	PHY specific register
11h	22h-23h	16	PHY specific register
12h	24h-25h	16	PHY specific register
13h	26h-27h	16	PHY specific register
14h	28h-29h	16	PHY specific register
15h	2Ah-2Bh	16	PHY specific register
16h	2Ch-2Dh	16	PHY specific register
17h	2Eh-2Fh	16	PHY specific register
18h	30h-31h	16	PHY specific register
19h	32h-33h	16	PHY specific register
1Ah	34h-35h	16	PHY specific register
1Bh	36h-37h	16	PHY specific register
1Ch	38h-39h	16	PHY specific register
1Dh	3Ah-3Bh	16	PHY specific register
1Eh	3Ch-3Dh	16	PHY specific register
1Fh	3Eh-3Fh	16	PHY specific register

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Global Registers

Table 329: Global Registers (Maps to All Pages)

Address	Bits	Description
0xF0	8	0 "SPI Data I/O Register" on page 375
0xF1	8	1 "SPI Data I/O Register" on page 375
0xF2	8	2 "SPI Data I/O Register" on page 375
0xF3	8	3 "SPI Data I/O Register" on page 375
0xF4	8	4 "SPI Data I/O Register" on page 375
0xF5	8	5 "SPI Data I/O Register" on page 375
0xF6	8	6 "SPI Data I/O Register" on page 375
0xF7	8	7 "SPI Data I/O Register" on page 375
0xF8h–0xFD	Reserved	
0xFE	8	"SPI Status Register" on page 375
0xFF	8	"Page Register" on page 376

SPI Data I/O Register

Table 330: SPI Data I/O Register (Maps to All Registers, Address F0h–F7h)

Bit	Name	R/W	Description	Default
7:0	SPI Data I/O	R/W	SPI data bytes[7:0]	–

SPI Status Register

Table 331: SPI Status Register (Maps to All Registers, Address FEh)

Bit	Name	R/W	Description	Default
7	SPIF	RO	SPI Read/Write Complete Flag.	0
6	WCOL	RO	SPI Write Collision	0
5	RACK	RO (SC)	SPI Read Data Ready Acknowledgement (Self-Clearing).	0
4:3	Reserved	RO	Write as 000, ignore when read.	0
2	MDIO Start	RO	Start/Done MDC/MDIO operation	0
1	RXRDY	RO	Rx Ready Flag—Should check every 8 bytes.	0
0	TXRDY	RO	Tx Ready Flag—Should check every 8 bytes.	0

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Page Register

Table 332: Page Register (Maps to All Registers, Address FFh)

Bit	Name	R/W	Description	Default
7:0	PAGE_REG	R/W	Binary value determines the value of the accessed register page.	0

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Section 9: Electrical Characteristics

Absolute Maximum Ratings

Table 333: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
$V_{1.2}$	Supply Voltage	GND–0.3	1.32	V
$V_{2.5}$	Supply Voltage	GND–0.3	2.75	V
$V_{3.3}$	Supply Voltage	GND–0.3	3.63	V
I_I	Input Current	–	±10	mA
T_{STG}	Storage Temperature	–40	+125	°C
V_{ESD}	Electrostatic Discharge	–	1000	V

Note: These specifications indicate conditions where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect the long-term reliability of the device.

Recommended Operating Conditions

Table 334: Recommended Operating Conditions

Sym	Parameter	Pins	Mode	Minimum	Maximum	Units
VDD	Supply voltage (see Note)	AVDD2, AVDDL, SAVDD, DVDD, PLLAVDD, PLL2AVDD	–	1.14	1.26	V
		AVDD, BIASVDD, XTALVDD, OVDD, VREG_AVDD	–	2.375	2.625	V
		OVDD2	–	3.135	3.465	V
			–	2.375	2.625	V
V_{IH}	High-level input voltage	All digital inputs	–	2.0	–	V
V_{IL}	Low-level input voltage	All digital inputs	–	–	0.8	V
V_{IDIFF}	Differential input voltage	RD± {24:47}	–	150	–	mV
CT	Magnetic center-tap	–	TX	2.375	2.625	V
V_{ICM}	Common mode input voltage	RD±{24:47}	TX	2.375	2.625	V
			FX	1.14	2.625	V
R_{DAC}	DAC current-setting resistance	RDAC	–	1.00	1.00	kΩ (1%)
T_A	Ambient operating temperature	–	–	0	70	°C

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Table 334: Recommended Operating Conditions

Sym	Parameter	Pins	Mode	Minimum	Maximum	Units
T_A	Ambient operating temperature (Industrial Grade)	–	–	-40	85	°C
T_J	Maximum Junction Temperature	–	–	–	125	°C

Note: OVDD2 can be set to 2.5V depending the device configuration. See Table 48: "Hardware Signal Descriptions," on page 137.

Note: It is recommended to power up the 1.2V, 2.5V and 3.3V supplies as quickly as possible with a delay separation within 1 to 5 ms. The total ramp-up time should be maintained at less than 10 ms.

Electrical Characteristics

Table 335: Electrical Characteristics

Sym	Parameter	Pins	Conditions	Minimum	Typical	Maximum	Units
$I_{DD1.2}$	1.2V supply current	SAVDD	100Base-TX	–	–	279	mA
			10Base-T	–	–	279	
		DVDD	100Base-TX	–	–	1180	
			10Base-T	–	–	998	
		AVDDL, PLLAVDD, PLL2AVDD, AVDD2	100Base-TX	–	–	477	
			10Base-T	–	–	113	
$I_{DD2.5}$	2.5V supply current	OVDD, AVDD	100Base-TX	–	–	132	mA
			100Base-T	–	–	123	
$I_{DD1.8}$	1.8V supply current	Transformer center taps, termination resistors	100Base-TX	–	–	1079	mA
			10Base-T	–	–	1719	
$I_{DD2.5/3.3}$	2.5 or 3.3V supply current	OVDD2	100Base-TX	–	–	20	mA
			10Base-T	–	–	20	
V_{OH}	High-level output voltage	Digital output	I_{OH} = –4/8/15 mA	2.0	–	–	V
		TD± {47:24}	Driving loaded magnetics module	–	–	VDD + 1.5	V
V_{OL}	Low-level output voltage	Digital output	I_{OL} = 4/8/15 mA	–	–	0.4	V
		TD± {47:24}	Driving loaded magnetics module	VDD – 1.5	–	–	V
V_{OP}	Transmitter output peak-to-peak differential voltage	Serdes output pins	Programmable	150	500	1000	mV

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Table 335: Electrical Characteristics

Sym	*Parameter*	*Pins*	*Conditions*	*Minimum*	*Typical*	*Maximum*	*Units*
V_{ID}	Peak-to-peak differential input voltage	Serdes Input Pins	AC coupled input signal, DC level biased in receiver	100	–	2000	mV
R_{IN}	Receiver input impedance	Serdes input pins	Differential, integrated on-chip	80	100	120	Ω
R_O	Transmitter output impedance	Serdes output pins	Differential	80	100	120	Ω
I_I	Input current	Digital inputs with pull-up resistors	V_I = OVDD	–	–	+100	µA
			V_I = GND	–	–	–200	µA
		Digital inputs with pull-down resistors	V_I = OVDD	–	–	+200	µA
			V_I = GND	–	–	–10	µA
		All other digital inputs	GND ≤ V_I ≤ OVDD	–	–	±100	µA
I_{OZ}	High-impedance output current	All three-state outputs	GND ≤ V_O ≤ OVDD	–	–	±10	µA
		All open-drain outputs	V_O = OVDD	–	–	+10	µA

* = Per GMII interface.

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Section 10: BCM53262M Timing Characteristics

Reset and Clock Timing

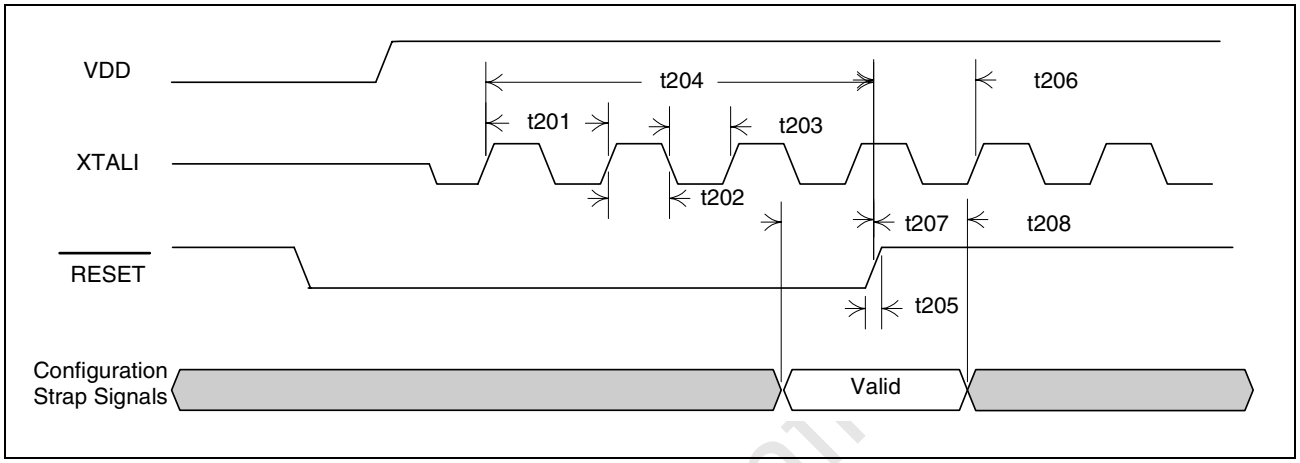

Figure 44: Reset and Clock Timing

Table 336: Reset and Clock Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t201	XTALI Period	39.998 ns	40 ns	40.002 ns
t202	XTALI High Time	18 ns	–	22 ns
t203	XTALI Low Time	18 ns	–	22 ns
t204	$\overline{\text{RESET}}$ Low Pulse Duration	400 ns	50 ms	–
t207	Configuration Valid Setup to $\overline{\text{RESET}}$ Rising	100 ns	–	–
t208	Configuration Valid Hold from $\overline{\text{RESET}}$ Rising	–	–	0 ns

SGMII/SerDes Interface Timing

The SGMII/SerDes Interface timing specifications are outlined in the subsequent sections.

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SGMII/SerDes Interface Output Timing

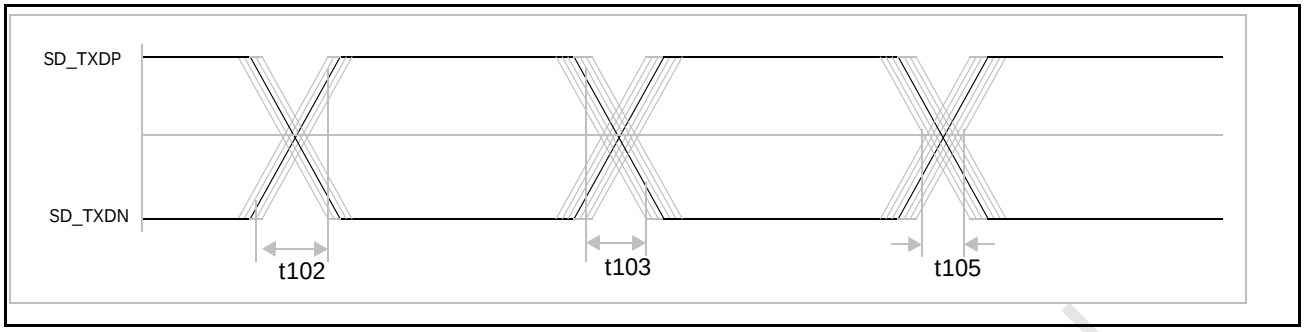

Figure 45: SGMII/SerDes Interface Output Timing

Table 337: SGMII/SerDes Interface Output Timings

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
SD_TXD Signaling Speed	t101	—	1.25	—	GBd
SD_TXD Rise Time (20%-80%)	t102	100	—	200	ps
SD_TXD Fall Time (20%- 80%)	t103	100	—	200	ps
SD_TXD Output Differential Skew (SD_TXDP vs. SD_TXDN)	t104	—	—	20	ps
SD_TXD Total Jitter	t105	—	—	192	ps

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SGMII/SerDes Interface Input Timing

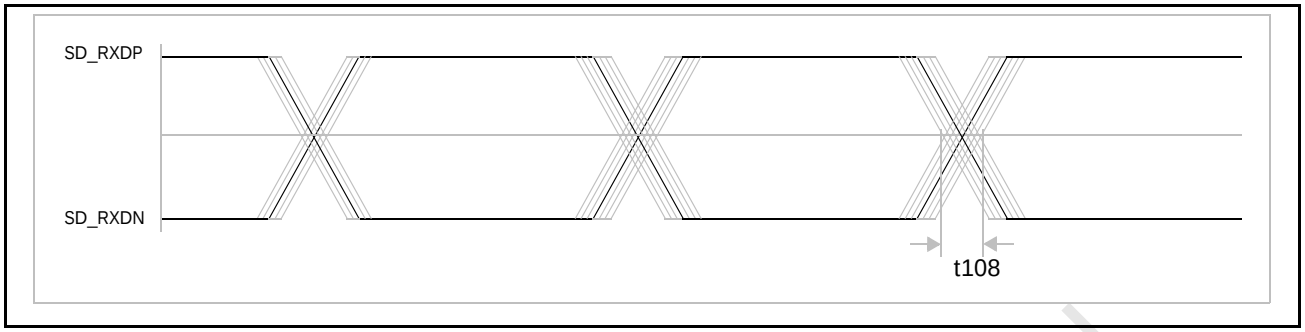

Figure 46: SGMII/SerDes Interface Input Timing

Table 338: SGMII/SerDes Interface Input Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
SD_RXD Signaling Speed	t106	—	1.25	—	GBd
SD_RXD Input Differential Skew (SD_RXDP vs. SD_RXDN)	t107	—	—	40	ps
SD_RXD Jitter (pk-pk)	t108	—	—	480	ps
SD_RXD Differential Input (pk-pk)	t109	0.1	—	2.0	V

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LED Timing

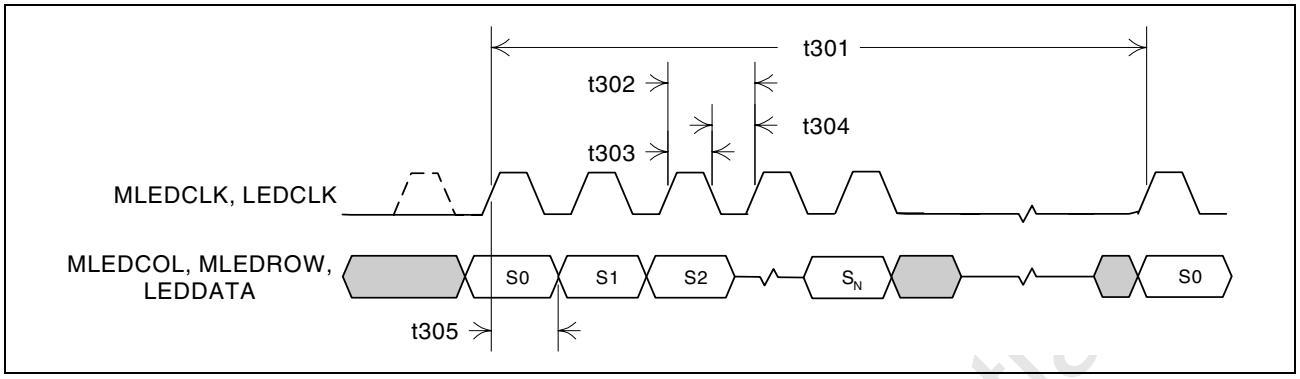

Figure 47: LED Timing

Table 339: LED Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t301	LED Update Cycle Period	–	40 ms	–
t302	MLEDCLK, LEDCLK Period	–	320 ns	–
t303	MLEDCLK, LEDCLK High Pulse Width	150 ns	–	170 ns
t304	MLEDCLK, LEDCLK Low Pulse Width	150 ns	–	170 ns
t305	LEDCLK to LEDDATA, MLEDCLK to MLEDCOL and MLEDROW Output time	140 ns	–	180 ns

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MII Input Timing

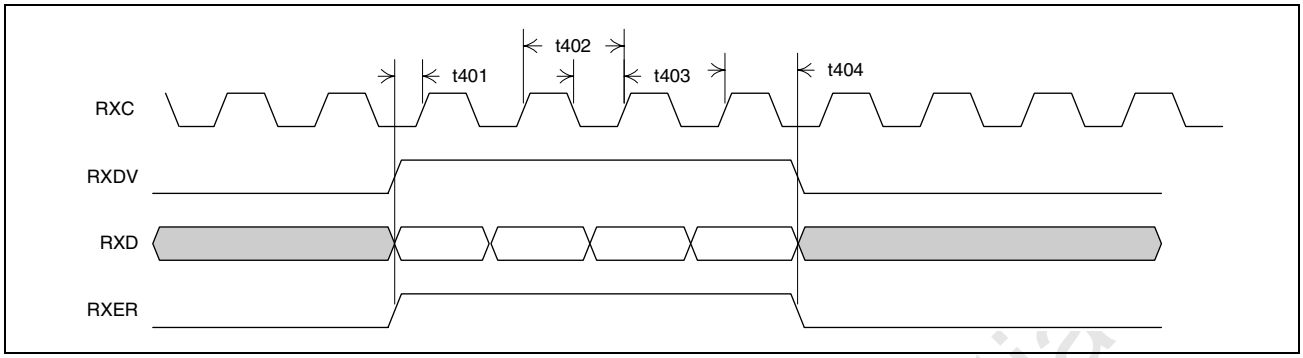

Figure 48: MII Input Timing

Table 340: MII Input Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t401	RXDV, RXD, RXER, to RXC Rising Setup Time	5 ns	–	–
t402	RXC Clock Period (10Base-T mode)	–	400 ns	–
	RXC Clock Period (100Base-T mode)	–	40 ns	–
t403	RXC High/Low Time (10Base-T mode)	160 ns	–	240 ns
	RXC High/Low Time (100Base-T mode)	14 ns	–	26 ns
t404	RXDV, RXD, RXER, to RXC Rising Hold Time	5 ns	–	–

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RvMII Input Timing

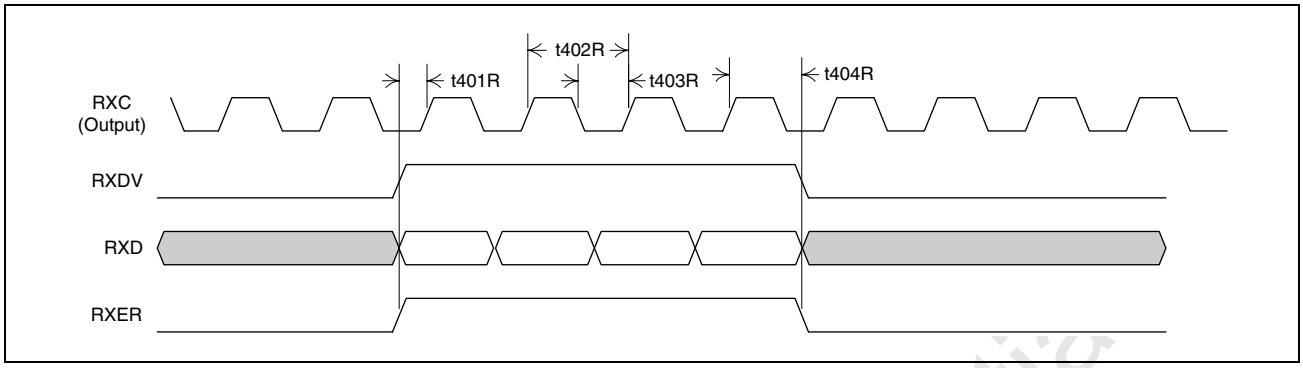

Figure 49: RvMII Input Timing

Table 341: RvMII Input Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t401R	RXDV, RXD, RXER, to RXC Rising Setup Time	10 ns	–	–
t402R	RXC Clock Period (100Base-T mode only)	–	40 ns	–
t403R	RXC High/Low Time (100Base-T mode only)	14 ns	–	26 ns
t404R	RXDV, RXD, RXER, to RXC Rising Hold Time	0 ns	–	–

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MII Output Timing

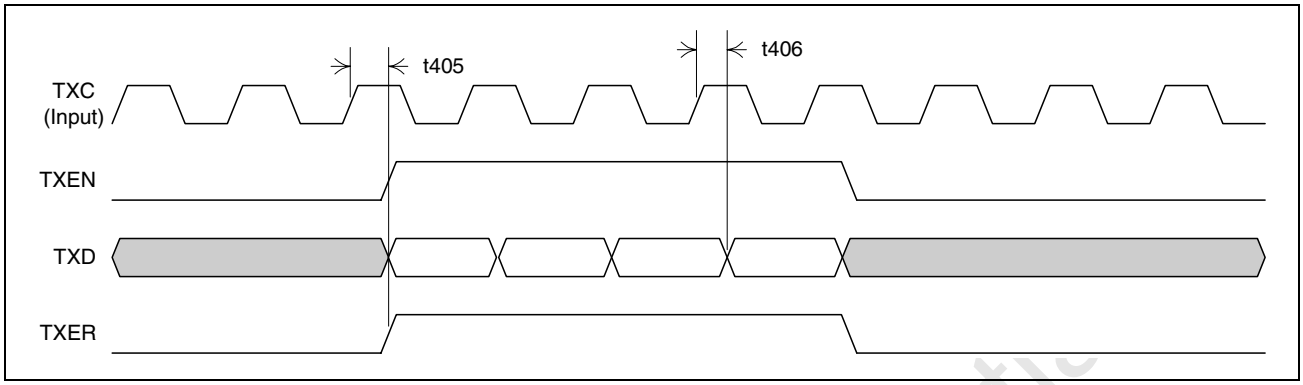

Figure 50: MII Output Timing

Table 342: MII Output Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t405	TXC High to TXEN, TXD, TXER Valid	–	–	22 ns
t406	TXC High to TXEN, TXD, TXER Invalid	3 ns	–	–

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RvMII Output Timing

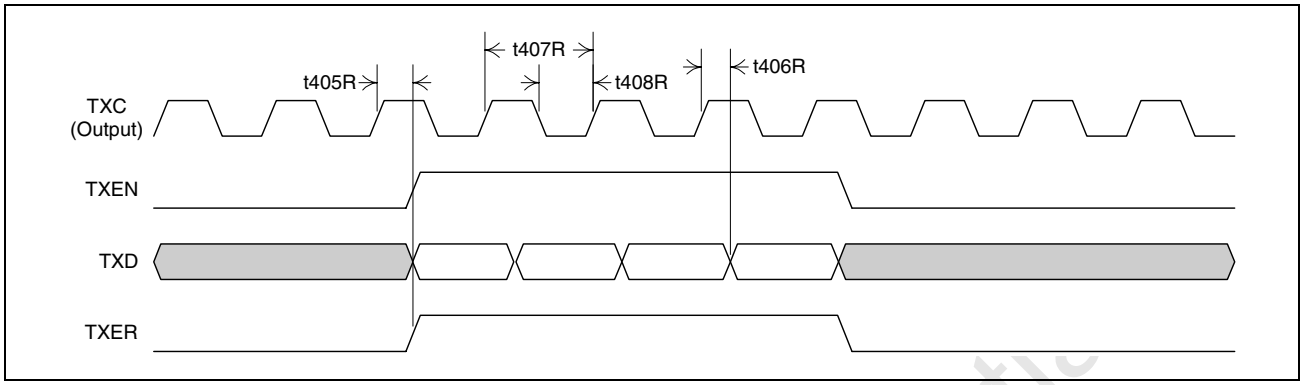

Figure 51: RvMII Output Timing

Table 343: RvMII Output Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t405R	TXC High to TXEN, TXD, TXER Valid	–	–	29 ns
t406R	TXC High to TXEN, TXD, TXER Invalid	11 ns	–	–
t407R	TXC Clock Period	–	40 ns	–
t408R	TXC High/Low Time	14 ns	–	26 ns

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GMII Interface Timing

GMII Interface Output Timing

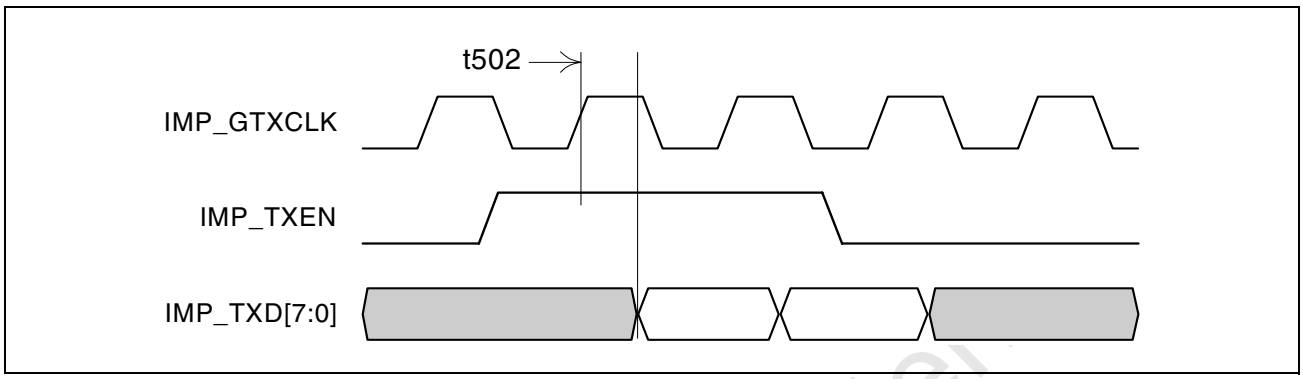

Figure 52: GMII Output Timing

Table 344: GMII Output Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
IMP_GTXCLK. clock period (1000M mode)	–	–	8	–	ns
IMP_GTXCLK. clock period (100M mode)	–	–	40	–	ns
IMP_GTXCLK. clock period (10M mode)	–	–	400	–	ns
Output delay from IMP_GTXCLK (rising)	t502	0.5	–	5.5	ns

GMII Interface Input Timing

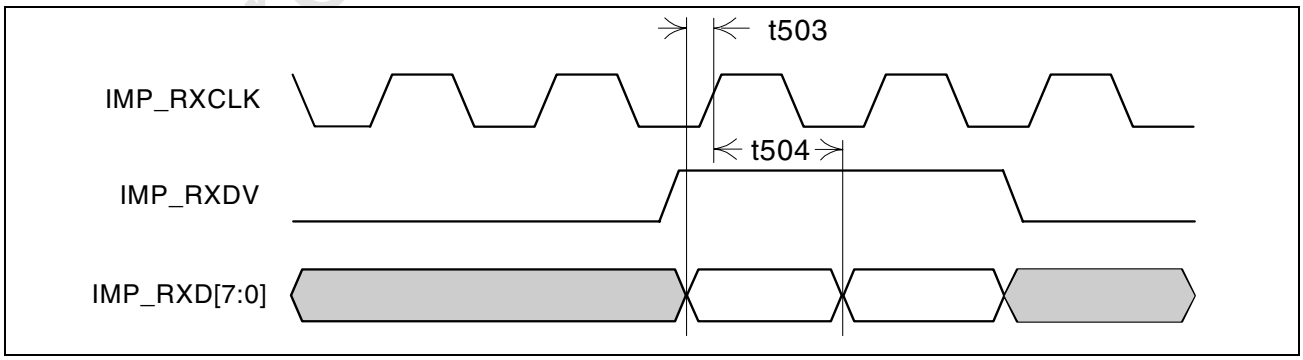

Figure 53: GMII Input Timing

Table 345: GMII Input Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
IMP_RXCLK clock period (1000M mode)	–	–	8	–	ns
IMP_RXCLK clock period (100M mode)	–	–	40	–	ns
IMP_RXCLK clock period (10M mode)	–	–	400	–	ns
Input setup time	t503	2.0	–	–	ns
Input hold time	t504	0.0	–	–	ns

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SPI Timing

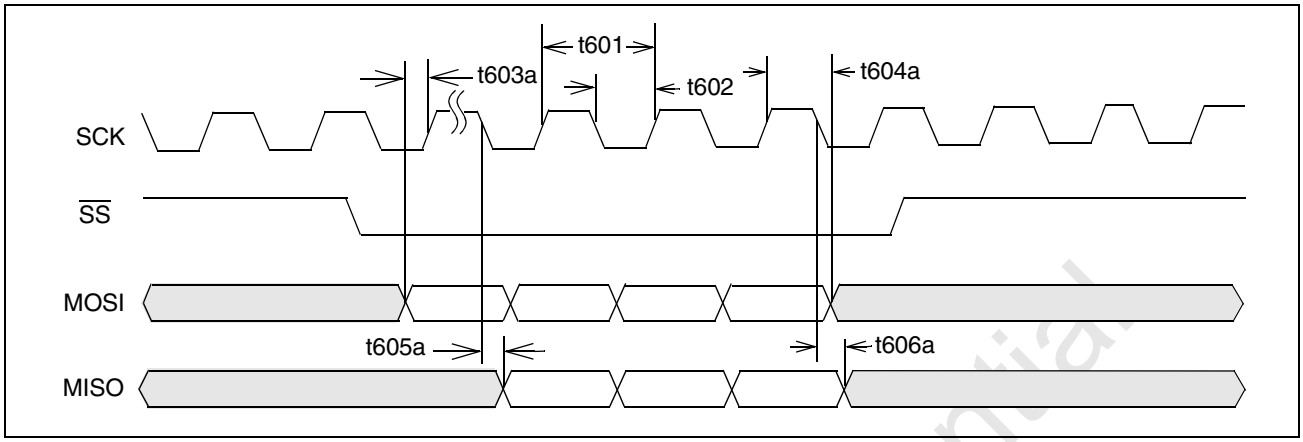

Figure 54: SPI Timing, SS Asserted During SCK High

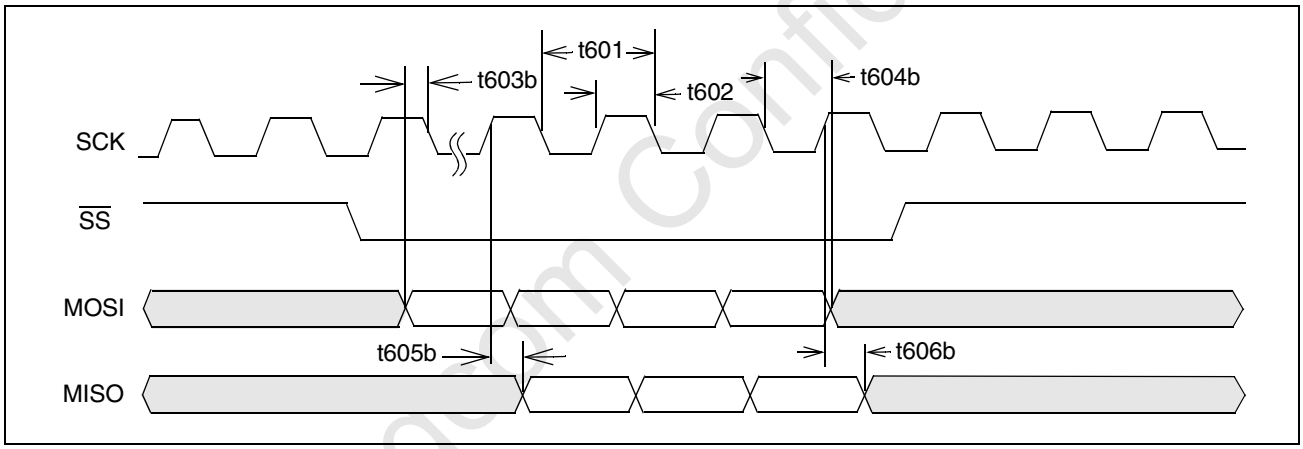

Figure 55: SPI Timing, SS Asserted During SCK Low

Table 346: SPI Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t601	SCK Clock Period	–	500 ns	–
t602	SCK High/Low Time	200 ns	–	300 ns
t603a, t603b	MOSI to SCK Setup Time	5 ns	–	–
t604a, t604b	MOSI to SCK Hold Time	12 ns	–	–
t605a, t605b	SCK to MISO Valid	–	–	25 ns
t606a, t606b	SCK to MISO Invalid	0 ns	–	–

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Note: The BCM53262M behaves only as a slave device. The $\overline{SS}$ is asynchronous. If $\overline{SS}$ is asserted during SCK high then BCM53262M samples data on the rising edge of SCK and references the falling edge to output data. Otherwise BCM53262M samples data on the falling edge and outputs data on the rising edge of SCK.

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EEPROM Timing

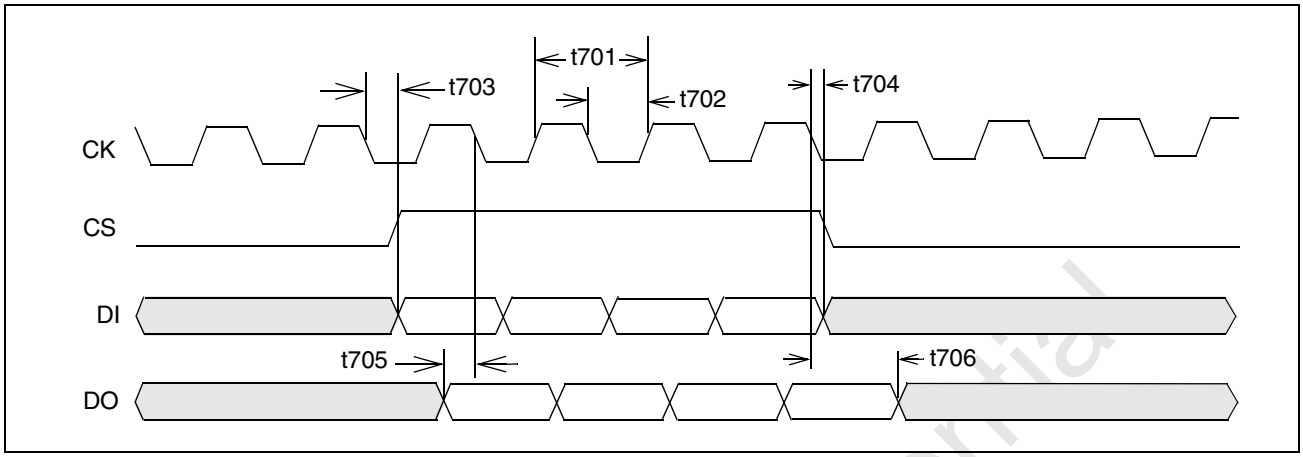

Figure 56: EEPROM Timing

Table 347: EEPROM Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t701	CK Clock Frequency	–	100 KHz	–
t702	CK High/Low Time	–	5 us	–
t703	CK low to CS, DI Valid	–	–	500 ns
t704	CK low to CS, DI Invalid	500 ns	–	–
t705	DO to CK falling Setup Time	200 ns	–	–
t706	DO to CK falling Hold Time	200 ns	–	–

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EB Bus Timing

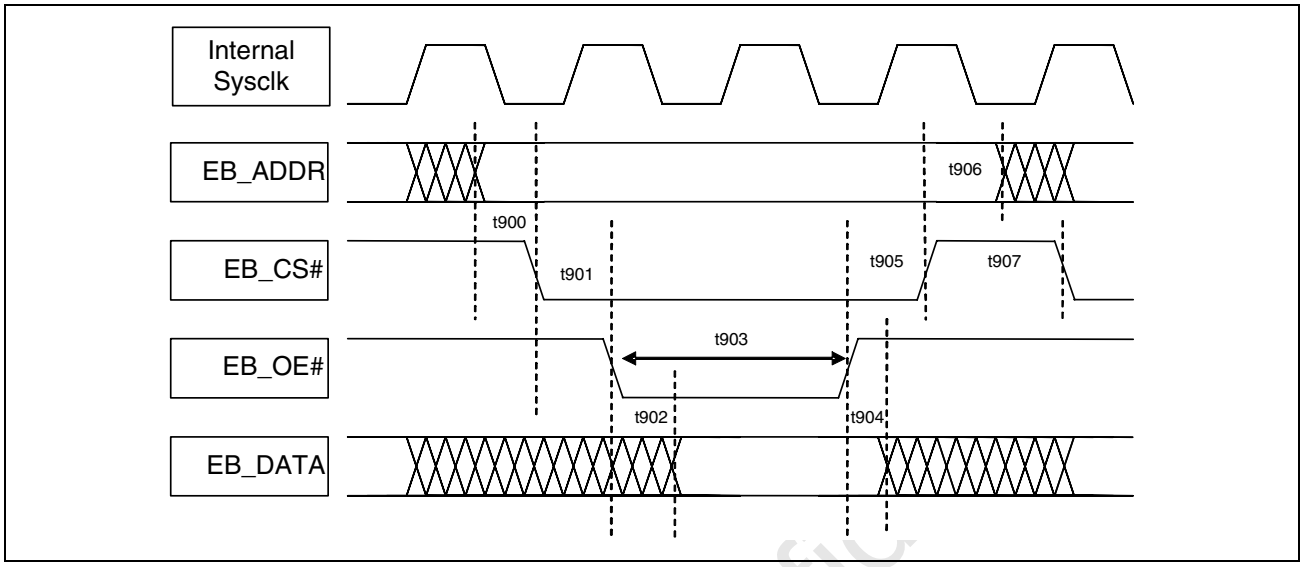

Figure 57: EB Bus Read Cycle

Table 348: EB Bus Read Cycle Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t900	Address setup time. (Address valid to CS# low)	0 ns	–	–
t901	CS# setup time. (CS# low to OE# low)	5 ns	–	–
t902	Data access time. (OE# low to Data valid)	–	20	–
t903	OE# active time (Based on 100 MHz system clock, minimum four cycles).	40 ns	–	–
t904	Data hold time. (OE# high to Data invalid)	0 ns	–	–
t905	CS# hold time. (OE# high to CS# high)	0 ns	–	–
t906	Address hold time. (CS# to Address invalid time)	5 ns	–	–
t907	CS# inactive time	5 ns	–	–

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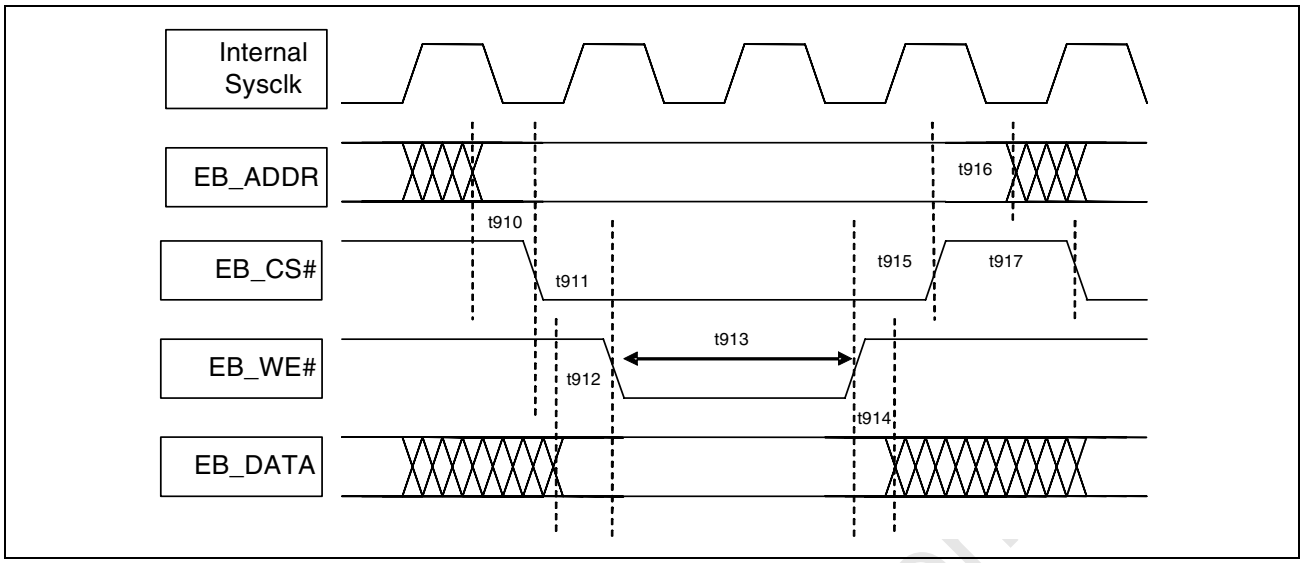

Figure 58: EB Bus Write Cycle

Table 349: EB Bus Write Cycle Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t910	Address setup time. (Address valid to CS# low)	0 ns	–	–
t911	CS# setup time. (CS# low to OE# low)	10 ns	–	–
t912	Data access time. (OE# low to Data valid)	10 ns	20	–
t913	WE# active time (Based on 100 MHz system clock, minimum four cycles).	40 ns	–	–
t914	Data hold time. (WE# high to Data invalid)	0 ns	–	–
t915	CS# hold time. (WE# high to CS# high)	0 ns	–	–
t916	Address hold time. (CS# to Address invalid time)	10 ns	–	–
t917	CS# inactive time	10 ns	–	–

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Management Data Interface

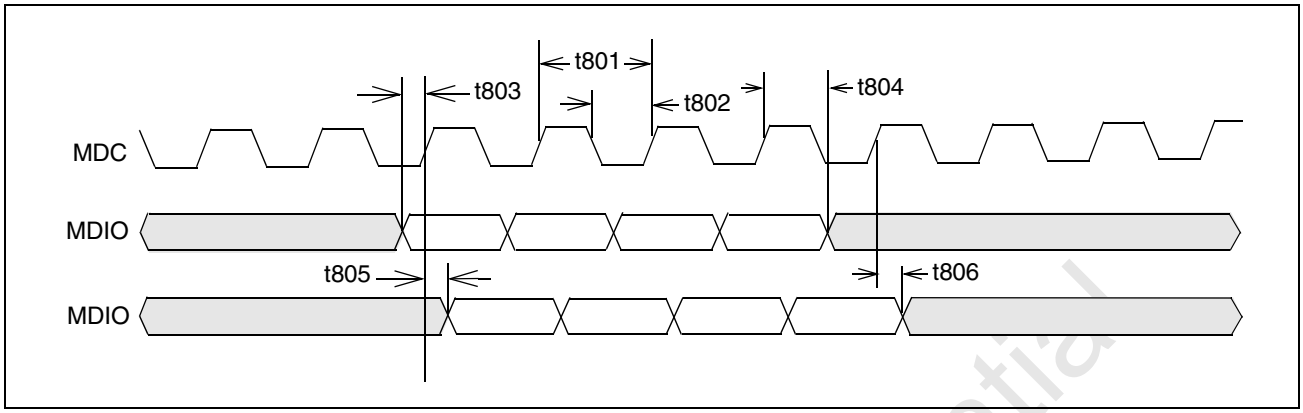

Figure 59: Management Data Interface

Table 350: Management Data Interface (Slave Mode)

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t801	MDC Clock Period	–	80 ns	–
t802	MDC High/Low Time	30 ns	–	50 ns
t803	MDIO to MDC rising Setup Time	5 ns	–	–
t804	MDIO to MDC rising Hold Time	5 ns	–	–
t805	MDC rising to MDIO Valid	–	–	50 ns
t806	MDC rising to MDIO Invalid	10 ns	–	–

Table 351: Management Data Interface (Master Mode)

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t801	MDC Clock Period	–	400 ns	–
t802	MDC High/Low Time	150 ns	–	250 ns
t803	MDIO to MDC rising Setup Time	10 ns	–	–
t804	MDIO to MDC rising Hold Time	10 ns	–	–
t805	MDC rising to MDIO Valid	–	–	100 ns
t806	MDC rising to MDIO Invalid	10 ns	–	–

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Section 11: Thermal Characteristics

Table 352: 676 PBGA Thermal Characteristics with External Heat Sink at 70°C

Air Flow (LFPM)	*0*	*100*	*200*	*400*	*600*
Theta-JA (^{O}C/W)	8.83	7.19	6.66	6.14	6.01
Theta-JB (^{O}C/W)	4.70	–	–	–	–
Theta-JC (^{O}C/W)	4.40	–	–	–	–
Maximum Junction Temperature T_J	118.58^{O}C	–	–	–	–
Heatsink: TwinPeaks Electronics Aluminum blade-fin, 45 mm x 45 mm x 25 mm, k = 180 W/m.K.					

Table 353: 676 PBGA Thermal Characteristics with External Heat Sink at 85°C

Air Flow (LFPM)	*0*	*100*	*200*	*400*	*600*
Theta-JA (^{O}C/W)	8.83	7.19	6.66	6.14	6.01
Theta-JB (^{O}C/W)	4.70	–	–	–	–
Theta-JC (^{O}C/W)	4.40	–	–	–	–
Maximum Junction Temperature T_J	133.58	124.55	121.63	118.78	118.07
Heat sink: TwinPeaks Electronics Aluminum blade-fin, 45 mm x 45 mm x 25 mm, k = 180 W/m.K.					

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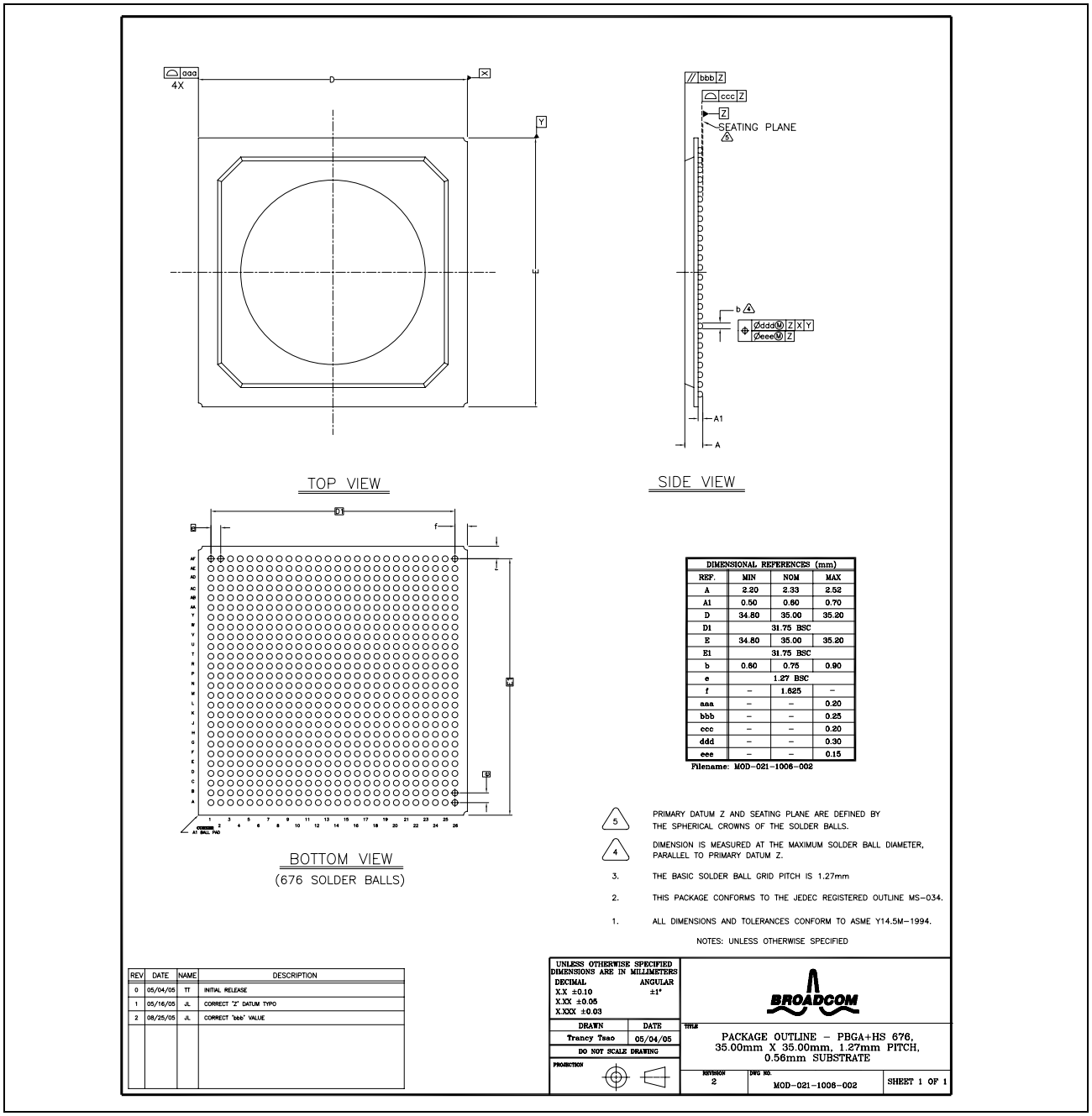
Section 12: Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	2.20	2.33	2.52
A1	0.50	0.60	0.70
D	34.80	35.00	35.20
D1		31.75 BSC	
E	34.80	35.00	35.20
E1		31.75 BSC	
b	0.60	0.75	0.90
e		1.27 BSC	
f	–	1.625	–
aaa	–	–	0.20
bbb	–	–	0.25
ccc	–	–	0.20
ddd	–	–	0.30
eee	–	–	0.15

Filename: MOD-021-1006-002

REV	DATE	NAME	DESCRIPTION
0	05/04/05	TT	INITIAL RELEASE
1	05/16/05	JL	CORRECT "Z" DATUM TYPO
2	08/25/05	JL	CORRECT "bbb" VALUE

Figure 60: 676 PBGA Package Outline Drawing

Section 13: Ordering Information

Table 354: Ordering Information

Part Number	*Package*	*Ambient Temperature*
BCM53262MKPB(G)	676 PBGA	Commercial grade 0°C to 70°C
BCM53262MIPB(G)	676 PBGA	Industrial grade –40°C to 85°C
Note: The letter *G* denotes the lead-free option.		

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