



Precision, Gain of 0.2 Level Translation DIFFERENCE AMPLIFIER

FEATURES

- GAIN OF 0.2 TO INTERFACE $\pm 10V$ SIGNALS TO SINGLE-SUPPLY ADCs
- GAIN ACCURACY: $\pm 0.024\%$ (max)
- WIDE BANDWIDTH: 1.5MHz
- HIGH SLEW RATE: $15V/\mu s$
- LOW OFFSET VOLTAGE: $\pm 100\mu V$
- LOW OFFSET DRIFT: $\pm 1.5\mu V/^\circ C$
- SINGLE-SUPPLY OPERATION DOWN TO 1.8V

APPLICATIONS

- INDUSTRIAL PROCESS CONTROLS
- INSTRUMENTATION
- DIFFERENTIAL TO SINGLE-ENDED CONVERSION
- AUDIO LINE RECEIVERS

DESCRIPTION

The INA159 is a high slew rate, $G = 1/5$ difference amplifier consisting of a precision op amp with a precision resistor network. The gain of $1/5$ makes the INA159 useful to couple $\pm 10V$ signals to single-supply analog-to-digital converters (ADCs), particularly those operating on a single +5V supply. The on-chip resistors are laser-trimmed for accurate gain and high common-mode rejection. Excellent temperature coefficient of resistance (TCR) tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The input common-mode voltage range extends beyond the positive and negative supply rails. It operates on a total of +1.8V to +5.5V single or split supplies. The INA159 reference input uses two resistors for easy mid-supply or reference biasing.

The difference amplifier is the foundation of many commonly-used circuits. The INA159 provides this circuit function without using an expensive external precision resistor network. The INA159 is available in an MSOP-8 surface-mount package and is specified for operation over the extended industrial temperature range, $-40^\circ C$ to $+125^\circ C$.

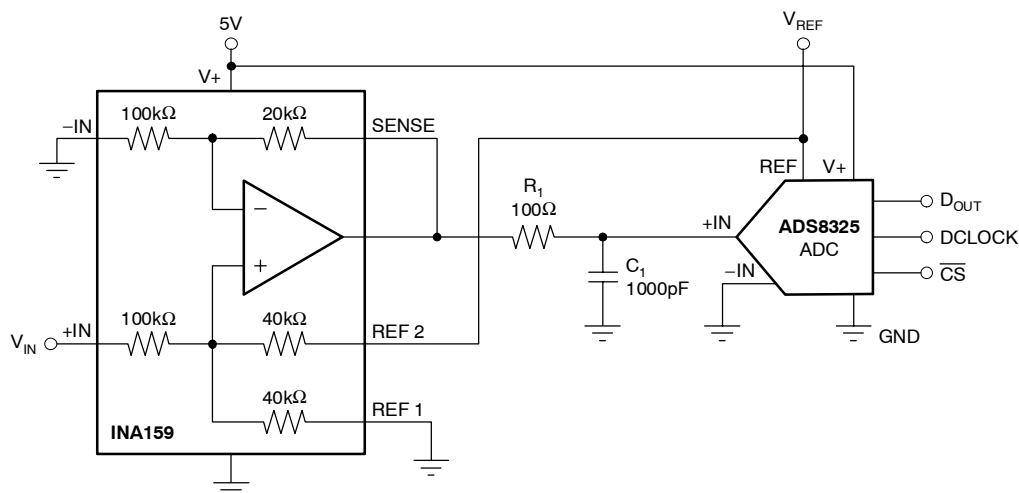


Figure 1. Typical Application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	+5.5V
Signal Input Terminals (-IN and +IN), Voltage	±30V
Reference (REF 1 and REF2) and Sense Pins	
Current	±10mA
Voltage	(V-) - 0.5V to (V+) + 0.5V
Output Short Circuit	Continuous
Operating Temperature	-40°C to +150°C
Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C
ESD Rating	
Human Body Model	4000V
Charged Device Model	1000V

⁽¹⁾ Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

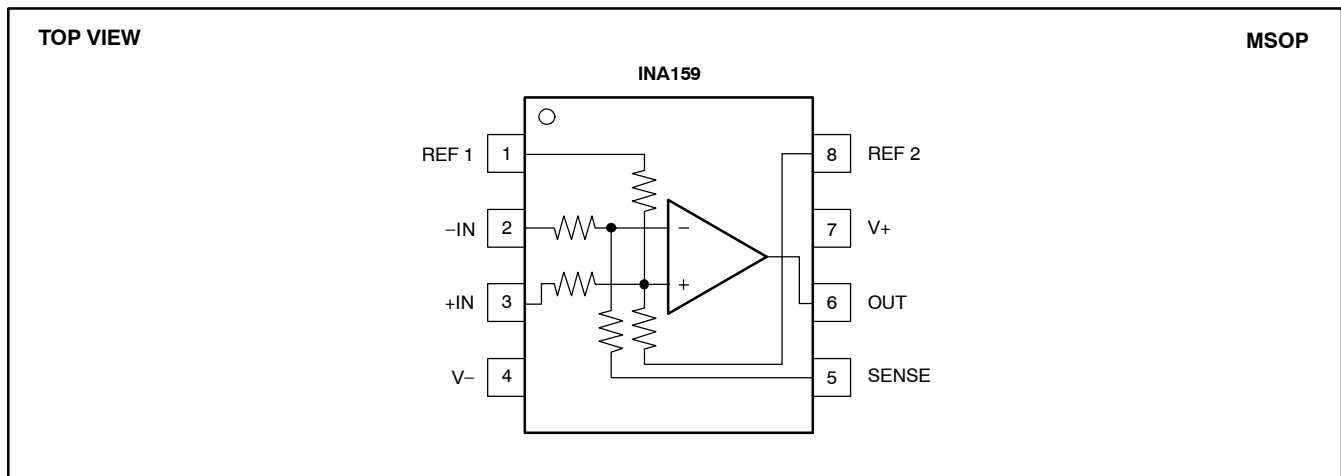
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA159	MSOP-8	DGK	CJB

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS



ELECTRICAL CHARACTERISTICS: $V_S = +5V$
Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

 At $T_A = +25^{\circ}\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{REF} = 5V$, unless otherwise noted.

PARAMETER	CONDITIONS	INA159			UNIT
		MIN	TYP	MAX	
OFFSET VOLTAGE⁽¹⁾	RTO				
Initial ⁽¹⁾ V_{OS}	$V_S = \pm 2.5V$, Reference and Input Pins Grounded		± 100	± 500	μV
vs Temperature			± 1.5		$\mu\text{V}/^{\circ}\text{C}$
vs Power Supply	$V_S = \pm 0.9V$ to $\pm 2.75V$		± 20	± 100	$\mu\text{V}/V$
Reference Divider Accuracy ⁽²⁾			± 0.002	± 0.024	%
over Temperature			± 0.002		%
INPUT IMPEDANCE⁽³⁾					
Differential			240		$\text{k}\Omega$
Common-Mode			60		$\text{k}\Omega$
INPUT VOLTAGE RANGE	RTI				
Common-Mode Voltage Range	V_{CM}		17.5		V
Positive			-12.5		V
Negative					
Common-Mode Rejection Ratio	$V_{CM} = -10V$ to $+10V$, $R_S = 0\Omega$	80	96		dB
over Temperature			94		dB
OUTPUT VOLTAGE NOISE⁽⁴⁾	RTO				
$f = 0.1\text{Hz}$ to 10Hz			10		μV_{PP}
$f = 10\text{kHz}$			30		$\text{nV}/\sqrt{\text{Hz}}$
GAIN	$V_{REF2} = 4.096V$, R_L Connected to GND, $(V_{IN+}) - (V_{IN-}) = -10V$ to $+10V$, $V_{CM} = 0V$				
Initial Error	G		0.2	± 0.024	V/V
vs Temperature			± 0.005		%
Nonlinearity			± 1		$\text{ppm}/^{\circ}\text{C}$
			± 0.0002		% of FS
OUTPUT					
Voltage, Positive	$V_{REF2} = 4.096V$, R_L Connected to GND	$(V+) - 0.1$	$(V+) - 0.02$		V
Voltage, Negative	$V_{REF2} = 4.096V$, R_L Connected to GND	$(V-) + 0.048$	$(V-) + 0.01$		V
Current Limit, Continuous to Common			± 60		mA
Capacitive Load		See Typical Characteristic			pF
Open-Loop Output Impedance	$f = 1\text{MHz}$, $I_O = 0$		110		Ω
FREQUENCY RESPONSE					
Small-Signal Bandwidth	-3dB		1.5		MHz
Slew Rate	SR		15		V/ μs
Settling Time, 0.01%	t_s	4V Output Step, $C_L = 100\text{pF}$	1		μs
Overload Recovery Time		50% Overdrive	250		ns
POWER SUPPLY					
Specified Voltage Range	V_S		+5		V
Operating Voltage Range		+1.8		+5.5	V
Quiescent Current	I_Q	$I_Q = 0\text{mA}$, $V_S = \pm 2.5V$, Reference and Input Pins Grounded	1.1	1.5	mA
TEMPERATURE RANGE					
Specified Range		-40		+125	$^{\circ}\text{C}$
Operating Range		-40		+150	$^{\circ}\text{C}$
Storage Range		-65		+150	$^{\circ}\text{C}$
Thermal Resistance	θ_{JA}	Surface-Mount	150		$^{\circ}\text{C}/\text{W}$
MSOP-8					

(1) Includes effects of amplifier input bias and offset currents.

(2) Reference divider accuracy specifies the match between the reference divider resistors using the configuration in Figure 2.

 (3) Internal resistors are ratio matched but have $\pm 20\%$ absolute value.

(4) Includes effects of amplifier input current noise and thermal noise contribution of resistor network.

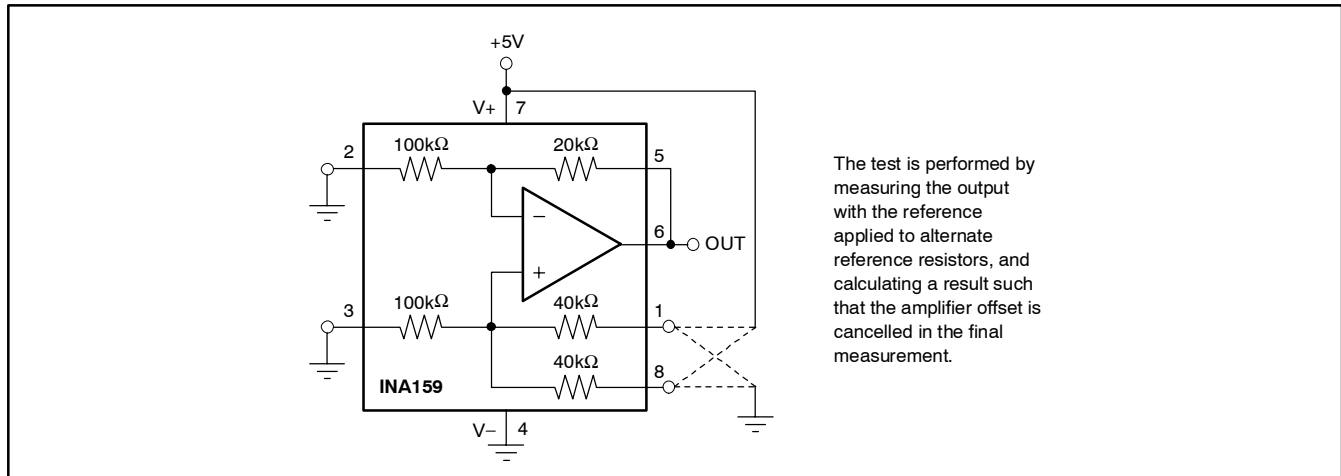
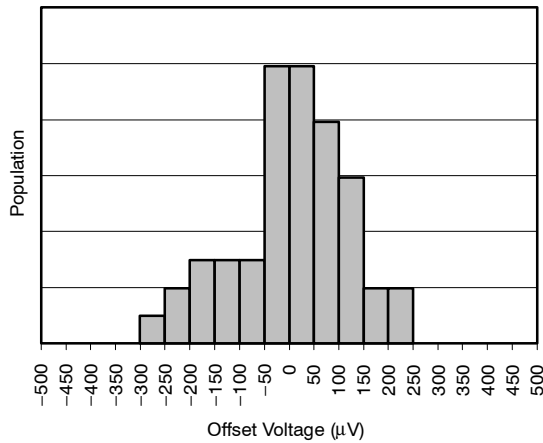


Figure 2. Test Circuit for Reference Divider Accuracy

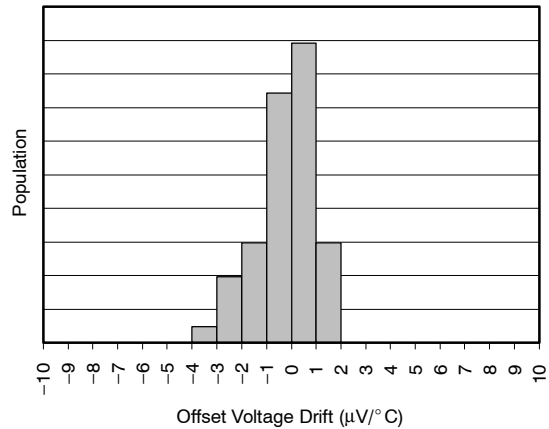
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{REF} = 5\text{V}$, unless otherwise noted.

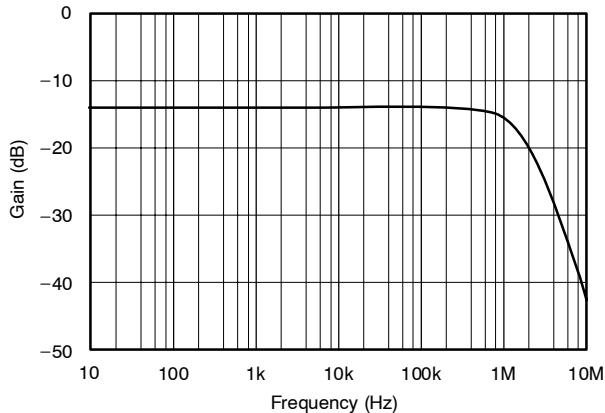
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



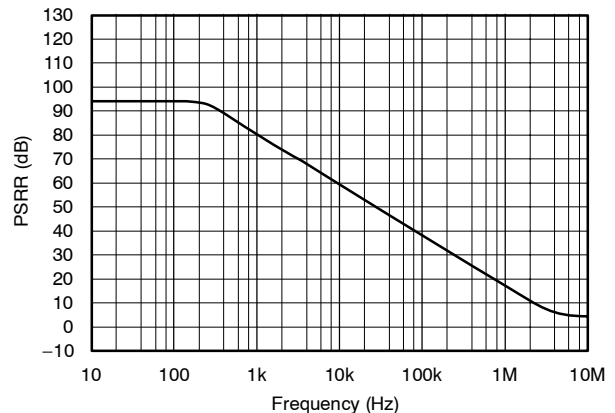
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



GAIN vs FREQUENCY

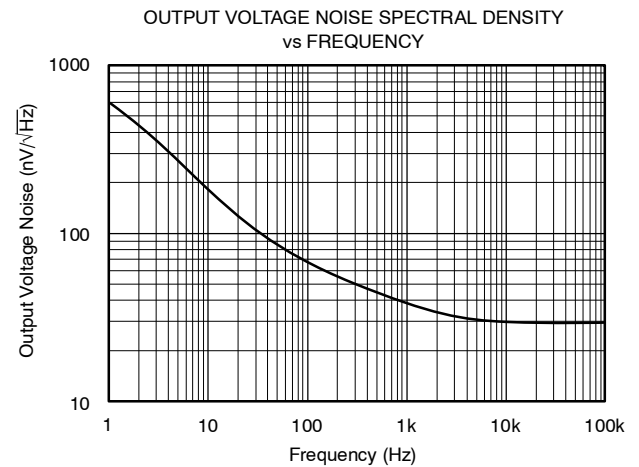
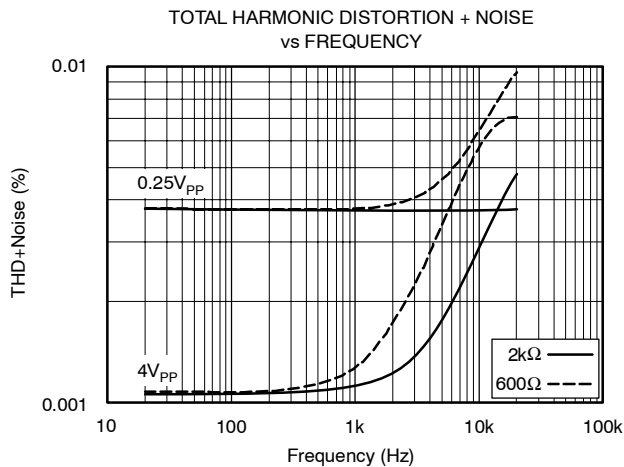
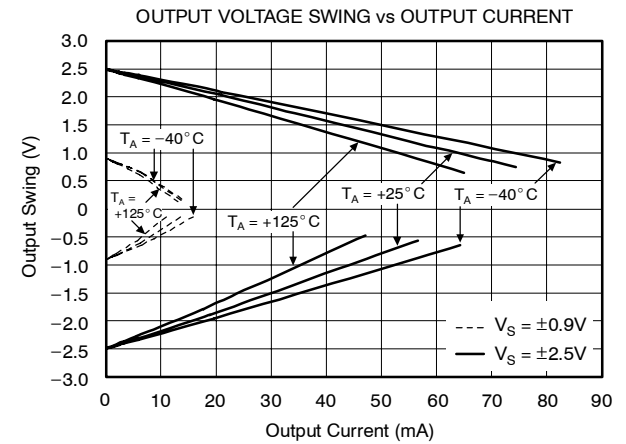
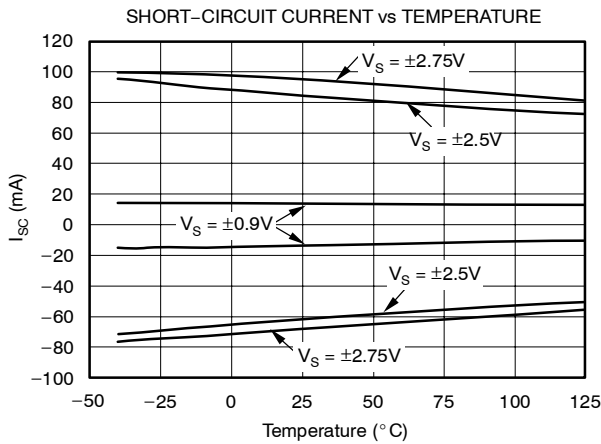
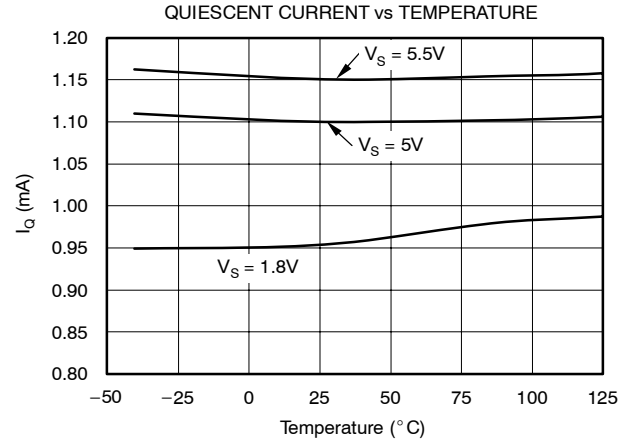
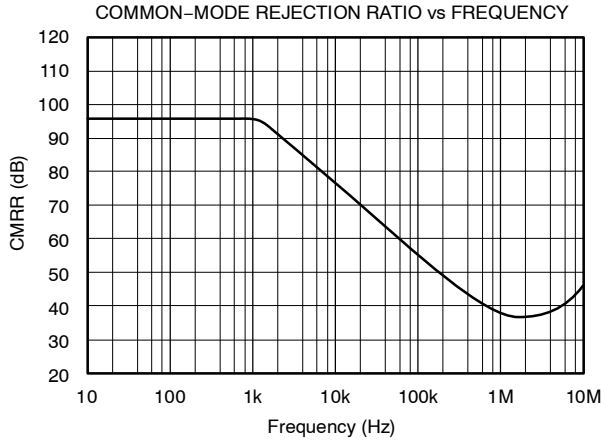


POWER-SUPPLY REJECTION RATIO vs FREQUENCY



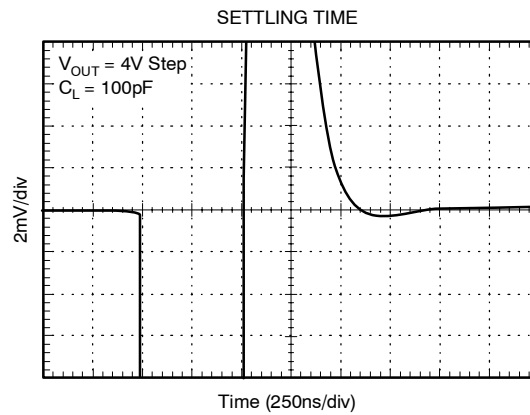
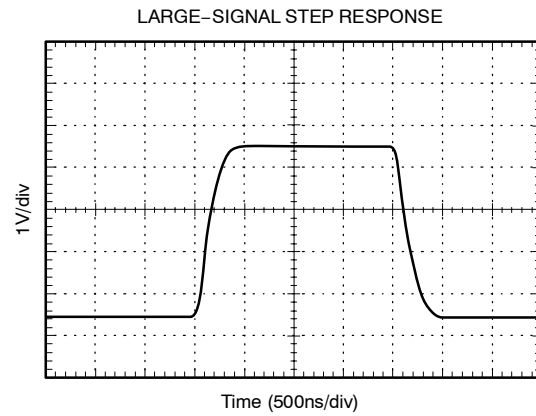
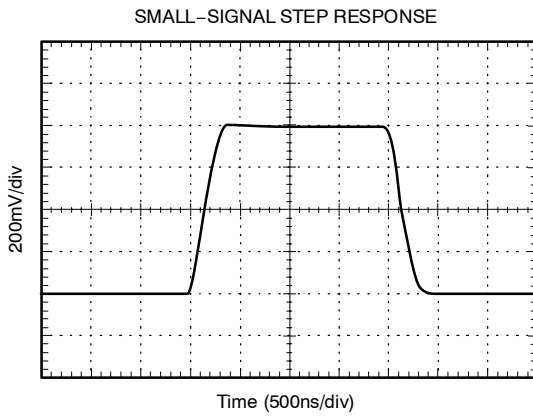
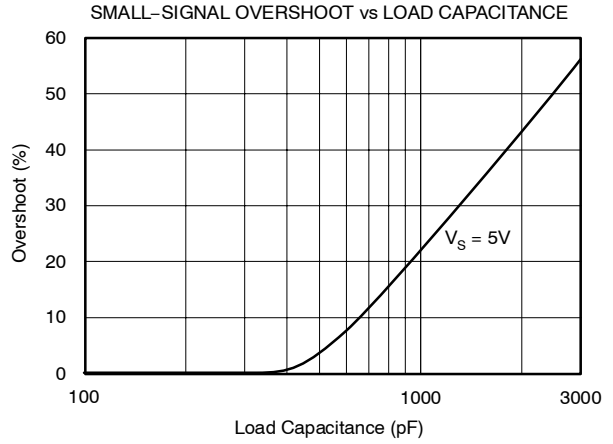
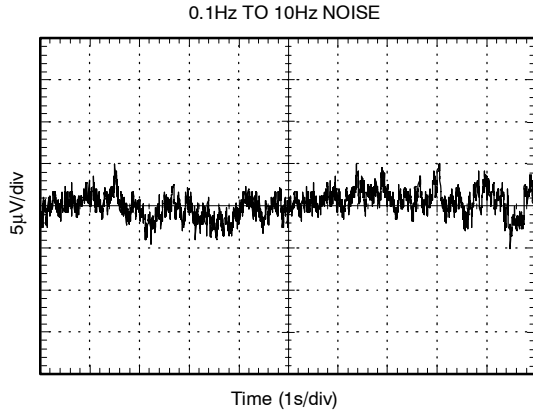
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{REF} = 5\text{V}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, REF pin 1 connected to ground, and REF pin 2 connected to $V_{REF} = 5\text{V}$, unless otherwise noted.



APPLICATION INFORMATION

The internal op amp of the INA159 has a rail-to-rail common-mode voltage capability at its inputs. A rail-to-rail op amp allows the use of $\pm 10V$ inputs into a circuit biased to 1/2 of a 5V reference (2.5V quiescent output). The inputs to the op amp will swing from approximately 400mV to 3.75V in this application.

The unique input topology of the INA159 eliminates the input offset transition region typical of most rail-to-rail complementary stage operational amplifiers. This allows the INA159 to provide superior glitch- and transition-free performance over the entire common-mode range.

Good layout practice includes the use of a 0.1 μ F bypass capacitor placed closely across the supply pins.

COMMON-MODE RANGE

The common-mode range of the INA159 is a function of supply voltage and reference. Where both pins, REF1 and REF2, are connected together:

$$V_{CM+} = (V+) + 5[(V+) - V_{REF}] \quad (1)$$

$$V_{CM-} = (V-) - 5[V_{REF} - (V-)] \quad (2)$$

Where one REF pin is connected to the reference, and the other pin grounded (1/2 reference connection):

$$V_{CM+} = (V+) + 5[(V+) - (0.5V_{REF})] \quad (3)$$

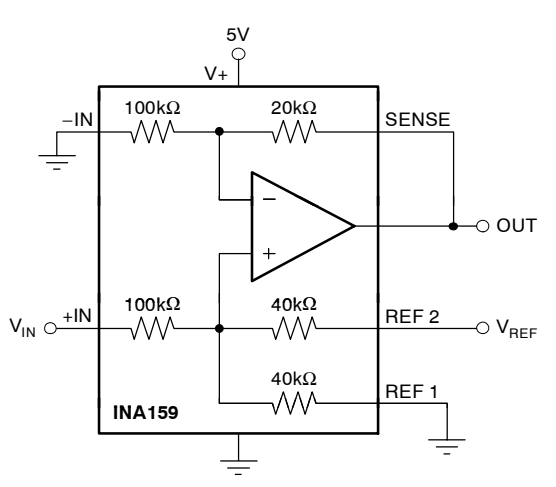
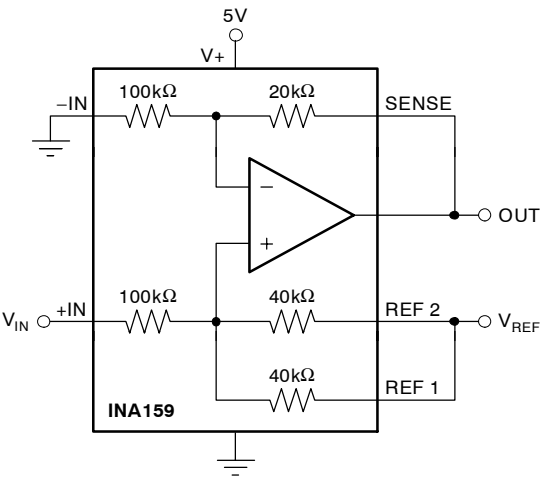
$$V_{CM-} = (V-) - 5[(0.5V_{REF}) - (V-)] \quad (4)$$

Some typical values are shown in Table 1.

Table 1. Common-Mode Range For Various Supply and Reference Voltages

REF 1 and REF 2 Connected Together				
V+	V-	V _{REF}	V _{CM+}	V _{CM-}
5	0	3	15	-15
5	0	2.5	17.5	-12.5
5	0	1.25	23.75	-6.25
1/2 Reference Connection				
V+	V-	V _{REF}	V _{CM+}	V _{CM-}
5	0	5	17.5	-12.5
5	0	4.096	19.76	-10.24
5	0	2.5	23.75	-6.25
3.3	0	3.3	11.55	-8.25
3.3	0	2.5	13.55	-6.25
3.3	0	1.25	16.675	-3.125

Table 2. Input and Output Relationships for Various Reference and Connection Combinations

V _{REF} (V)	REF CONNECTION	V _{OUT} for V _{IN} = 0 (V)	LINEAR V _{IN} RANGE (V)	USEFUL V _{OUT} SWING (V)
5		2.5	+10 0 -10	4.5 (±2V swing) 0.5
4.096		2.048	+10 0 -10	4.048 (±2V swing) 0.048
3.3		1.65	+10 0 -7.885	3.65 (-1.577V, +2V swing) 0.048
2.5		1.25	+10 (also +5) 0 -6 (also -5)	3.25 (-1.2V, +2V swing) 0.048
1.8		0.9	+10 0 -4.26	2.9 (-0.852V, +2V swing) 0.048
2.5		2.5	+10 0 -10	4.5 (±2V swing) 0.5
1.8		1.8	+10 0 -8.76	3.8 (-1.752V, +2V swing) 0.048
1.2		1.2	+10 0 -5.76	3.2 (-1.15V, +2V swing) 0.048

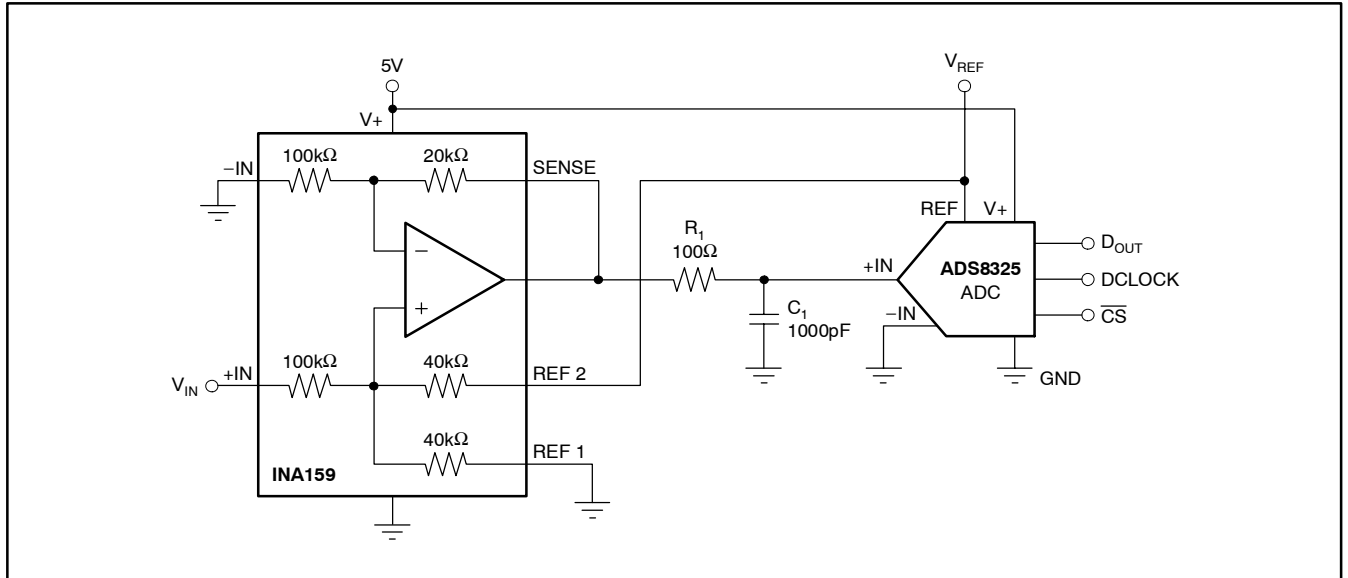


Figure 3. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs

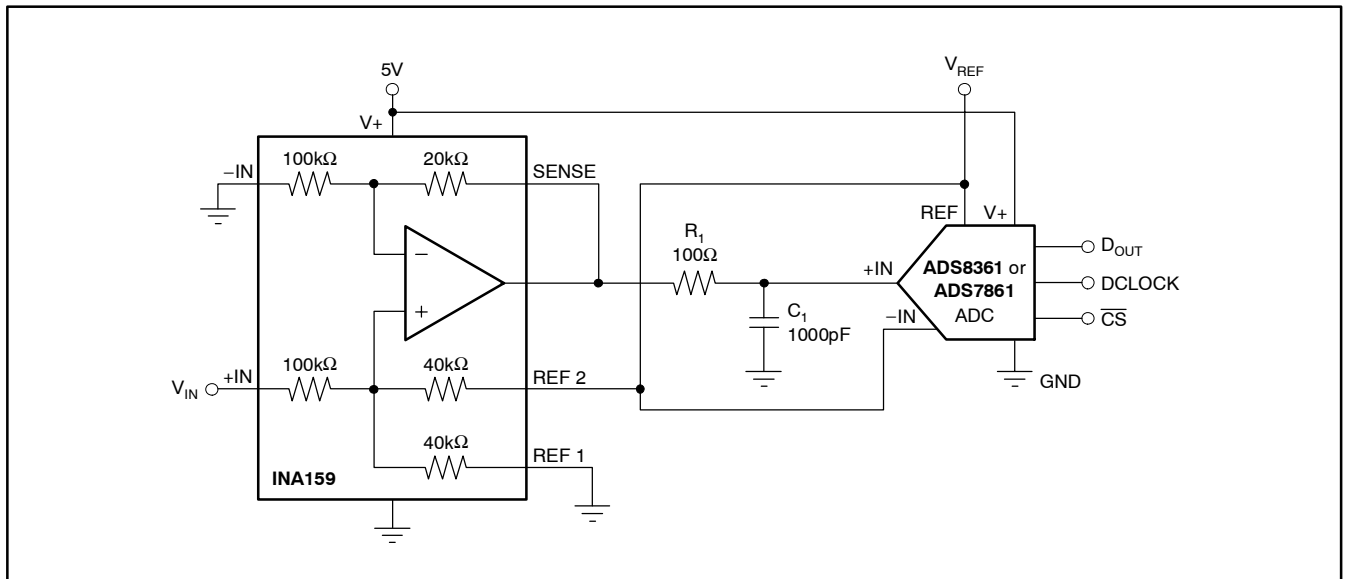
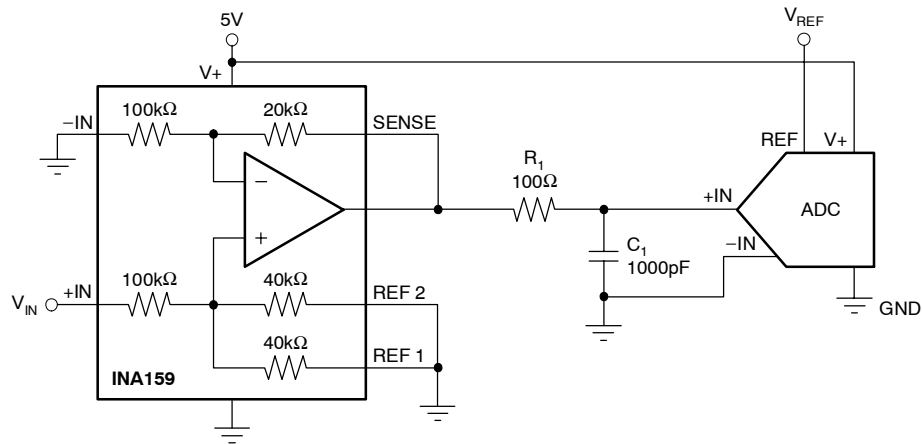
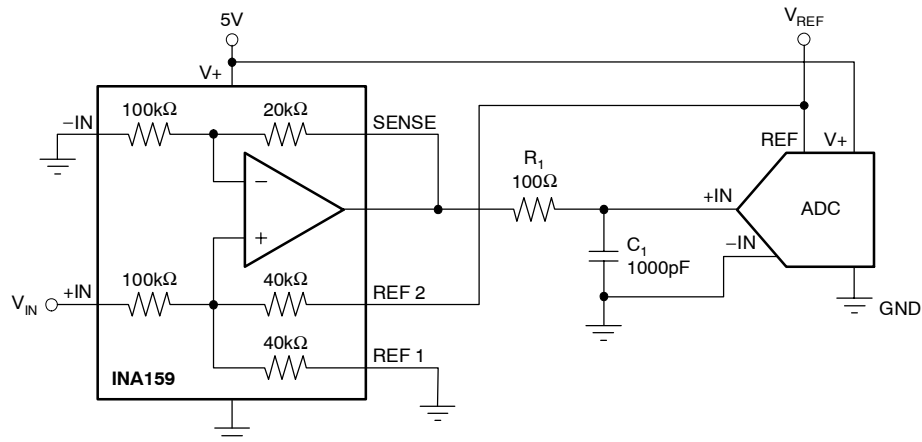


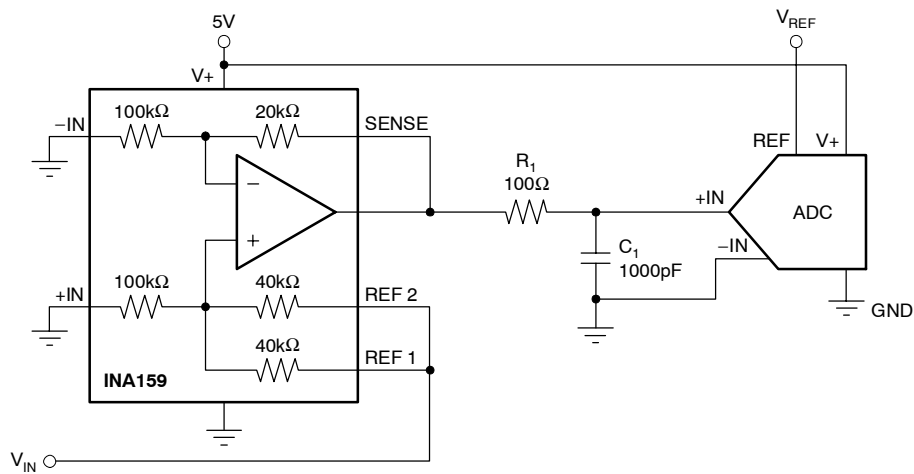
Figure 4. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs with Pseudo-Differential Inputs (such as the ADS7861 and ADS8361)



a) Unipolar, Noninverting, $G = 0.2$



b) Bipolar, Noninverting, $G = 0.2$



c) Unipolar, Unity Gain

Figure 5. Basic INA159 Configurations

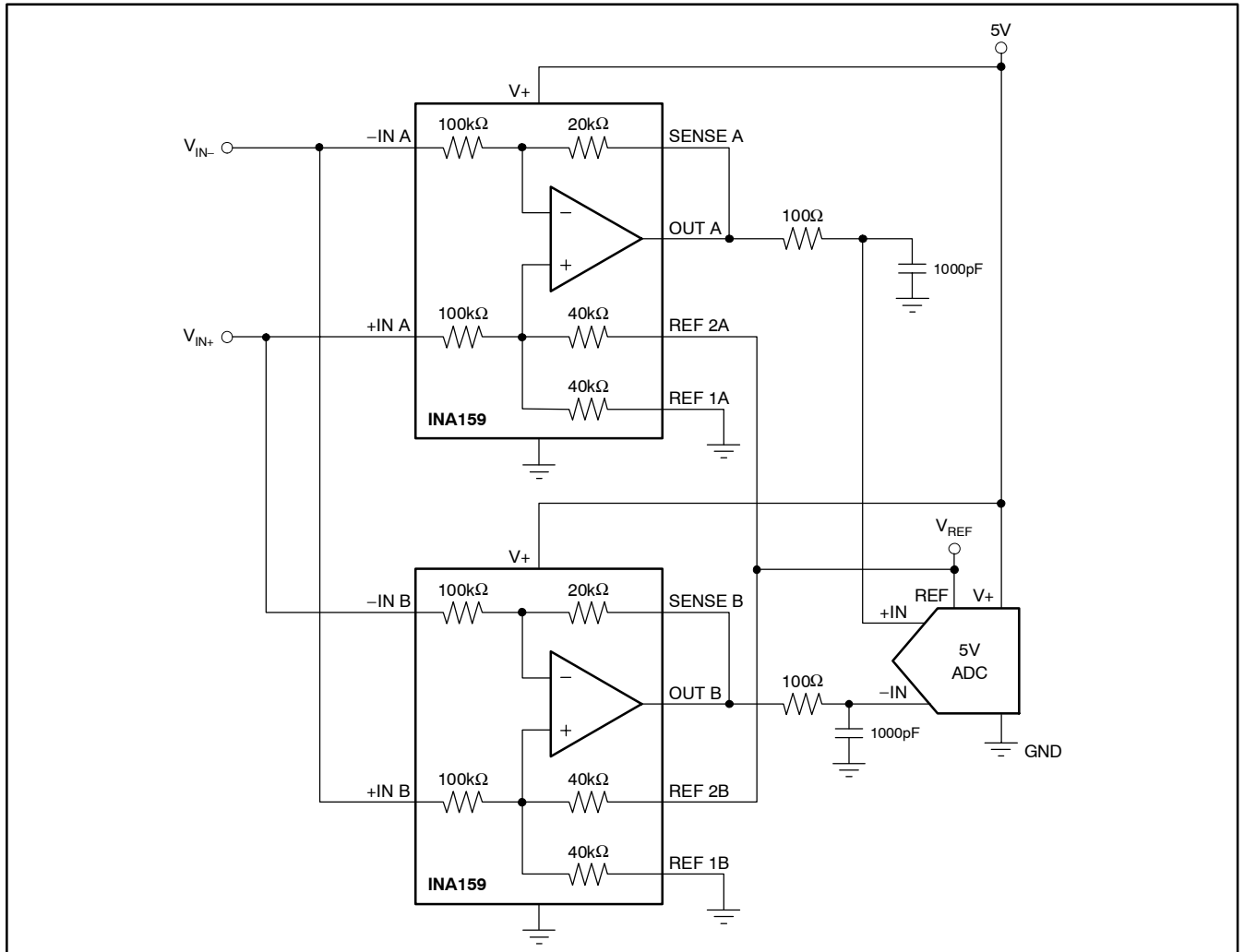


Figure 6. Differential ADC Drive

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA159AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI NIPDAUAG NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJB	Samples
INA159AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	CJB	Samples
INA159AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI NIPDAUAG NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJB	Samples
INA159AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	CJB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA159 :

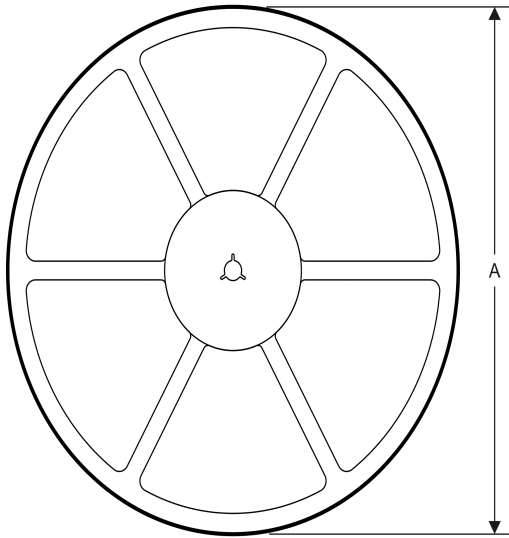
- Enhanced Product : [INA159-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA159AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA159AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA159AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
INA159AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated