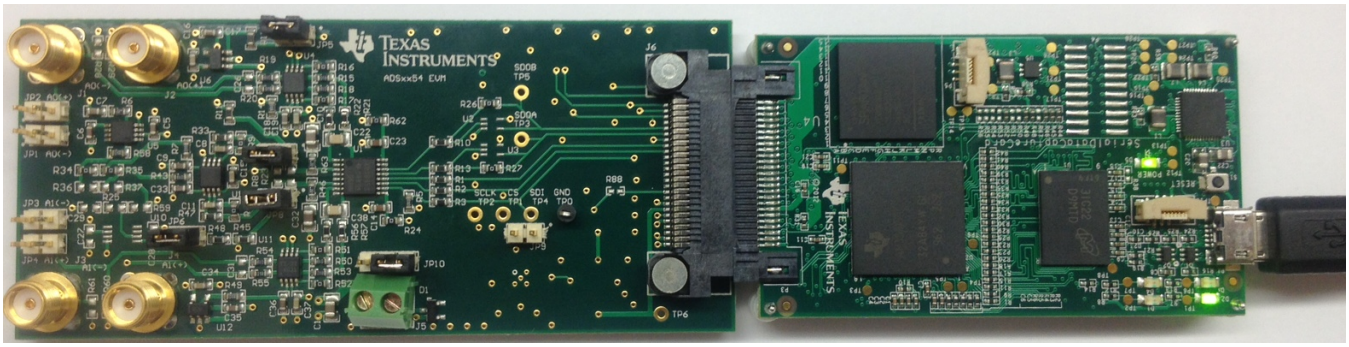
ADS8354EVM-PDK and ADS7854EVM-PDK



ADSxx54EVM-PDK

This user's guide describes the characteristics, operation and use of the ADS8354EVM and ADS7854EVM performance demonstration kits (PDKs). These kits are evaluation platforms for the ADS8354 and ADS7854, dual-channel, 16-bit and 14-bit, simultaneous sampling, successive approximation register (SAR) analog-to-digital converters (ADCs) that support fully-differential analog inputs. These EVMs ease the evaluation of the ADS8354 and ADS7854 devices with hardware and software for computer connectivity through a universal serial bus (USB). This user's guide includes complete circuit descriptions, schematic diagrams, and bills of material.

Throughout this document, the terms ADSxx54EVM-PDK, demonstration kit, evaluation board, evaluation module are synonymous with the ADS8354EVM-PDK and ADS7854EVM-PDK.

The following related documents are available through the Texas Instruments web site at http://www.ti.com.

Related Documentation

Device	Literature Number
ADS7854	SBAS556
ADS8354	SBAS556
REF5025	SBOS410
OPA2350	SBOS099
OPA376	SBOS432
THS4521	SBOSF458
TPS3836E18	SLVS292
TPS7A4700	SBVS204
REG71055	SBAS221

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1 Overview

The ADSxx54EVM-PDK is a platform for evaluation of the ADSxx54 analog-to-digital converter (ADC). The evaluation kit combines the ADSxx54EVM board with a serial data capture card (SDCC) controller board. The SDCC controller board consists of a TI Sitara embedded microcontroller (AM3352) and a field programmable gate array (FPGA). The SDCC controller board provides an interface from the EVM to the computer through a universal serial bus (USB) port. The included software communicates with the SDCC controller board platform, and the SDCC board provides the power and digital signals used to communicate with the ADSxx54EVM board. These demonstration kits include the ADSxx54EVM board, the SDCC controller board, a microSD memory card, and an A-to-micro-B USB cable.

1.1 ADSxx54EVM Features

- Contains support circuitry as a design example to match ADC performance
- 3.3-V slave serial peripheral interface (SPI™)
- Onboard 5-V analog supply
- Onboard REF5025 (2.5-V) reference
- Voltage reference buffering with OPA2350
- Onboard THS4521 (200-MHz bandwidth, 1-mA quiescent current) ADC input drivers

1.2 ADSxx54EVM-PDK Features

- Jumper-selectable ±1 x V_{ref} range or ±2 x V_{ref} range.
- USB port for computer interfacing
- Easy-to-use evaluation software for Windows XP®, Windows 7®, Windows 8® operating systems
- Data collection to text files
- Built-in analysis tools including scope, FFT, and histogram displays
- Complete control of board settings

2 EVM Analog Interface

The ADSxx54 is a dual-channel, simultaneous-sampling ADC that supports fully-differential analog inputs. Each channel of the ADSxx54 uses a THS4521 fully-differential amplifier to drive the differential inputs of the ADC. The ADSxx54EVM is designed for easy interfacing to multiple analog sources. SMA connectors allow the EVM to have input signals connected through coaxial cables. In addition, header connectors JP1 through JP4 provide a convenient way to connect input signals. All analog inputs are buffered by THS4521 high-speed, fully differential amplifier in order to properly drive the ADSxx54 ADC inputs.

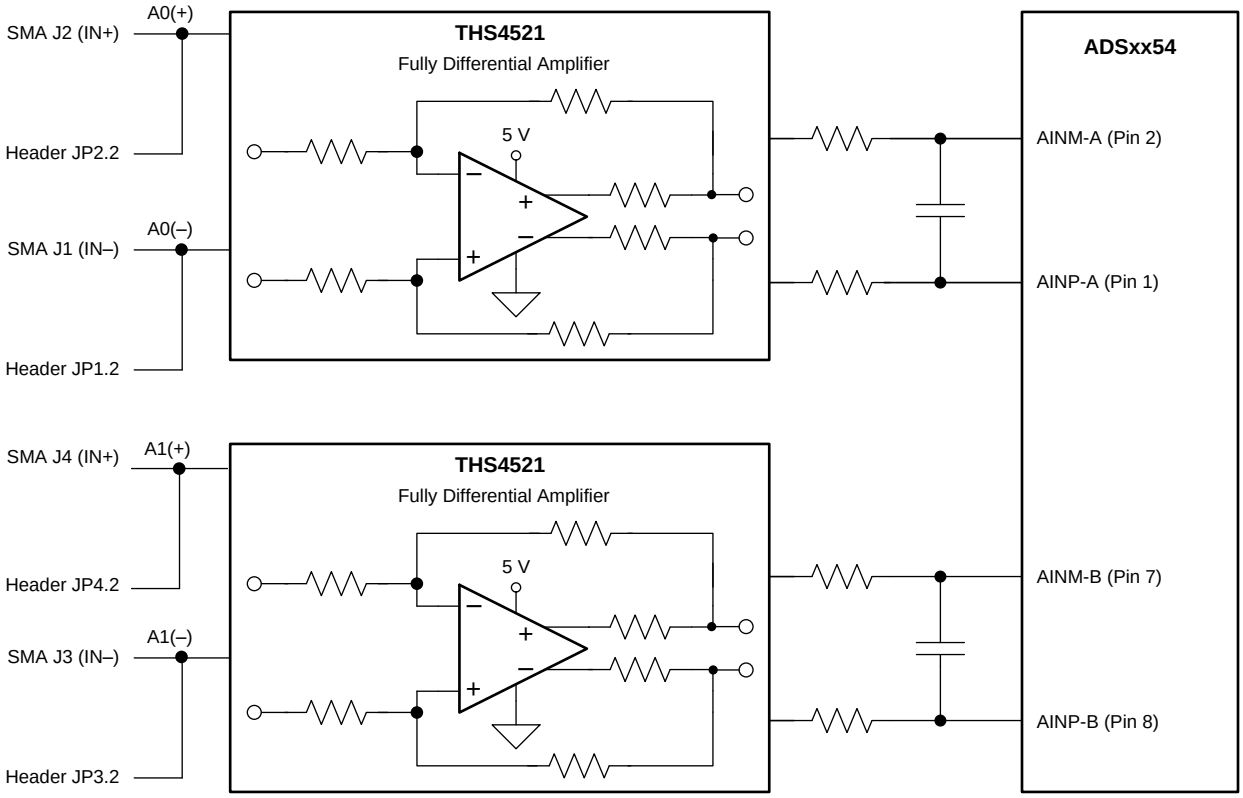


Figure 1. ADSxx54EVM Analog Interface Input Connections

Table 1 summarizes the JP1 through JP4 analog interface connectors.

Table 1. JP1 to JP4: Analog Interface Connections

Terminal Number	Signal	Description
JP1.2	A0(–)	CHA negative differential input. This terminal can be grounded for single-ended signals.
JP2.2	A0(+)	CHA positive differential input or input for single-ended signals.
JP3.2	A1(–)	CHB negative differential input. This terminal can be grounded for single-ended signals.
JP4.2	A1(+)	CHB positive differential input or input for single-ended signals.

Table 2 lists the SMA analog inputs.

Table 2. SMA Analog Interface Connections

Terminal Number	Signal	Description
J1	A0(–)	CHA negative differential input. This SMA connector can be grounded by shunting JP1 terminal1 and JP1 terminal 2 for single-ended signals.
J2	A0(+)	CHA positive differential input or input for single-ended signals.
J3	A1(–)	CHB negative differential input. This SMA connector can be grounded by shunting JP3 terminal 1 and JP3 terminal 2 for single-ended signals.
J4	A1(+)	CHB positive differential input or input for single-ended signals.

2.1 Analog Input Range Settings

The ADSxx54 dual simultaneous ADC supports fully-differential analog input signals on both channels. The full-scale range (FSR) of the ADSxx54 device can be programmed to either a (±1 × V_{ref}) or (±2 × V_{ref}) range by setting bit B9 of the ADSxx54 configuration register. This register is common to both ADCs in the device (ADC_A and ADC_B). Configure the full-scale range setting in the EVM by navigating to the *ADSxx54EVM Settings page* on the graphical user interface (GUI). Refer to *Section 6.3* of this user guide for more information. Set the ADC differential inputs at a common-mode voltage of FSR_ADC_A / 2 and FSR_ADC_B / 2, respectively. Configure jumpers JP5 and JP6 on the ADSxx54EVM to bias the ADC input signal at the correct common-mode voltage level. Table 3 describes the appropriate range jumper settings.

Table 3. Analog Input Range Jumper Settings

Jumper Number	Default Position	Description
JP5	Installed	Installed when FSR = ±1 × V_{ref}; removed when FSR = ±2 × V_{ref}. Sets ADC_A common-mode voltage.
JP6	Installed	Installed when FSR = ±1 × V_{ref}; removed when FSR = ±2 × V_{ref}. Sets ADC_B common-mode voltage.

The ADSxx54EVM incorporates two THS4521 fully-differential amplifiers to drive the ADC inputs. The fully-differential amplifiers shift the signal to the appropriate common-mode voltage level. Figure 2 shows an example where the ADSxx54 device is configured with the ±2 × V_{ref} FSR. A differential input signal with a common-mode voltage of 0 V is applied to the inputs of the THS4521. The THS4521 shifts the signal to the required common-mode voltage of FSR / 2. Because the THS4521 is powered by a 5-V supply , the input signals must be limited to a differential voltage from –4.3 V to 4.3 V to avoid saturating the amplifier output.

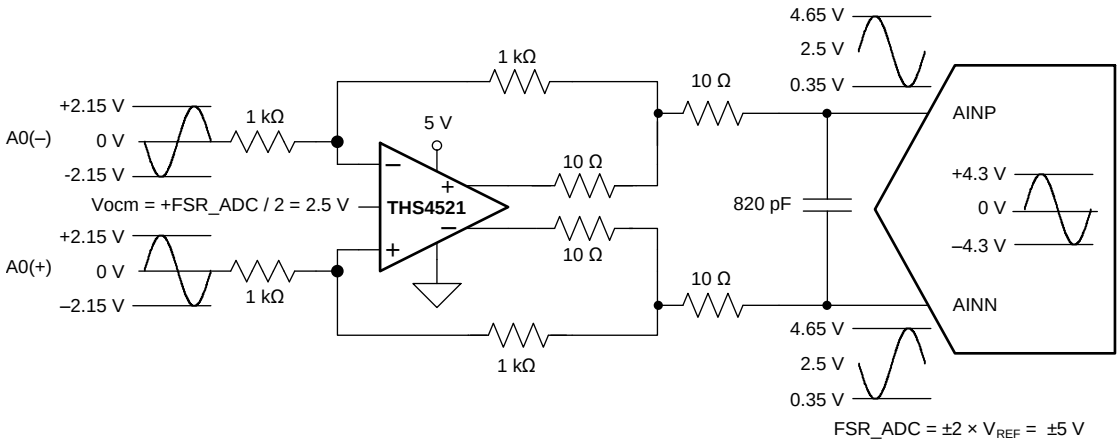


Figure 2. THS4521 Fully-Differential Amplifier Driver

2.2 ADSxx54EVM Onboard Reference and ADSxx54 Device Internal Reference

The ADSxx54 dual, simultaneous ADC operates with reference voltages VREF_A and VREF_B present on pins REFIO_A and REFIO_B, respectively. The ADSxx54 device incorporates two internal individually programmable 2.5-V reference sources. Alternatively, the onboard 2.5-V reference, REF5025 (U5), can also be selected. The reference voltage source is determined by setting bit B6 of the ADC configuration register. Note that this bit is common to ADC_A and ADC_B. Configure the reference settings on the ADSxx54EVM-PDK by navigating to the *ADSxx54EVM Settings* page on the GUI. Refer to Section 5.2 for more information. By default, the evaluation module is set up with the onboard external reference source, with jumpers JP7 and JP8 installed, as shown in Figure 3 . If the ADSxx54 must be configured with the internal reference, make sure to remove jumpers JP7 and JP8 before enabling the internal reference.

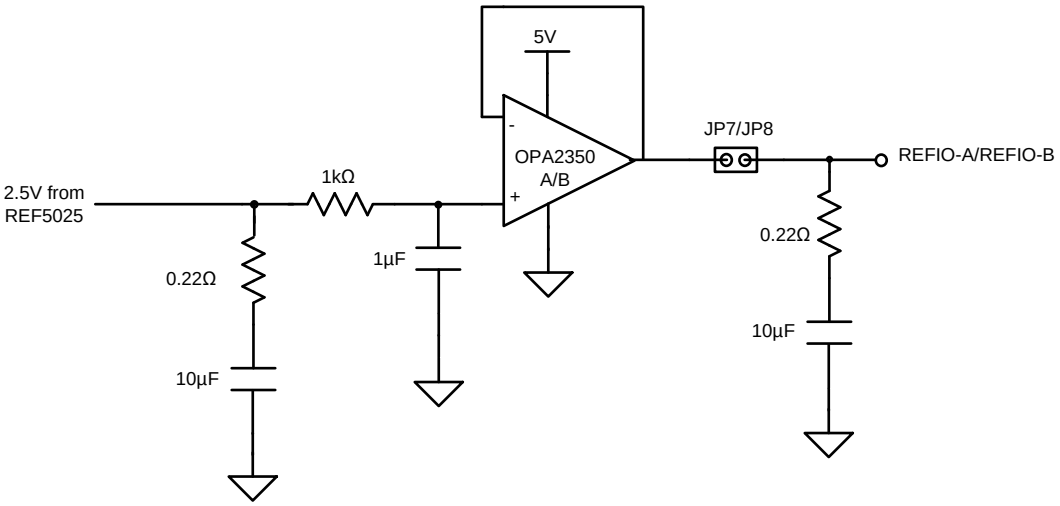


Figure 3. REF5025 2.5-V External Reference Source and OPA2350 Reference Driver

3 Digital Interface

Socket strip connector J6 provides the digital I/O connections between the ADSxx54EVM board and the SDCC board.

Table 4 Summarizes the pinout for connector J6.

Table 4. Connector J6 Pinout

Pin Number	Signal	Description
J6.2, J6.10, J6.15, J6.16, J6.18	GND	Ground connections
J6.4	$\overline{\text{EVM PRESENT}}$	EVM present, active low
J6.11, J6.12	I^2C™ bus	I^2C bus; used only used to program the U7 EEPROM on the EVM board
J6.13	DVDD	3.3-V digital supply from SDCC controller board
J6.34	$\overline{\text{CS}}$	Chip select, active low
J6.36	SCLK	Serial interface clock
J6.38	SDI	Serial data input
J6.40	SDO_A	Serial data output for channel A
J6.42	SDO_B	Serial data output for channel B

3.1 Serial Peripheral Interface (SPI)

The ADSxx54 digital output is available in SPI-compatible format, which makes interfacing with microprocessors, digital signal processors (DSPs), and FPGAs easy. The ADSxx54EVM offers 47-Ω resistors between the SPI signals and connector J6 to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these 47-Ω resistors slow down the signal edges in order to minimize signal overshoot.

3.2 I^2C Bus for Onboard EEPROM

The ADSxx54EVM has an I^2C bus to communicate with the onboard EEPROM that records the board name and assembly date. It is not used in any form by the ADSxx54 converter.

4 Power Supplies

The analog portion of the ADSxx54EVM-PDK requires a 5-V supply. The ADSxx54EVM-PDK is configured at the factory using the onboard regulated analog 5-V supply (+VA); and an onboard 3.3-V digital supply. Alternatively, set the AVDD analog supply voltage by connecting an external power source through two-terminal connector J5.Table 5 lists the configuration details for P3.

Table 5. Power-Supply Jumpers

Pin Number	Position	Function
JP10	Shunt 2-3 (default)	Onboard 5-V AVDD analog supply selected
	Shunt 1-2	External 5-V AVDD connected through two-terminal block J5
JP9	Open	Onboard regulated AVDD supply set to 5.0 V
	Closed	Onboard regulated AVDD supply set to 5.2 V

CAUTION

The external AVDD supply applied to external two-terminal connector J5 must not exceed 5.5 V or device damage may occur. The external AVDD supply must be in the range of 5.0 V to 5.5 V for proper ADSxx54EVM operation.

5 ADSxx54EVM-PDK Initial Setup

This section presents the steps required to set up the ADSxx54EVM-PDK kit before operation.

5.1 Default Jumper Settings

A silkscreen plot detailing the default jumper settings is shown in Figure 4. Table 6 explains the configuration for these jumpers.

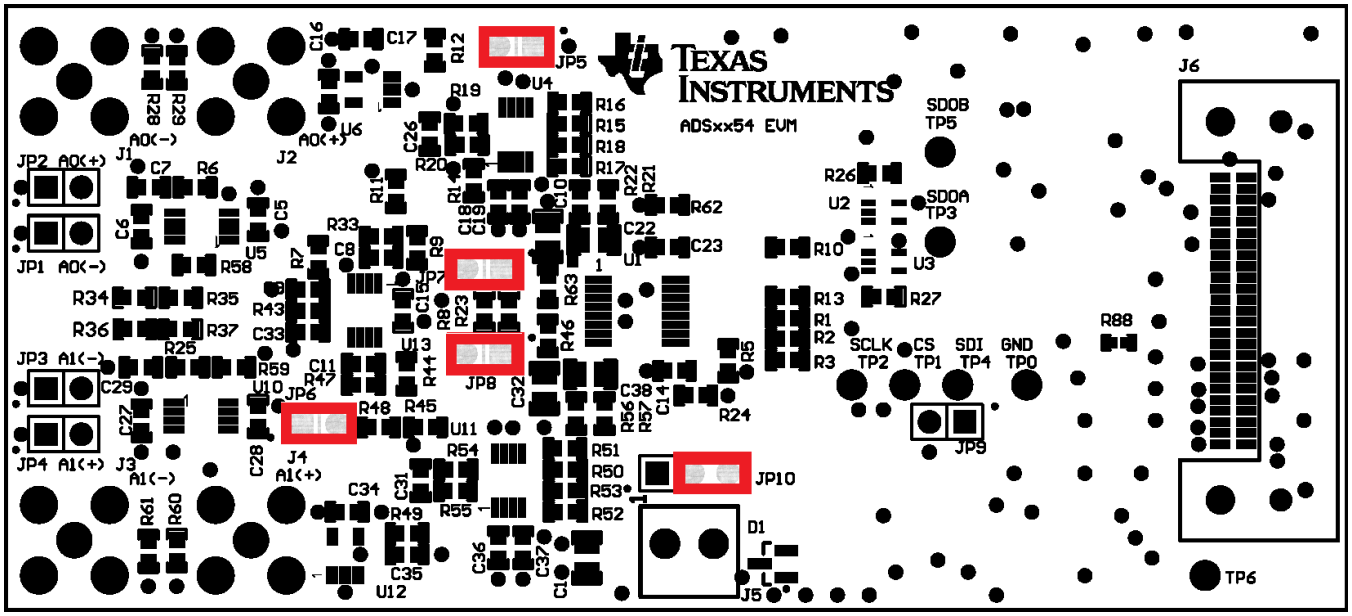


Figure 4. ADSxx54EVM Default Jumper Settings

Table 6. Default Jumper Configuration

Pin Number	Default Position	Switch Description
JP1	Open	JP1.2 header connector to A0(-)
JP2	Open	JP2.2 header connector to A0(+)
JP3	Open	JP3.2 header connector to A1(-)
JP4	Open	JP4.2 header connector to A1(+)
JP5	Closed	Closed when configured in $\pm V_{ref}$ range; open to support $\pm 2 \times V_{ref}$ range
JP6	Closed	Closed when configured in $\pm V_{ref}$ range; Open to support $\pm 2 \times V_{ref}$ range
JP7	Closed	Closed to connect onboard 2.5-V reference to REFIO_A; open when using ADSxx54 internal reference
JP8	Closed	Closed to connect onboard 2.5-V reference to REFIO_B; open when using ADSxx54 internal reference.
JP9	Open	Open: onboard AVDD set to +5 V; closed: onboard AVDD set to +5.2 V
JP10	Short 2-3	Short 2-3 selects onboard regulated AVDD supply; short 1-2 selects external AVDD through J1

5.2 Software Installation

This section presents the steps required to the install the software. Section 6 explains how to operate the software to acquire data.

NOTE: Ensure the microSD memory card included in the kit is installed in the microSD socket (P6) on the back of the SDCC board before connecting the EVM to the PC. Otherwise, as a result of improper boot up, Windows cannot recognize the ADSxx54EVM-PDK as a connected device.

Complete the following steps to install the software:

Step 1. Install the microSD memory card on the SDCC controller board.

Step 2. Verify jumpers are in the factory-default position and connect the hardware.

Step 3. Install the ADSxx54EVM-PDK software.

Step 4. Complete the SDCC device driver installation.

Each task is described in the following subsections.

5.2.1 Install the microSD Memory Card on the SDCC Controller Board

The ADSxx54EVM-PDK includes a microSD memory card that contains the EVM software and SDCC controller board firmware required for the EVM operation.

NOTE: Ensure the microSD memory card that contains the software is installed in the microSD socket (P6) on the back of the SDCC board.

Figure 5 shows the bottom view of the SDCC controller board with the microSD card installed.

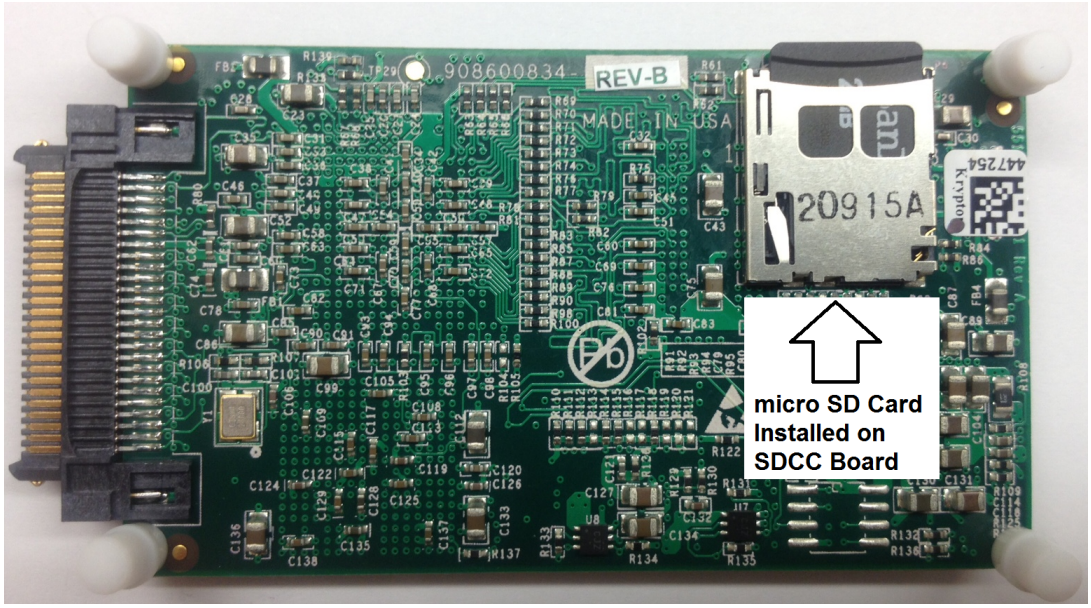


Figure 5. Bottom View of SDCC Board with microSD Memory Card Installed

The microSD memory card is formatted at the factory with the necessary firmware files for the SDCC controller board to boot properly. In addition to the SDCC firmware files (app and MLO files), the microSD memory card contains the ADSxx54EVM-PDK software installation files inside the *ADS835x EVM V#.#.#* folder. <*V#.#.#*> refers to the installation software version number, and increments with software installer releases.

5.2.2 Verify Jumpers are in the Factory-Default Position and Connect the Hardware

The ADSxx54EVM-PDK includes both the ADSxx54EVM and the SDCC controller board; however, the devices are shipped unconnected. Follow these steps to verify that ADSxx54EVM-PDK kit is configured and connected properly.

Step 1. Verify the microSD card is installed on the back of the SDCC board, as shown in Figure 5.

Step 2. Verify the ADSxx54EVM jumpers are configured as shown inFigure 4.

Step 3. Connect the ADSxx54EVM board to the SDCC controller board as Figure 6 illustrates.

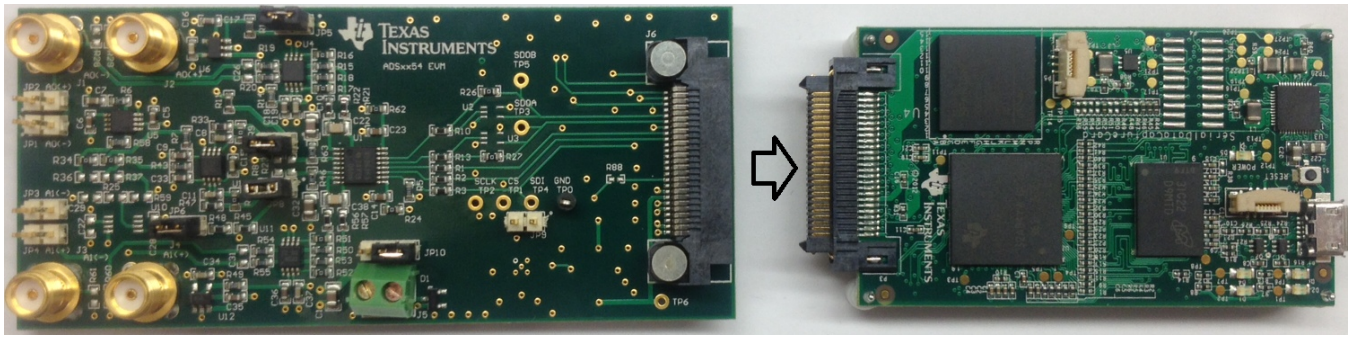


Figure 6. Connecting ADSxx54EVM Board to SDCC Controller Board

Step 4. Connect the SDCC controller board to the PC through the micro USB cable.

Step 5. Verify that the LED D5 *Power Good* indicator is illuminated. Wait approximately ten seconds and verify that diode D2 blinks, indicating that USB communication with the host PC is functioning properly. Figure 7 shows the location of the LED indicators in the SDCC controller board.

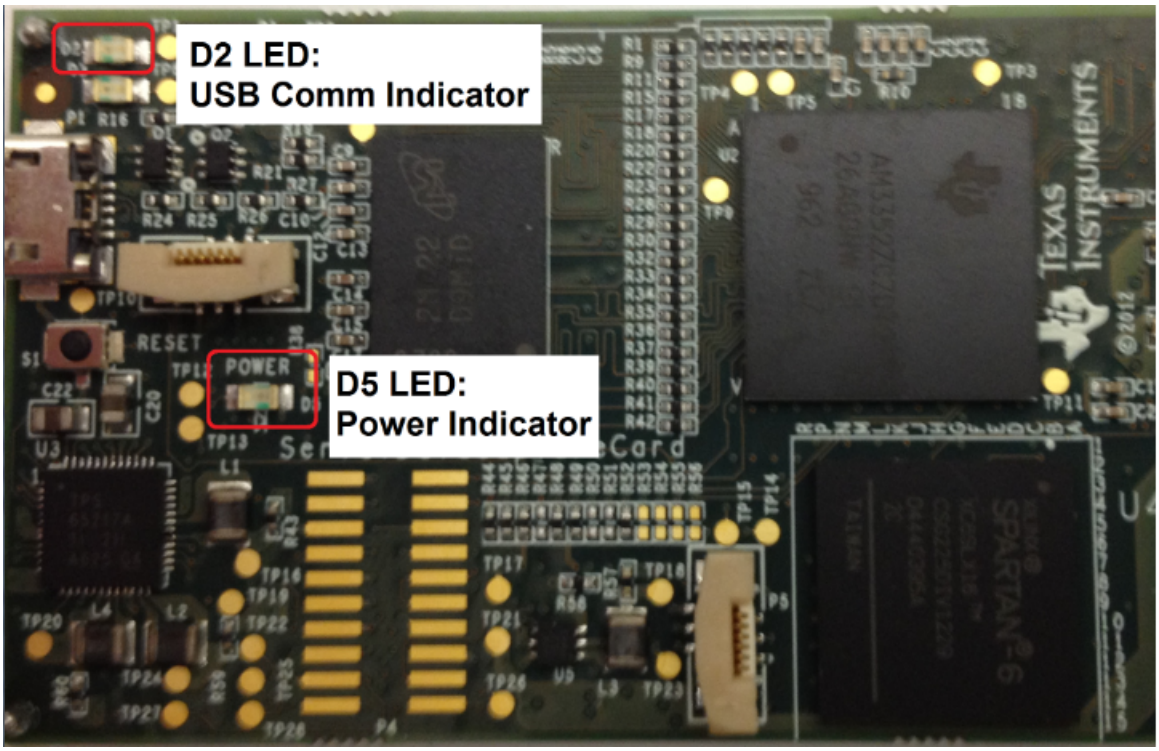


Figure 7. LED Indicators on the SDCC Board

5.2.3 Install the ADSxx54EVM-PDK Software

The *ADS835x EVM V#.#.#* software must be installed on the PC. This software supports the ADSxx54EVM-PDK. The user must have administrator privileges to install the EVM software. The following steps list the directions to install the software.

1. Open Windows explorer and find the microSD memory card in the browser as a storage device.
2. Navigate to the *...\ADS835x EVM Vx.x.x\Volume* folder.
3. Run the installer by double-clicking the file *setup.exe*. This action installs the EVM GUI software and the required and SDCC device driver components.
4. After the installer begins, a welcome screen displays. Click *Next* to continue.
5. A prompt appears with the destination directory; select the default directory under: *...\Program Files(x86)\Texas Instruments\ads835xevm*.

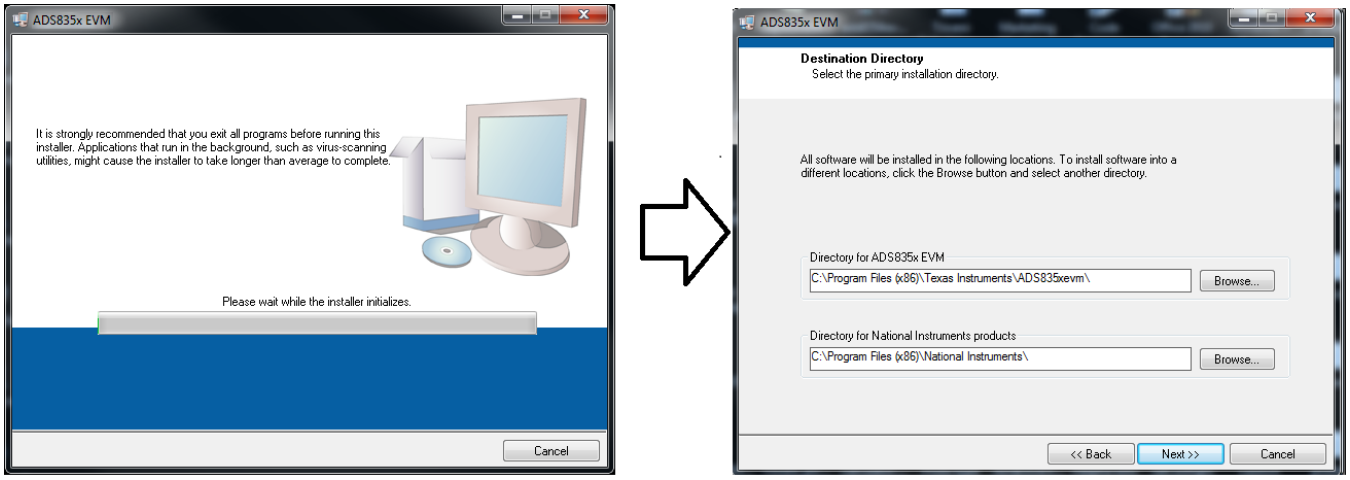


Figure 8. Welcome Screen and Destination Directory Screens

6. One or more software license agreements appear. Select *I Accept the License Agreement* and click *Next*.
7. The *Start Installation* screen appears. Click *Next*.

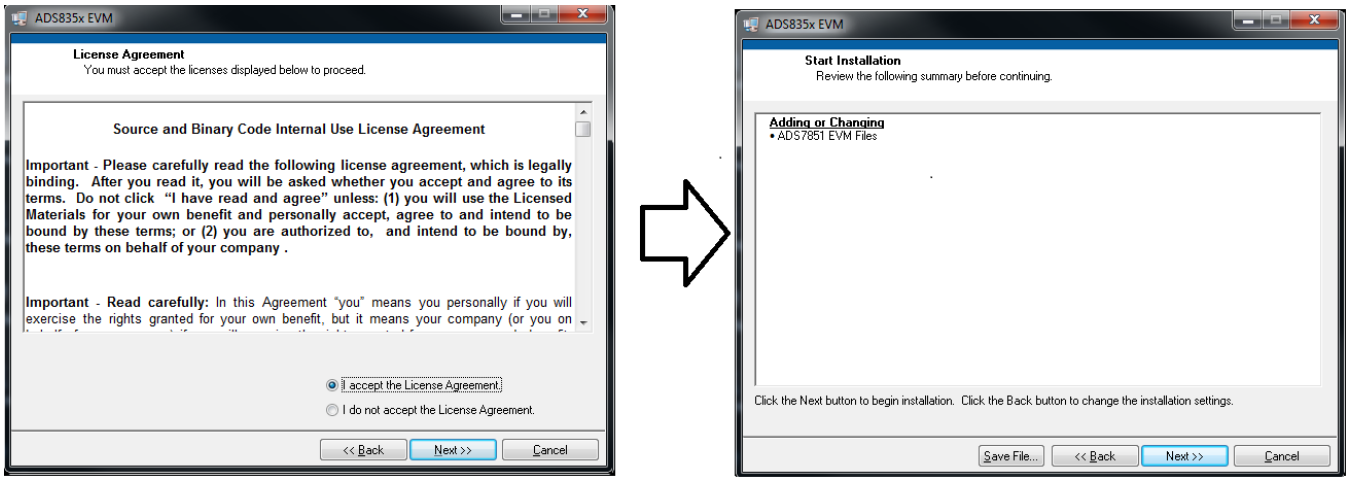


Figure 9. License Agreement and Start Installation Screens

8. A progress bar appears; this step takes a few minutes.
9. The progress bar is followed by an installation complete notice.

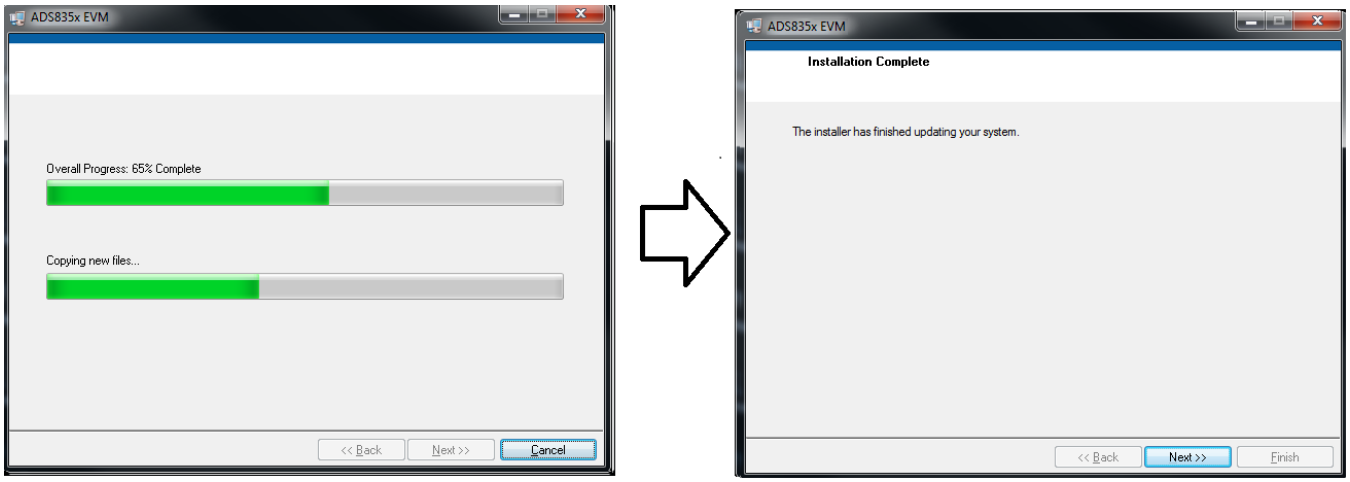


Figure 10. Progress Bar and Installation Complete Screens

5.2.4 Complete the SDCC Device Driver Installation

During installation of the SDCC device driver, a prompt may appear with the Windows security message shown in Figure 11. Select *Install this driver software anyway* to install the driver required for proper operation of the software. The drivers contained within the installers are safe for installation to your system.

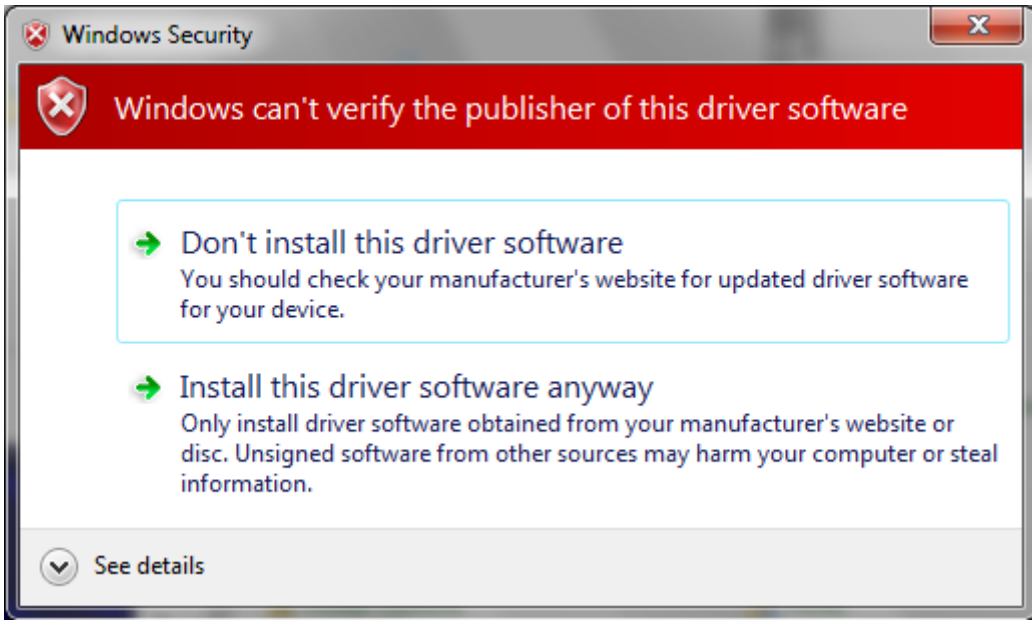


Figure 11. Windows 7 Driver Installation Warning

NOTE: Driver installation prompts do not appear if the SDCC device driver has been installed on your system previously.

The following steps describe how to install the SDCC device driver.

Step 1. Immediately after the ADS835x EVM software installation is complete, prompts appear to install the SDCC device driver, as shown in Figure 12 and Figure 13

Step 2. A computer restart may be required to finish the software installation. If prompted, restart the PC to complete the installation.

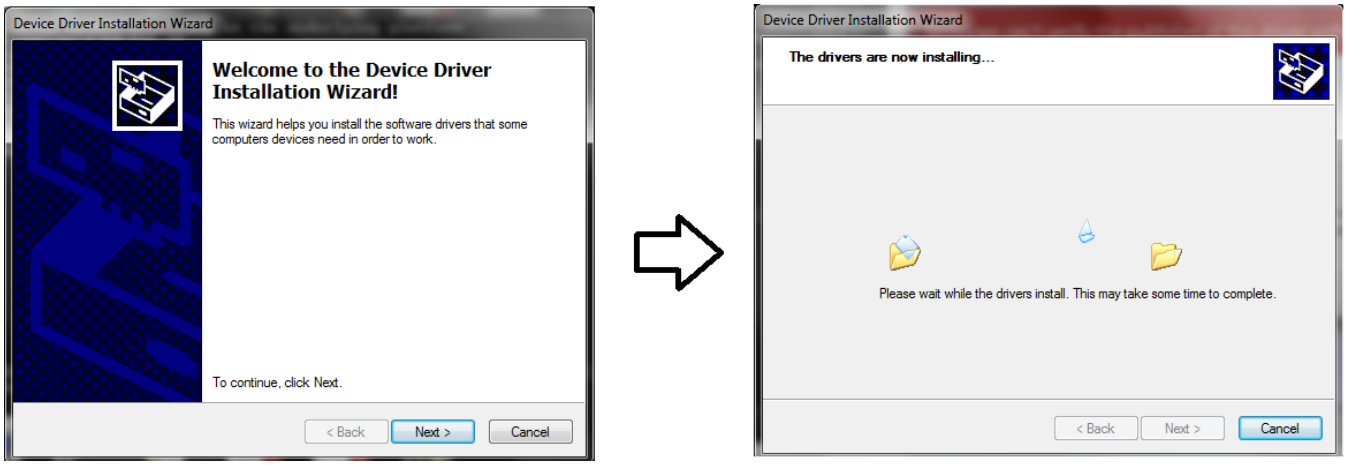


Figure 12. SDCC Device Driver Installation

Figure 13. SDCC Device Driver Completion

6 ADSxx54EVM-PDK Kit Operation

This section describes how to use ADSxx54EVM-PDK and the ADSxx54EVM software to configure the EVM and acquire data.

6.1 About the SDCC Controller Board

The SDCC controller board provides the USB interface between the PC and the ADSxx54EVM. The controller board is designed around the AM335x processor, a USB 2.0 high-speed capability, 32-bit ARM core. The SDCC controller board incorporates an onboard FPGA subsystem and 256MB of onboard DDR SRAM memory.

The SDCC controller board is not sold as a development board, and it is not available separately. TI cannot offer support for the SDCC controller` board except as part of this EVM kit.

6.2 Loading the ADSxx54EVM-PDK Software

The ADS835x EVM software (this software also supports the ADSxx54EVM-PDK) provides control over the settings of the ADSxx54. Adjust the ADSxx54EVM settings when the EVM is not acquiring data. During acquisition, all controls are disabled and settings cannot be changed.

Settings on the ADSxx54EVM correspond to settings described in the ADSxx54 product data sheet (available for download at http://www.ti.com); see the product data sheet for details.

To load the *ADS835x EVM* software, follow these steps:

Step 1. Make sure the EVM kit is configured and powered up as explained in Section 5.

Step 2. Start the ADS835x EVM software. Go to *Start → All Programs →Texas Instruments → ADS835x EVM* and click *ADS835x EVM* to run the software.

Step 3. Verify that the software detects the ADSxx54EVM. The GUI identifies the EVM hardware that is connected to the controller board and displays either *Loading the ADS8354evm Settings* or *Loading the ADS7854evm Settings*. After the settings are loaded, *ADS8354EVM GUI* or *ADS7854 EVM GUI* displays at the top of the GUI screen, as shown in Figure 14.

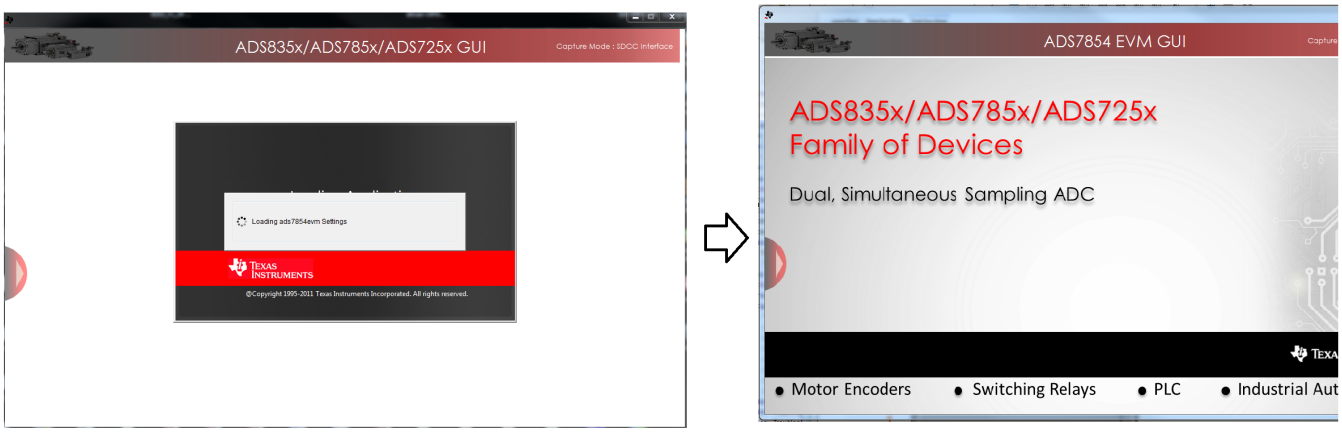


Figure 14. GUI Display Prompt

6.3 ADSxx54EVM Settings

Configure the ADSxx54EVM with different settings for evaluation. In order to configure the device settings, follow these steps:

1. Load the ADSxx54 EVM settings page in the GUI. Hover the cursor over the red arrow at the left-center side of the GUI screen; a menu with different GUI pages appears. Click on *ADSxx54 EVM Settings*, as shown in Figure 15.

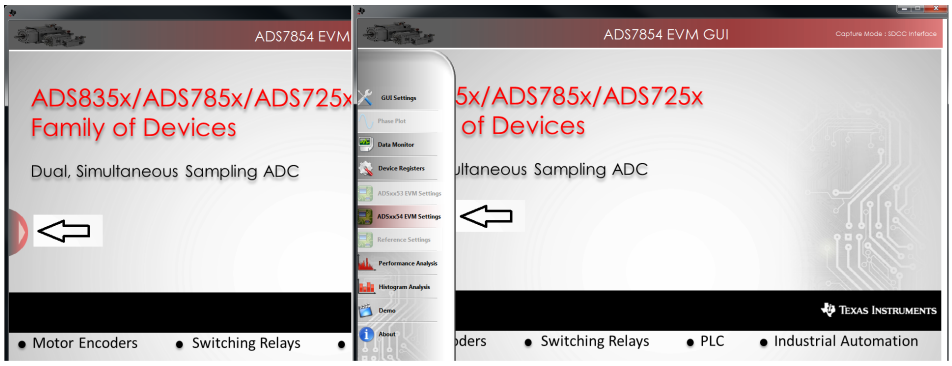


Figure 15. Open the ADSxx54EVM Settings Page

2. In the *ADSxx54EVM Settings* page, find the *Internal Reference [CFR, Bit[6]]* button to select the internal or external onboard reference sources. Jumpers JP7 and JP8 must be installed when selecting the external REF5025 (U5) onboard reference. Make sure to uninstall jumpers JP7 and JP8 when selecting the ADSxx54 device internal reference. The GUI displays the appropriate reference jumper settings, as shown in Figure 16.

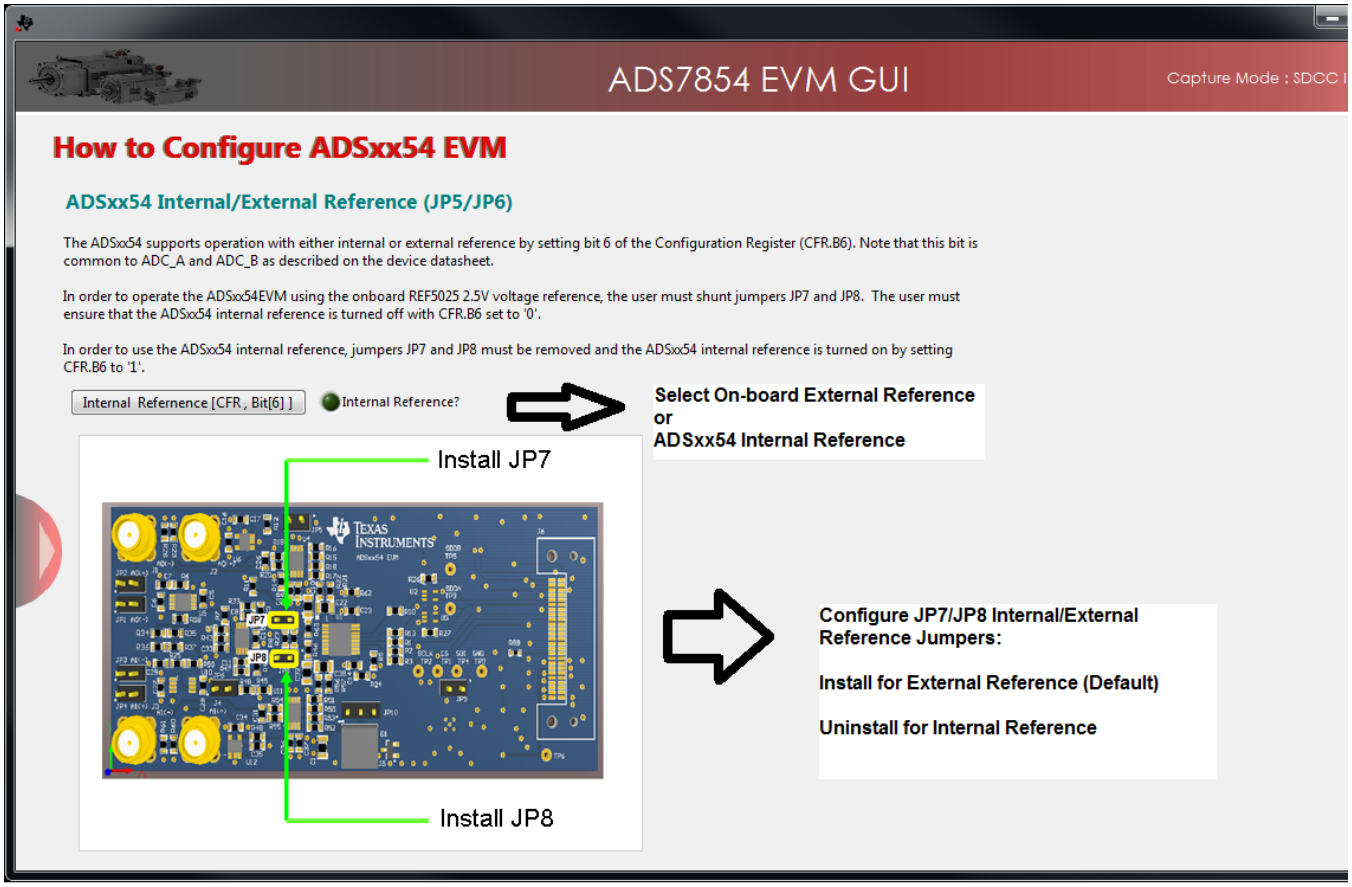


Figure 16. Selecting the External Onboard Reference or the ADSxx54 Internal Dual Reference

3. The ADSxx54 device incorporates two internal programmable 2.5-V reference sources. When selecting the dual, internal programmable reference, independently change the voltages at VREF_A and VREF_B by writing to user-programmable registers REFDAC_A and REFDAC_B. The *Vref Value-ADC A* and *Vref Value-ADC B* control panels contain the REFDAC_x register settings. The reference voltage can be programmed in the range of 2.5 V to 2.0 V by entering the REFDAC_x register value in the control panel and clicking the *Write REFDAC_x* button. Figure 17 shows the internal reference *Vref Value-ADC x* control panels in the *ADSxx54EVM Settings* page of the GUI.

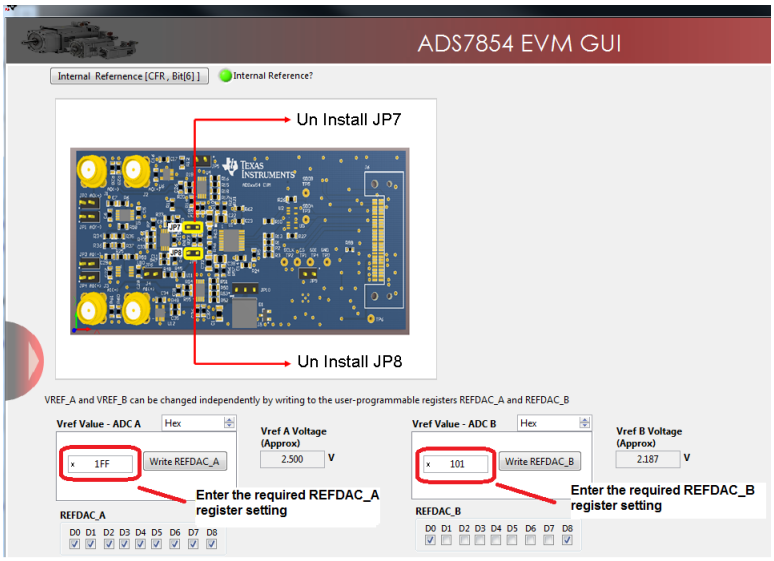


Figure 17. Programming the REFDAC Registers in the ADSxx54EVM

4. Scroll down in the *ADSxx54EVM Settings* page and find the *Input Range Selection [CFR, Bit[9]]* button to select the ±1 × V_{ref} range mode or ±2 × V_{ref} range mode. Jumpers JP5 and JP6 must be installed when selecting the ±1 × V_{ref} range. Uninstall jumpers JP5 and JP6 when selecting the ±2 × V_{ref} range mode . The GUI displays the appropriate JP5 and JP6 jumper settings, as shown in Figure 18

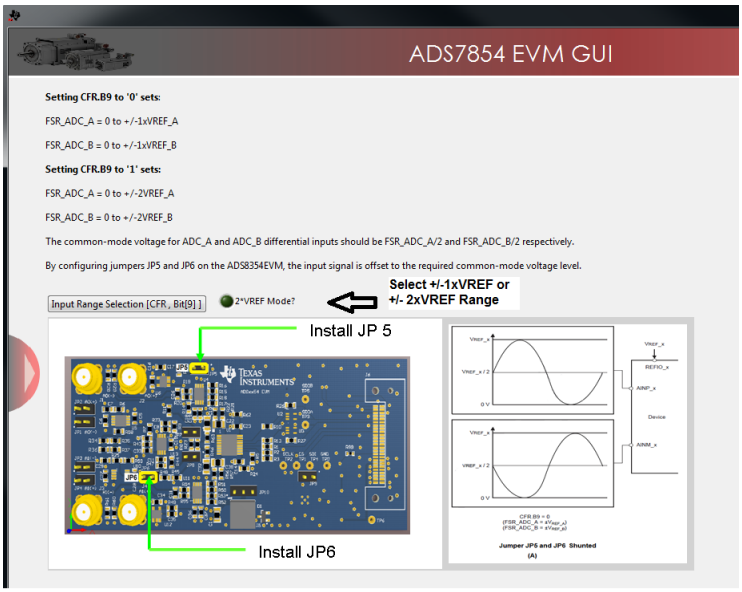


Figure 18. Selecting ±1 × V_{ref} Range or ±2 × V_{ref} Range

6.4 Device Registers

In addition to the *ADSxx54EVM Settings* page, the GUI also allows access to the SCLK frequency and the ADSxx54 register settings on the *Device Registers* page of the GUI. Use the EVM software to change the following register settings of the configuration register (CFR):

- INPUT_RANGE (CFR.B9)
- REF_SEL (CFR.B6)
- STANDBY (CFR.B5)

Use the EVM software to also program the REFDAC register settings. Refer to *Section 6.3* of this user guide, or the ADSxx54 device datasheet for more information. Figure 19 shows the *Device Registers* page of the GUI.

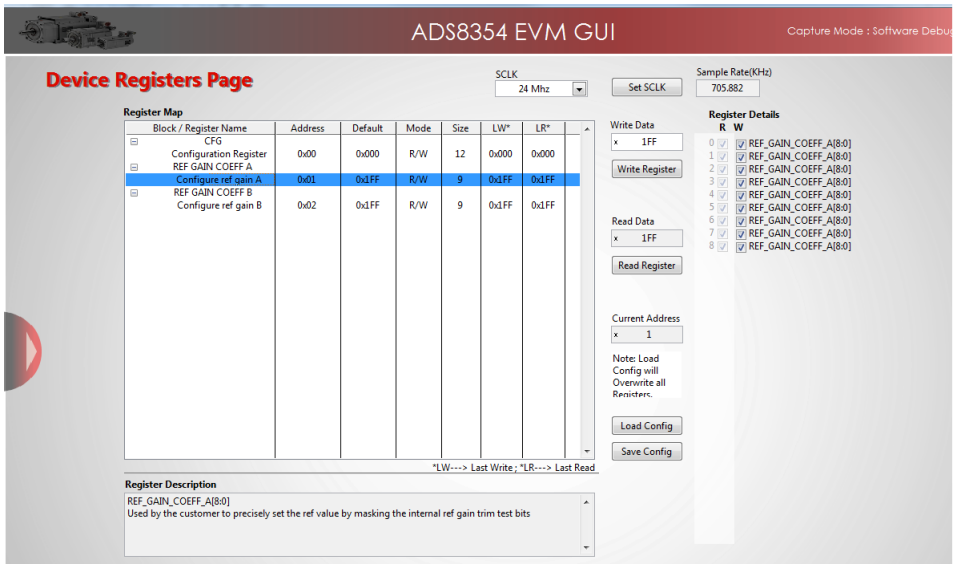


Figure 19. Device Registers Page

6.5 Capturing Data with the ADSxx54EVM-PDK

Access the *Data Monitor* page in the GUI to monitor data acquired by the ADSxx54. This GUI page displays the acquired data versus time. To access the *Data Monitor* page, hover the cursor over the red arrow at the left center side of the GUI screen; a menu with different GUI pages appear. Click on the *Data Monitor* option in the menu as shown in Figure 20

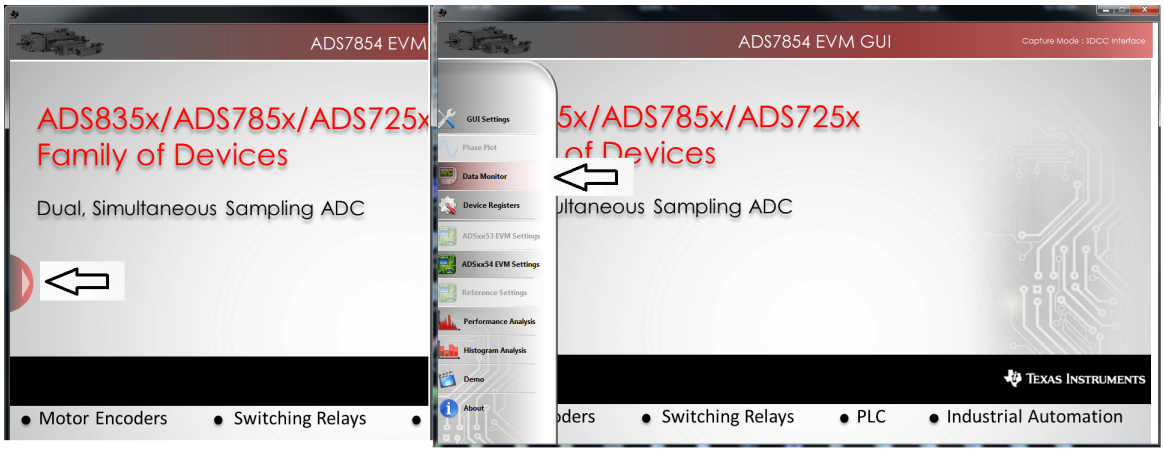


Figure 20. Open the *Data Monitor* page on the GUI

Figure 21 shows the *Data Monitor* page of the EVM GUI. Configure the device sampling rate and capture settings by using the *Capture Settings* portion of the *Data Monitor* page. The change in configuration settings are executed immediately after pressing the *Configure Device* button. The following list describes the different options available on the *Data Monitor* page.

# of Samples— This option is used to select the number of samples captured in a block.

The number of samples captured in a block are contiguous. The drop-down menu is used to select a data block in the range of 1024 samples to 1,048,576 samples per channel. This control provides a drop-down list for values restricted to 2^n, where *n* is an integer.

SCLK— This control sets the clock frequency used by the SPI interface to capture data.

By configuring the SCLK frequency, the data rate of the ADSxx54 is configured. The ADS8354EVM-PDK software supports SCLK frequencies of 24 MHz, 20 MHz, and 16.2 MHz. These SCLK frequencies correspond to data rates of 705.8 kSPS, 588 kSPS, and 476.5 kSPS, respectively. The ADS7854EVM-PDK software supports SCLK frequencies of 34 MHz, 24 MHz, 20 MHz, and 16.2 MHz. These SCLK frequencies correspond to data rates of 1 MSPS, 705.8 kSPS, 588 kSPS, and 476.5kSPS, respectively.

Internal Reference?— Use this button to select the ADSxx54 device internal reference, or the onboard REF5025 2.5 external reference.

Program the internal reference settings by navigating into the *ADSxx54 EVM Settings* GUI page, as described in Section 6.3 of this document.

2*VREF Mode— This option is used to configure the ADSxx54 in the ±1 × V_{ref} or ±2 × V_{ref} range mode.

Make sure to configure jumpers JP5 and JP6 appropriately, depending on the mode of operation.

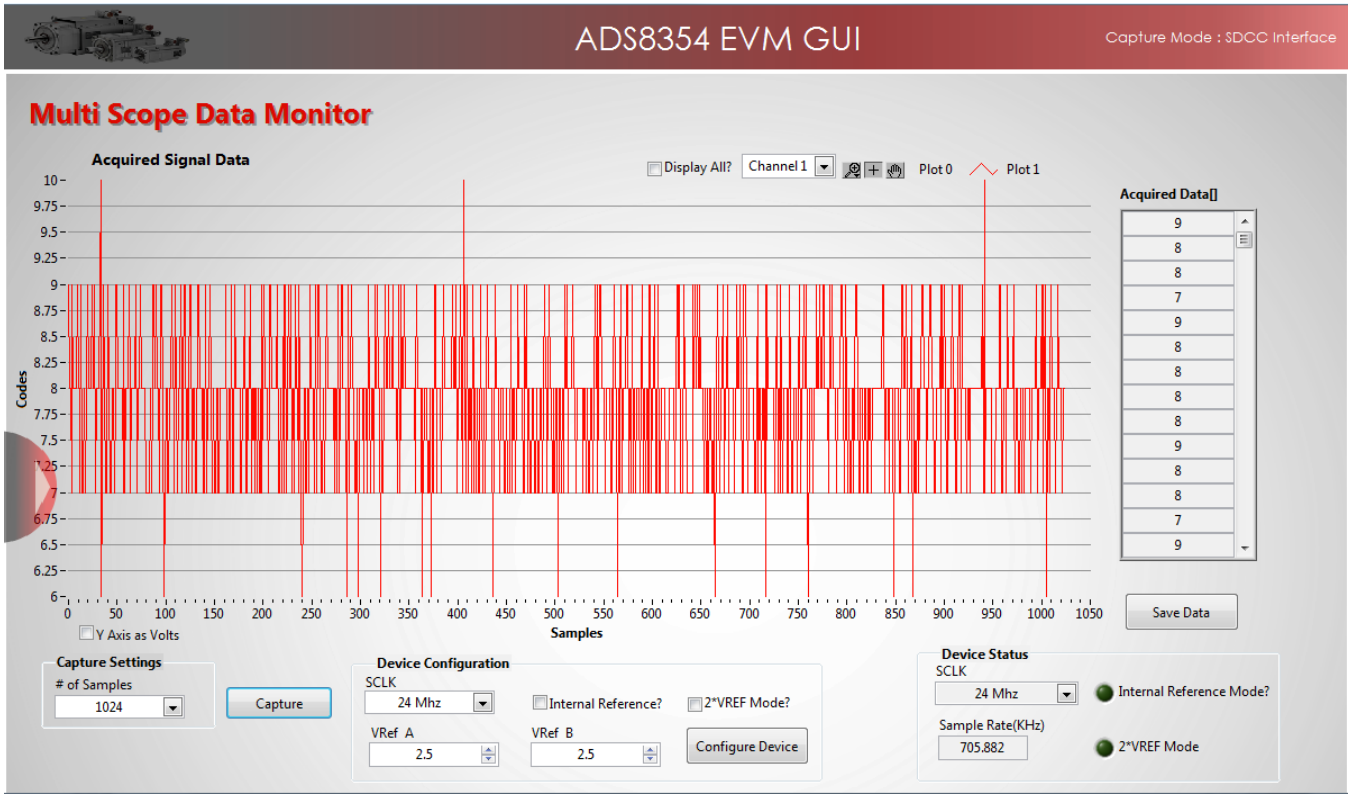


Figure 21. Data Monitor Page

6.5.1 Data Collection to Text Files

The *Data Monitor* page of the GUI allows data to be saved in a tab-delimited text file format that can be imported into Excel®, or other spreadsheet software tools. The text file contains the raw ADC data of both channel A and channel B in decimal data format. Information such as the device name, date and time, the sampling frequency, and number of samples of the data record are also stored. In order to save any data captured by the EVM, click on the *Save Data* button and specify the file path and file name of the data file, as shown in Figure 22.

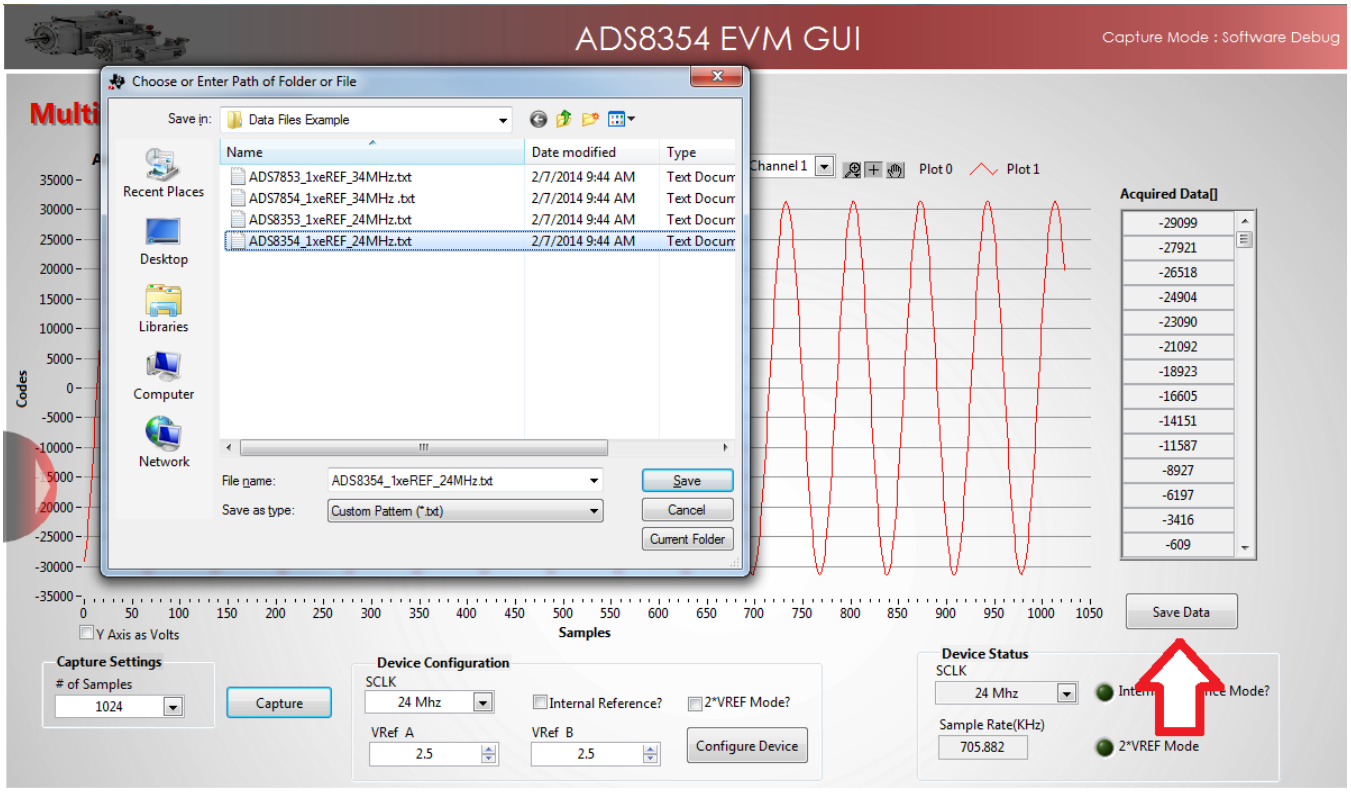


Figure 22. Saving Data to a Text File

6.6 FFT Analysis

The *Performance Analysis* page in the GUI performs the fast fourier transform (FFT) of the captured data, and displays the resulting frequency domain plots of channel A and channel B of the ADSxx54. This page also calculates key ADC dynamic performance parameters, such as signal-to-noise ratio (SNR), total harmonic distortion (THD), signal-to-noise and distortion ratio (SINAD), and spurious-free dynamic range (SFDR). Figure 23 shows the FFT performance analysis display. The FFT calculated parameters are shown on the right side of the display.

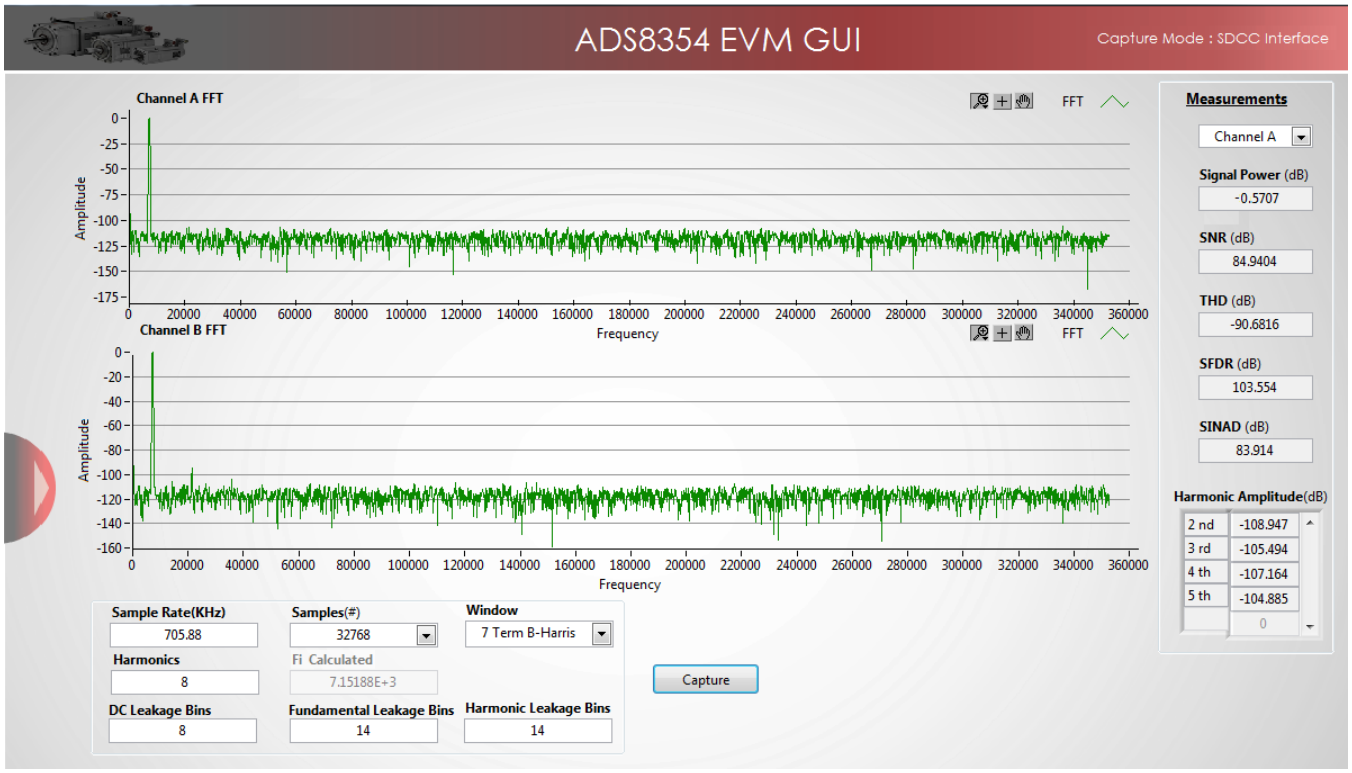


Figure 23. FFT Performance Analysis Page

6.6.1 FFT Analysis Settings and Controls

Sample Rate (kHz)— This field indicates the sampling frequency of the ADC data (kHz).

Samples (#)— The FFT requires a time domain record with a number of samples that is a power of 2. The Samples (#) drop-down menu provides a list of values that satisfy this requirement.

Fi Calculated— This field displays the frequency of the largest amplitude input signal computed from the FFT data, typically the fundamental frequency.

Window— The window function is a mathematical function that reduces the signal to zero at the end points of the data block.

In applications where coherent sampling cannot be achieved, a window-weighting function can be applied to the data to minimize spectral leakage. The following opions are available:

- None (no window weighting function applied; use for coherent data)
- Hanning
- Hamming
- Blackman-Harris
- Exact Blackman
- Blackman
- Flat Top
- 4-Term Blackman-Harris
- 7-Term Blackman-Harris
- Low Sidelobe

For a more thorough discussion of windowing, refer to IEEE1241-2000.

Harmonics— This field sets the number of harmonics that are included in the FFT performance calculations.

Leakage Bins— These fields provide for the removal of the unwanted frequency bins that may be the result of noncoherent data sampling.

Set the *Fundamental Leakage Bins* and *Harmonic Leakage Bins* fields to the number of adjacent bins on either side of the fundamental or harmonic frequencies to include the main frequency power. The *DC Leakage Bins* field allows the number of frequency bins that are a result of the dc portion of the measurement to be excluded from the calculations.

6.7 Histogram Analysis

Histogram testing is commonly used when characterizing ADCs. A histogram is merely a count of the number of times a code has occurred in a particular data set. The *Histogram Analysis* page of the GUI creates a histogram of the data of the acquired data set and displays it. Figure 24 shows the *Histogram Analysis* page of the GUI.

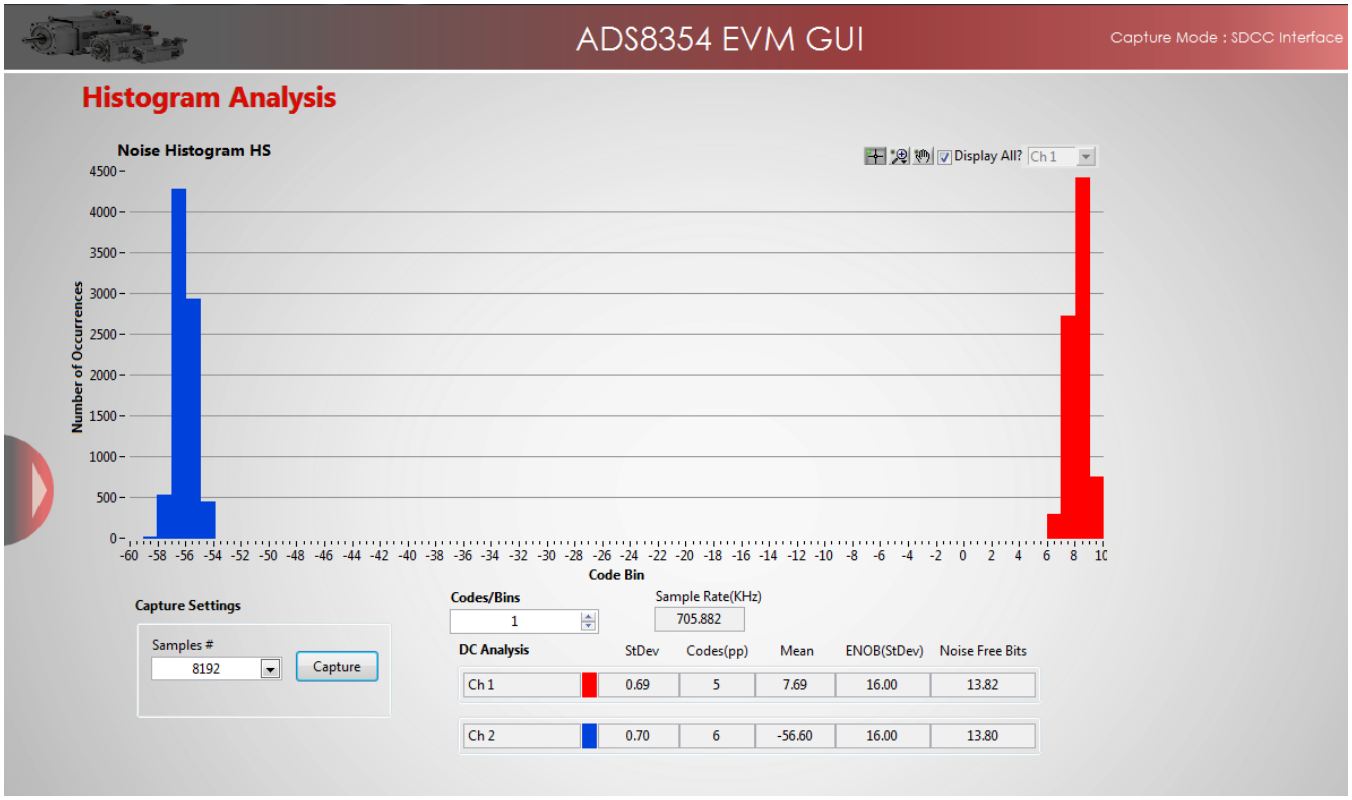


Figure 24. Histogram Analysis Page

The *DC Analysis* table shown in Figure 24 displays several parameters of the captured data set:

- The *StDev* column displays the standard deviation of the data set. This value is equivalent to the RMS noise of the signal when analyzing a dc data set.
- The *Codes(pp)* column shows the peak-to-peak spread of the codes in the data set; for a dc data set, this range would be the peak-to-peak noise.
- The *Mean* column displays the average value of the data set.
- The *ENOB(StDev)* column displays the effective number of bits of the converter, as calculated from the standard deviation or RMS noise.
- The *Noise Free Bits* column displays the effective bits of the converter when calculated using the peak-to-peak noise.

6.8 Troubleshooting

If the ADSxx54EVM software stops responding while the ADSxx54EVM-PDK is connected, unplug the USB cable from the EVM, unload the ADSxx54EVM-PDK software, reconnect the ADSxx54EVM-PDK to the PC, and reload the ADSxx54EVM software.

When initially setting up the EVM, the software detects the EVM hardware, and loads the appropriate hardware settings. If the EVM hardware is not detected, the GUI defaults to the *Capture Mode: Software Debug* mode of operation using a preloaded captured data file for demonstration purposes.

While using the EVM-PDK hardware for data acquisition, keep the GUI in the *Capture Mode: SDCC interface* mode of operation. The GUI indicates the selected mode of operation on the top-right corner of the GUI display. In order to select the SDCC interface mode of operation, navigate to the *GUI Settings* page and select the *SDCC Interface* option on the *Capture Mode* drop-down menu, as shown in Figure 25 and Figure 26.

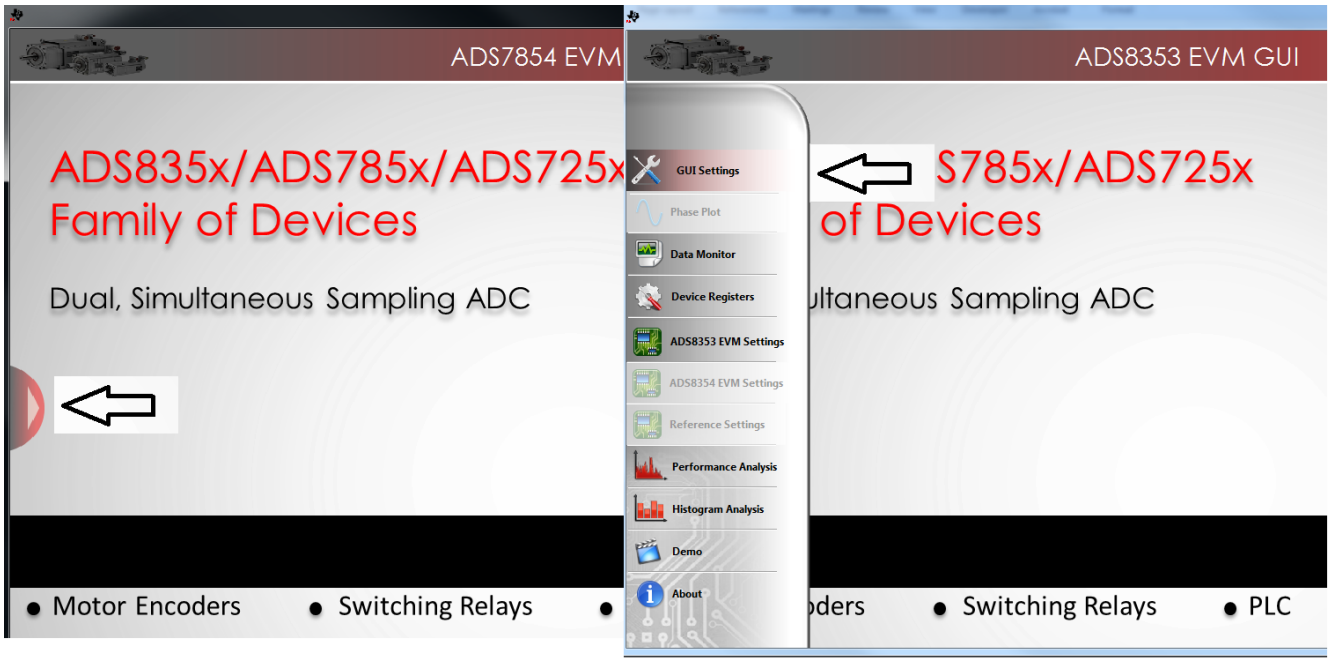


Figure 25. Open the *GUI Settings* page

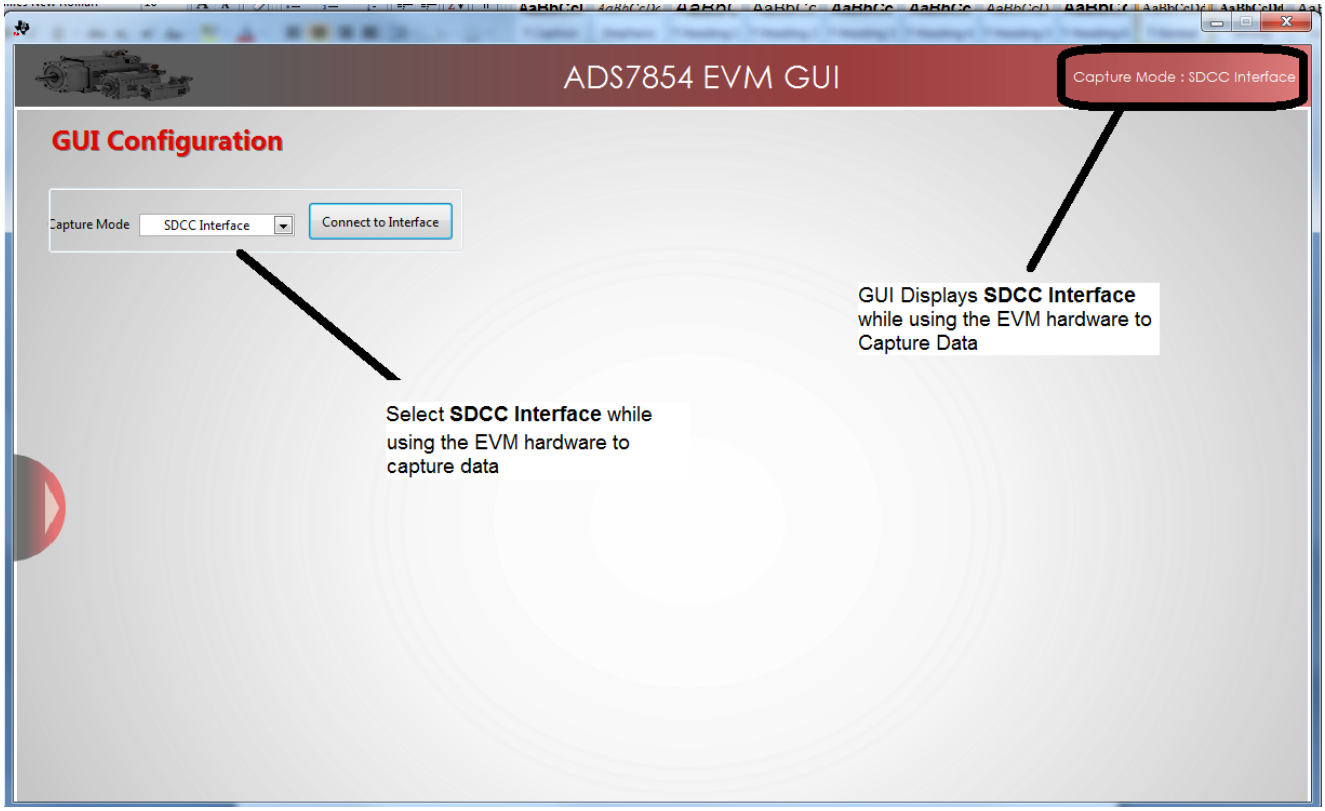


Figure 26. Set Capture Mode to *SDCC Interface* While Using the EVM Hardware

7 Bill of Materials, PCB Layout, and Schematics

Section 7.1 lists the bill of materials. Section 7.2 shows the printed circuit board (PCB) layout for the ADSxx54EVM. The schematics for the ADSxx54EVM are appended to the end of this user's guide.

7.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant.

Table 7. ADSxx54EVM Bill of Materials

Item No.	Qty	Ref Des	Description	Vendor	Part Number
1	11	C1, C10, C32, C39, C41, C42, C43, C44, C45, C46, C54	Capacitor, Ceramic, 10uF, 16V, +/-10%, X5R, 0805	Murata	GRM21BR61C106KE15L
2	9	C5, C6, C9, C17, C18, C33, C35, C36, C40	Capacitor, Ceramic, 1uF, 6.3V, +/-10%, X7R, 0603	Murata	GRM188R70J105KA01D
3	4	C7, C14, C23, C51	Capacitor, Ceramic, 10uF, 6.3V, +/-20%, X5R, 0603	TDK	C1608X5R0J106M
4	10	C8, C11, C15, C16, C19, C34, C37, C48, C52, C53	Capacitor, Ceramic, 0.1uF, 16V, +/-5%, X7R, 0603	AVX	0603YC104JAT2A
5	2	C22, C38	Capacitor, Ceramic, 4700pF, 25V, +/-5%, C0G/NP0, 0805	AVX	08053A472JAT2A
6	2	C47, C50	Capacitor, Ceramic, 2.2uF, 16V, +/-10%, X5R, 0603	Murata	GRM188R61C225KE15D
7	1	C49	Capacitor, Ceramic, 0.22uF, 16V, +/-10%, X5R, 0603	TDK	GRM188R61C224KA88D
8	0	C26, C27, C28, C29, C31	Not Install: Capacitor, C0603	N/A	Not Install
9	1	D1	DIODE ZENER 5.9V 250MW SOT23	NXP Semiconductors	PLVA659A.215
10	4	J1, J2, J3, J4	Connector, TH, SMA	TE Connectivity	142-0701-201
11	1	J5	2 Terminal Block 3.5MM 2POS PCB)	On Shore Technology Inc	ED555/2DS
12	1	J6	SAMTEC, dual-row, right-angle, female, latching	Samtec	ERF8-025-01-L-D-RA-L-TR
13	0	J7	Not Install: Connector for microSD card	Molex	Not Install (MOLEX 502570-0893)
14	9	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	Samtec	TSW-102-07-G-S
15	1	JP10	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator)	Samtec	TSW-103-07-G-S
16	8	R1, R2, R3, R10, R13, R31, R33, R47	Resistor, 47.0 ohm, 1%, 0.1W, 0603	Yageo	RC0603FR-0747RL
17	2	R5, R86	Resistor, 100k ohm, 5%, 0.1W, 0603	Vishay Dale	CRCW0603100KJNEA
18	3	R6, R46, R63	RES, 0.22 ohm, 1%, 0.1W, 0603	Panasonic Electronic	ERJ-3RQFR22V
19	10	'R7, R15, R18, R19, R20, R43, R50, R53, R54, R55	RES 1K OHM 1/10W .1% 0603 SMD	Panasonic Electronic	ERA-3AEB102V
20	14	R9, R16, R17, R24, R26, R27, R34, R35, R44, R51, R52, R62, R89, R90	RES, 0 ohm, 5%, 0.1W, 0603	Vishay Dale	CRCW060320K0FKEA
21	4	R11, R12, R45, R48	RES, 20.0k ohm, 1%, 0.1W, 0603	Vishay Dale	CRCW060320K0FKEA
22	3	R14, R49, R58	RES, 100 ohm, 1%, 0.1W, 0603	Yageo	RC0603FR-07100RL
23	4	R21, R22, R56, R57	RES, 10.0 ohm, 1%, 0.1W, 06033	Vishay Dale	CRCW060310R0FKEA
24	7	'R70, R71, R72, R73, R74, R75, R76	RES, 10k ohm, 5%, 0.063W, 0402	Vishay Dale	CRCW040210K0JNED

Table 7. ADSxx54EVM Bill of Materials (continued)

Item No.	Qty	Ref Des	Description	Vendor	Part Number
25	2	R80, R84	RES, 0 ohm, 5%, 0.125W, 08053	Vishay Dale	CRCW08050000Z0EA
26	0	R83	Not Install: Resistor 0805	N/A	N/A
27	0	R8, R23, R25, R28, R29, R30, R36, R37, R59, R60, R617	Not Install: Resistor 0603	N/A	N/A
28	0	R87, R88	Not Install: Resistor 0402	N/A	N/A
29	1	U1	IC, Dual, 700ksps 16-Bit or 1-MSPS 14-Bit, Simultaneous Sampling, Fully-Diff ADC	Texas Instruments	ADS8354IPWR or ADS7854IPWR
30	0	U2, U3	Not Install	Texas Instruments	SN74LVC1G34DCK
31	2	U4, U11	IC, Low Power, Negative Rail Input, R-to-R, Fully Diff Amp	Texas Instruments	THS4521IDGKT
32	1	U5	IC, Low Noise, Low Drift, Precision Voltage Reference	Texas Instruments	REF5025IDGK
33	2	U6, U12	IC, Low Noise, Low Quiescent Current, Precision OPA	Atmel	OPA376AIDBV
34	1	U7	IC, I2C Compatible (2-Wire) Serial EEPROM	Texas Instruments	AT24C02C-XHM
35	1	U8	IC,36-V, 1-A, 4.17uVRMS RF LDO Voltage Regulator	Texas Instruments	TPS7A4700RGW
36	1	U9	IC, 60mA, 5.5V, Buck/Boost Charge Pump	Texas Instruments	REG71055DDC
37	0	U10	Not Install: Low Noise, Low Drift, Precision Voltage Reference	Texas Instruments	Not Install: REF5050IDGK
38	1	U13	IC, High-Speed, Single-Supply, Rail-to-Rail OPA	Texas Instruments	OPA2350EA
39	1	U14	IC, NanoPower Supervisory Circuit	Texas Instruments	TPS3836E18DBVT
40	5	N/A	Conn Shunt, Pitch 0.100"; Height 0.240" , Gold Plated	Samtec	SNT-100-BK-G
41	1	TP0	TEST POINT PC MINI .040"D BLACK	Keystone Electronics	5001
42	0	TP1, TP2, TP3, TP4, TP5, TP6	Not Install: TEST POINT PC MINI .040"D BLACK	Keystone Electronics	Not Install: 5001
43	2	N/A	BUMPON CYLINDRICAL .375X.135 BLK	3M	SJ61A8

7.2 PCB Layout

Figure 27 through Figure 30 show the PCB layouts for the ADSxx54EVM.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing ADSxx54EVM PCBs.

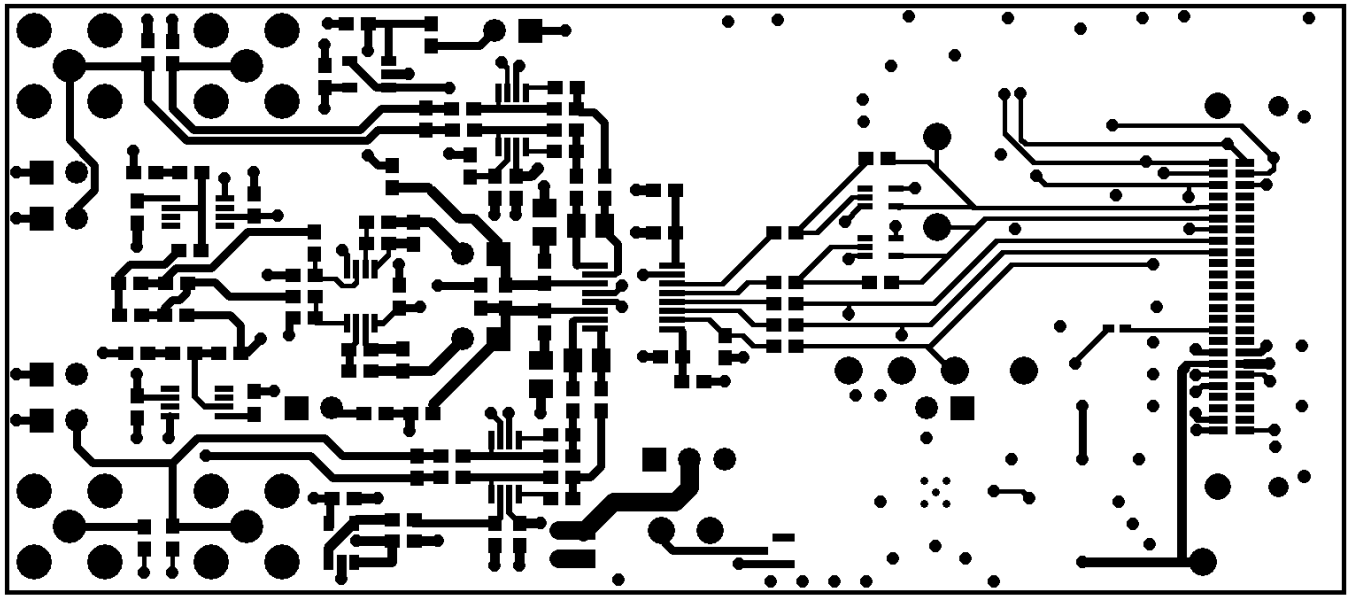


Figure 27. ADSxx54EVM PCB: Top Layer

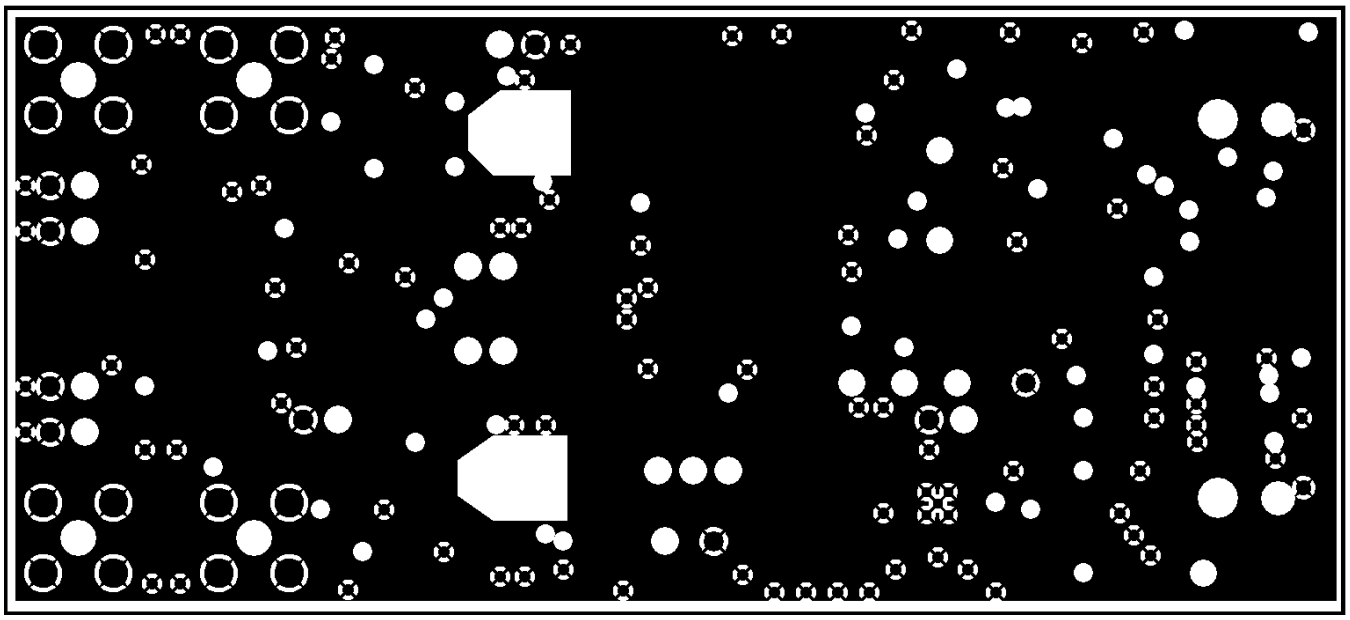


Figure 28. ADSxx54EVM PCB: Ground Layer

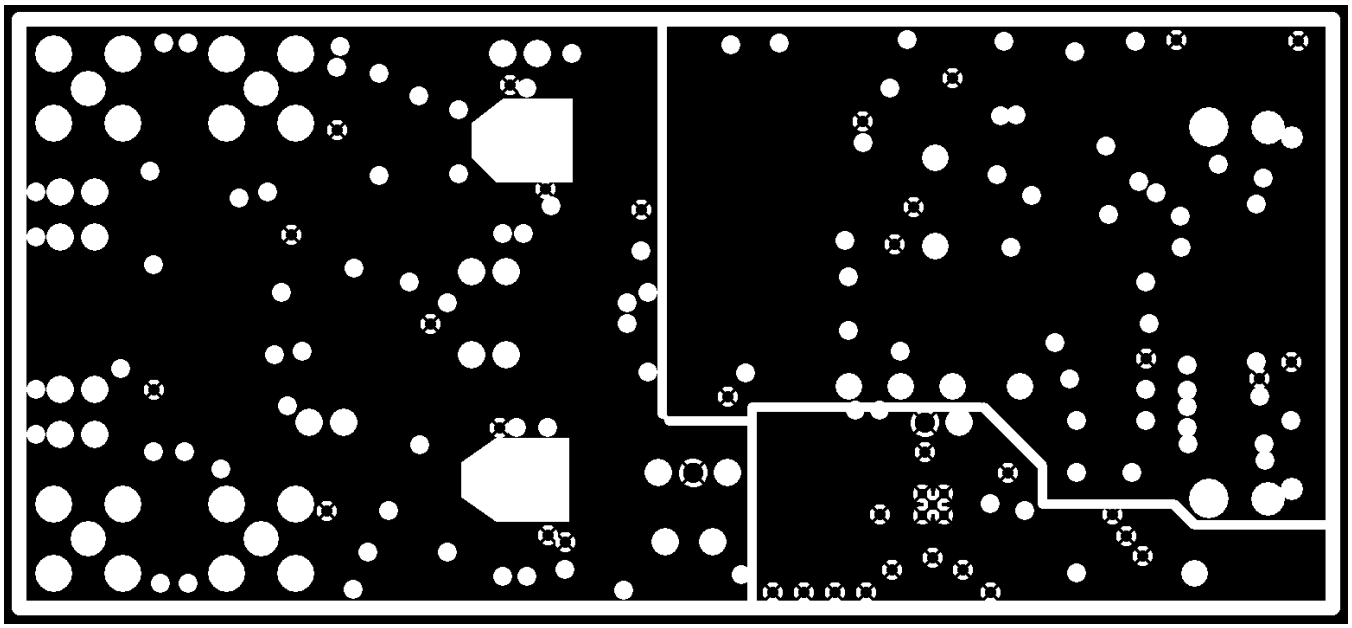


Figure 29. ADSxx54EVM PCB: Power Layer

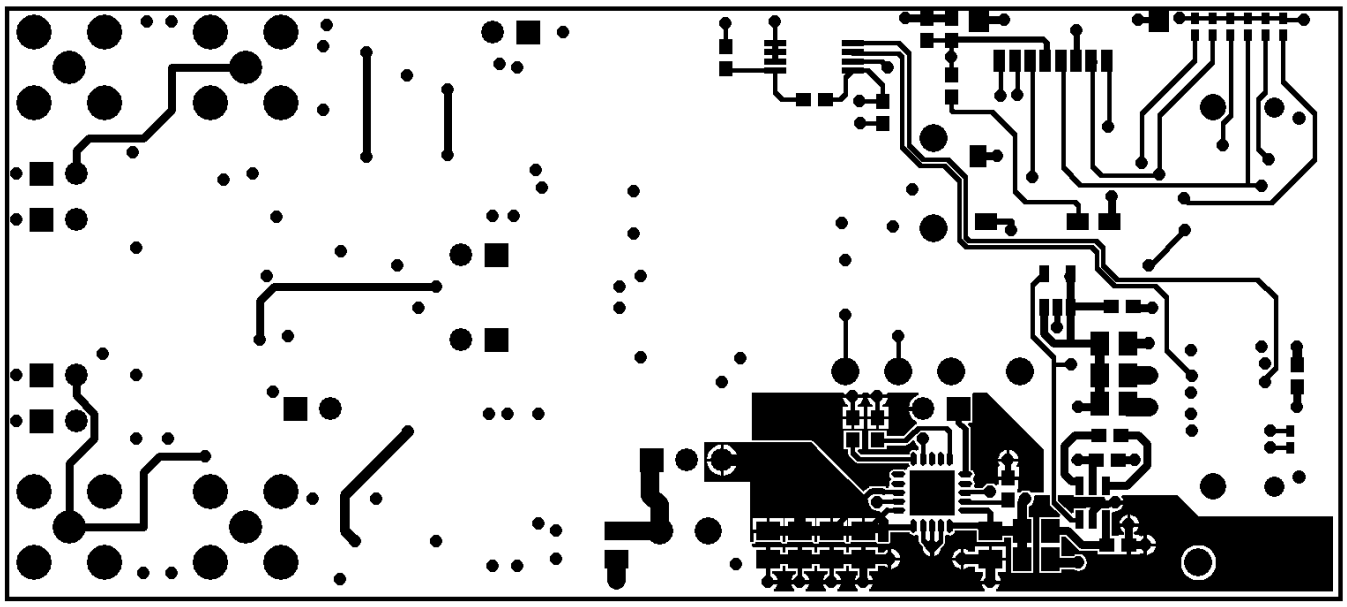
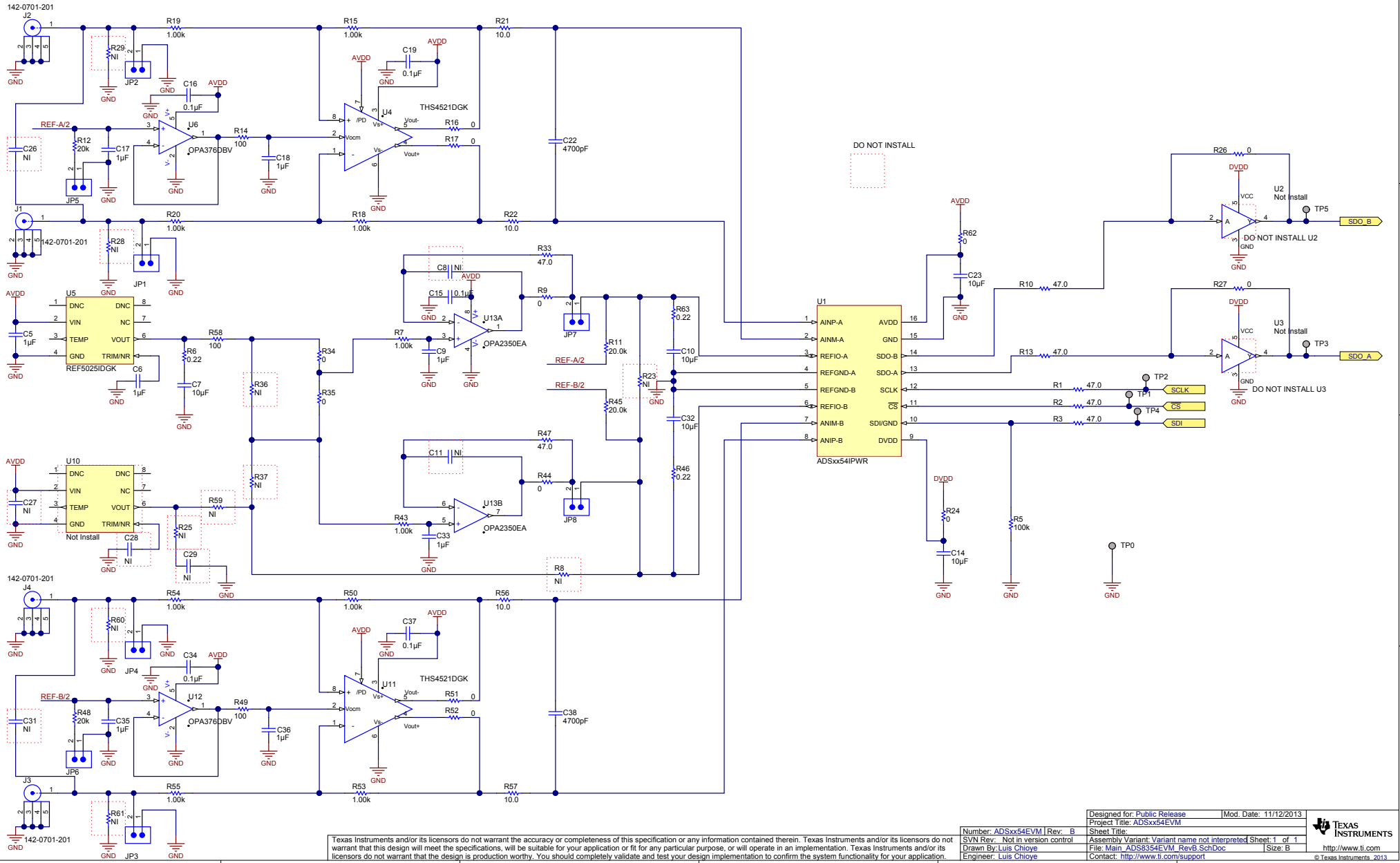


Figure 30. ADSxx54EVM PCB: Bottom Layer

7.3 Schematics

The schematics for the ADSxx54EVM are appended to the end of this user's guide.

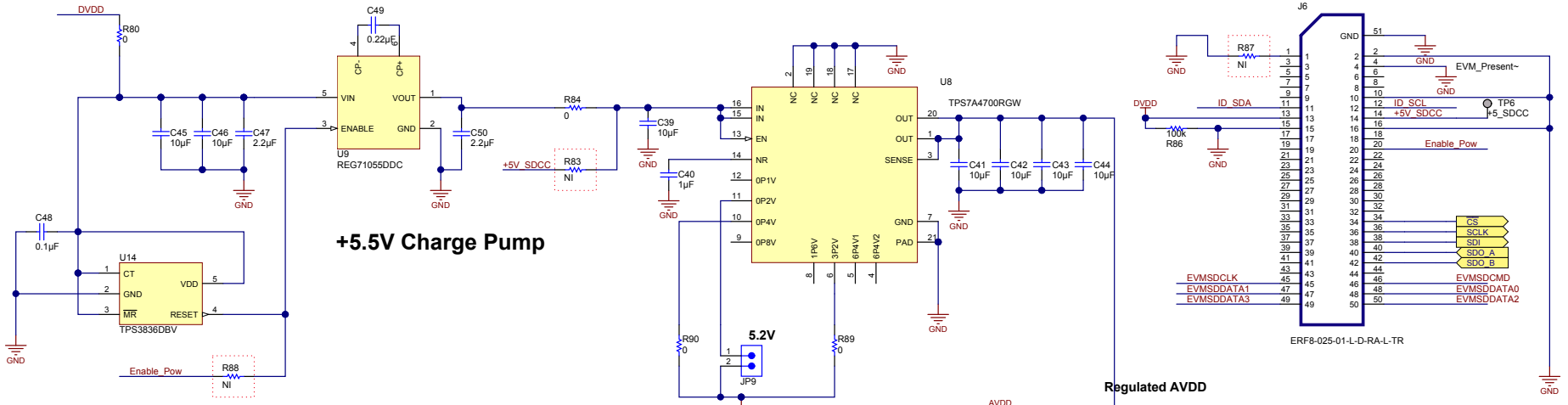


Number: ADSxx54EVM	Rev: B
SVN Rev: Not in version control	
Drawn By: Luis Chioye	
Engineer: Luis Chioye	

Designed for: Public Release	Mod. Date: 11/12/2013
Project Title: ADSxx54EVM	
Sheet Title:	
Assembly Variant: Variant name not interpreted	Sheet: 1 of 1
File: Main_ADS8354EVM_RevB.SchDoc	Size: B
Contact: http://www.ti.com/support	

Texas Instruments
http://www.ti.com

+3.3V SDCC Digital Supply



Number: ADSxx54EVM	Rev: B	Designed for: Public Release	Mod. Date: 11/12/2013
SVN Rev: Not in version control		Project Title: ADSxx54EVM	
Drawn By:		Sheet Title:	
Engineer: Luis Chioye		Assembly Variant: Variant name not interpreted	Sheet: 1 of 1
		File: Connector_ADS854EVM_RevB.SchDoc	Size: B
		Contact: http://www.ti.com/support	

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For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Important Notice for Users of EVMs Considered "Radio Frequency Products" in Japan

EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

http://www.tij.co.jp

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