High Voltage Latch-Up Proof, Triple/Quad SPDT Switches

Data Sheet

ADG5433/ADG5434

FEATURES

- Latch-up proof
- Human body model (HBM) ESD rating: 8 kV
- Low on resistance (13.5 Ω)
- ±9 V to ±22 V dual-supply operation
- 9 V to 40 V single-supply operation
- 48 V supply maximum ratings
- Fully specified at ±15 V, ±20 V, +12 V, and +36 V
- V_{SS} to V_{DD} analog signal range

APPLICATIONS

- Relay replacement
- Automatic test equipment
- Data acquisition
- Instrumentation
- Avionics
- Audio and video switching
- Communication systems

FUNCTIONAL BLOCK DIAGRAMS

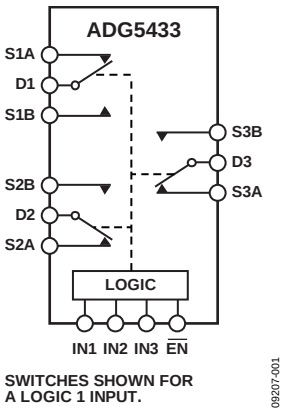

Figure 1. ADG5433 TSSOP and LFCSP_WQ

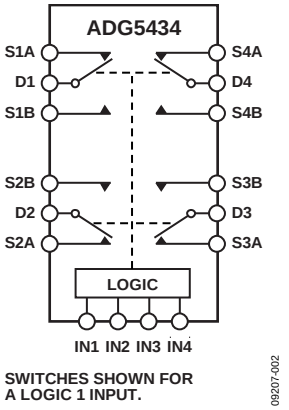

Figure 2. ADG5434 TSSOP and LFCSP_WQ

GENERAL DESCRIPTION

The ADG5433 and ADG5434 are monolithic industrial CMOS analog switches comprising three independently selectable single-pole, double-throw (SPDT) switches and four independently selectable SPDT switches, respectively.

All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An $\overline{EN}$ input on the ADG5433 (LFCSP and TSSOP packages) is used to enable or disable the device. When disabled, all channels are switched off.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications, where low distortion is critical.

PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON}.
3. Dual-supply operation. For applications where the analog signal is bipolar, the ADG5433/ADG5434 can be operated from dual supplies up to ±22 V.
4. Single-supply operation. For applications where the analog signal is unipolar, the ADG5433/ADG5434 can be operated from a single-rail power supply up to 40 V.
5. 3 V logic compatible digital inputs: V_{INH} = 2.0 V, V_{INL} = 0.8 V.
6. No V_L logic power supply required.

Rev. C
Document Feedback

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SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	13.5			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 27
	15	18	22	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	1.8			Ω typ	V_S = ±10 V, I_S = −10 mA
	2.2	2.6	3	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±10 V, V_D = ∓10 V
	±0.25	±1	±7	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±10 V, V_D = ∓10 V
	±0.4	±4	±30	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = ±10 V; see Figure 26
	±0.4	±4	±30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	157			ns typ	R_L = 300 Ω, C_L = 35 pF
	207	245	272	ns max	V_S = 10 V
t_{ON} ($\overline{EN}$)	160			ns typ	R_L = 300 Ω, C_L = 35 pF
	196	241	274	ns max	V_S = 10 V; see Figure 34
t_{OFF} ($\overline{EN}$)	91			ns typ	R_L = 300 Ω, C_L = 35 pF
	106	138	140	ns max	V_S = 10 V; see Figure 34
Break-Before-Make Time Delay, t_D	45			ns typ	R_L = 300 Ω, C_L = 35 pF
			21	ns min	V_{S1} = V_{S2} = 10 V; see Figure 33
Charge Injection, Q_{INJ}	130			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 35
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 28
Total Harmonic Distortion + Noise	0.01			% typ	R_L = 1 kΩ, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	145			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	−0.9			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	14			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	24			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	53			pF typ	V_S = 0 V, f = 1 MHz

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	45			µA typ	Digital inputs = 0 V or V_{DD}
	55		70	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1	µA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	12.5			Ω typ	V_S = ±15 V, I_S = −10 mA; see Figure 27
	14	17	21	Ω max	V_{DD} = +18 V, V_{SS} = −18 V
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	V_S = ±15 V, I_S = −10 mA
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	2.3			Ω typ	V_S = ±15 V, I_S = −10 mA
	2.7	3.1	3.5	Ω max	
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±15 V, V_D = ∓15 V
	±0.25	±1	±7	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓15 V
	±0.4	±4	±30	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = ±15 V; see Figure 26
	±0.4	±4	±30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	199	230	253	ns max	V_S = 10 V
t_{ON} ($\overline{EN}$)	152			ns typ	R_L = 300 Ω, C_L = 35 pF
	186	223	253	ns max	V_S = 10 V; see Figure 34
t_{OFF} ($\overline{EN}$)	90			ns typ	R_L = 300 Ω, C_L = 35 pF
	104	118	130	ns max	V_S = 10 V; see Figure 34
Break-Before-Make Time Delay, t_D	36			ns typ	R_L = 300 Ω, C_L = 35 pF
			17	ns min	V_{S1} = V_{S2} = 10 V; see Figure 33
Charge Injection, Q_{INJ}	176			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 35
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1MHz; see Figure 29
Channel-to-Channel Crosstalk	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise	0.012			% typ	R_L = 1 kΩ, 20 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	140			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	15			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	23			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	52			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +22 V, V_{SS} = −22 V
I_{DD}	50			μA typ	Digital inputs = 0 V or V_{DD}
	70		110	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	26			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 27
	30	36	42	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	1	1.5	1.6	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	5.5			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	6.5	8	12	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V
	±0.25	±1	±7	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V
	±0.4	±4	±30	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = 1 V/10 V; see Figure 26
	±0.4	±4	±30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	220			ns typ	R_L = 300 Ω, C_L = 35 pF
	290	357	400	ns max	V_S = 8 V
t_{ON} ($\overline{EN}$)	228			ns typ	R_L = 300 Ω, C_L = 35 pF
	289	370	426	ns max	V_S = 8 V; see Figure 34
t_{OFF} ($\overline{EN}$)	90			ns typ	R_L = 300 Ω, C_L = 35 pF
	115	131	151	ns max	V_S = 8 V; see Figure 34
Break-Before-Make Time Delay, t_D	106			ns typ	R_L = 300 Ω, C_L = 35 pF
			54	ns min	V_{S1} = V_{S2} = 8 V; see Figure 33
Charge Injection, Q_{INJ}	60			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 35
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Channel-to-Channel Crosstalk	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise	0.1			% typ	R_L = 1 kΩ, 6 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	150			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	18			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	28			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	54			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	40			µA typ	Digital inputs = 0 V or V_{DD}
	50		65	µA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	14.5			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA; see Figure 27
	16	19	23	Ω max	V_{DD} = 32.4 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	3.5			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	4.3	5.5	6.5	Ω max	
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V
	±0.25	±1	±7	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V
	±0.4	±4	±30	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = 1 V/30 V; see Figure 26
	±0.4	±4	±30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	180			ns typ	R_L = 300 Ω, C_L = 35 pF
	262	274	289	ns max	V_S = 18 V
t_{ON} ($\overline{EN}$)	176			ns typ	R_L = 300 Ω, C_L = 35 pF
	216	238	268	ns max	V_S = 18 V; see Figure 34
t_{OFF} ($\overline{EN}$)	98			ns typ	R_L = 300 Ω, C_L = 35 pF
	123	127	129	ns max	V_S = 18 V; see Figure 34
Break-Before-Make Time Delay, t_D	50			ns typ	R_L = 300 Ω, C_L = 35 pF
			21	ns min	V_{S1} = V_{S2} = 18 V; see Figure 33

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Charge Injection, Q_{INJ}	150			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF; see Figure 35
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise	0.4			% typ	R_L = 1 kΩ, 18 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	135			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	−1			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	18			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	28			pF typ	V_S = 18 V, f = 1 MHz
C_D (On), C_S (On)	46			pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 39.6 V
I_{DD}	80			µA typ	Digital inputs = 0 V or V_{DD}
	100		130	µA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5. ADG5433

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
V_{DD} = +15 V, V_{SS} = −15 V				
TSSOP (θ_{JA} = 112.6°C/W)	80	58	36	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	147	103	70	mA maximum
V_{DD} = +20 V, V_{SS} = −20 V				
TSSOP (θ_{JA} = 112.6°C/W)	85	63	39	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	156	109	74	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	63	45	28	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	116	84	53	mA maximum
V_{DD} = 36 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	83	60	37	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	151	107	72	mA maximum

Table 6. ADG5434

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
V_{DD} = +15 V, V_{SS} = −15 V				
TSSOP (θ_{JA} = 112.6°C/W)	70	51	31	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	117	76	49	mA maximum
V_{DD} = +20 V, V_{SS} = −20 V				
TSSOP (θ_{JA} = 112.6°C/W)	74	54	33	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	123	79	50	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	54	39	23	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	94	64	44	mA maximum
V_{DD} = 36 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	73	53	32	mA maximum
LFCSP (θ_{JA} = 30.4°C/W)	120	78	50	mA maximum

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	
ADG5433	280 mA (pulsed at 1 ms, 10% duty cycle maximum)
ADG5434	240 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[2]	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112.6°C/W
20-Lead TSSOP (4-Layer Board)	143°C/W
16-Lead LFCSP (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C

[1] Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] See Table 5 and Table 6.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

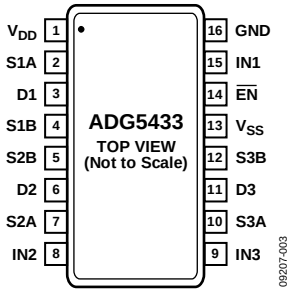


Figure 3. ADG5433 TSSOP Pin Configuration

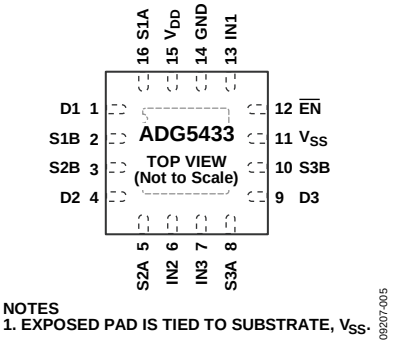


Figure 4. ADG5433 LFCSP_WQ Pin Configuration

Table 8. ADG5433 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP_WQ**	**Mnemonic**	**Description**
1	15	V_{DD}	Most Positive Power Supply Potential.
2	16	S1A	Source Terminal 1A. This pin can be an input or an output.
3	1	D1	Drain Terminal 1. This pin can be an input or an output.
4	2	S1B	Source Terminal 1B. This pin can be an input or an output.
5	3	S2B	Source Terminal 2B. This pin can be an input or an output.
6	4	D2	Drain Terminal 2. This pin can be an input or an output.
7	5	S2A	Source Terminal 2A. This pin can be an input or an output.
8	6	IN2	Logic Control Input 2.
9	7	IN3	Logic Control Input 3.
10	8	S3A	Source Terminal 3A. This pin can be an input or an output.
11	9	D3	Drain Terminal 3. This pin can be an input or an output.
12	10	S3B	Source Terminal 3B. This pin can be an input or an output.
13	11	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
14	12	$\overline{EN}$	Active Low Digital Input. When high, the device is disabled and all switches are off. When low, INx logic inputs determine the on switches.
15	13	IN1	Logic Control Input 1.
16	14	GND	Ground (0 V) Reference.
	EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 9. ADG5433 Truth Table

$\overline{EN}$	INx	SxA	SxB
1	X	Off	Off
0	0	Off	On
0	1	On	Off

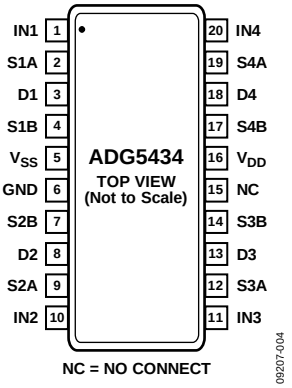


Figure 5. ADG5434 TSSOP Pin Configuration

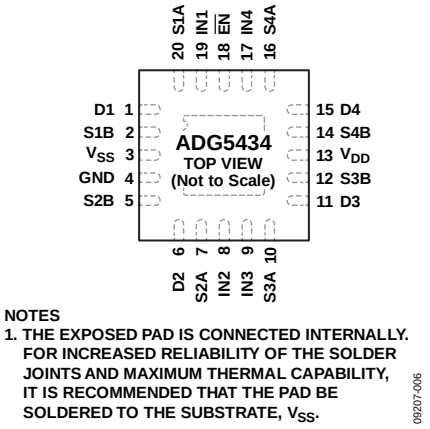


Figure 6. ADG5434 LFCSP_WQ Pin Configuration

Table 10. ADG5434 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP_WQ**	**Mnemonic**	**Description**
1	19	IN1	Logic Control Input 1.
2	20	S1A	Source Terminal 1A. This pin can be an input or an output.
3	1	D1	Drain Terminal 1. This pin can be an input or an output.
4	2	S1B	Source Terminal 1B. This pin can be an input or an output.
5	3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
6	4	GND	Ground (0 V) Reference.
7	5	S2B	Source Terminal 2B. This pin can be an input or an output.
8	6	D2	Drain Terminal 2. This pin can be an input or an output.
9	7	S2A	Source Terminal 2A. This pin can be an input or an output.
10	8	IN2	Logic Control Input 2.
11	9	IN3	Logic Control Input 3.
12	10	S3A	Source Terminal 3A. This pin can be an input or an output.
13	11	D3	Drain Terminal 3. This pin can be an input or an output.
14	12	S3B	Source Terminal 3B. This pin can be an input or an output.
15	N/A	NC	No Connect.
16	13	V_{DD}	Most Positive Power Supply Potential.
17	14	S4B	Source Terminal 4B. This pin can be an input or an output.
18	15	D4	Drain Terminal 4. This pin can be an input or an output.
19	16	S4A	Source Terminal 4A. This pin can be an input or an output.
20	17	IN4	Logic Control Input 4.
N/A	18	$\overline{EN}$	Active Low Digital Input. When high, the device is disabled and all switches are off. When low, INx logic inputs determine the on switches.
N/A	EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 11. ADG5434 Truth Table

INx	SxA	SxB
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

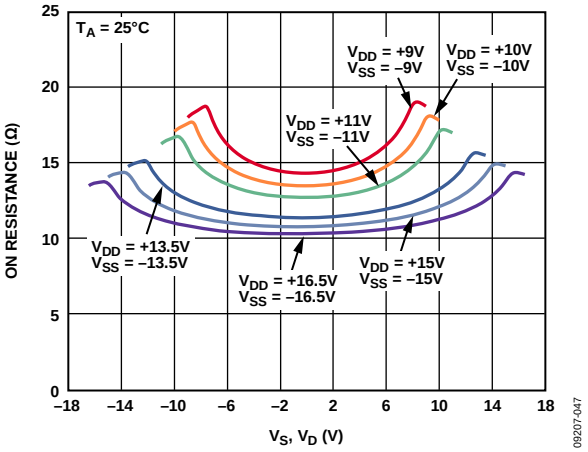


Figure 7. On Resistance as a Function of V_S, V_D (Dual Supply)

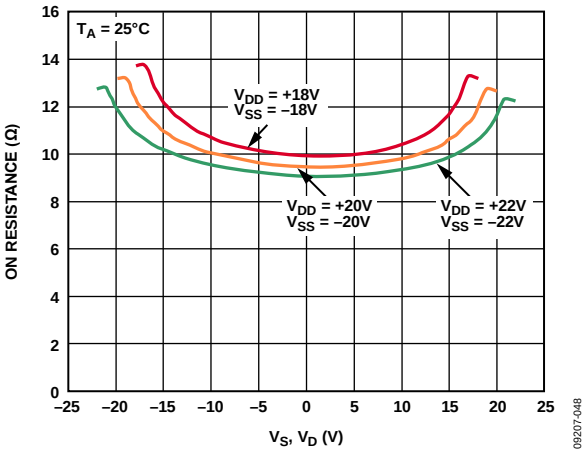


Figure 8. On Resistance as a Function of V_S, V_D (Dual Supply)

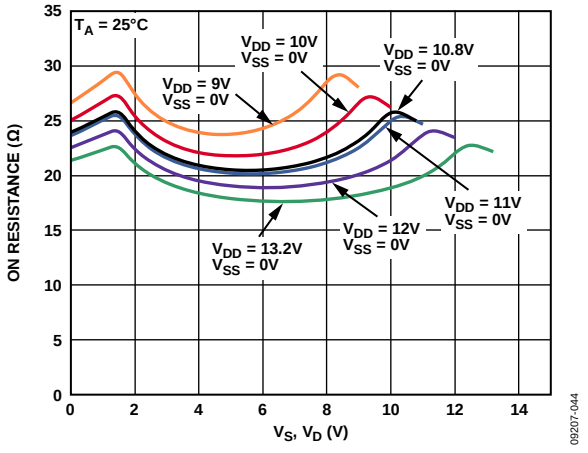


Figure 9. On Resistance as a Function of V_S, V_D (Single Supply)

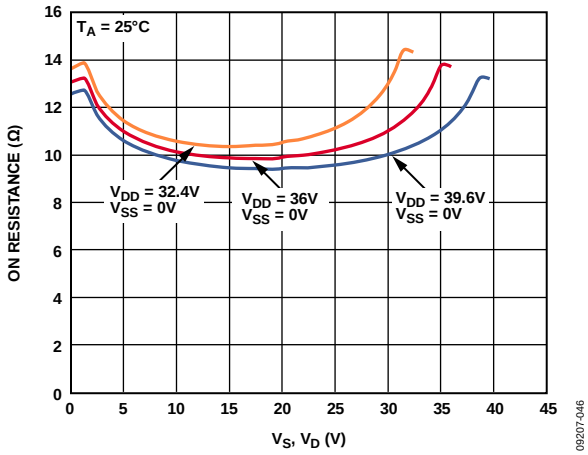


Figure 10. On Resistance as a Function of V_S, V_D (Single Supply)

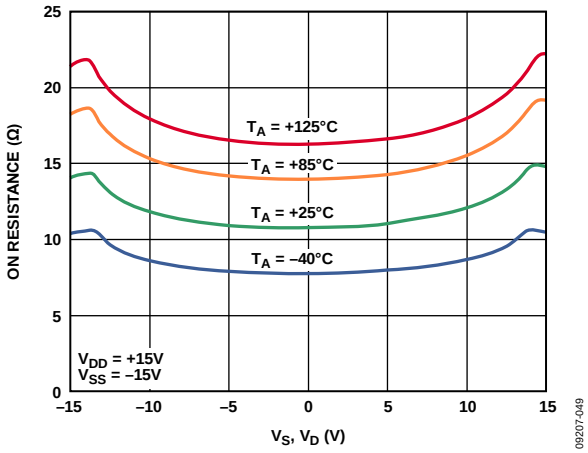


Figure 11. On Resistance as a Function of V_S (V_D) for Different Temperatures, ±15 V Dual Supply

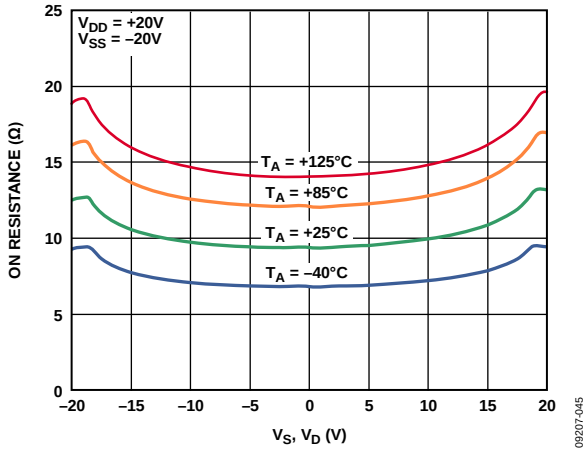


Figure 12. On Resistance as a Function of V_S (V_D) for Different Temperatures, ±20 V Dual Supply

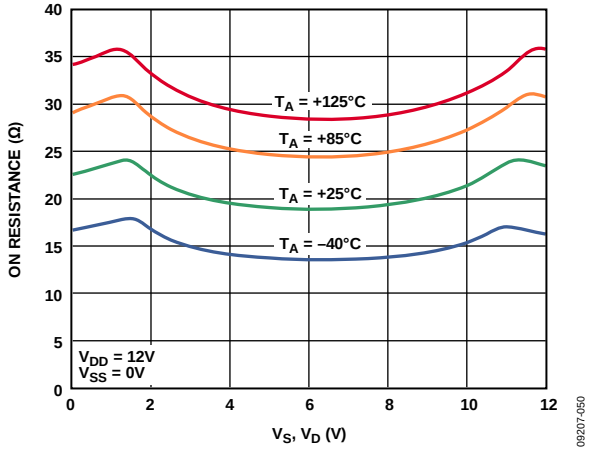


Figure 13. On Resistance as a Function of V_S (V_D) for Different Temperatures, 12 V Single Supply

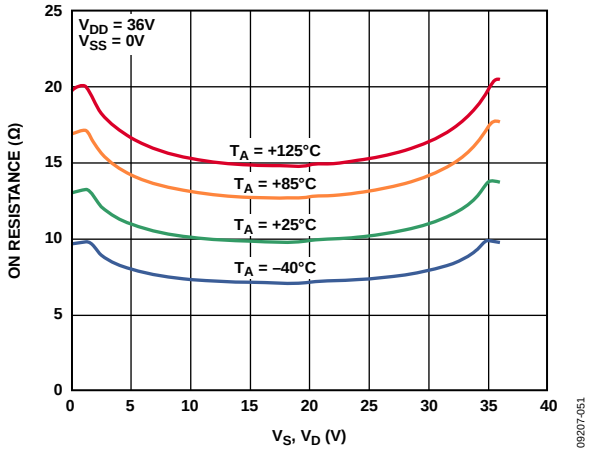


Figure 14. On Resistance as a Function of V_S (V_D) for Different Temperatures, 36 V Single Supply

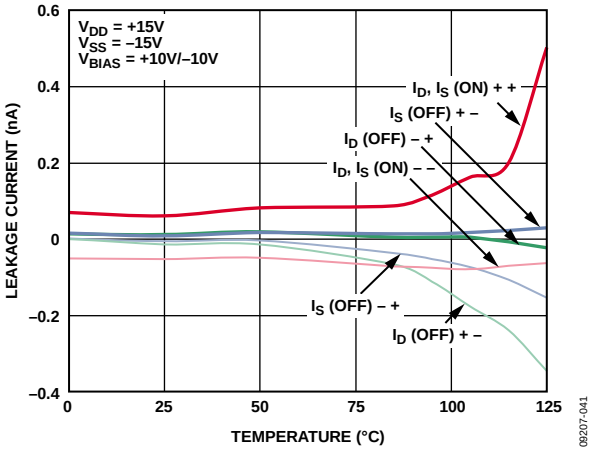


Figure 15. Leakage Currents as a Function of Temperature, ±15 V Dual Supply

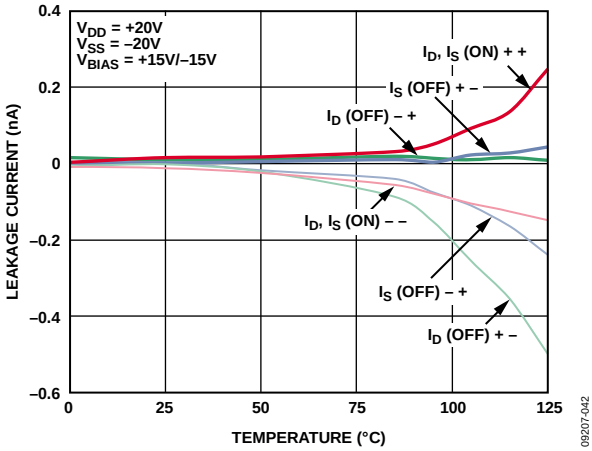


Figure 16. Leakage Currents as a Function of Temperature, ±20 V Dual Supply

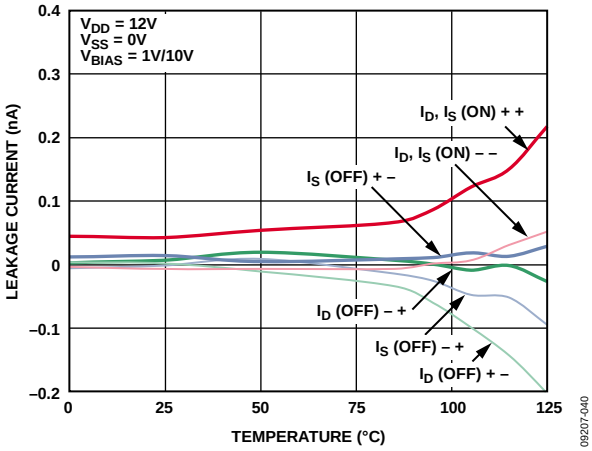


Figure 17. Leakage Currents as a Function of Temperature, 12 V Single Supply

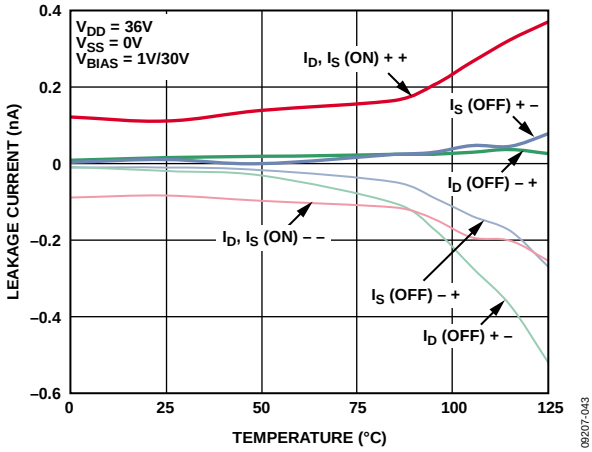


Figure 18. Leakage Currents as a Function of Temperature, 36 V Single Supply

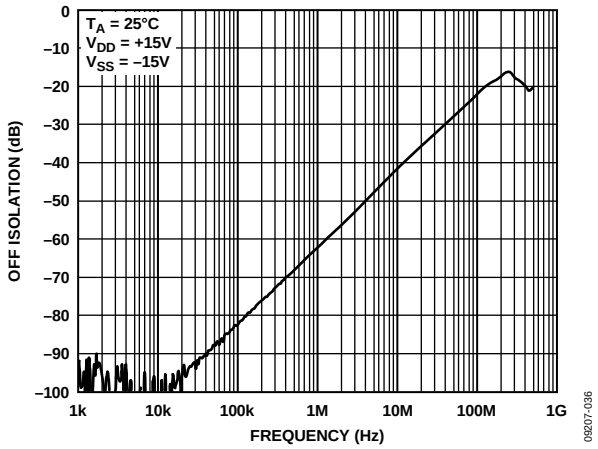


Figure 19. Off Isolation vs. Frequency

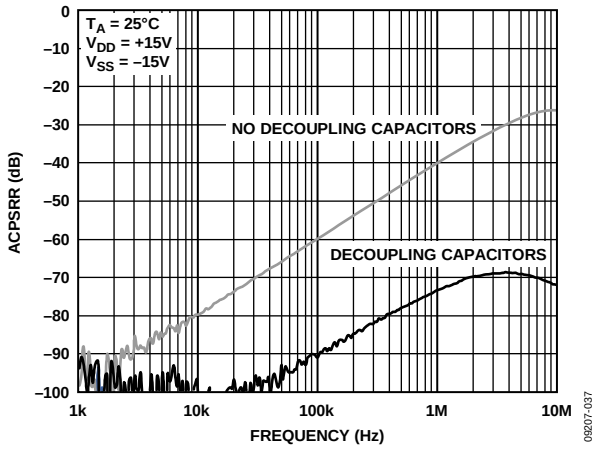


Figure 22. ACPSRR vs. Frequency

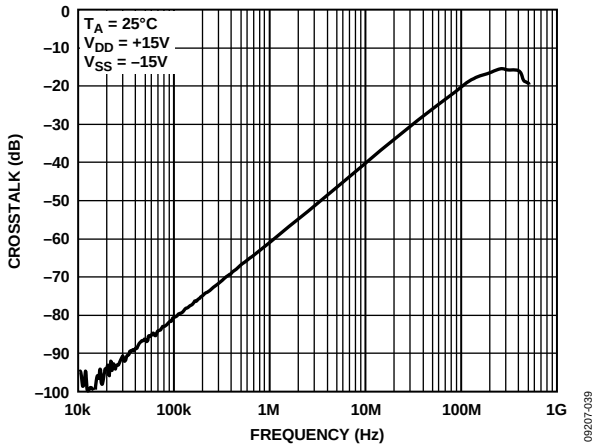


Figure 20. Crosstalk vs. Frequency

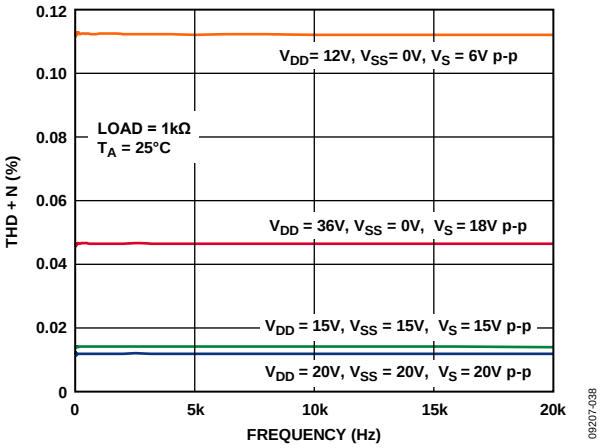


Figure 23. THD + N vs. Frequency

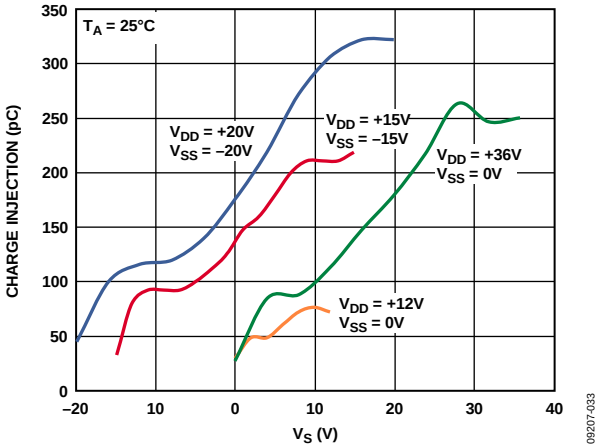


Figure 21. Charge Injection vs. Source Voltage

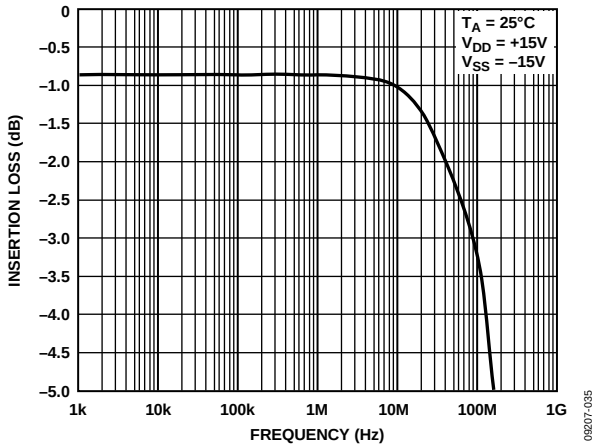


Figure 24. Bandwidth

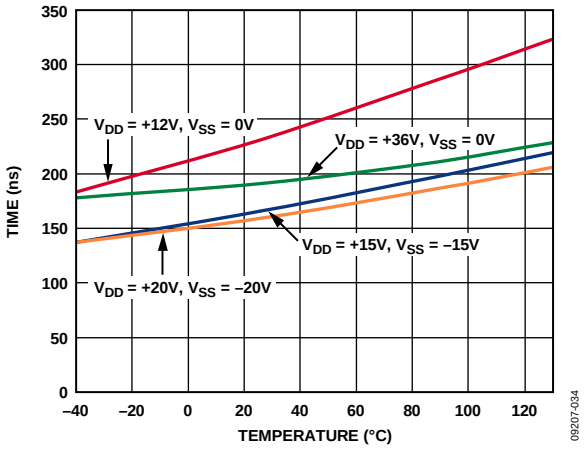


Figure 25. $t_{TRANSITION}$ Times vs. Temperature

TEST CIRCUITS

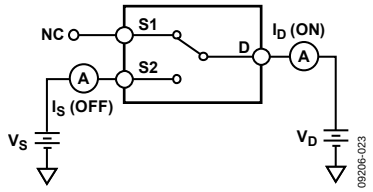


Figure 26. On and Off Leakage

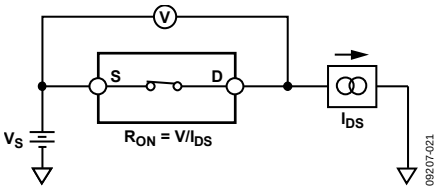


Figure 27. On Resistance

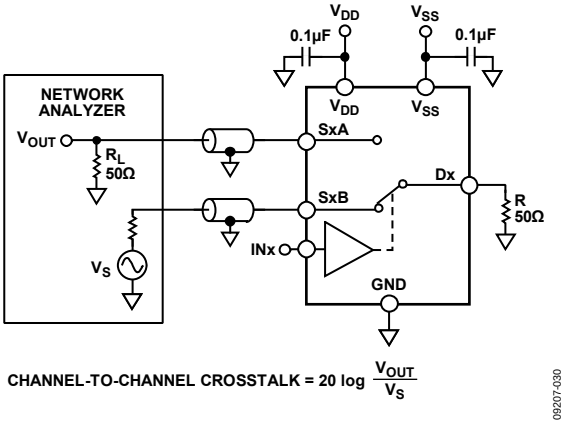


Figure 28. Channel-to-Channel Crosstalk

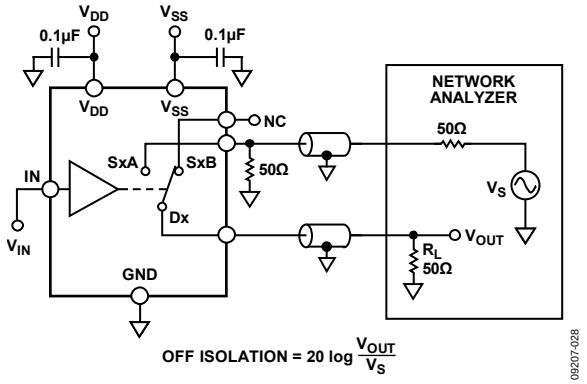


Figure 29. Off Isolation

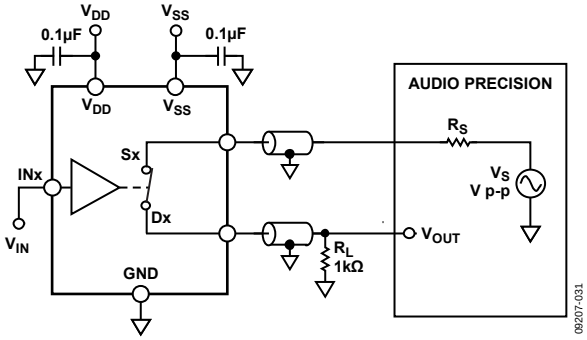


Figure 30. THD + Noise

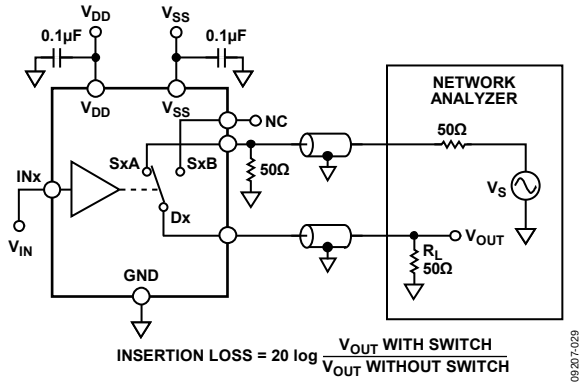


Figure 31. Bandwidth

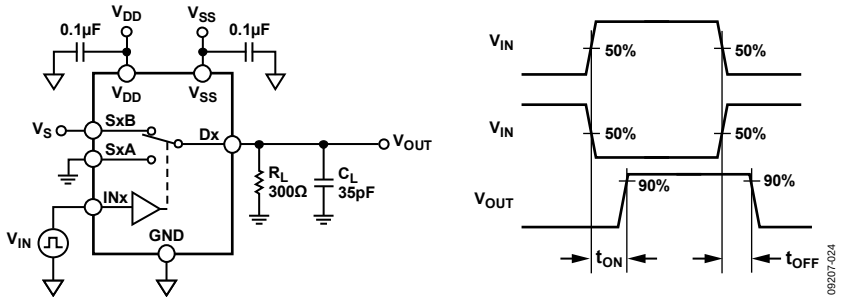


Figure 32. Switching Timing

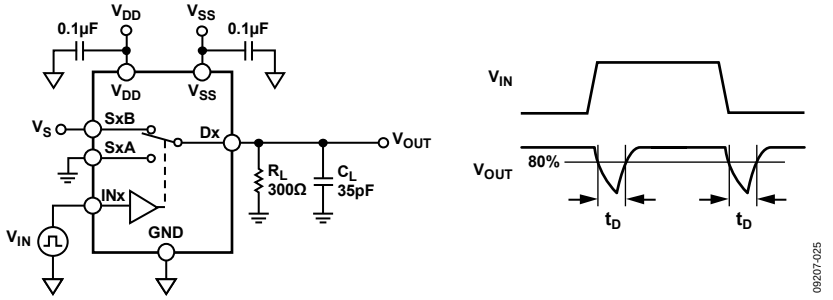


Figure 33. Break-Before-Make Delay, t_D

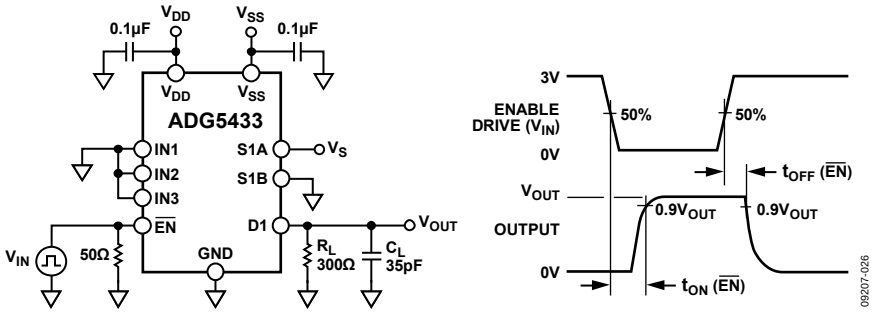


Figure 34. Enable Delay, t_{ON} ($\overline{EN}$), t_{OFF} ($\overline{EN}$)

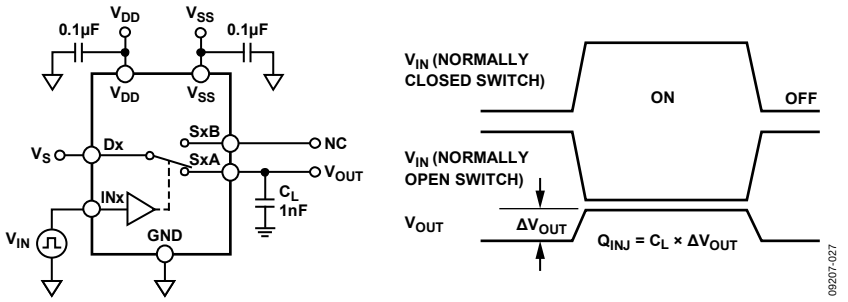


Figure 35. Charge Injection

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}
R_{ON} is the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
The difference between the maximum and minimum value of on resistance as measured over the specified analog signal range is represented by $R_{FLAT (ON)}$.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} represents digital input capacitance.

t_{ON} ($\overline{EN}$)
t_{ON} ($\overline{EN}$) represents the delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} ($\overline{EN}$)
t_{OFF} ($\overline{EN}$) represents the delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D
t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is a measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

TRENCH ISOLATION

In the ADG5433/ADG5434, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

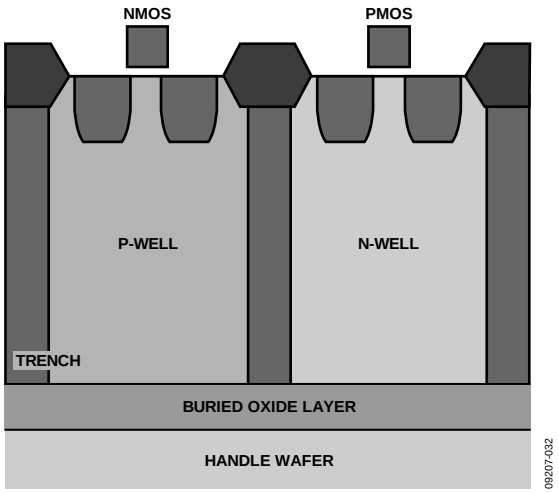
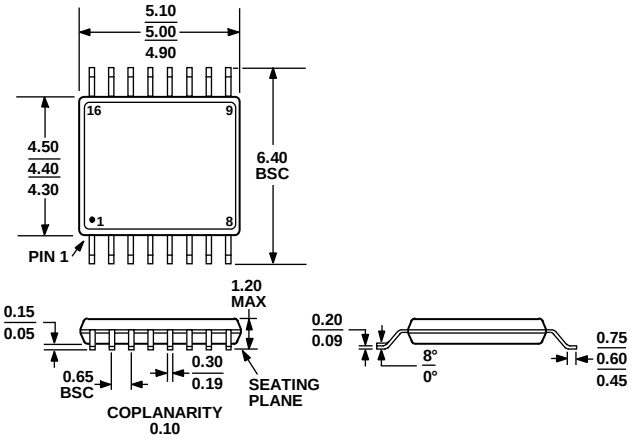


Figure 36. Trench Isolation

APPLICATIONS INFORMATION

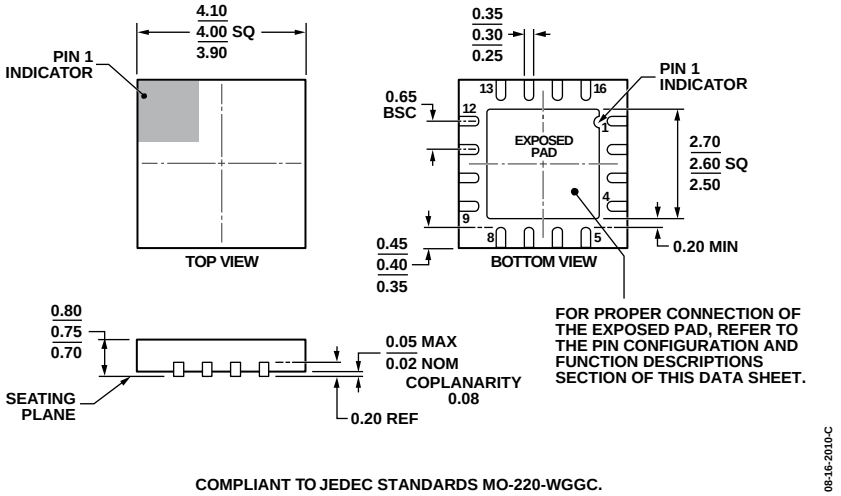
The ADG54xx family of switches and multiplexers provide a robust solution for instrumentation, industrial, aerospace and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The ADG5433/ADG5434 high voltage switches allow single-supply operation from 9 V to 40 V and dual supply operation from ±9 V to ±22 V. The ADG5433/ADG5434 (as well as other select devices within this family) achieve 8 kV human body model ESD ratings, which provide a robust solution eliminating the need for separate protect circuitry designs in some applications.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 37. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-17)
Dimensions shown in millimeters

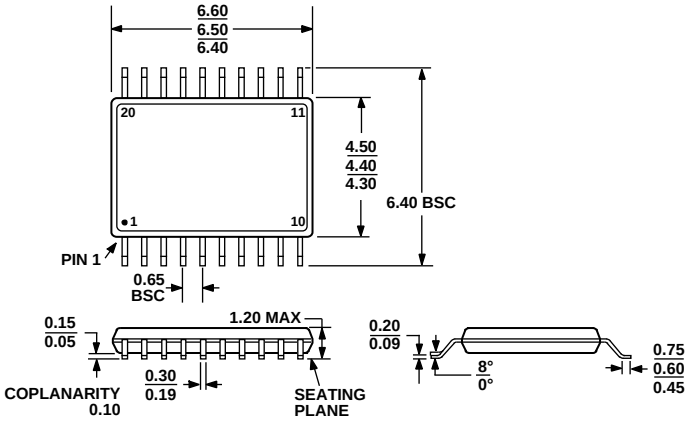


Figure 39. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

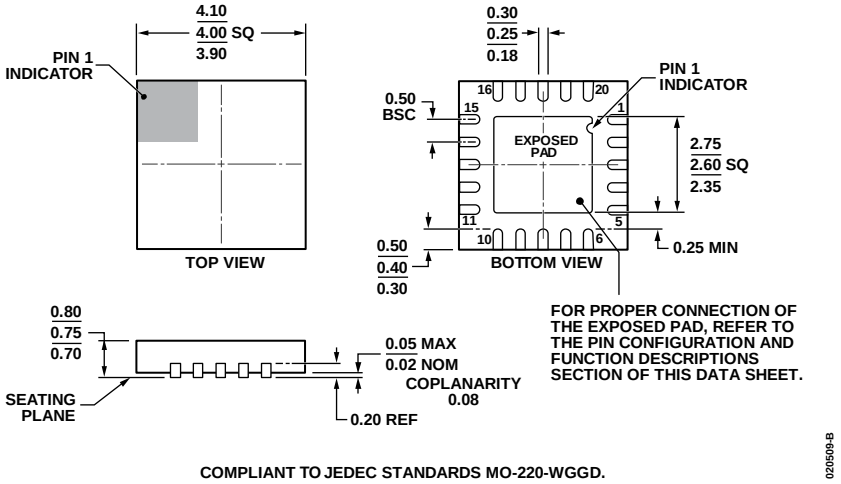


Figure 40. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Description	$\overline{\text{EN}}$ Pin	Package Option
ADG5433BRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	Yes	RU-16
ADG5433BRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	Yes	RU-16
ADG5433BCPZ-REEL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	Yes	CP-16-17
ADG5434BRUZ	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	No	RU-20
ADG5434BRUZ-REEL7	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	No	RU-20
ADG5434BCPZ-REEL7	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	Yes	CP-20-8

[1] Z = RoHS Compliant Part.

NOTES

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D09207-0-6/13(C)

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADG5434BRUZ-REEL7 ADG5433BRUZ-REEL7 ADG5434BRUZ ADG5433BRUZ ADG5433WBRUZ ADG5434BCPZ-REEL7