DEM-OPA-SO-2B Demonstration Fixture

1 Description

The DEM-OPA-SO-2B demonstration fixture is a noninverting configuration, unpopulated printed circuit board (PCB) for dual op amps in SO-8 packages. This board has been optimized to minimize parasitics and provide good harmonic distortion for wideband, high-gain, high-speed amplifiers. Figure 1 shows the package pinout for this type of op amp. For more information on these op amps, as well as good PCB layout techniques, see the individual amplifier data sheets.

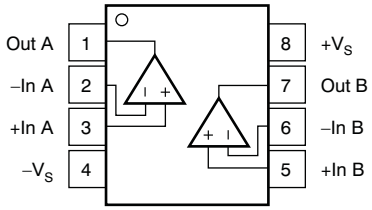

Figure 1. SO Package Pinout, Top View

2 Circuit

The circuit schematic in Figure 2 shows the connections for all possible components. (Only one amplifier is shown in the schematic.)

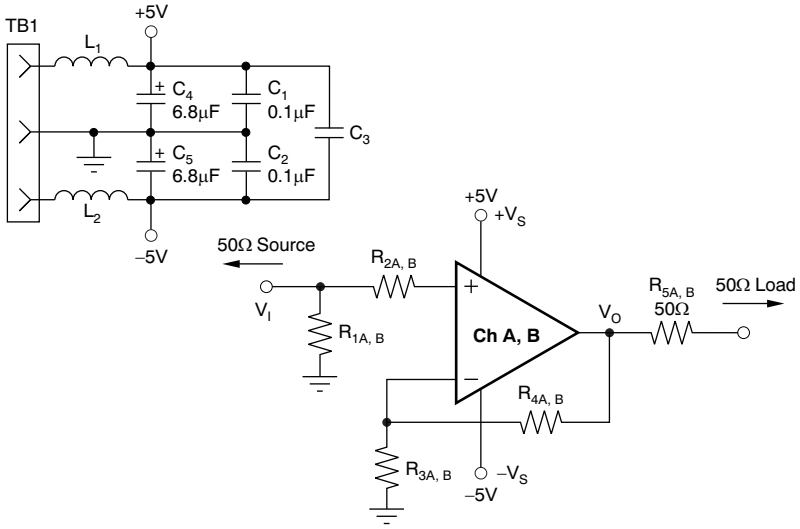

Figure 2. Schematic for DEM-OPA-SO-2B

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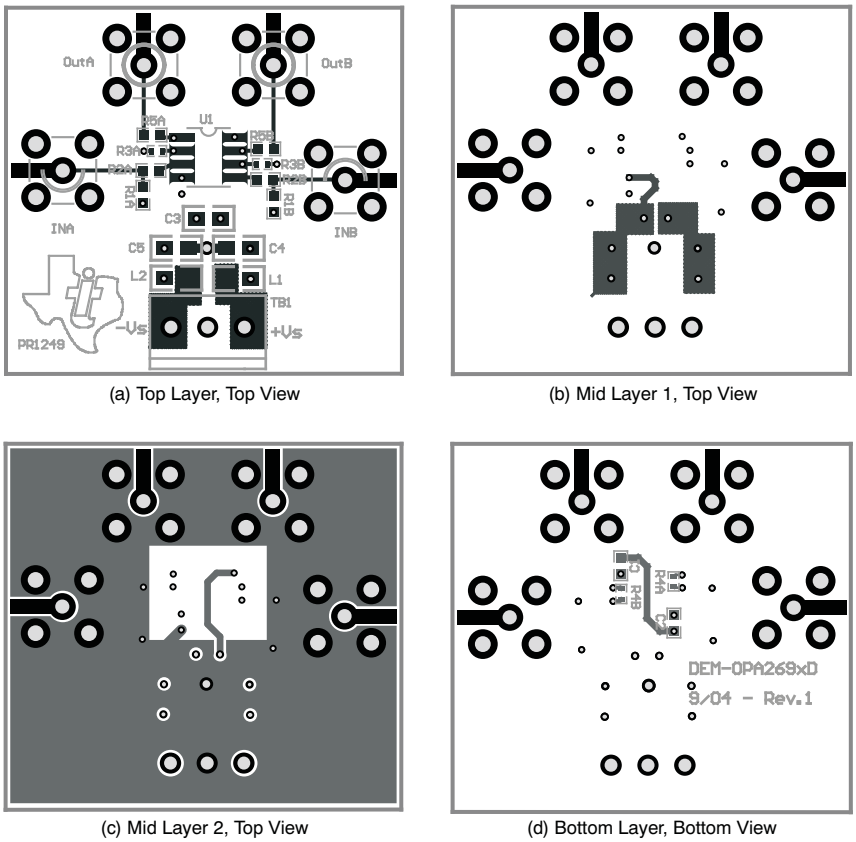
3 Components

Components that have RF performance similar to the ones in Table 1 may be substituted.

Table 1. Component Descriptions

PART	DESCRIPTION
C_4, C_5	Tantalum Chip Capacitor, SMD EIA Size 0805, 20V
C_3	Multilayer Ceramic Chip Capacitor, SMD 0805, 50V
C_1, C_2	Multilayer Ceramic Chip Capacitor, SMD 0603, 50V
L_1, L_2	EMI-Suppression Ferrite Chip, SMD 0805
U1	Dual Operational Amplifier
$R_{1A,B}$, $R_{2A,B}$, $R_{5A,B}$	Metal Film Chip Resistor, SMD 0603, 1/10W
$R_{3A,B}$, $R_{4A,B}$	Metal Film Chip Resistor, SMD 0402, 1/16W
TB1	Terminal Block, 3.5mm Centers (On-Shore Technology ED555/2DS)
In A, In B, Out A, Out B	SMA or SMB Board Jack (Amphenol 901-144-8)

Refer to Figure 3 for the location of the following components. $R_{1A, B}$ and $R_{5A, B}$ set the I/O impedance. $R_{3A, B}$ and $R_{4A, B}$ set the gain. $R_{2A, B}$ is used to form a simple, high-frequency pole with parasitic input capacitance. C_1, C_2, C_3, C_4, and C_5 are supply bypass capacitors. C_3 is optional; it adds a bypass between the supplies, which may improve distortion performance for some models.



(a) Top Layer, Top View

(b) Mid Layer 1, Top View

(c) Mid Layer 2, Top View

(d) Bottom Layer, Bottom View

(1) The board name shown in the silkscreen is DEM-OPA269xD with the Burr-Brown Revision 1 design finalized in September 2004.

Figure 3. DEM-OPA-SO-2B Demonstration Fixture Layout

4 Board Layout

This demonstration fixture is a four-layer PCB (see Figure 3). The top layer has power traces and signal traces. The bottom layer has signal traces only. Both inner layers have ground planes to have impedance matching with signal traces on top and bottom layers. The ground plane has been opened up around op amp pins sensitive to capacitive loading. Power-supply traces are laid out to keep current loop areas to a minimum. Mount the SMA (or SMB) vertically. The location and type of capacitors used for power-supply bypassing are crucial for high-frequency amplifiers. The tantalum capacitors, C_4 and C_5, do not need to be as close to pins 4 and 8 on the PCB and may be shared with other amplifiers. See the individual op amp data sheet for more information on component selection.

5 Measurement Tips

This demonstration fixture, and the component values shown, is designed to operate in a 50Ω environment; most data sheet plots are obtained under these conditions. It is easy to change the component values for different input and output impedance levels. However, do not use high-impedance probes; they represent a heavy capacitive load to the op amp, and will alter the amplifier response. Instead, use low-impedance (≤ 500Ω) probes with adequate bandwidth. The probe input capacitance and resistance set an upper limit on the measurement bandwidth. If a high-impedance probe must be used, place a 100Ω resistor on the probe tip to isolate its capacitance from the circuit.

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