

Applications

- Repeaters
- Mobile Infrastructure
- Defense Communications
- General Purpose Wireless
- TDD or FDD systems

Product Features

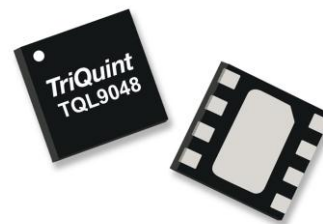
- 50-4000 MHz Operational Bandwidth
- Medium 15 dB gain
- High linearity, +40.5 dBm Output IP3
- Unconditionally stable
- Integrated on-chip matching, 50 ohm in/out
- Integrated active bias
- Integrated shutdown control pin

General Description

The TQL9048 is a cascadable, high linearity gain block amplifier in a low-cost surface-mount package. At 1.9 GHz, the amplifier typically provides 14.5 dB gain, +40.5 dBm OIP3, and 1.7 dB Noise Figure while only drawing 130 mA current. The device is housed in a very small 2x2 mm package.

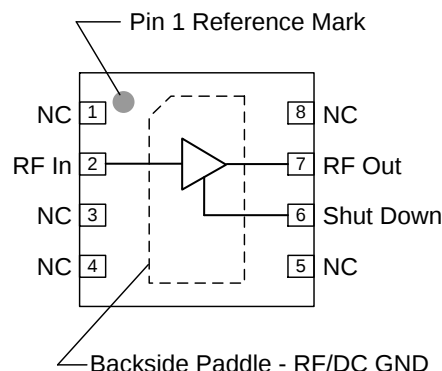
The TQL9048 has good noise figure and high linearity performance allowing the device to be used in both receiver and transmitter chains for high performance systems. The gain block is internally matched using a high performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias to maintain high performance over temperature and integrates a shut-down biasing capability to allow for operation for TDD applications.

The TQL9048 covers the 50-4000 MHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.



8 pin 2x2 mm DFN Package

Functional Block Diagram



Pin Configuration

Pin No.	Label
1, 3, 4, 5, 8	NC
2	RF In
6	Shut Down
7	RF Out
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
TQL9048	High Linearity Gain Block
TQL9048-PCB_RF	0.7-2.7 GHz Evaluation Board
TQL9048-PCB_IF	50-500 MHz Evaluation Board

Standard T/R size = 2500 pieces on a 7" reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150°C
Supply Voltage (V_{DD})	7 V
RF Input Power, CW, 50Ω, T=25°C	+20 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})		5.0	5.25	V
T_{CASE}	-40		+85	°C
Tj for >10 ⁶ hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5V, Temp = +25°C, 50 Ω system.

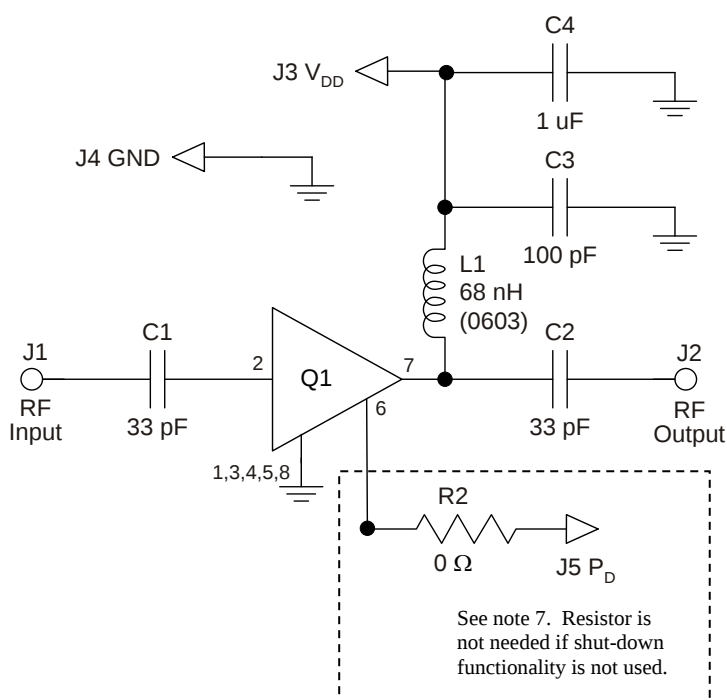
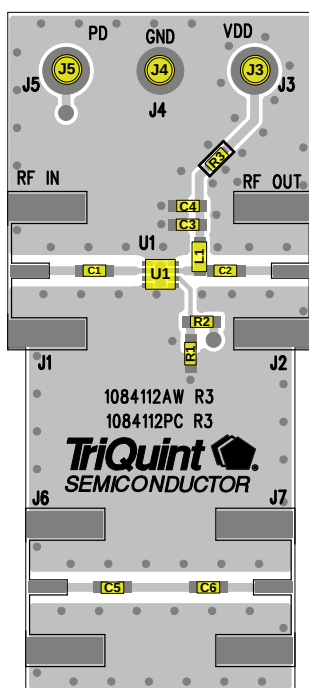
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		50		4000	MHz
Test Frequency			1900		MHz
Gain		13	14.5	16	dB
Input Return Loss			-10		dB
Output Return Loss			-13		dB
Noise Figure			1.7		dB
Output P1dB		+20	+22		dBm
Output IP3	Pout = +6 dBm/tone, Δf = 1 MHz	+36	+40.5		dBm
Power Shutdown Control (Pin 6)	On state	0		0.5	V
	Off state (Power down)	1.4		5	V
Current, I_{DD}	On state		130	160	mA
	Off state (Power down)		3	5	mA
Shutdown pin current, I_{SD}	$V_{PD} \geq 1.4$ V		15		μA
Thermal Resistance, θ_{jc}	channel to case			35.4	°C/W

S-Parameters

Test Conditions: $V_{DD}=+5$ V, $I_{DD}=130$ mA (typ.), $T=+25^{\circ}\text{C}$, unmatched 50 ohm system, calibrated to device leads

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.05	-14.2	-100.9	17.9	163.5	-20.4	10.9	-14.8	-62.9
0.1	-18.0	-132.2	17.1	163.6	-20.1	3.4	-16.3	-159.5
0.2	-19.9	-159.3	16.8	158.9	-20.0	-1.9	-16.4	174.8
0.3	-20.6	-172.6	16.6	151.9	-20.0	-5.4	-16.5	158.1
0.4	-21.5	-179.0	16.6	144.3	-19.9	-8.4	-16.9	144.0
0.5	-22.8	175.2	16.5	136.6	-19.9	-11.2	-17.2	132.5
0.6	-24.0	172.6	16.4	128.7	-19.8	-14.0	-17.6	121.5
0.7	-25.8	172.4	16.2	120.9	-19.8	-16.8	-18.0	110.5
0.8	-27.7	175.0	16.1	113.1	-19.8	-19.6	-18.5	99.2
0.9	-30.2	-177.2	16.0	105.4	-19.7	-22.6	-19.1	88.6
1	-32.3	-158.5	15.9	97.7	-19.7	-25.5	-19.8	77.5
1.1	-32.6	-130.3	15.8	90.0	-19.7	-28.5	-20.7	66.4
1.2	-30.7	-107.2	15.6	82.3	-19.6	-31.4	-21.7	54.2
1.3	-28.4	-96.0	15.5	74.7	-19.6	-34.6	-22.8	40.6
1.4	-26.1	-91.0	15.4	67.2	-19.6	-37.6	-24.2	25.6
1.5	-24.3	-89.7	15.2	59.6	-19.5	-40.8	-25.7	6.4
1.6	-22.9	-89.8	15.1	52.1	-19.5	-44.0	-26.8	-16.8
1.7	-21.7	-91.2	15.0	44.6	-19.5	-47.3	-27.2	-43.2
1.8	-20.8	-92.9	14.9	37.1	-19.5	-50.6	-26.6	-70.0
1.9	-20.0	-95.1	14.8	29.7	-19.4	-53.9	-25.3	-92.9
2	-19.4	-97.8	14.6	22.1	-19.4	-57.3	-23.7	-111.4
2.1	-18.9	-100.2	14.5	14.6	-19.4	-60.7	-22.1	-125.7
2.2	-18.5	-103.2	14.4	7.0	-19.4	-64.3	-20.8	-138.8
2.3	-18.3	-105.8	14.3	-0.6	-19.3	-67.8	-19.6	-150.3
2.4	-18.2	-108.3	14.2	-8.3	-19.3	-71.5	-18.6	-160.3
2.5	-18.1	-110.3	14.1	-16.1	-19.2	-75.3	-17.7	-170.6
2.6	-18.2	-112.0	14.0	-24.0	-19.2	-79.1	-16.9	179.8
2.7	-18.2	-113.2	14.0	-31.9	-19.1	-83.0	-16.2	170.2
2.8	-18.3	-114.1	13.9	-40.0	-19.1	-87.1	-15.5	160.9
2.9	-18.4	-113.9	13.8	-48.3	-19.0	-91.3	-14.9	151.5
3	-18.5	-113.1	13.6	-56.7	-19.0	-95.6	-14.3	141.8
3.1	-18.4	-111.2	13.5	-65.3	-18.9	-100.2	-13.8	132.1
3.2	-18.1	-108.3	13.4	-74.0	-18.8	-104.9	-13.3	122.4
3.3	-17.6	-105.6	13.3	-83.0	-18.8	-109.8	-12.9	112.7
3.4	-16.8	-103.6	13.1	-92.1	-18.7	-114.9	-12.5	102.4
3.5	-15.8	-102.9	12.9	-101.4	-18.7	-120.3	-12.2	92.3
3.6	-14.6	-103.0	12.6	-110.9	-18.6	-125.8	-11.9	81.7
3.8	-12.2	-107.2	12.1	-130.3	-18.6	-137.6	-11.5	59.7
4	-9.8	-115.5	11.3	-150.3	-18.7	-150.3	-11.4	36.5

TQL9048-PCB Evaluation Board



Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. R3 (0 Ω jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. C1 is a critical parameter that effects switching speed. Smaller capacitor values will give quicker response.
5. C2, and C3 are non-critical values. The reactive impedance should be as low as possible at the frequency of operation for optimal performance.
6. The L1 value is non-critical and needs to provide high reactive impedance at the frequency of operation.
7. R2 is optional and do not need to be loaded if the shut-down functionality is not needed; i.e. FDD applications. If R2 is not loaded, the LNA will operate in its standard "ON" state.
8. A through line is included on the evaluation board to de-embed the board losses.

Bill of Material – TQL9048-PCB_RF

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	TriQuint	N/A
U1	N/A	High Linearity Gain Block	TriQuint	TQL9048
R1	N/A	Do not load	N/A	N/A
R2	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
L1	68 nH	Inductor, 0603, 5%, Ceramic	various	various
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	various
C1, C2, C5, C6	33 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	various	various
C3	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	Various	various

Typical Performance – TQL9048-PCB_RF

Test conditions unless otherwise noted: $V_{DD} = +5V$, $I_{DD} = 130$ mA (typ.), Temp = +25°C

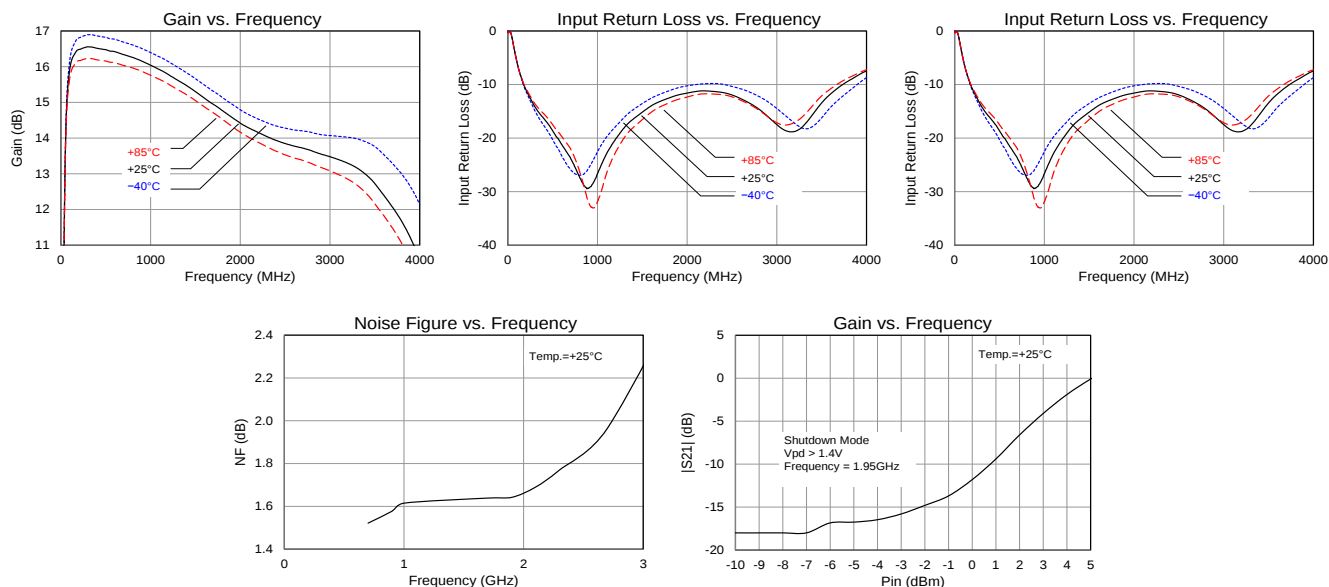
Parameter	Conditions	Typical Values				Units
Frequency		900	1950	2700	3500	MHz
Gain		16	14.5	13.5	12.7	dB
Input Return Loss		-28	-11	-12	-12	dB
Output Return Loss		-20	-13	-16	-12	dB
Output P1dB		+22.4	+22.4	+21.9	+19.8	dBm
OIP3	Pout = +6 dBm/tone, $\Delta f = 1$ MHz	+41	+40.5	+40	+37.5	dBm
Noise figure ⁽¹⁾		1.6	1.7	1.9	2.8	dB

Notes:

- Noise figure data shown in the table above is de-embedded from the eval board loss.

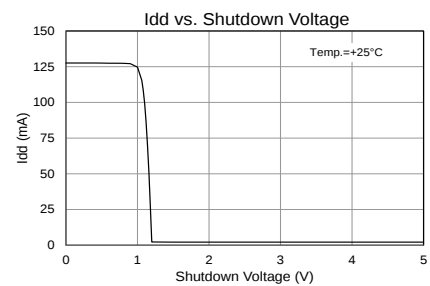
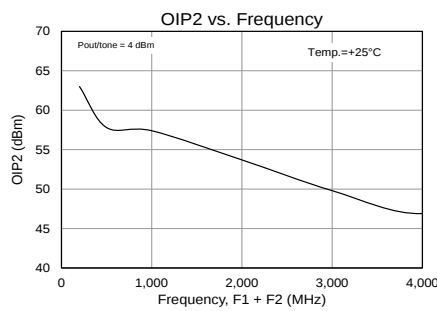
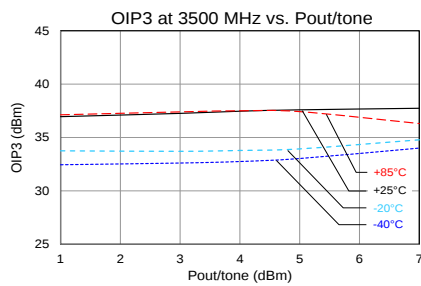
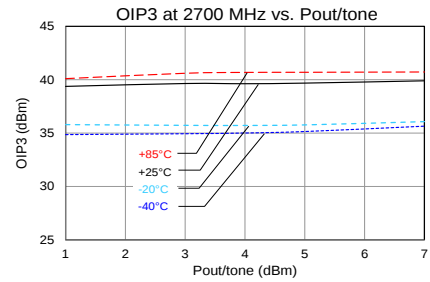
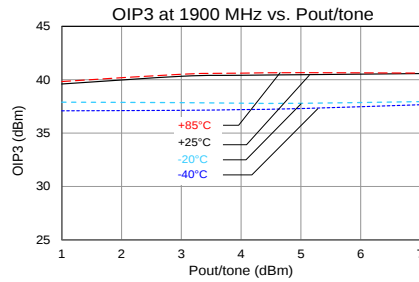
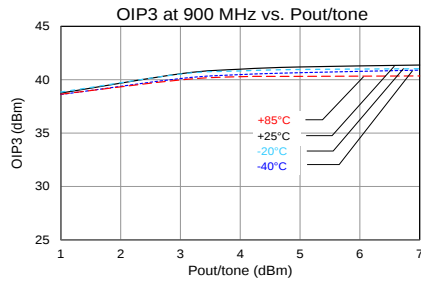
Performance Plots – TQL9048-PCB_RF

Test conditions unless otherwise noted: $V_{DD} = +5V$, $I_{DD} = 130$ mA (typ.), Temp = +25°C



Performance Plots – TQL9048-PCB_RF (continued)

Test conditions unless otherwise noted: $V_{DD} = +5V$, $I_{DD} = 130\text{ mA}$ (typ.), Temp = $+25^{\circ}C$



Typical Performance – TQL9048-PCB_IF

Test conditions unless otherwise noted: $V_{DD} = +5V$, $I_{DD} = 130$ mA (typ.), Temp = +25°C, C1 and C2 = 1000 pF, L1 = 330 nH

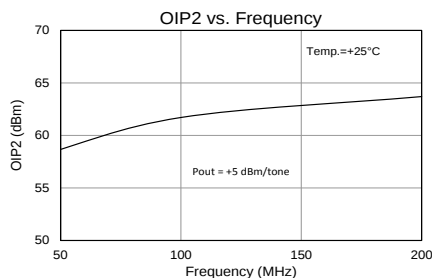
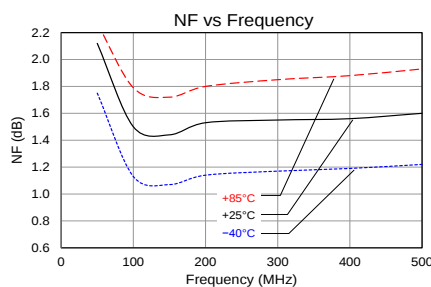
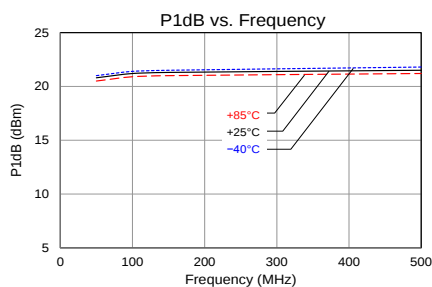
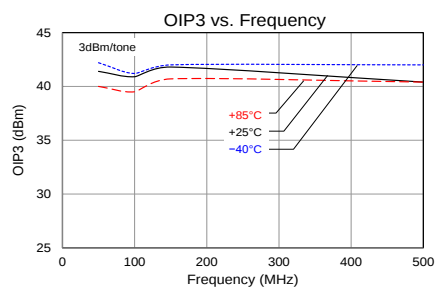
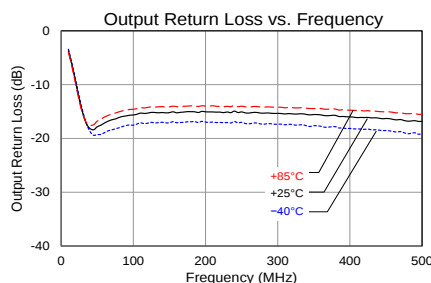
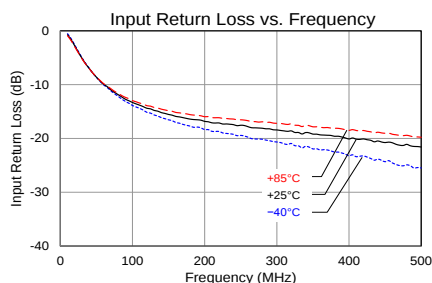
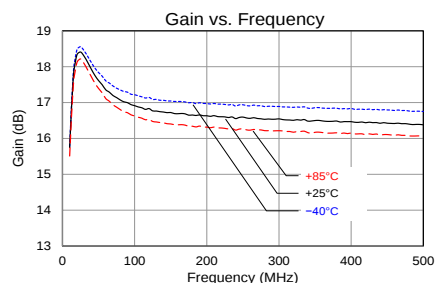
Parameter	Conditions	Typical Values				Units
Frequency		50	100	150	500	MHz
Gain		17.5	16.9	16.7	16.3	dB
Input Return Loss		-8	-13	-12	-20	dB
Output Return Loss		-18	-17	-17	-17	dB
Output P1dB		+20.8	+21.2	+21.3	+21.5	dBm
OIP3	Pout = +6 dBm/tone, $\Delta f = 1$ MHz	+41.4	+40.9	+41.8	+40.4	dBm
Noise figure ⁽¹⁾		2.1	1.5	1.5	1.6	dB

Notes:

- Noise figure data shown in the table above is de-embedded from the eval board loss.

Performance Plots – TQL9048-PCB_IF

Test conditions unless otherwise noted: $V_{DD} = +5V$, $I_{DD} = 130$ mA (typ.), Temp = +25°C, C1 and C2 = 1000 pF, L1 = 330 nH

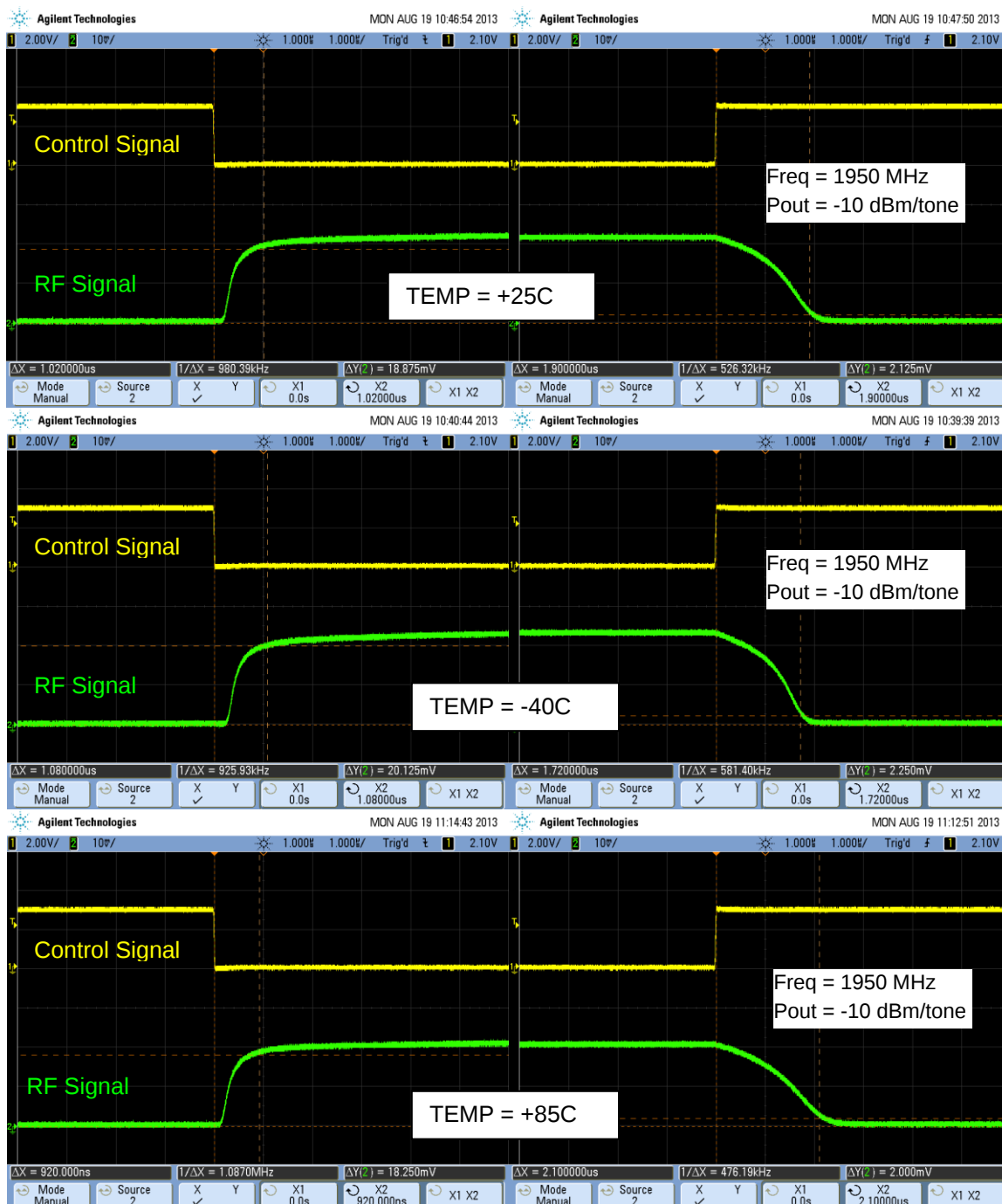


Switching Speed

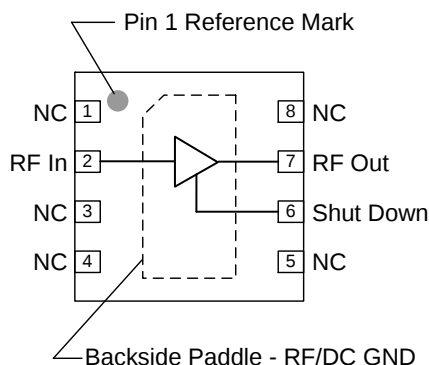
Switching Speed Measurement based on TQS Application Board

Using Shutdown Circuit: $V_{PD}=3V$, $V_{DD}=5V$

Parameter	-40C	+25C	+85C
Turn-off Transition (50% CNTR – 10% RF)	1.72 μs	1.90 μs	2.10 μs
Turn-on Transition (50% CNTR – 90% RF)	1.08 μs	1.02 μs	0.92 μs



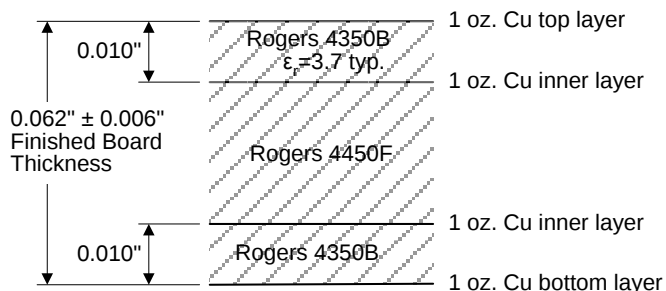
Pin Configuration and Description



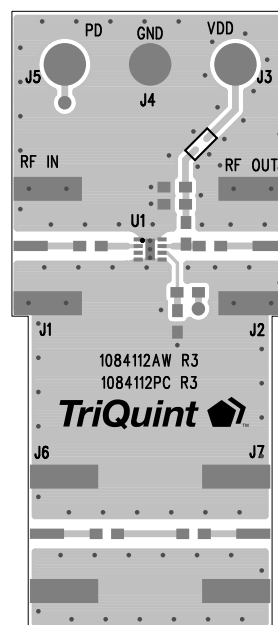
Pin No.	Label	Description
2	RF In	RF Input pin. A DC Block is required.
6	Shut Down	A high voltage turns off the device. If the pin is not connected or is less than 0.5V, then the device will operate under its normal operating condition.
7	RF Out	RF Output pin. DC bias will also need to be injected through a RF bias choke/inductor for operation.
1, 3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

TriQuint PCB 1084112 Material and Stack-up



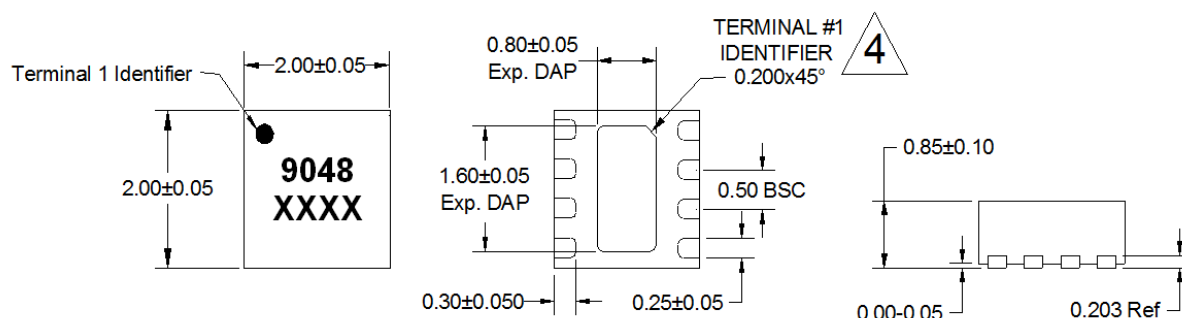
50 ohm line dimensions: width = 0.020", spacing = 0.032"



Mechanical Information

Package Marking and Dimensions

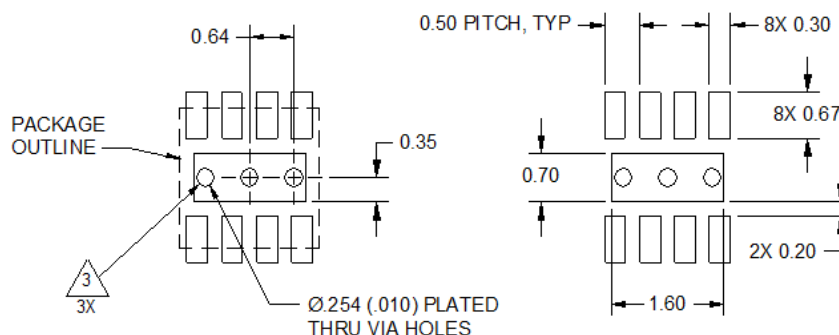
Marking: Part number – 9048
Lot code – XXXX



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35 mm ($\#80/.0135$ ") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10 ").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: Passes ≥ 250 V to < 500 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: Passes 1000 V to < 2000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 1
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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