1.8-V MICROPOWER CMOS OPERATIONAL AMPLIFIERS ZERO-DRIFT SERIES

FEATURES

- Low Offset Voltage: 23 μV (Max)
- 0.01-Hz to 10-Hz Noise: 1.1 μV_{PP}
- Quiescent Current: 17 μA
- Single-Supply Operation
- Supply Voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input/Output
- MicroSize Packages: SC70 and SOT23

APPLICATIONS

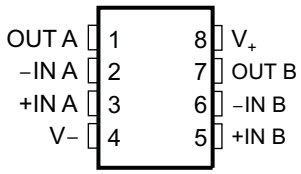
- Transducer Applications
- Temperature Measurements
- Electronic Scales
- Medical Instrumentation
- Battery-Powered Instruments
- Handheld Test Equipment

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (–55°C/125°C) Temperature Range(1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

(1) Custom temperature ranges available

D PACKAGE
(TOP VIEW)



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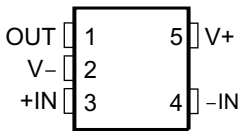
(TOP VIEW)



DCK PACKAGE
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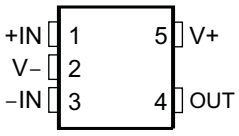
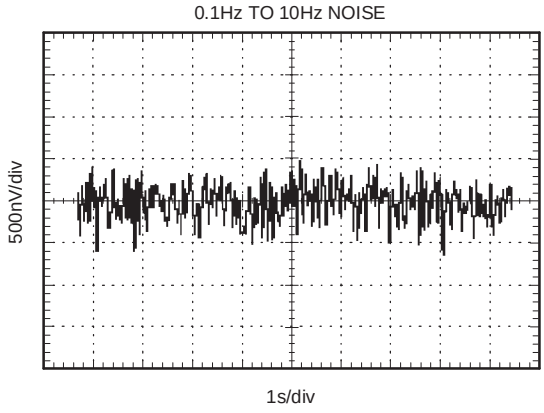




DESCRIPTION/ORDERING INFORMATION

The OPA333A series of CMOS operational amplifiers uses a proprietary auto-calibration technique to simultaneously provide very low offset voltage (10 μV max) and near-zero drift over time and temperature. These miniature, high-precision, low-quiescent-current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 50 mV of the rails. Single or dual supplies as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V) may be used. They are optimized for low-voltage single-supply operation.

The OPA333A family offers excellent common-mode rejection ratio (CMRR) without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

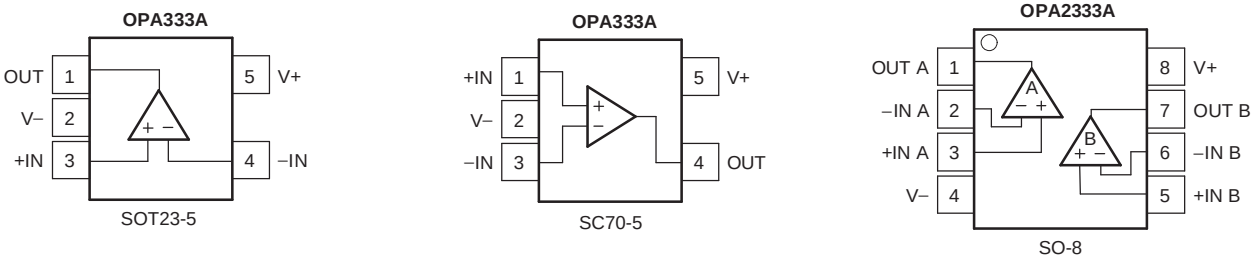
The OPA333A (single version) is available in the SC70-5 and SOT23-5 packages. The OPA2333A (dual version) is offered in the SO-8 package. All versions are specified for operation from –55°C to 125°C.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING(2)
OPA333AMDBVREP	SOT23-5	DBV	OBYM
OPA333AMDCKREP	SC70-5	DCK	CHQ
OPA2333AMDREP	SO-8	D	2333EP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PIN CONFIGURATIONS



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage			7	V
Signal input terminals, voltage(2)		–0.3	(V+) + 0.3	V
Output short circuit(3)			Continuous	
Operating temperature range		–55	125	°C
Storage temperature range		–65	150(4)	°C
Junction temperature			150	°C
ESD rating	Human-Body Model (HBM)		4000	V
	Charged-Device Model (CDM)		1000	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short circuit to ground, one amplifier per package
(4) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

Electrical Characteristics: V_S = 1.8 V to 5.5 V

Boldface limits apply over the specified temperature range, **T_A = –55°C to 125°C**. At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}	V_S = 5 V		2	10	µV
over temperature					**22**	**µV**
vs temperature	**dV_{OS}/d_T**			**0.02**		**µV/°C**
vs power supply	**PSRR**	**V_S = 1.8 V to 5.5 V**		**1**	**6**	**µV/V**
Long-term stability(1)				(1)		
Channel separation, dc				0.1		µV/V
INPUT BIAS CURRENT						
Input bias current	I_B			±70	±200	pA
over Temperature				**±150**		**pA**
Input offset current	I_{OS}			±140	±400	pA
NOISE						
Input voltage noise, f = 0.01 Hz to 1 Hz				0.3		$µV_{PP}$
Input voltage noise, f = 0.1 Hz to 10 Hz				1.1		$µV_{PP}$
Input current noise, f = 10 Hz	i_n			100		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common mode voltage range	V_{CM}		(V–) – 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	**(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V**	**102**	**130**		**dB**
INPUT CAPACITANCE						
Differential				2		pF
Common mode				4		pF
OPEN-LOOP GAIN						
Open-loop voltage gain	***A_{OL}***	**(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ**	**104**	**130**		**dB**
FREQUENCY RESPONSE						
Gain-bandwidth product	GBW	C_L = 100 pF		350		kHz
Slew rate	SR	G = 1		0.16		V/µs
OUTPUT						
Voltage output swing from rail		R_L = 10 kΩ		30	50	mV
over temperature		**R_L = 10 kΩ**			**85**	**mV**
Short-circuit current	ISC			±5		mA
Capacitive load drive	CL					
(2)Open-loop output impedance		f = 350 kHz, I_O = 0		2		kΩ
POWER SUPPLY						
Specified voltage range	V_S		1.8		5.5	V
Quiescent current per amplifier	I_Q	I_O = 0		17	25	µA
over temperature					**30**	**µA**
Turn-on time		V_S = 5 V		100		µs
TEMPERATURE RANGE						
Specified range			–55		125	°C

(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV
(2) See Typical Characteristics

Electrical Characteristics: V_S = 1.8 V to 5.5 V (continued)

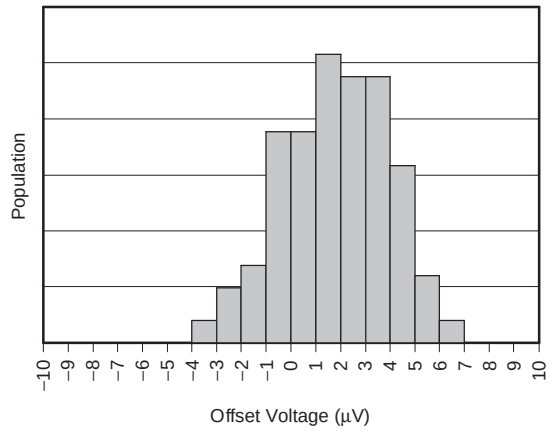
Boldface limits apply over the specified temperature range, **T_A = –55°C to 125°C**. At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating range			–55		125	°C
Storage range			–65		150	°C
Thermal resistance	θ_{JA}					
SOT23-5				200		°C/W
SO-8				150		°C/W
SC70-5				250		°C/W

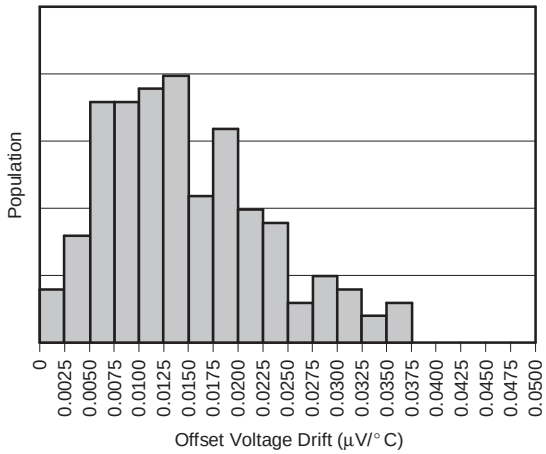
TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted).

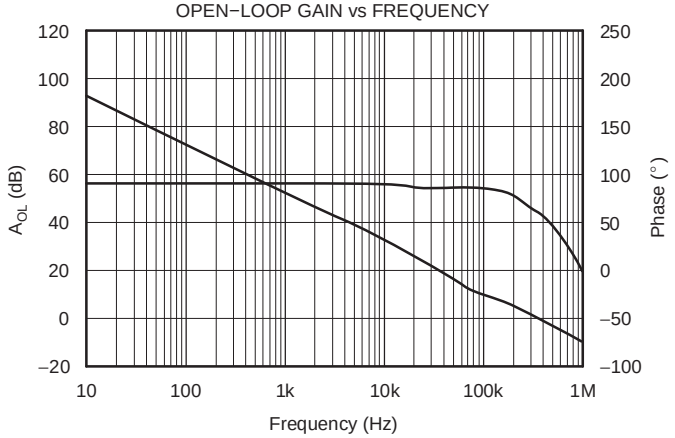
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



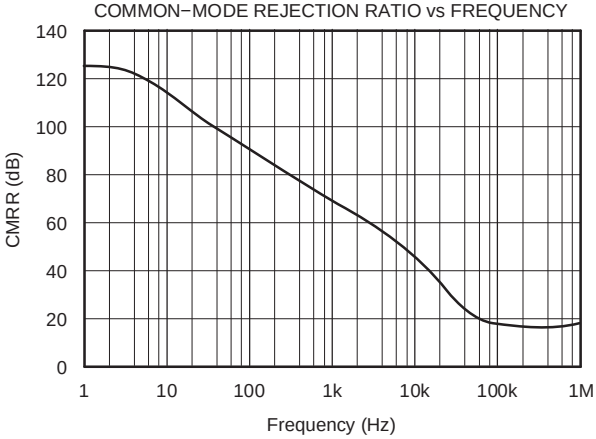
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



OPEN−LOOP GAIN vs FREQUENCY

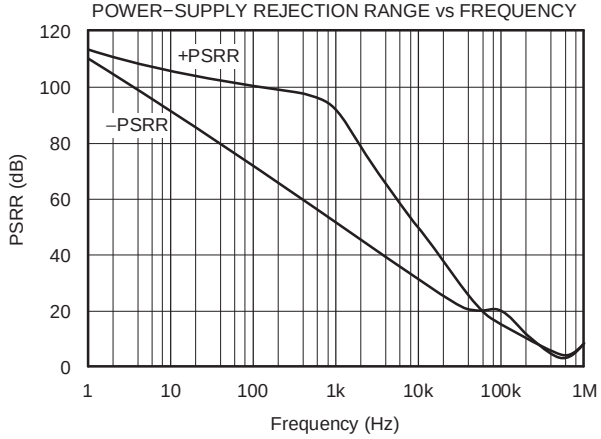


COMMON−MODE REJECTION RATIO vs FREQUENCY

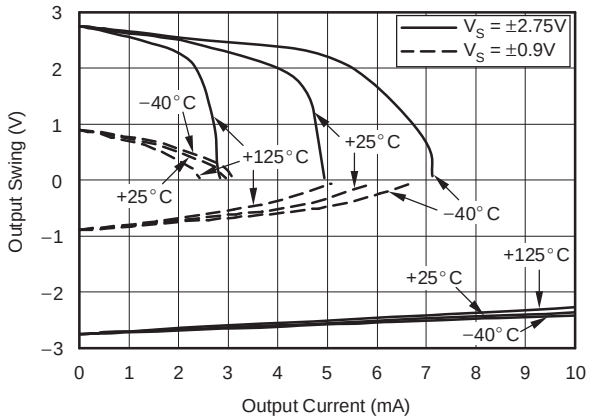


TYPICAL CHARACTERISTICS (continued)

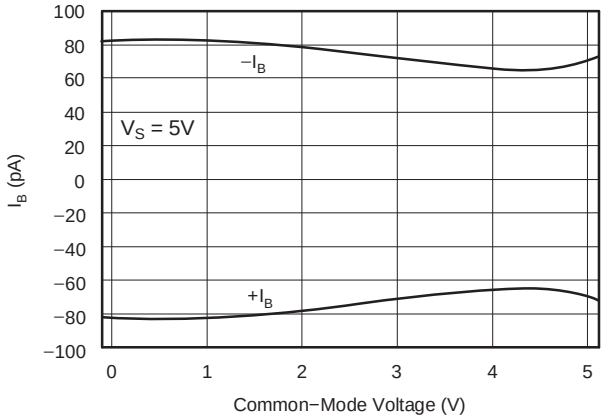
POWER–SUPPLY REJECTION RANGE vs FREQUENCY



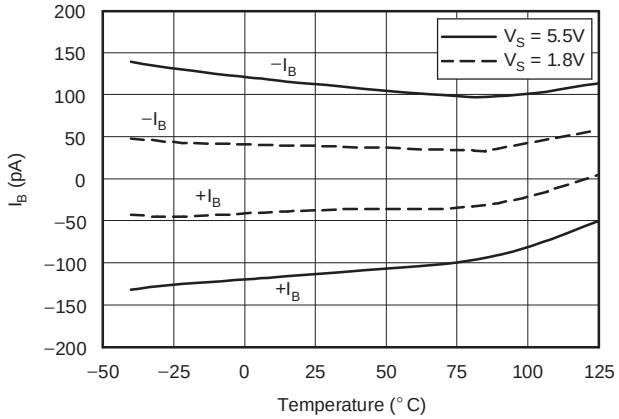
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



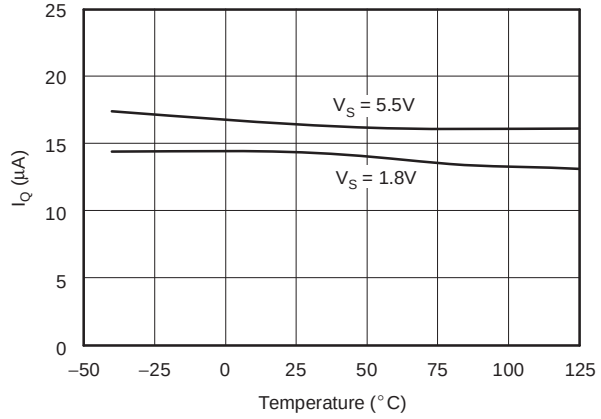
INPUT BIAS CURRENT vs COMMON–MODE VOLTAGE



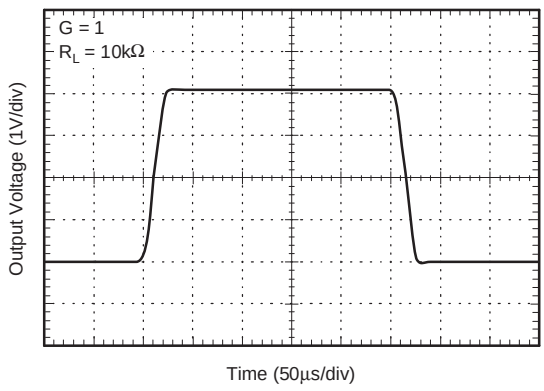
INPUT BIAS CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE

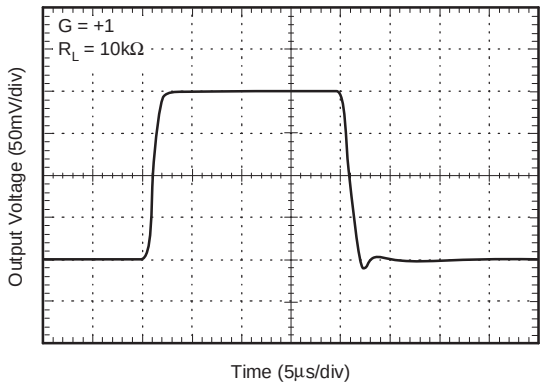


LARGE–SIGNAL STEP RESPONSE

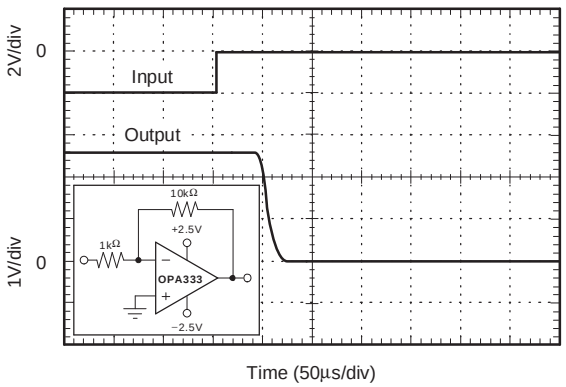


TYPICAL CHARACTERISTICS (continued)

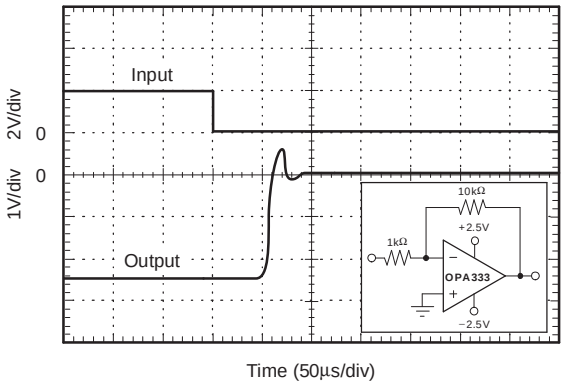
SMALL−SIGNAL STEP RESPONSE



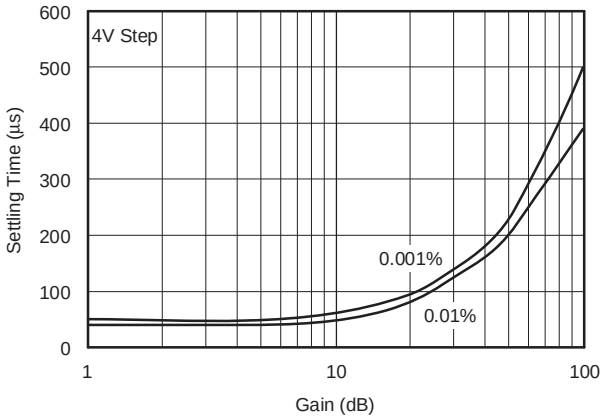
POSITIVE OVER−VOLTAGE RECOVERY



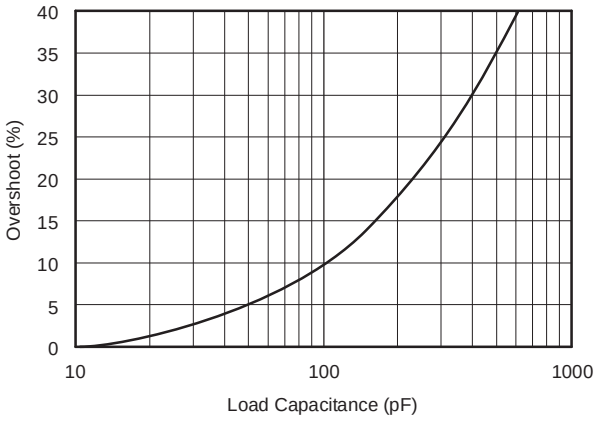
NEGATIVE OVER−VOLTAGE RECOVERY



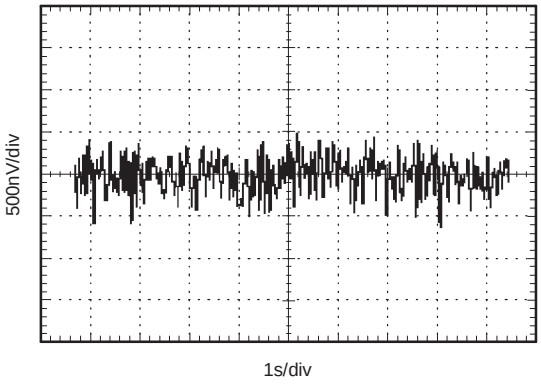
SETTLING TIME vs CLOSED−LOOP GAIN



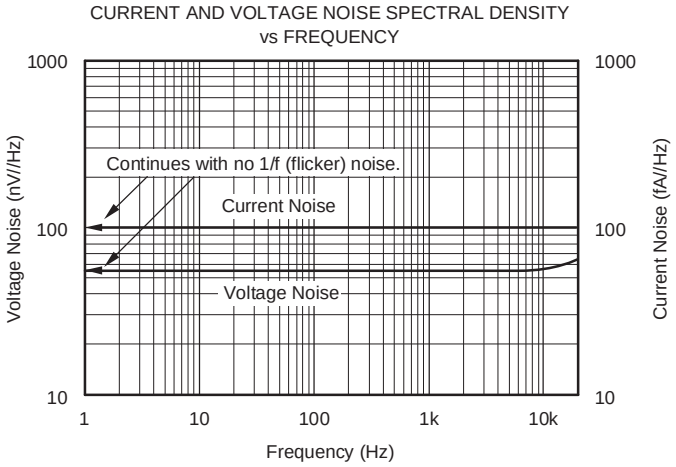
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



0.1Hz TO 10Hz NOISE



TYPICAL CHARACTERISTICS (continued)



APPLICATION INFORMATION

The OPA333A and OPA2333A are unity-gain stable and free from unexpected output phase reversal. They use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by ensuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals)
- Thermally isolate components from power supplies or other heat sources
- Shield op amp and input circuitry from air currents, such as cooling fans

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

Operating Voltage

The OPA333A and OPA2333A op amps operate over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

Input Voltage

The OPA333A and OPA2333A input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA333A is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Normally, input bias current is about 70 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor(see Figure 1).

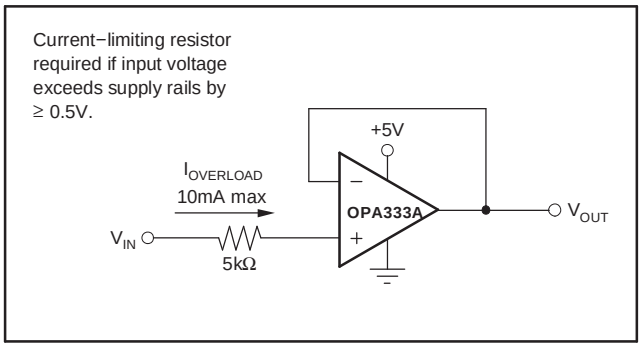


Figure 1. Input Current Protection

Internal Offset Correction

The OPA333A and OPA2333A op amps use an auto-calibration technique with a time-continuous 350-kHz op amp in the signal path. This amplifier is zero corrected every 8 μs using a proprietary technique. Upon power up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA333A and OPA2333A can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve (see Figure 2).

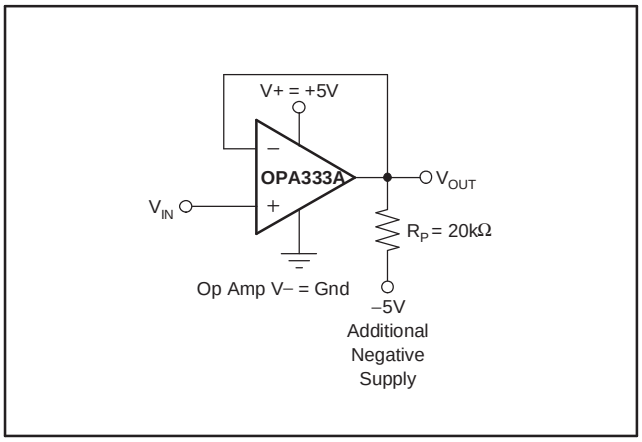


Figure 2. V_{OUT} Range to Ground

The OPA333A and OPA2333A have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA333A and OPA2333A have been characterized to perform with this technique; however, the recommended resistor value is approximately 20 kΩ. Note that this configuration will increase the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occurs below –2 mV, but excellent accuracy returns as the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the op amp to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

General Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in their susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The OPA333A has been specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous-generation devices. Strong RF fields may still cause varying offset levels.

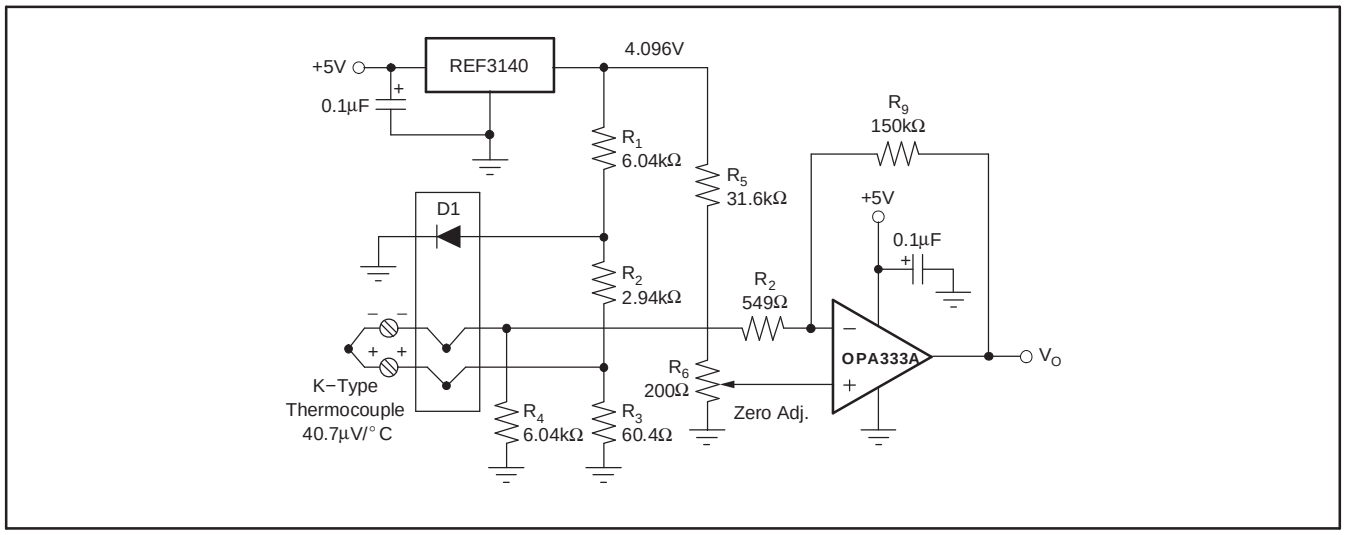


Figure 3. Temperature Measurement

Figure 4 shows the basic configuration for a bridge amplifier.

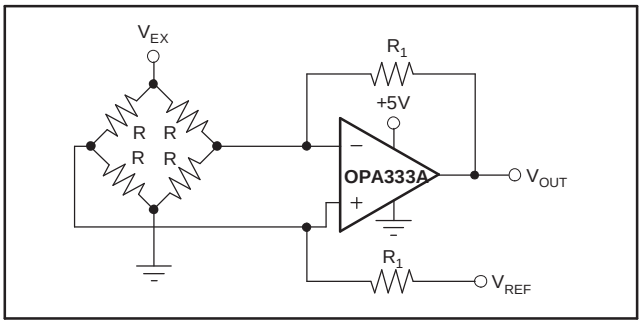


Figure 4. Single Op-Amp Bridge Amplifier

A low-side current shunt monitor is shown in Figure 5. R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. Since the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5-V power supply is sufficiently stable, the REF3130 may be omitted.

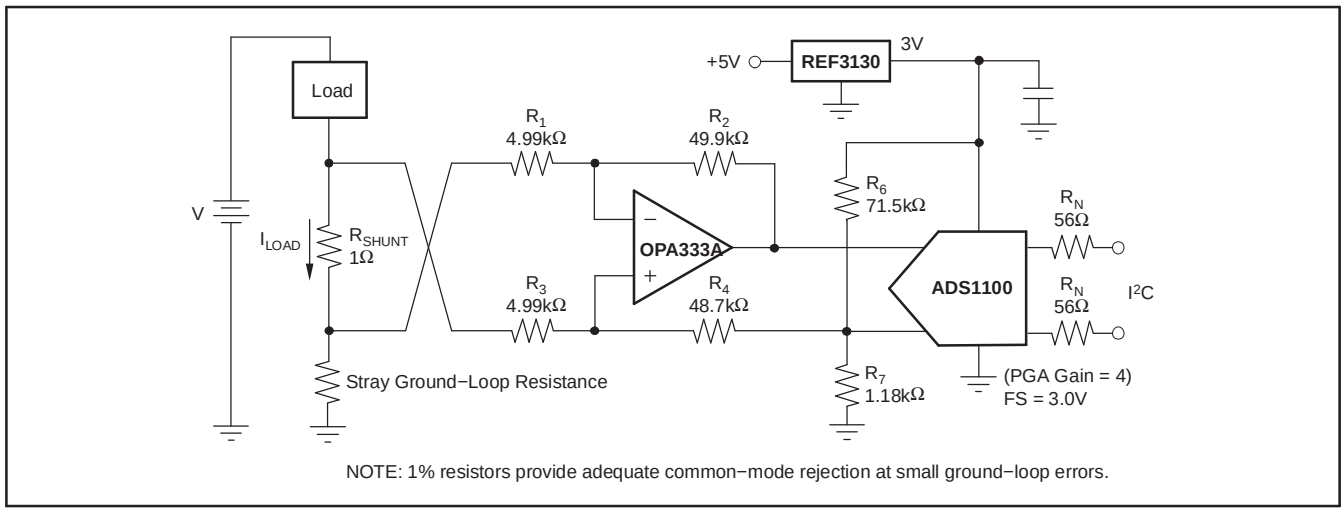


Figure 5. Low-Side Current Monitor

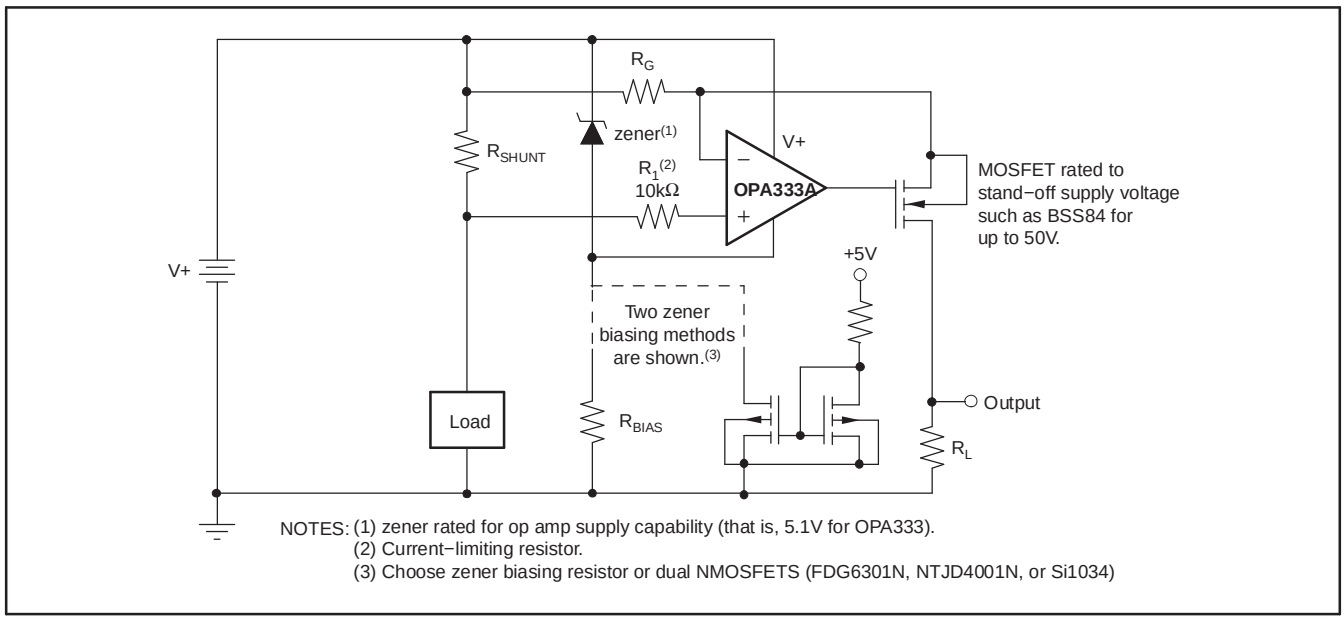


Figure 6. High-Side Current Monitor

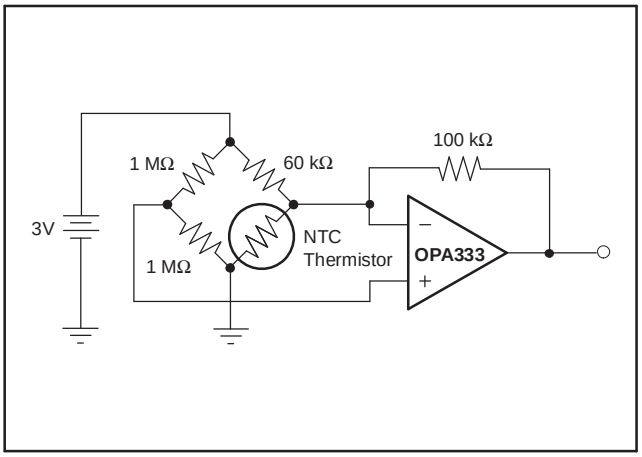


Figure 7. Thermistor Measurement

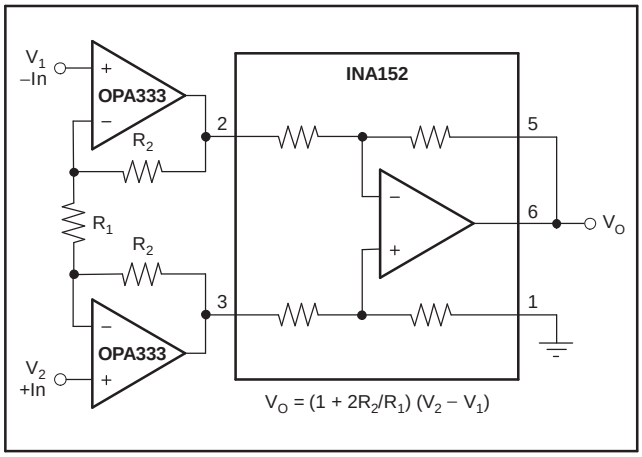


Figure 8. Precision Instrumentation Amplifier

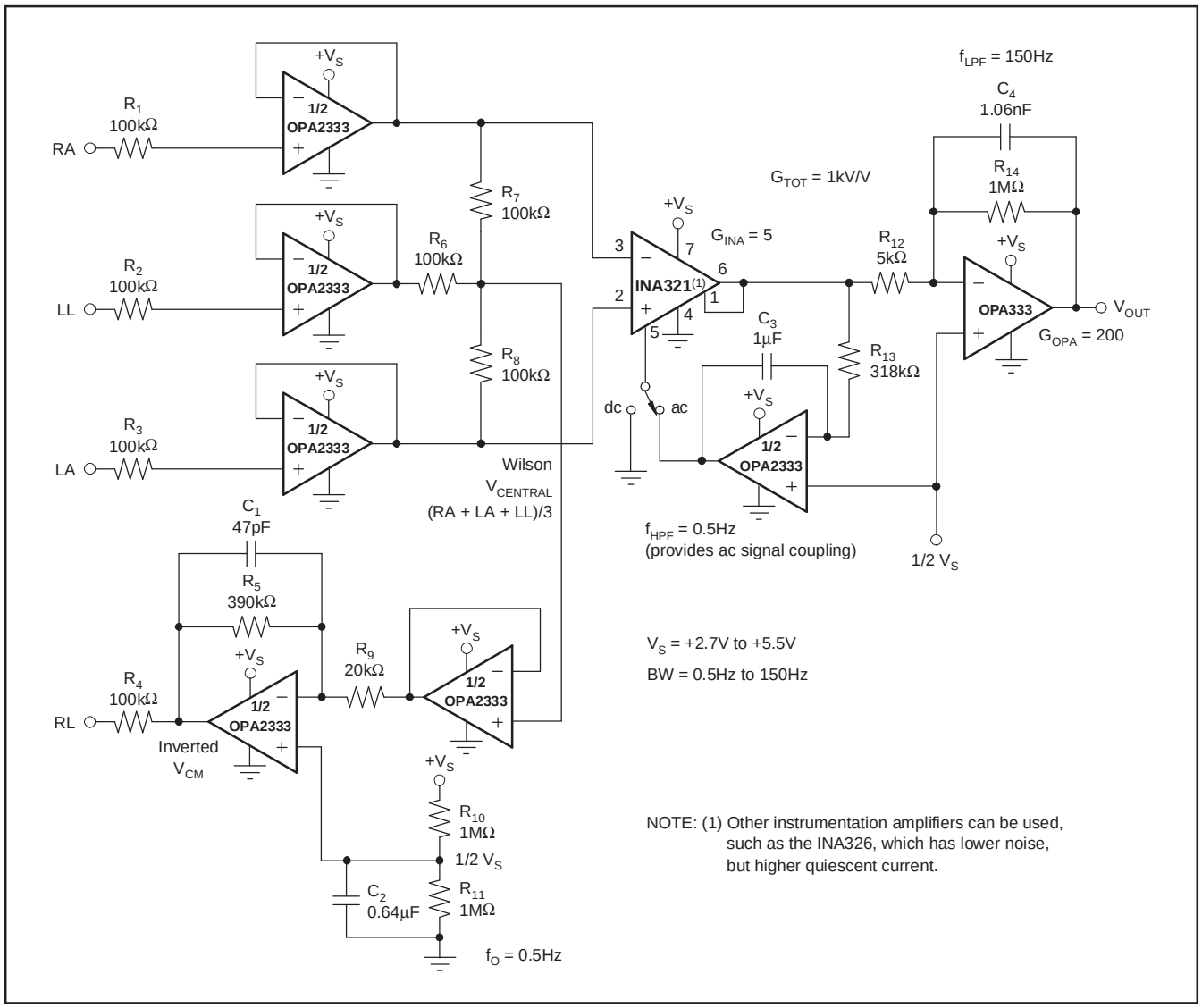


Figure 9. Single-Supply, Very-Low-Power ECG Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2333AMDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2333EP	Samples
OPA2333AMDREPG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2333EP	Samples
OPA333AMDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 0	OBYM	Samples
OPA333AMDCKREP	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 0	CHQ	Samples
V62/07633-01XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	OBYM	Samples
V62/07633-01YE	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 0	CHQ	Samples
V62/07633-02ZE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2333EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

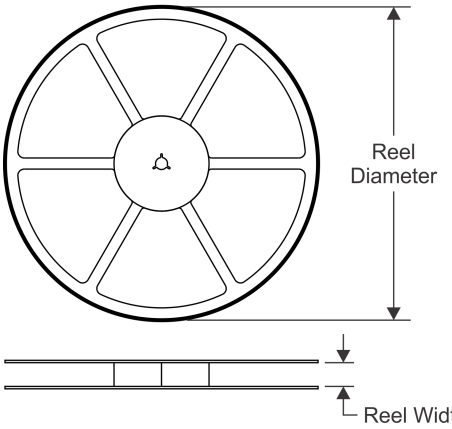
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

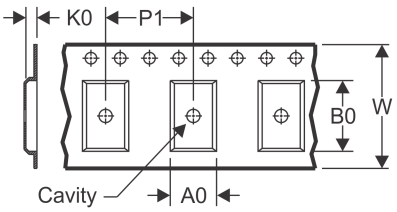
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

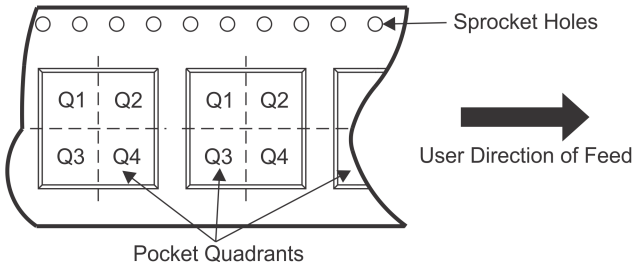


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

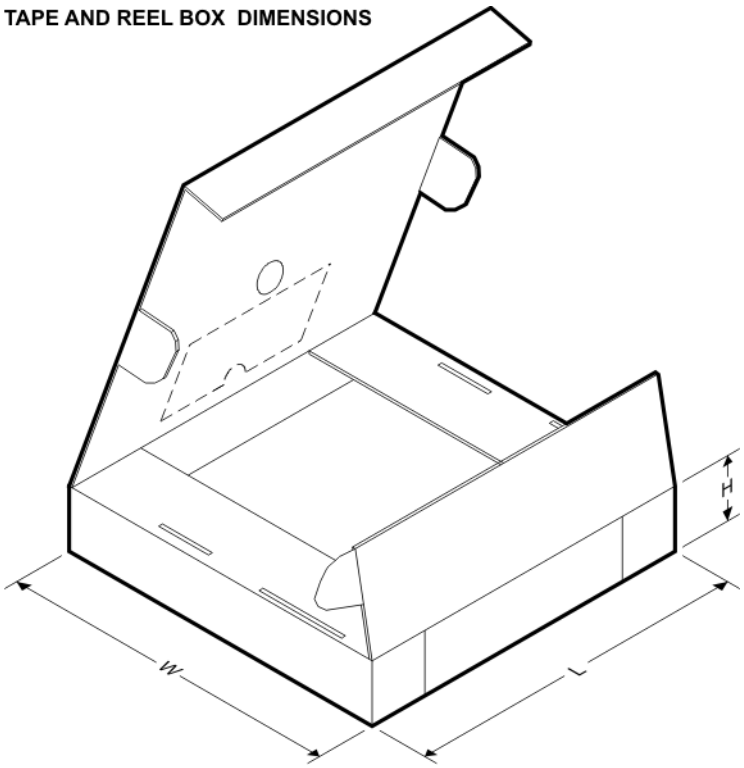
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

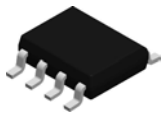
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2333AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA333AMDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA333AMDCKREP	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2333AMDREP	SOIC	D	8	2500	367.0	367.0	35.0
OPA333AMDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA333AMDCKREP	SC70	DCK	5	3000	203.0	203.0	35.0

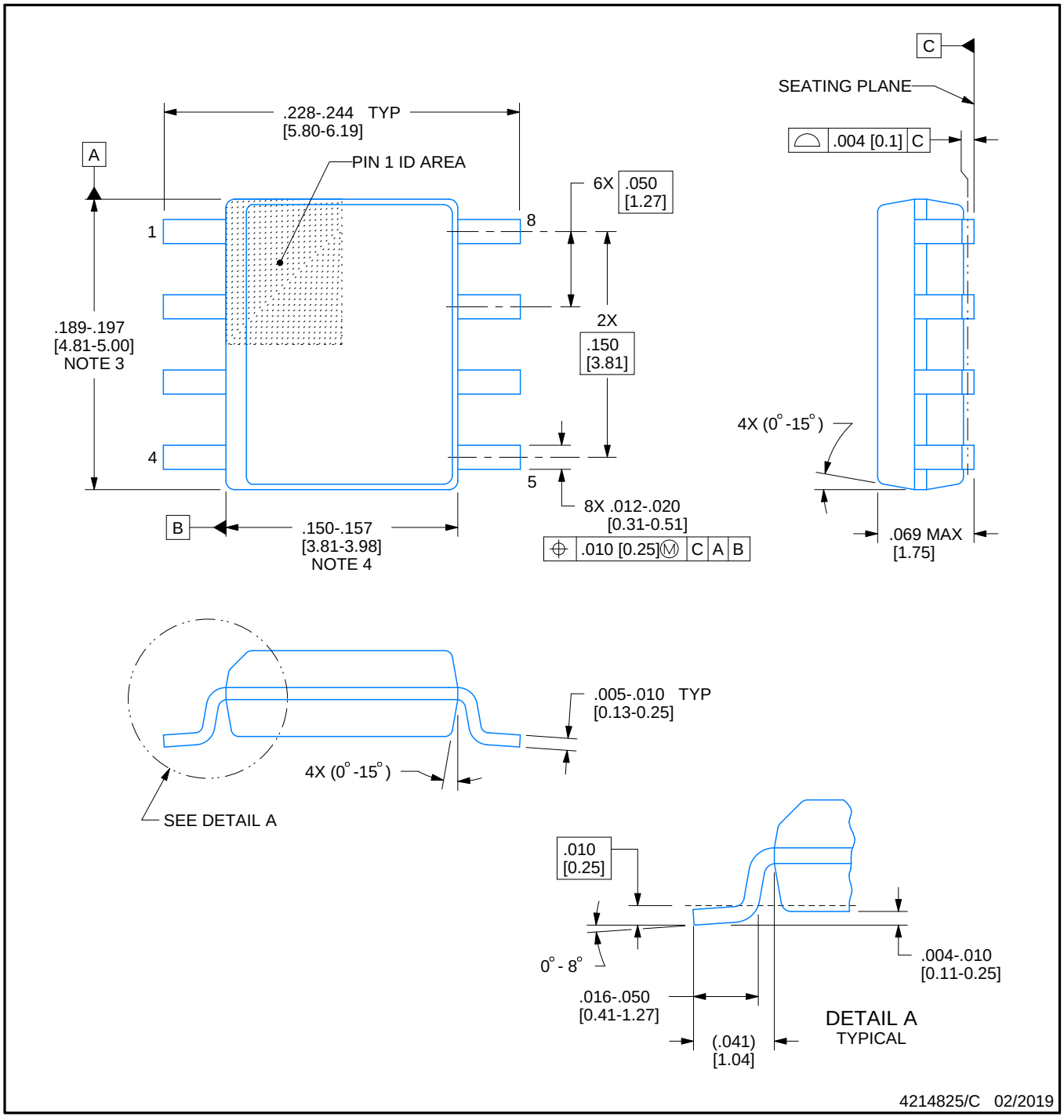


PACKAGE OUTLINE

D0008A

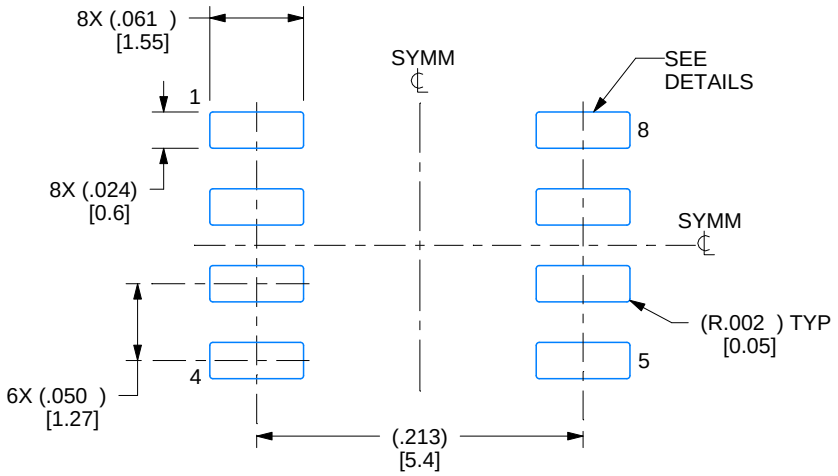
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

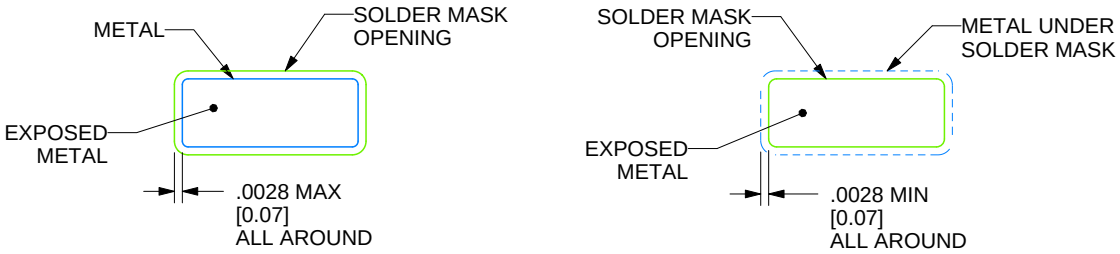


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

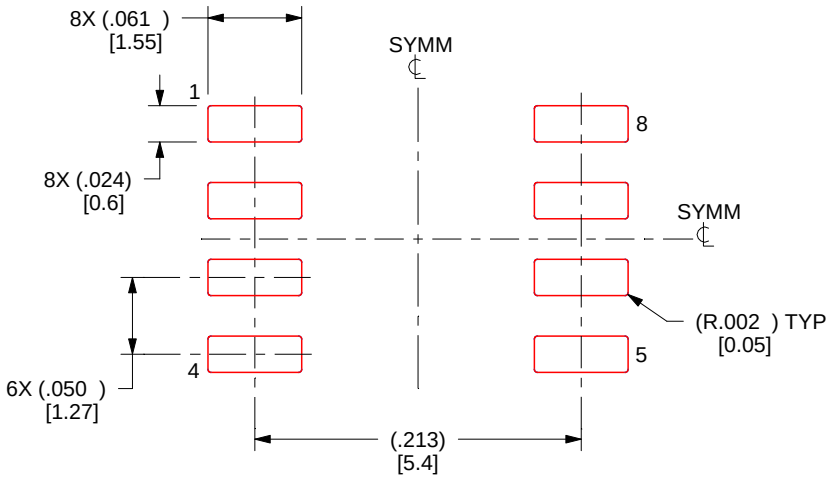
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

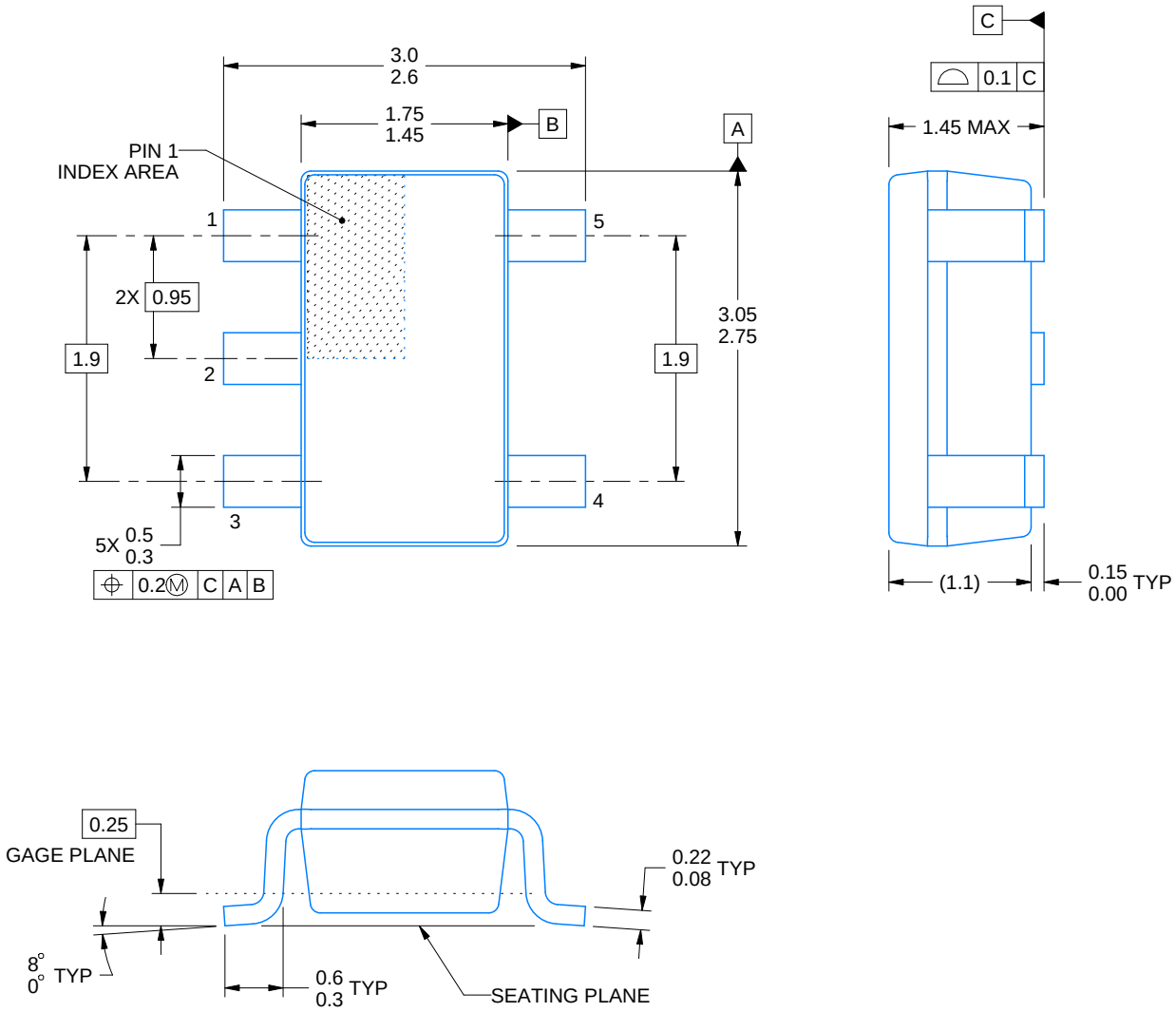
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

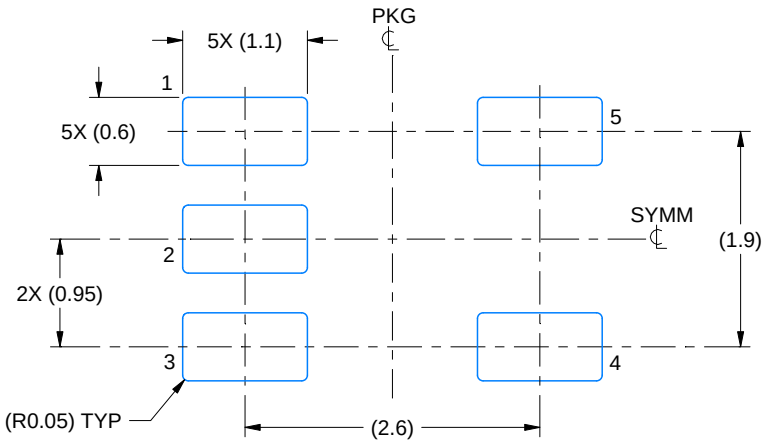
SMALL OUTLINE TRANSISTOR



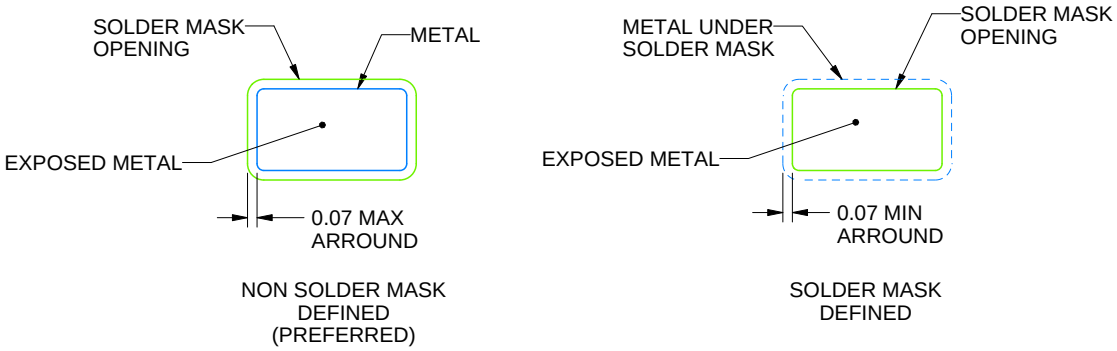
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

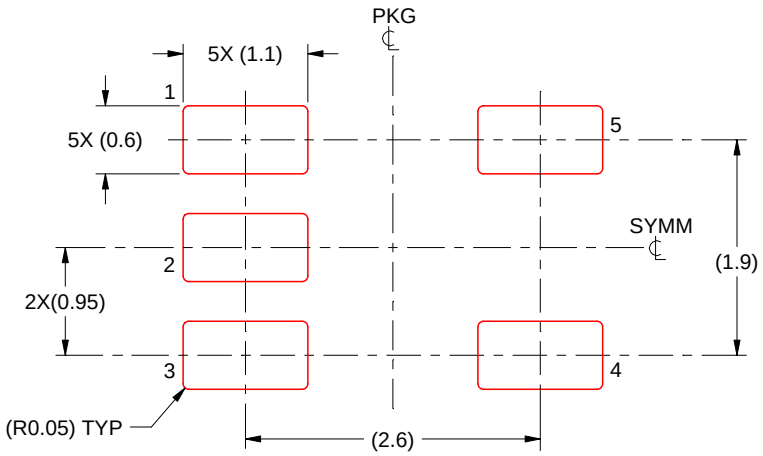


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



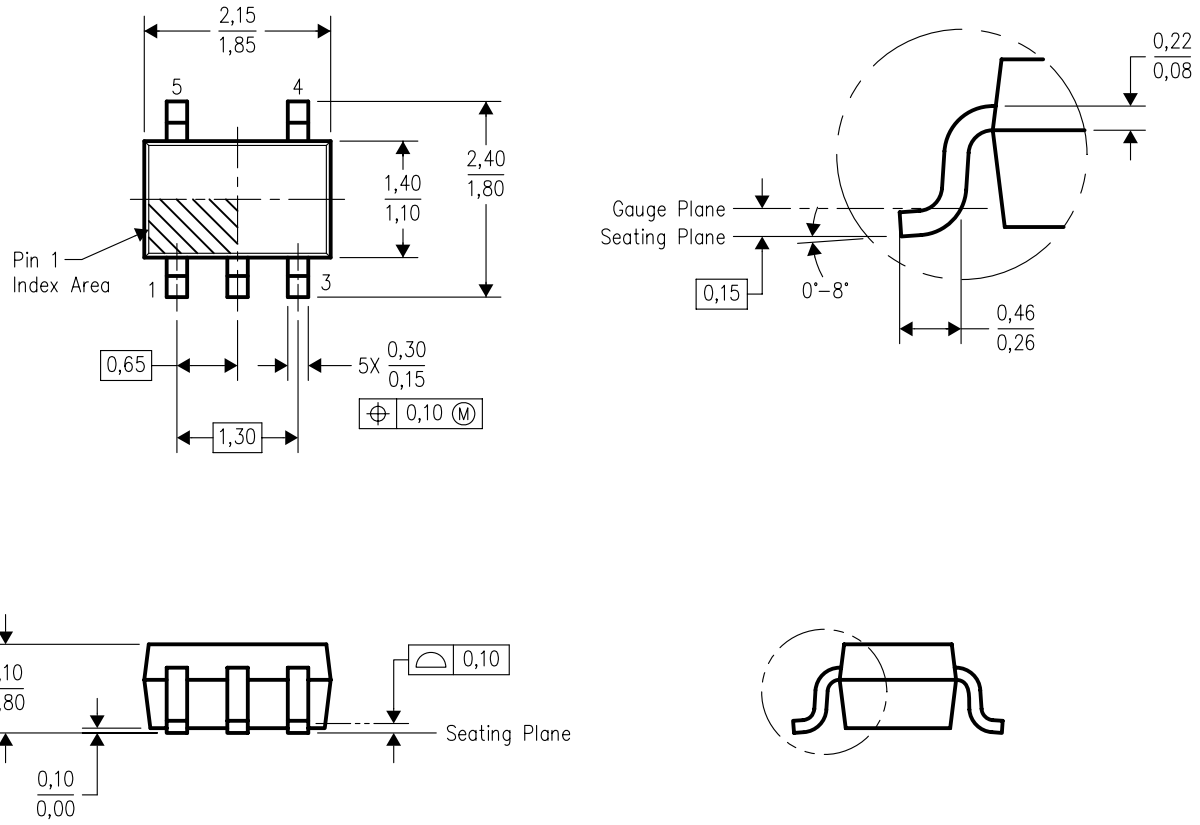
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

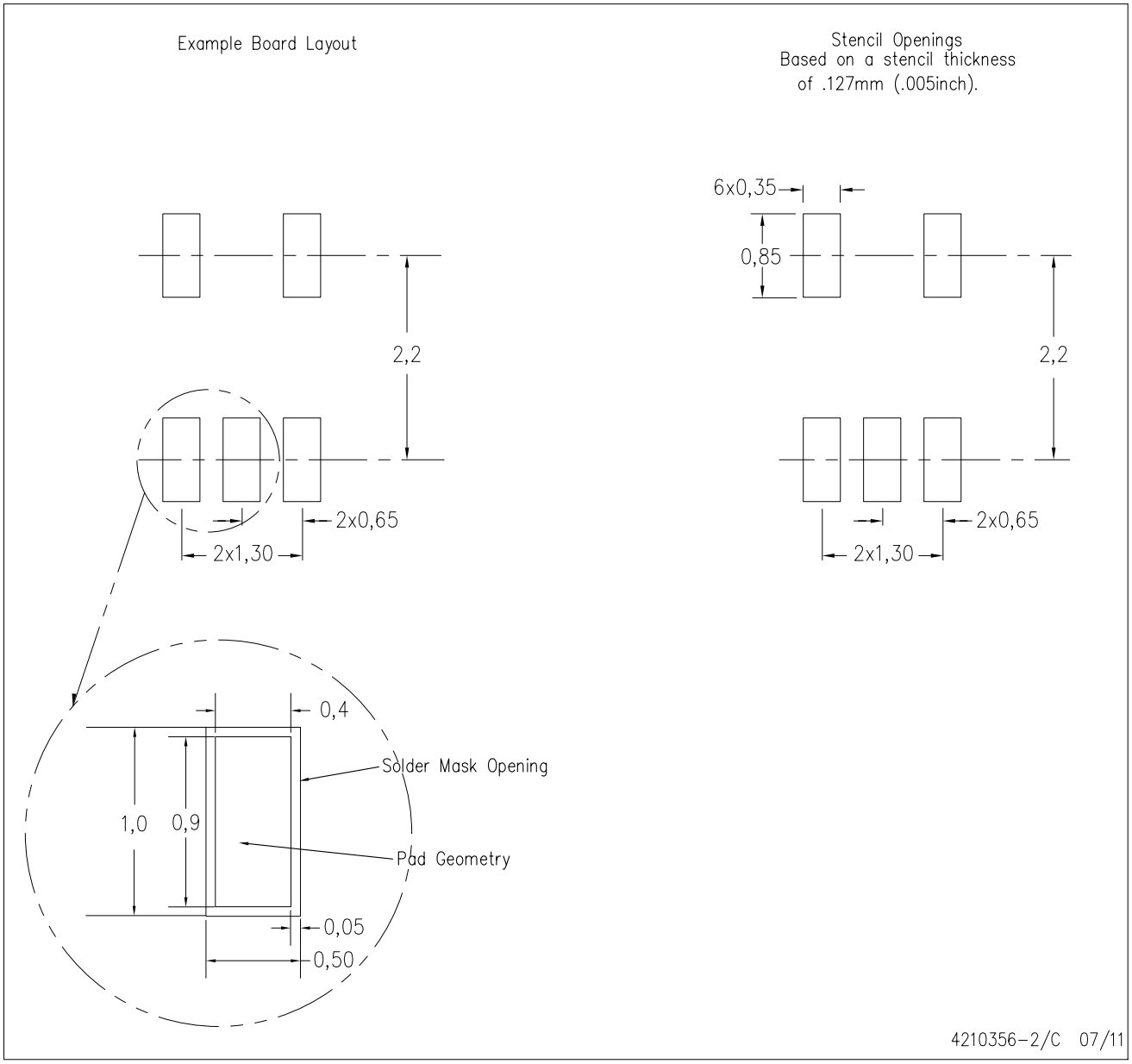
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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