TPS723xx-Q1
200-mA Low-Noise, High-PSRR, Negative-Output, Low-Dropout Linear Regulators

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Ultralow Noise: 60 μV_{RMS} Typical
- High PSRR: 65 dB Typical at 1kHz
- Low Dropout Voltage:
  280 mV Typical at 200 mA, 2.5 V
- Available in –2.5 V and Adjustable
  (–1.2 V to –10 V) Versions
- Stable With a 2.2-µF Ceramic Output Capacitor
- Less Than 2-µA Typical Quiescent Current in Shutdown Mode
- 2% Overall Accuracy
  (Line, Load, Temperature)
- Thermal and Overcurrent Protection
- SOT23-5 (DBV) Package
- Operating Junction Temperature Range:
  –40°C to 125°C

2 Applications

- Optical Drives
- Optical Networking
- Noise-Sensitive Circuitry
- GaAs FET Gate Bias
- Video Amplifiers

3 Description

The TPS723xx-Q1 family of low-dropout (LDO) negative voltage regulators offers an ideal combination of features to support low-noise applications. This device is capable of operating with input voltages from –10 V to –2.7 V. The TPS72325-Q1 regulator is stable with small, low-cost ceramic capacitors, and includes enable (EN) and noise-reduction (NR) functions. Internal detection and shutdown logic provide thermal short-circuit and overcurrent protection. High PSRR (65 dB at 1 kHz) and low noise (60 μV_{RMS}) make the TPS723xx-Q1 ideal for low-noise applications.

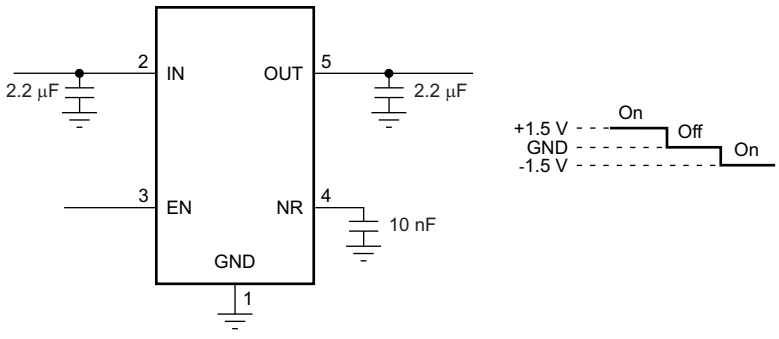
The TPS723xx-Q1 uses a precision voltage reference to achieve 2% overall accuracy over load, line, and temperature variations. Available in a small SOT23-5 package, the TPS723xx-Q1 specification covers the full temperature range of –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS723xx-Q1	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2012) to Revision C	Page
• Added *Device Information* table, *ESD Ratings* table, *Pin Configuration and Functions* section, *Feature Description* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added *AEC-Q100 Qualified With the Following Results* bullets	1
• Deleted Ordering Information table	3
• Changed HBM value from ±2000 kV to ±2000 V in *ESD Ratings* table	3

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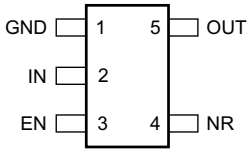
5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	GND	—	Ground
2	IN	I	Input supply
3	EN	I	Bipolar enable pin. Driving this pin above the positive enable threshold or below the negative enable threshold turns on the regulator. Driving this pin below the positive disable threshold and above the negative disable threshold puts the regulator into shutdown mode.
4	NR	—	Fixed-voltage versions only. Connecting an external capacitor between this pin and ground bypasses noise generated by the internal band gap. This configuration allows output noise to be reduced to very low levels.
5	OUT	O	Regulated output voltage. The device requires the connection of a small 2.2-μF ceramic capacitor from this pin to GND to ensure stability.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Input voltage range, V_{IN}	–11	0.3	V
Noise reduction pin voltage range, V_{NR}	–11	5.5	V
Enable voltage range, V_{EN}	$-V_{IN}$	5.5	V
Output current, I_{OUT}	Internally limited		
Output short-circuit duration	Indefinite		
Continuous total power dissipation, P_D	See the *Power Dissipation Ratings* table		
Latch-up performance meets 100 mA per AEC-Q100 | Class I	100		mA
Junction temperature range, T_J	–55	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	
		Machine model	±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Power Dissipation Ratings

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low-K(1)	DBV	64°C/W	255°C/W	3.9 mW/°C	390 mW	215 mW	155 mW
High-K(2)	DBV	64°C/W	180°C/W	5.6 mW/°C	560 mW	310 mW	225 mW

(1) The JEDEC low-K (1s) board design used to derive this data was a 3-inch × 3- inch (7,62-cm × 7,62-cm), two-layer board with 2-ounce (0.071-mm thick) copper traces on top of the board.
(2) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch × 3 inch (7,62-cm × 7,62-cm), multilayer board with 1-ounce (0.035-mm thick) internal power and ground planes and 2-ounce (0.071-mm thick) copper traces on the top and bottom of the board.

6.4 Electrical Characteristics

Over operating junction temperature range, $V_{IN} = V_{OUTnom} – 0.5V$, I_{OUT} = 1mA, V_{EN} = 1.5V, C_{OUT} = 2.2µF, and C_{NR} = 0.01µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			–10		–2.7	V
V_{OUT}	Accuracy	Nominal	T_J = 25°C	–1%		1%	
		TPS723xx-Q1 versus V_{IN} / I_{OUT} / T	–10V ≤ V_{IN} ≤ V_{OUT} – 0.5V, 10 µA ≤ I_{OUT} ≤ 200 mA	–2%	±1%	2%	
V_{OUT}% / V_{IN}	Line regulation		–10 V ≤ V_{IN} ≤ $V_{OUT(nom)}$ – 0.5 V		0.04		%/V
V_{OUT}% / I_{OUT}	Load regulation		0 mA ≤ I_{OUT} ≤ 200 mA		0.002		%/mA
V_{DO}	Dropout voltage at V_{OUT} = 0.96 × V_{OUTnom}		I_{OUT} = 200 mA		280	500	mV
I_{CL}	Current limit		V_{OUT} = 0.85 × $V_{OUT(nom)}$	300	550	800	mA
I_{GND}	Ground pin current		I_{OUT} = 0 mA (I_Q), –10 V ≤ V_{IN} ≤ V_{OUT} – 0.5 V		130	200	µA
			I_{OUT} = 200 mA, –10 V ≤ V_{IN} ≤ V_{OUT} – 0.5 V		350	500	
I_{SHDN}	Shutdown ground pin current		–0.4 V ≤ V_{EN} ≤ 0.4 V, –10V ≤ V_{IN} ≤ V_{OUT} – 0.5 V		0.1	2	µA
PSRR	Power-supply rejection ratio		I_{OUT} = 200 mA, 1 kHz, C_{IN} = C_{OUT} = 10 µF		65		dB
			I_{OUT} = 200 mA, 10 kHz, C_{IN} = C_{OUT} = 10 µF		48		
V_n	Output noise voltage		C_{OUT} = 10 µF, 10 Hz to 100 kHz, I_{OUT} = 200 mA		60		μV_{RMS}
t_{STR}	Startup time		V_{OUT} = –2.5 V, C_{OUT} = 1 µF, R_L = 25 Ω		1		ms
$V_{EN(HI)}$	Enable threshold positive			1.5			V
$V_{EN(LO)}$	Enable threshold negative					–1.5	V
$V_{DIS(HI)}$	Disable threshold positive					0.4	V
$V_{DIS(LO)}$	Disable threshold negative			–0.4			V
I_{EN}	Enable pin current		–10 V ≤ V_{IN} ≤ V_{OUT} – 0.5 V, –10 V ≤ V_{EN} ≤ ±3.5 V		0.1	2	µA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		165		°C
			Reset, temperature decreasing		145		
T_J	Operating junction temperature			–40		125	°C

(1) Maximum V_{IN} = (V_{OUT} – V_{DO}) or – 2.7 V, whichever is more negative.

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6.5 Typical Characteristics

TPS723xx-Q1 at $V_{IN} = V_{OUTnom} – 0.5$ V, $I_{OUT} = 1$ mA, $V_{EN} = 1.5$ V, $C_{OUT} = 2.2$ µF, and $C_{NR} = 0.01$ µF, unless otherwise noted.

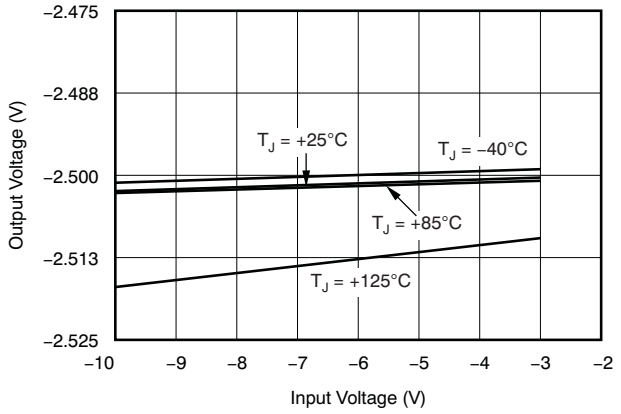

Figure 1. Output Voltage vs Input Voltage

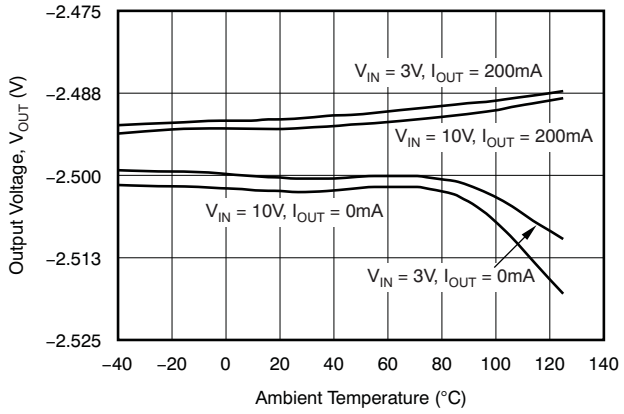

Figure 2. Output Voltage vs Ambient Temperature

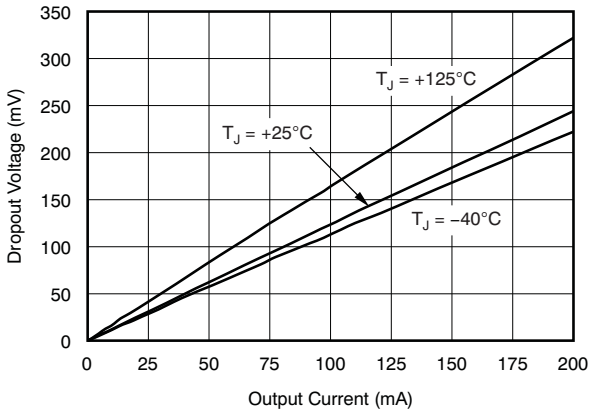

Figure 3. Dropout Voltage vs Output Current

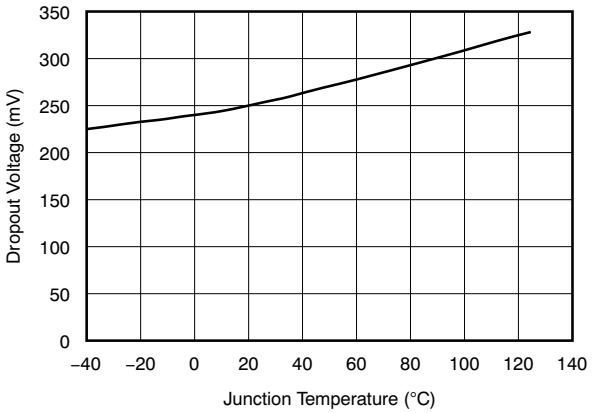

Figure 4. TPS723xx-Q1 Dropout Voltage vs Junction Temperature

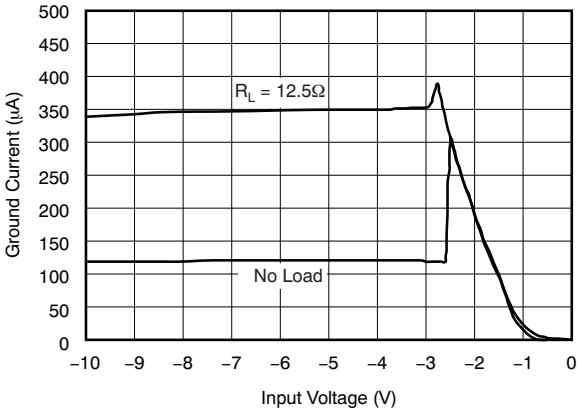

Figure 5. Ground Current vs Input Voltage

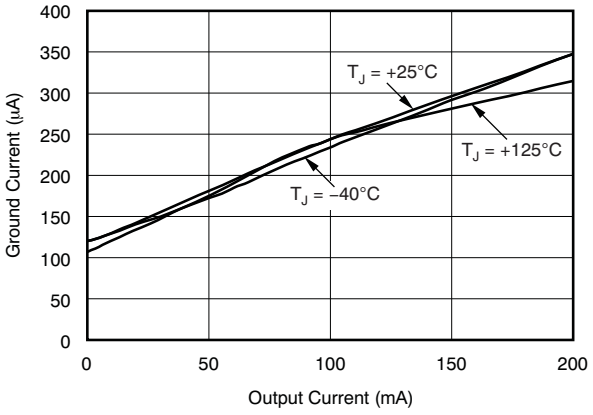

Figure 6. Ground Current vs Output Current

Typical Characteristics (continued)

TPS723xx-Q1 at V_{IN} = V_{OUTnom} – 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.5 V, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF, unless otherwise noted.

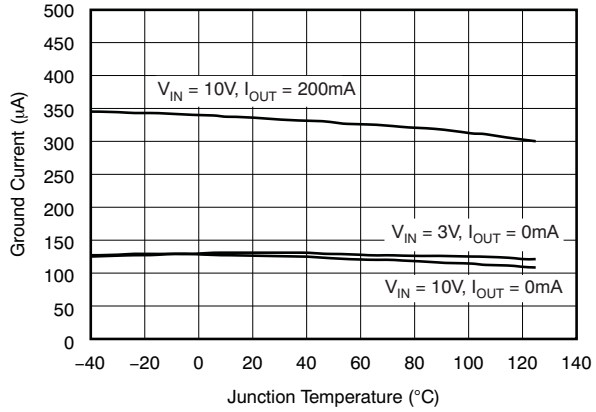

Figure 7. Ground Current vs Junction Temperature

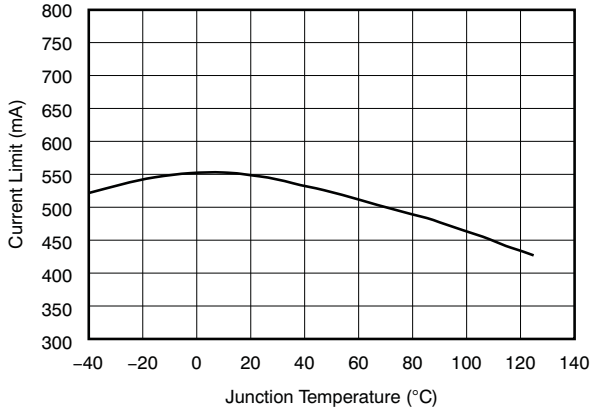

Figure 8. Current Limit vs Junction Temperature

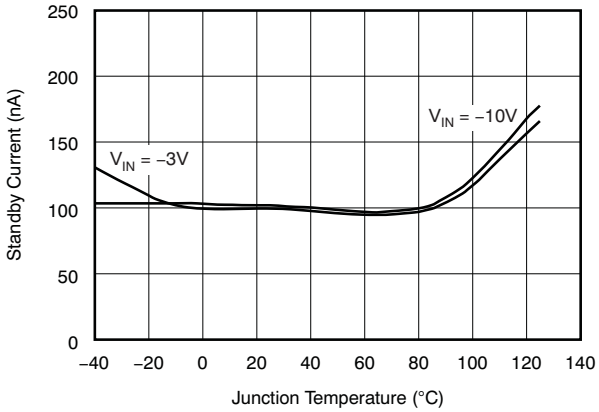

Figure 9. Standby Current vs Junction Temperature

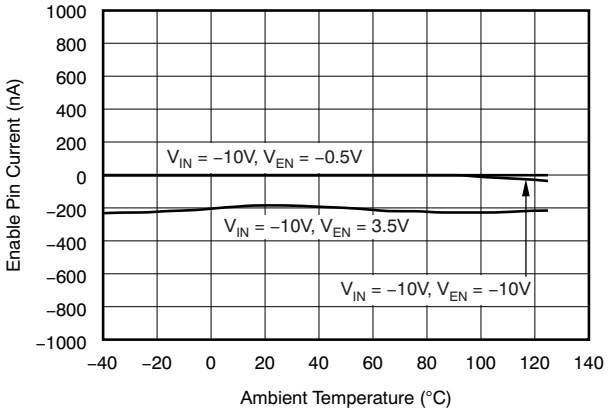

Figure 10. Enable Pin Current vs Junction Temperature

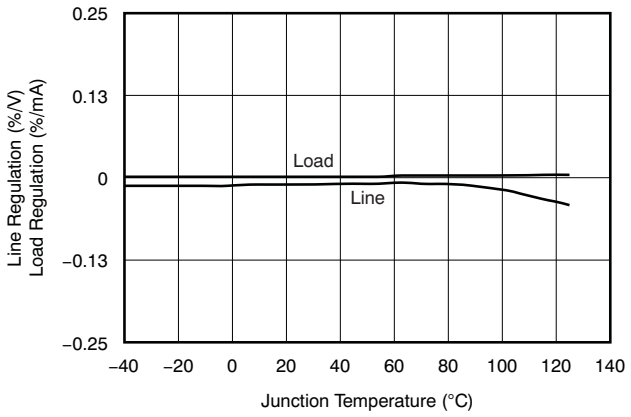

Figure 11. Line and Load Regulation vs Junction Temperature

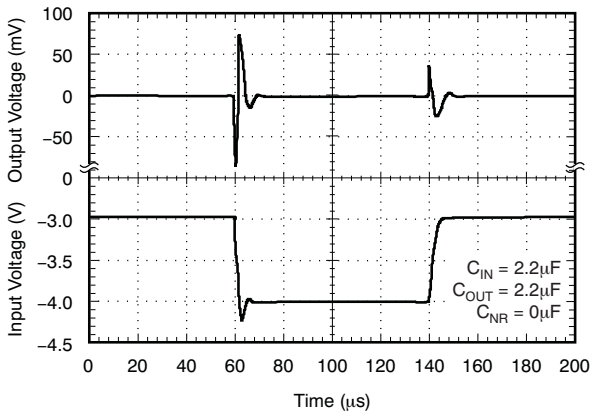

Figure 12. Line Transient Response

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Typical Characteristics (continued)

TPS723xx-Q1 at V_{IN} = V_{OUTnom} – 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.5 V, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF, unless otherwise noted.

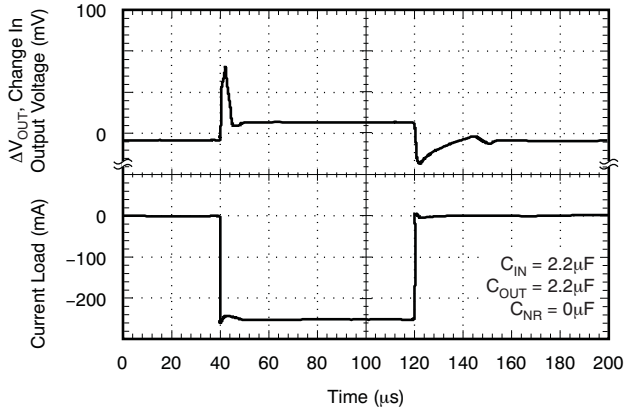

Figure 13. Load Transient Response

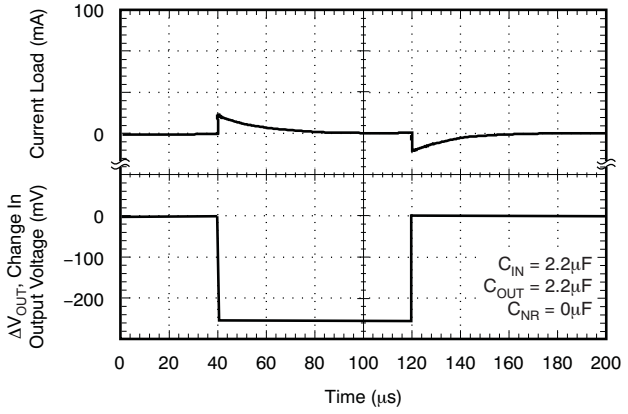

Figure 14. Load Transient Response

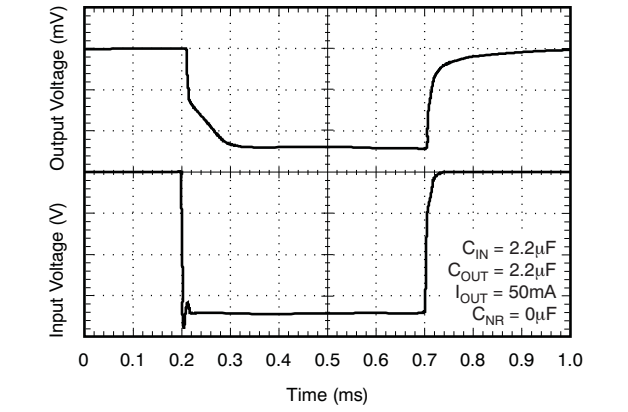

Figure 15. Start-Up Response

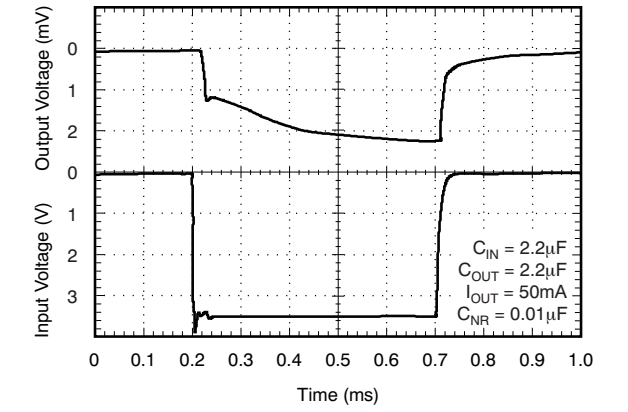

Figure 16. Start-Up Response

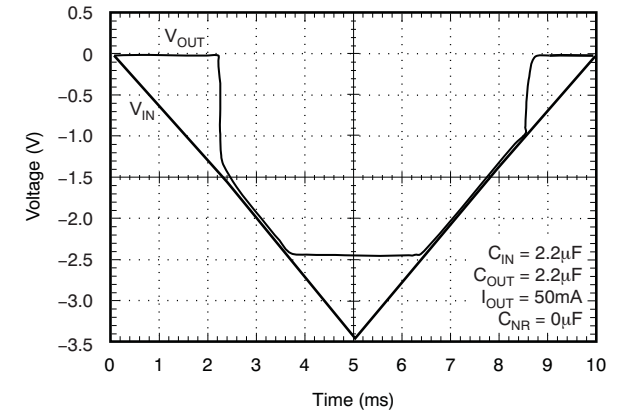

Figure 17. Power Up and Power Down

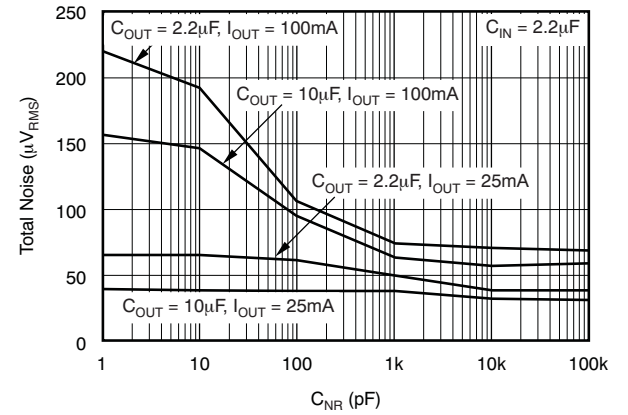

Figure 18. Total Noise vs C_{NR} (10 Hz to 100 kHz)

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Typical Characteristics (continued)

TPS723xx-Q1 at $V_{IN} = V_{OUTnom} – 0.5$ V, $I_{OUT} = 1$ mA, $V_{EN} = 1.5$ V, $C_{OUT} = 2.2$ µF, and $C_{NR} = 0.01$ µF, unless otherwise noted.

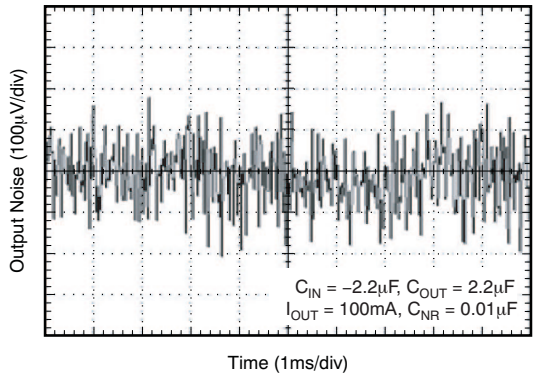

Figure 19. Output Noise vs Time

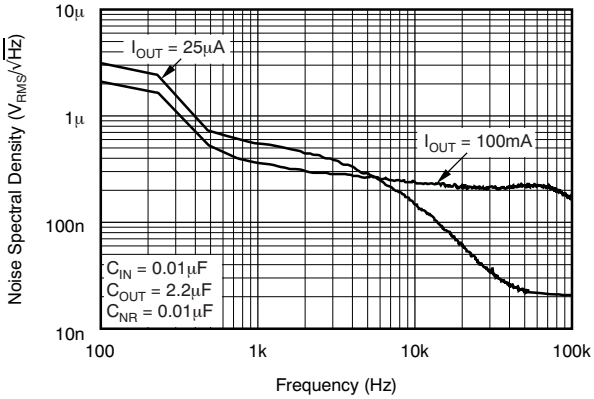

Figure 20. Noise Spectral Density vs Frequency

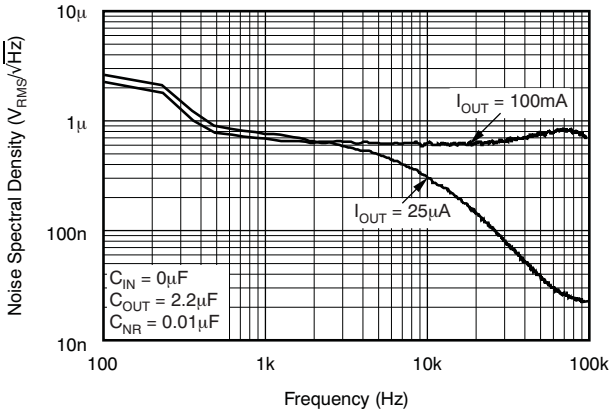

Figure 21. Noise Spectral Density vs Frequency

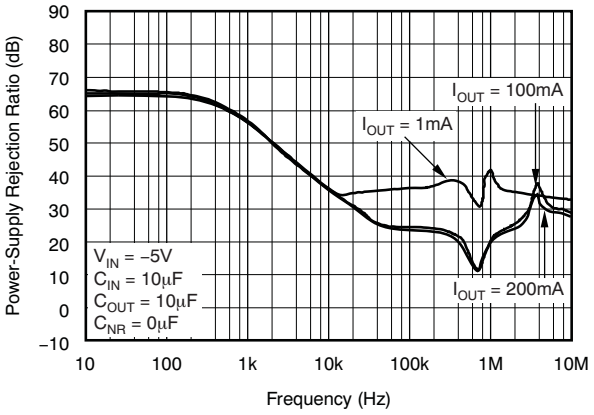

Figure 22. PSRR vs Frequency

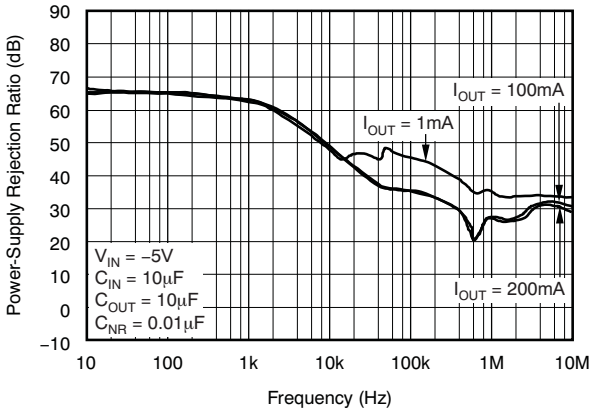

Figure 23. PSRR vs Frequency

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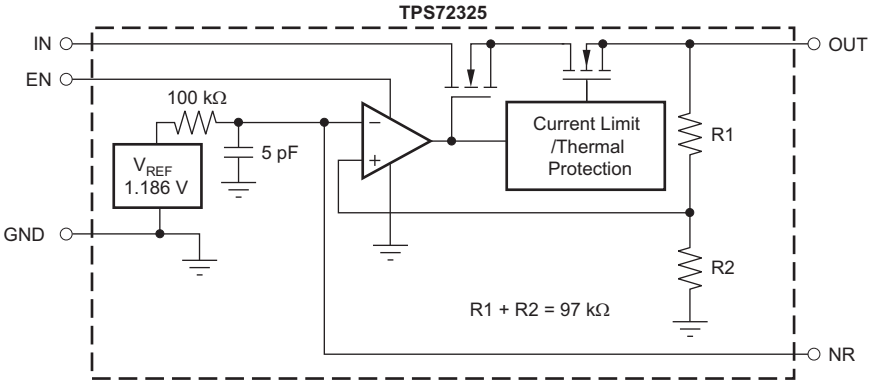
7 Detailed Description

7.1 Overview

The TPS723xx-Q1 is a low-dropout negative linear voltage regulator with a rated current of 200 mA. It features very low noise and high power-supply rejection ratio (PSRR), making it ideal for high-sensitivity analog and RF applications. A shutdown mode is available, reducing ground current to 2 μA maximum over temperature and process. The TPS723xx-Q1 comes in a small SOT23 package, specified over a –40°C to 125°C junction-temperature range.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable

The enable pin is active above 1.5 V and below –1.5 V, allowing control by a standard TTL signal or by connection to V_I if not used. Driving the pin to GND turns off most internal circuitry, putting the TPS723xx-Q1 into shutdown mode, drawing 2-μA maximum ground current.

7.3.2 Capacitor Selection for Stability

Use appropriate input and output capacitors for the intended application. The TPS723xx-Q1 only requires the use of a 2.2-μF ceramic output capacitor for stable operation. Both the capacitor value and ESR affect stability, output noise, PSRR, and transient response. For typical applications, a 2.2-μF ceramic output capacitor located close to the regulator is sufficient.

7.3.3 Output Noise

Without external bypassing, output noise of the TPS723xx-Q1 from 10 Hz to 100 kHz is 200 μV_{RMS} typical. The dominant contributor to output noise is the internal band-gap reference. Adding an external 0.01-μF capacitor to ground reduces the noise to 60 μV_{RMS}. To achieve best noise performance, use appropriate low-ESR capacitors for bypassing noise at the NR and OUT pins. See Figure 18 in the *Typical Characteristics* section.

7.3.4 Power-Supply Rejection

The TPS723xx-Q1 offers a very high PSRR for applications with noisy input sources or highly sensitive output supply lines. For best PSRR, use high-quality input and output capacitors.

7.3.5 Current Limit

The TPS723xx-Q1 has internal circuitry that monitors and limits output current to protect the regulator from damage under all load conditions. When output current reaches the output-current limit (550 mA typical), protection circuitry turns on, reducing output voltage to ensure that current does not increase. See Figure 8 in the *Typical Characteristics* section.

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Feature Description (continued)

Do not drive the output more than 0.3 V above the input. Doing so biases the body diode in the pass FET, allowing current to flow from the output to the input. The device does not limit this current. If this condition is likely, take care to limit the reverse current externally.

7.3.6 Thermal Protection

As protection from damage due to excessive junction temperatures, the TPS723xx-Q1 has internal protection circuitry. When junction temperature reaches approximately 165°C, the output device turns off. After the device has cooled by about 20°C, the output device turns on, allowing normal operation. For reliable operation, design is for worst-case junction temperature of ≤ 125°C, taking into account worst-case ambient temperature and load conditions.

7.3.7 Adjustable Voltage Applications

The TPS72301-Q1 allows designers to specify any output voltage from –10 V to –1.2 V. As shown in the application circuit in Figure 24, use of an external resistor divider scales the output voltage (V_{OUT}) to the reference voltage. For best accuracy, use precision resistors for R1 and R2. Use the equations in Figure 24 to determine the values for the resistor divider.

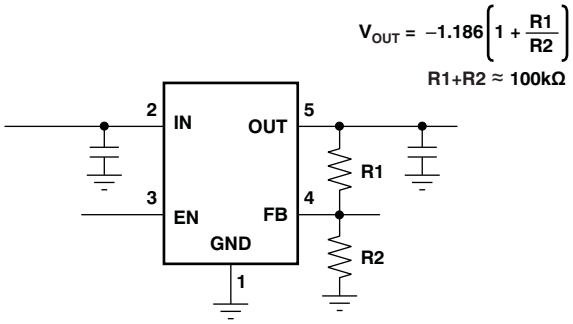

Figure 24. TPS72301-Q1 Adjustable LDO Regulator Programming

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8 Device and Documentation Support

8.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS72325-Q1	Click here	Click here	Click here	Click here	Click here
TPS72301-Q1	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.4 Trademarks

E2E is a trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS72301QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PPHQ	Samples
TPS72325QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PSBQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS723-Q1 :

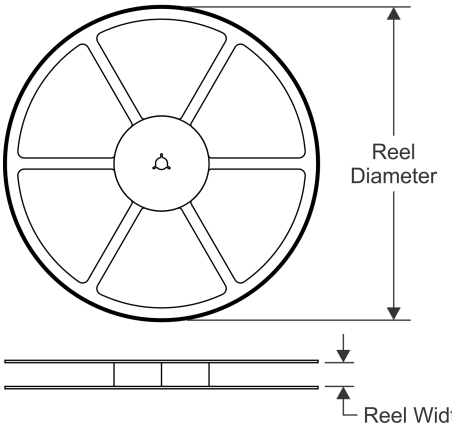
- Catalog: TPS723

NOTE: Qualified Version Definitions:

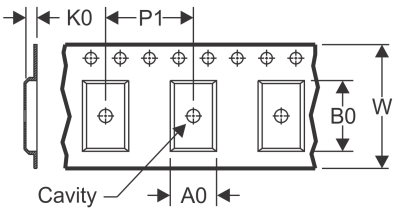
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

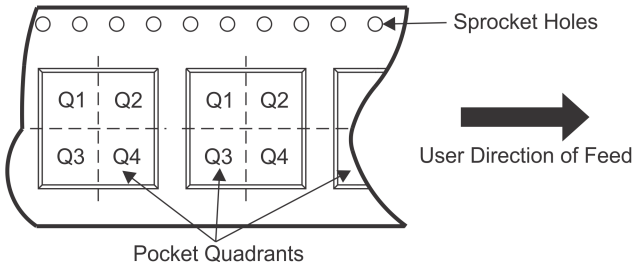


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

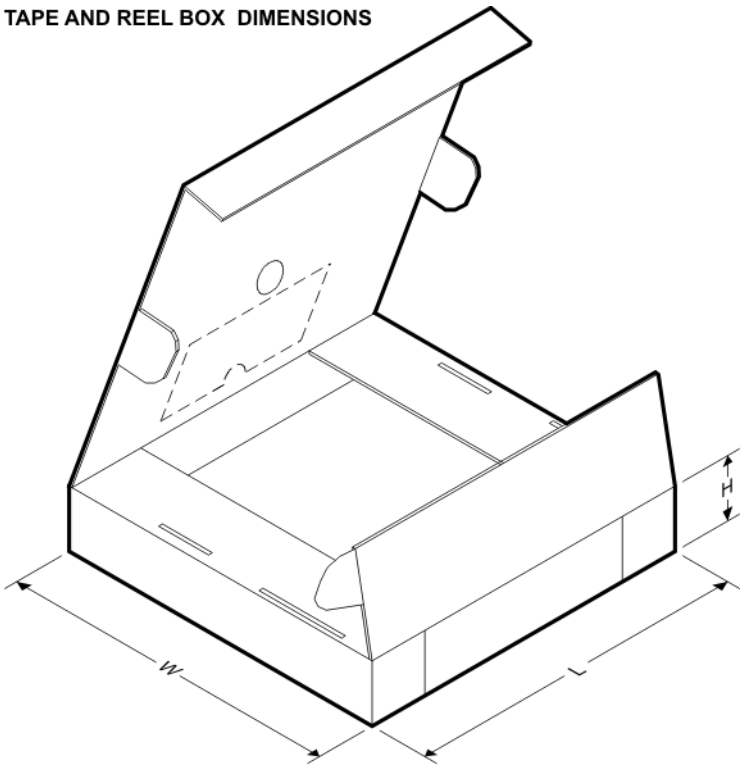
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72301QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72325QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

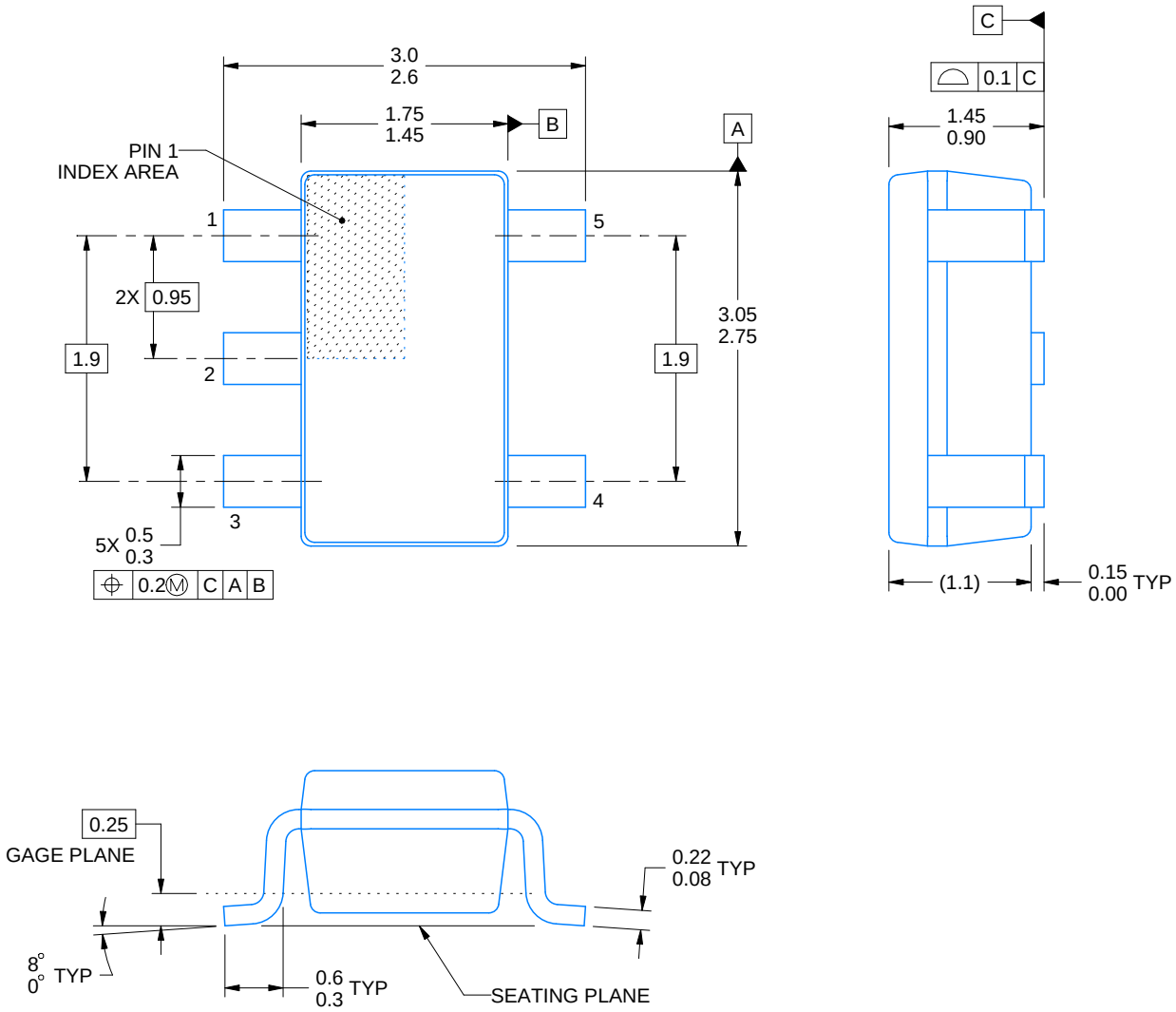
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72301QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS72325QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

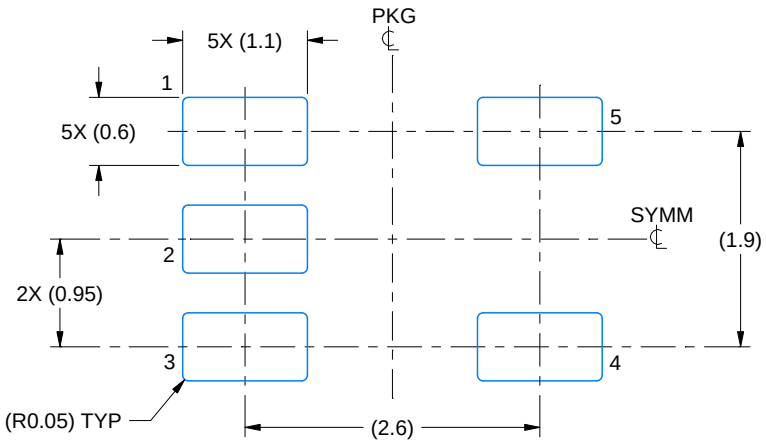
SMALL OUTLINE TRANSISTOR



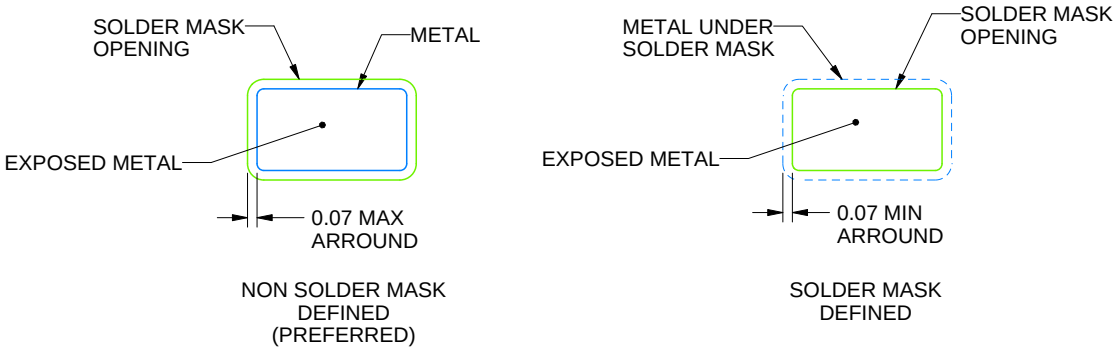
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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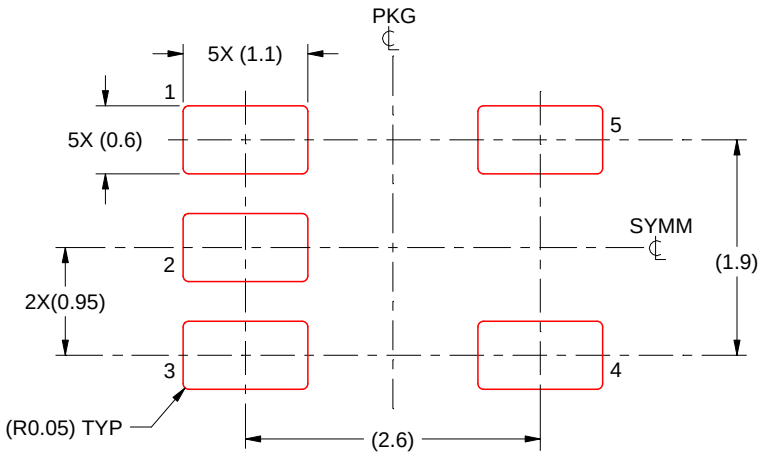
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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