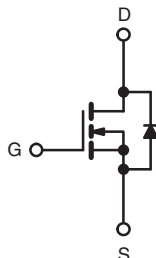
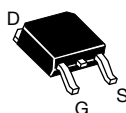


Power MOSFET

PRODUCT SUMMARY

V _{DS} (V)	50	
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.20
Q _g (Max.) (nC)	10	
Q _{gs} (nC)	2.6	
Q _{gd} (nC)	4.8	
Configuration	Single	

**DPAK
(TO-252)**



N-Channel MOSFET

FEATURES

- Low Drive Current
- Surface Mount
- Fast Switching
- Ease of Paralleling
- Excellent Temperature Stability
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dV/dt capability.

The power MOSFET transistors also feature all of the well established advantages of MOSFET'S such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The DPAK (TO-252) surface mount package brings the advantages of power MOSFET's to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9012, SiHFR9012 is provided on 16 mm tape. The straight lead option IRFU9012, SiHFU9012 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, dc-to-dc converters, and a wide range of consumer products.

ORDERING INFORMATION

Package	DPAK (TO-252)
Lead (Pb)-free	IRFR010PbF
	SiHFR010-E3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	50	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed Drain Current ^a	I _{DM}	33	
Avalanche Current ^b	I _{AS}	1.5	
Linear Derating Factor		0.20	W/°C
Maximum Power Dissipation	P _D	25	W
Peak Diode Recovery dV/dt ^c	dV/dt	2.0	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s	300	

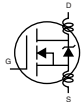
Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 25 V, starting T_J = 25 °C, L = 100 μH, R_g = 25 Ω.
- I_{SD} ≤ 8.2 A, dI/dt ≤ 130 A/μs, V_{DD} ≤ 40 V, T_J ≤ 150 °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W
Case-to-Sink	R_{thCS}	-	1.7	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	5.0	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		50	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 500	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 50 V, V _{GS} = 0 V		-	-	250	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 125 °C		-	-	1000	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 4.6 A ^b	-	0.16	0.20	Ω
Forward Transconductance	g _{fs}	V _{DS} ≥ 50 V, I _D = 3.6 A		2.1	3.1	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 10		-	250	-	pF
Output Capacitance	C _{oss}			-	150	-	
Reverse Transfer Capacitance	C _{rss}			-	29	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 7.3 A, V _{DS} = 40 V, see fig. 6 and 13 ^b	-	6.7	10	nC
Gate-Source Charge	Q _{gs}			-	1.8	2.6	
Gate-Drain Charge	Q _{gd}			-	3.2	4.8	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 25 V, I _D = 7.3 A, R _g = 24 Ω, R _D = 3.3 Ω, see fig. 10 ^b		-	11	17	ns
Rise Time	t _r			-	33	50	
Turn-Off Delay Time	t _{d(off)}			-	12	18	
Fall Time	t _f			-	23	35	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact ^c 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	8.2	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	33	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 8.2 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 7.3 A, dI/dt = 100 A/μs ^b		41	86	190	ns
Body Diode Reverse Recovery Charge	Q _{rr}			0.15	0.33	0.78	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

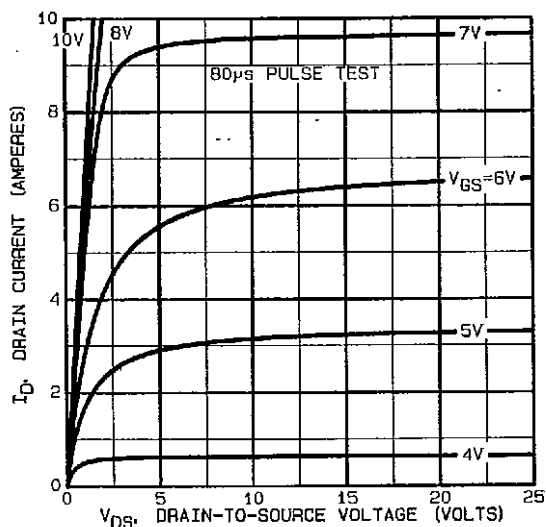


Fig. 1 - Typical Output Characteristics

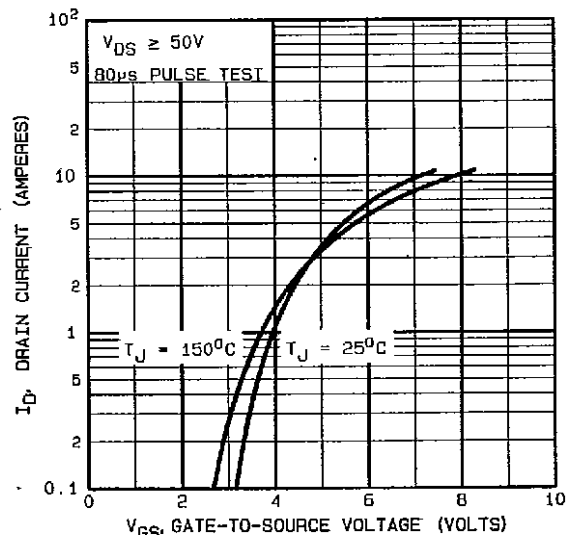


Fig. 3 - Typical Transfer Characteristics

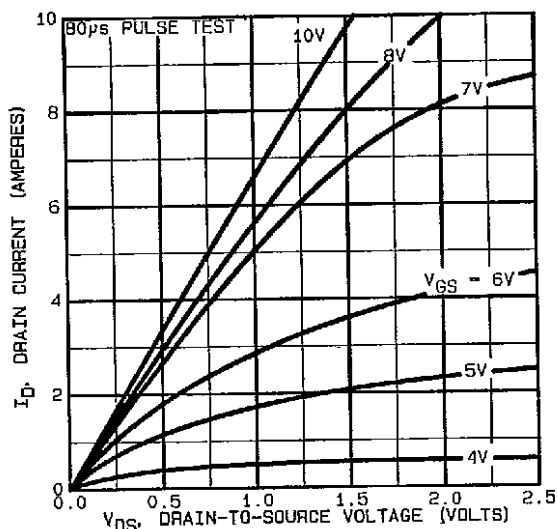


Fig. 2 - Typical Output Characteristics

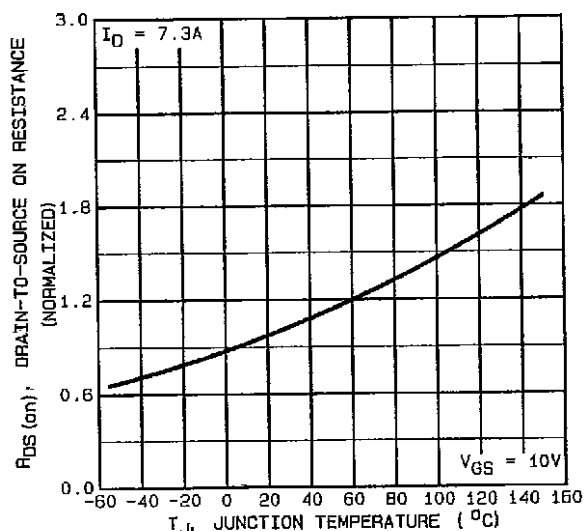
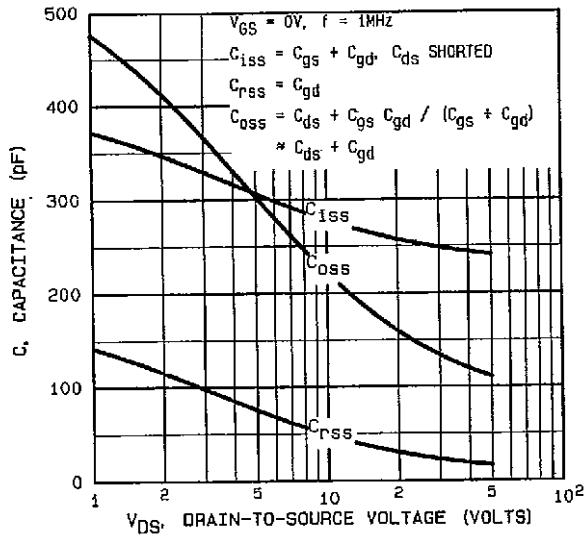
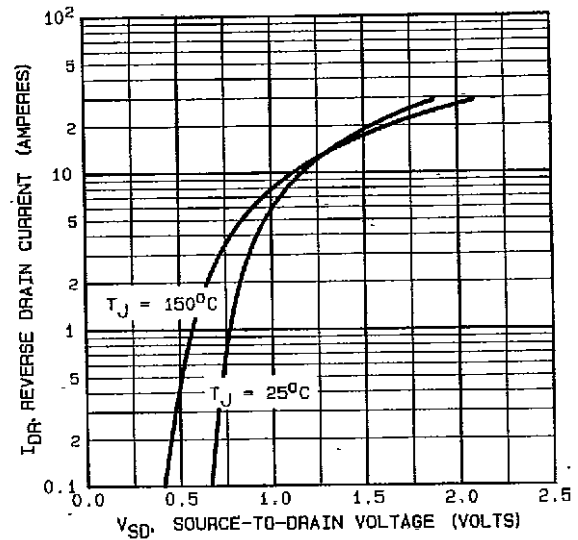
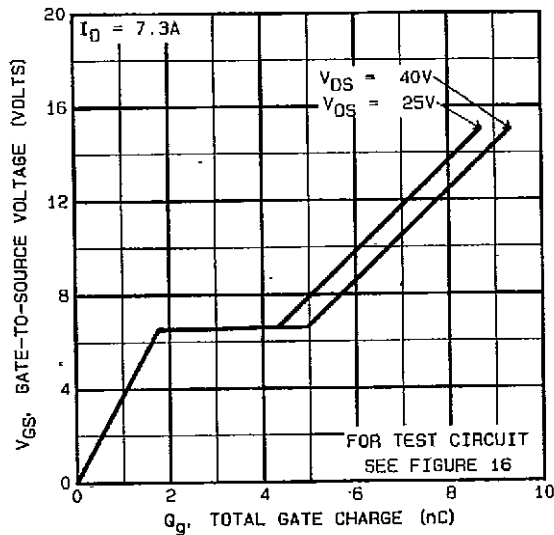
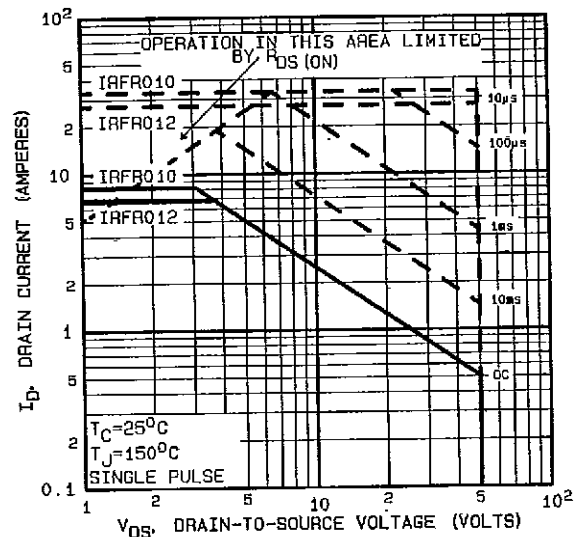
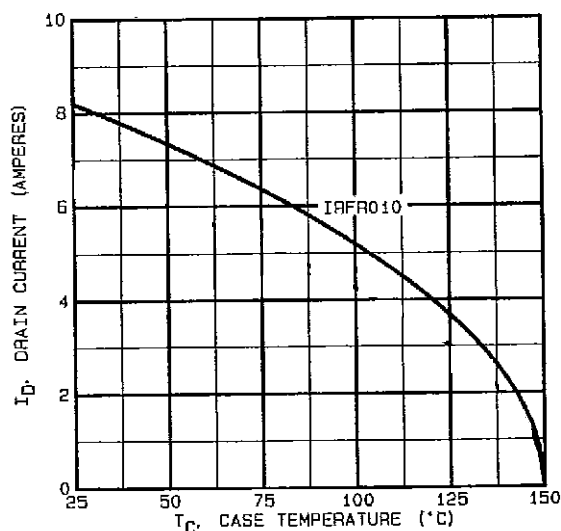
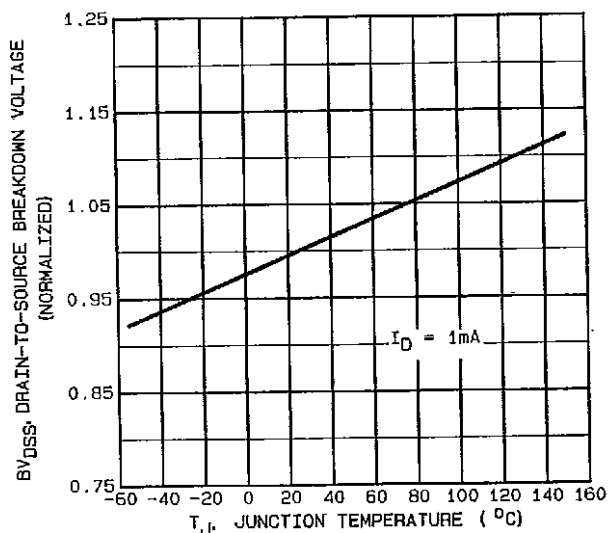
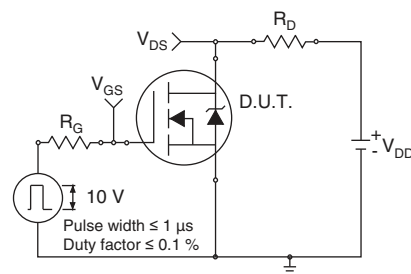
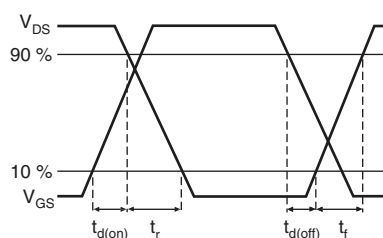
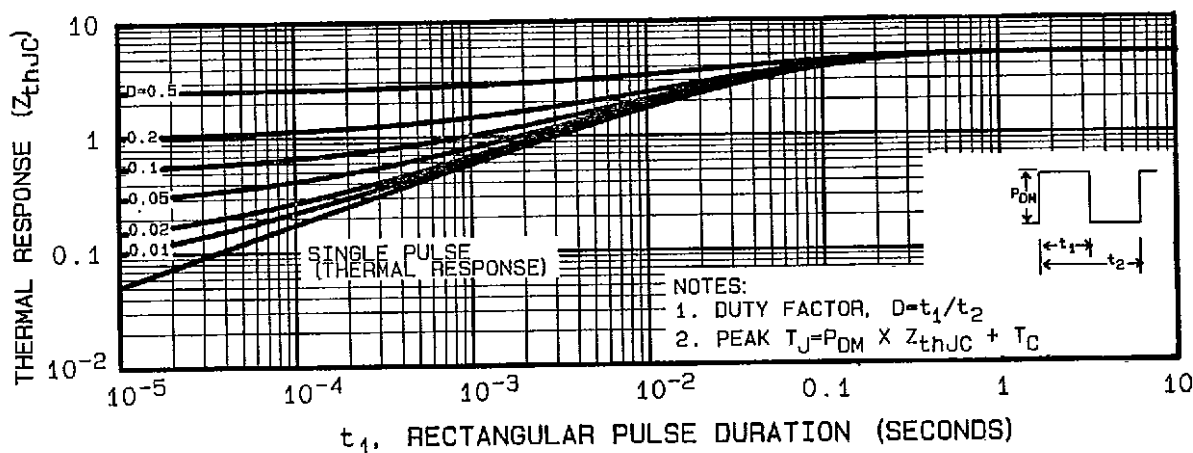
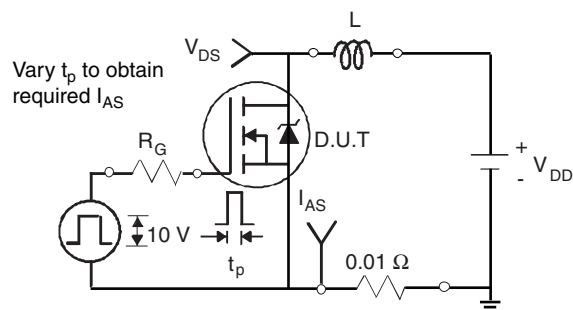
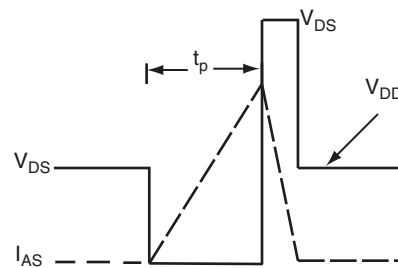
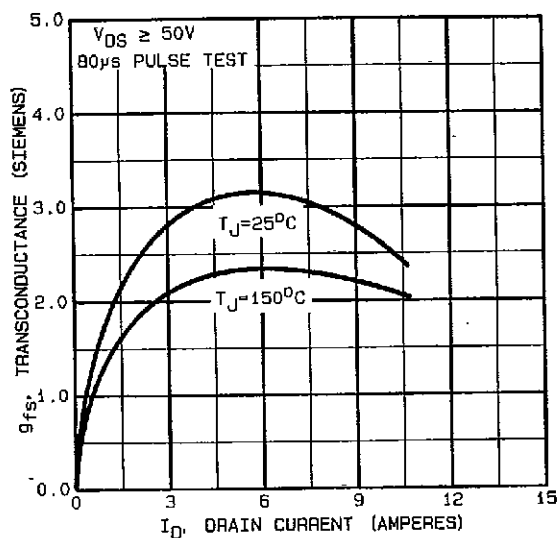
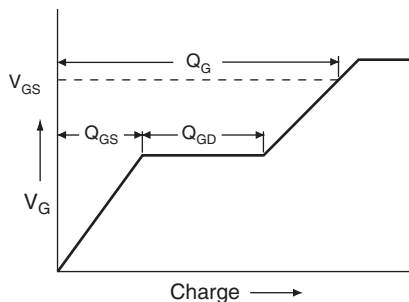
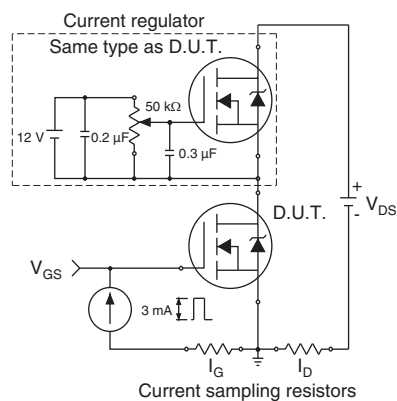
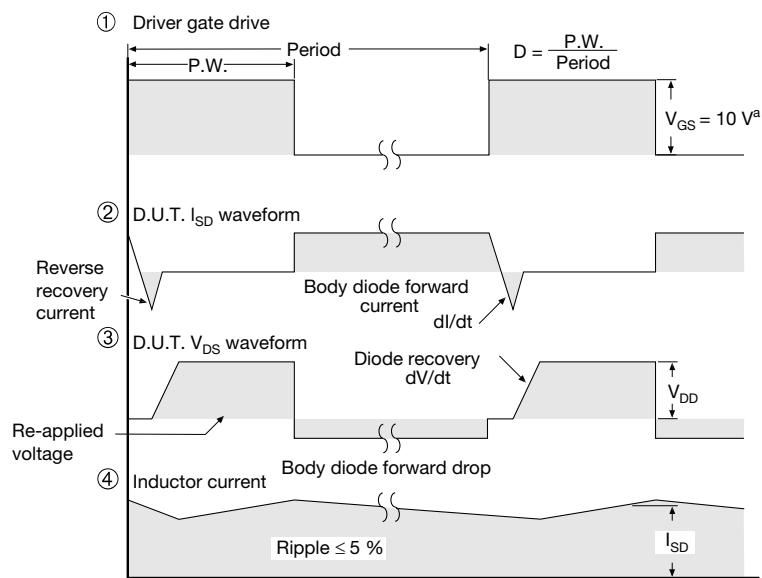
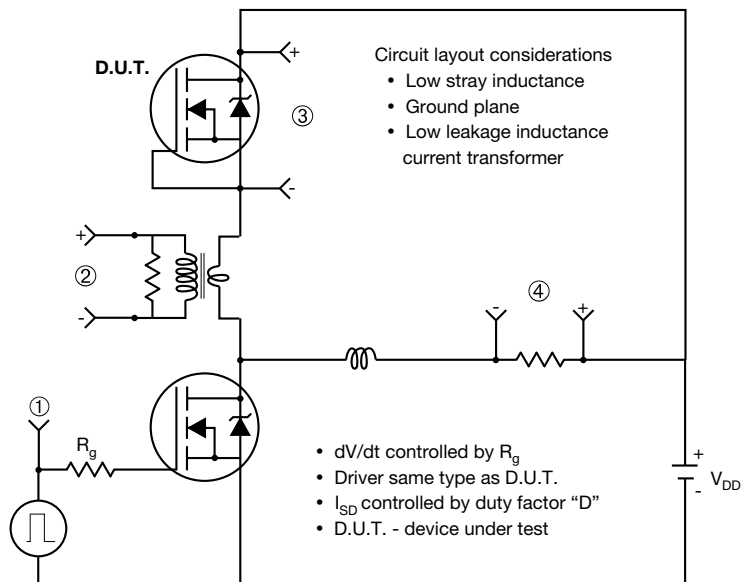


Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10 - Breakdown Voltage vs. Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Typical Transconductance vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Note

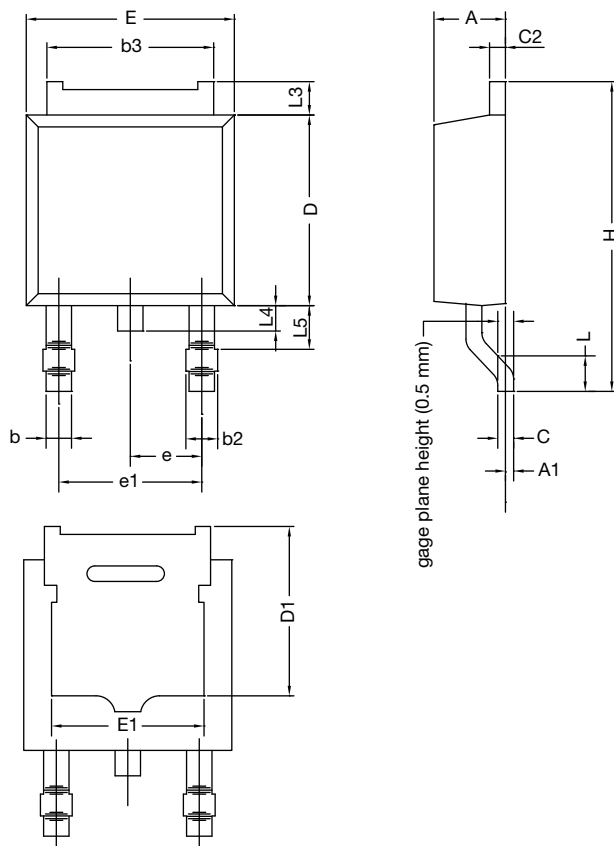
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-252AA Case Outline

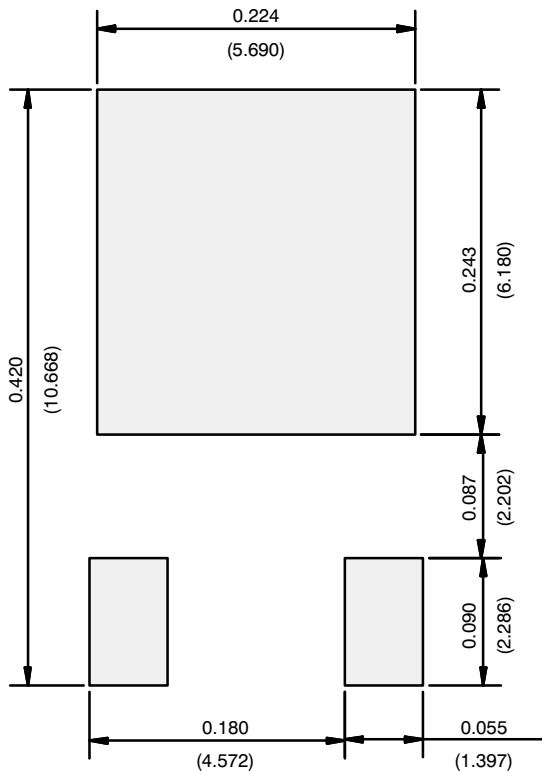


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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