CD74HC652, CD74HCT652

Data sheet acquired from Harris Semiconductor
SCHS194A

February 1998 - Revised May 2003

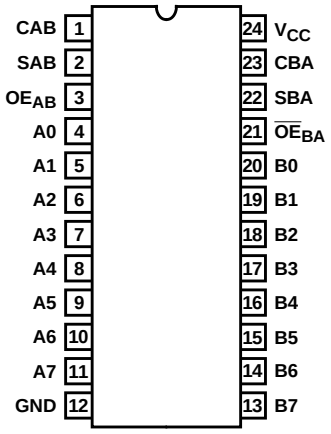
High-Speed CMOS Logic Octal-Bus Transceiver/Registers, Three-State

Features

- **CD74HC652, CD74HCT652 . . . . . Non-Inverting**
- **Independent Registers for A and B Buses**
- **Three-State Outputs**
- **Drives 15 LSTTL Loads**
- **Typical Propagation Delay = 12ns at V_{CC} = 5V, C_L = 15pF**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{o}C to 125^{o}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **Alternate Source is Philips**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Pinout

CD74HC652
(PDIP)
CD74HCT652
(SOIC)
TOP VIEW



Description

The CD74HC652 and CD74HCT652 three-state, octal-bus transceiver/registers use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits. The CD74HC652 and CD74HCT652 have non-inverting outputs. These devices consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OE_{AB} and OE_{BA} are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrates the four fundamentals bus-management functions that can be performed with the octal-bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select of the control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the D-type flip-flops by simultaneously enabling OE_{AB} and OE_{BA}. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

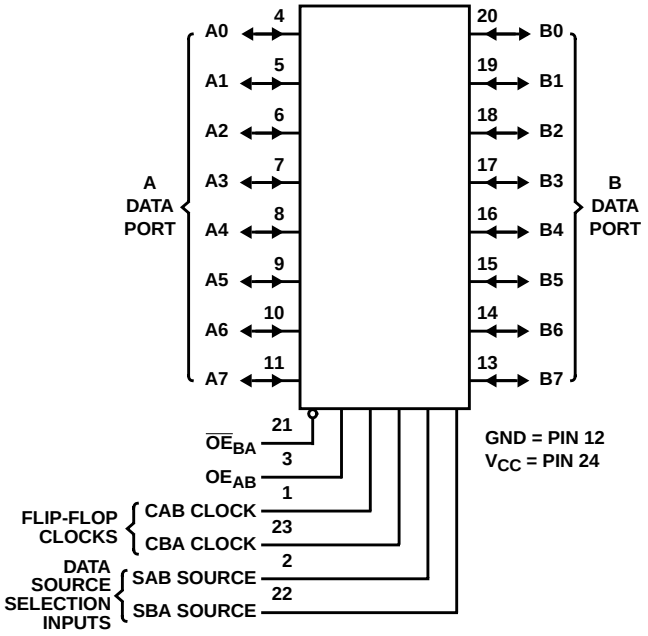
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD74HC652EN	-55 to 125	24 Ld PDIP
CD74HCT652M	-55 to 125	24 Ld SOIC
CD74HCT652M96	-55 to 125	24 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram



FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OE_{AB}	$\overline{OE}_{BA}$	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	651	652
L	H	H or L	H or L	X	X	Input	Input	Isolation (Note 1)	Isolation (Note 1)
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified (Note 2)	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X (Note 3)	X	Input	Output	Store A in Both Registers	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified (Note 2)	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X (Note 3)	Output	Input	Store B in Both Registers	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and	Stored A Data to B Bus
								Stored B Data to A Bus	Stored B Data to A Bus

NOTES:

1. To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.
2. The data output functions may be enabled or disabled by various signals at the OE_{AB} or $\overline{OE}_{BA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
3. Select Control = L: Clocks can occur simultaneously.
   Select Control = H: Clocks must be staggered in order to load both registers.

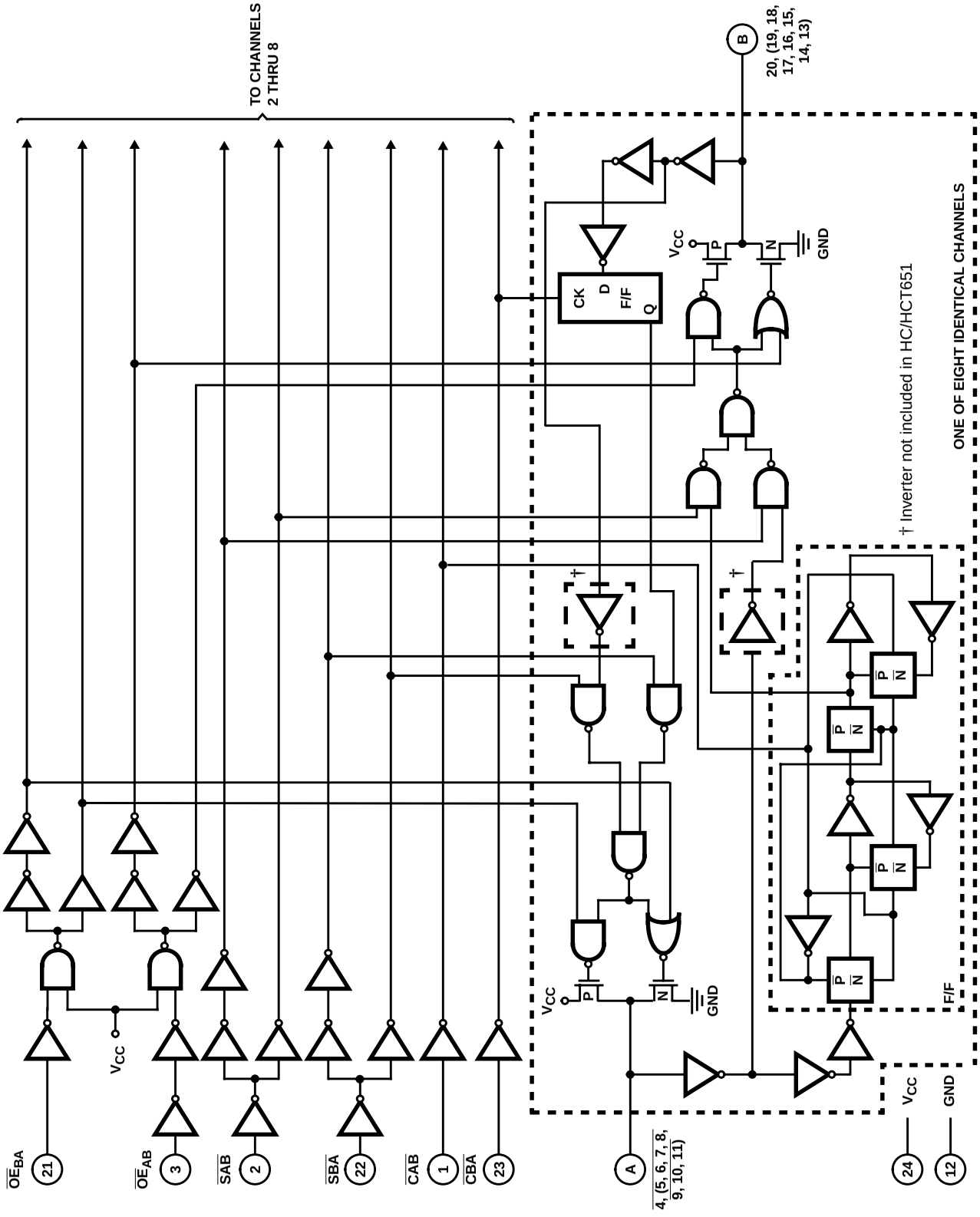


FIGURE 1. LOGIC BLOCK DIAGRAM

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}
(Voltages Referenced to Ground) . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Drain Current, I_O
For -0.5V < V_O < V_{CC} + 0.5V . . . . . ±35mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55^oC to 125^oC
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^oC/W$)
EN (PDIP) Package (Note 4)	67
M (SOIC) Package (Note 5).	46

Maximum Junction Temperature (Hermetic Package or Die) . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

4. The package thermal impedance is calculated in accordance with JESD 51-3.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.3	-	0.3	-	0.3	V
				4.5	-	-	0.9	-	0.9	-	0.9	V
				6	-	-	1.2	-	1.2	-	1.2	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA
Three- State Leakage Current	V_{IL} or V_{IH}	V_O = V_{CC} or GND	-	6	-	-	±0.5	-	±5.0	-	±10	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Three- State Leakage Current	V_{IL} or V_{IH}	V_O = V_{CC} or GND	-	5.5	-	-	±0.5	-	±5.0	-	±10	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 6)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

6. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
$\overline{OE}_{BA}$	1.3
OE_{AB}	0.75
Clock A to B, B to A	0.6
Select A, Select B	0.45
Inputs A_0-A_7, B_0-B_7	0.3

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
Maximum Clock Frequency	f_{MAX}	2	6	-	-	5	-	-	4	-	-	MHz
		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
Setup Time Data to Clock	t_{SU}	2	60	-	-	75	-	-	90	-	-	ns
		4.5	12	-	-	15	-	-	18	-	-	ns
		6	10	-	-	13	-	-	15	-	-	ns
Hold Time Data to Clock	t_H	2	35	-	-	45	-	-	55	-	-	ns
		4.5	7	-	-	9	-	-	11	-	-	ns
		6	6	-	-	8	-	-	9	-	-	ns
Clock Pulse Width	t_W	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
HCT TYPES												
Maximum Clock Frequency	f_{MAX}	4.5	25	-	-	20	-	-	17	-	-	MHz
Setup Time Data to Clock	t_{SU}	4.5	12	-	-	15	-	-	18	-	-	ns
Hold Time Data to Clock	t_H	4.5	5	-	-	5	-	-	5	-	-	ns
Clock Pulse Width	t_W	4.5	25	-	-	31	-	-	38	-	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, Store A Data to B Bus Store B Data to A Bus	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	220	-	275	-	300	ns
			4.5	-	-	44	-	55	-	66	ns
			6	-	-	37	-	47	-	5.6	ns
		C_L = 15pF	5	-	18	-	-	-	-	-	ns
Propagation Delay, A Data to B Bus B Data to A Bus	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
			6	-	-	23	-	29	-	35	ns
		C_L = 15pF	5	-	12	-	-	-	-	-	ns
Propagation Delay, Select to Data	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	170	-	215	-	255	ns
			4.5	-	-	34	-	43	-	51	ns
			6	-	-	29	-	37	-	43	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns

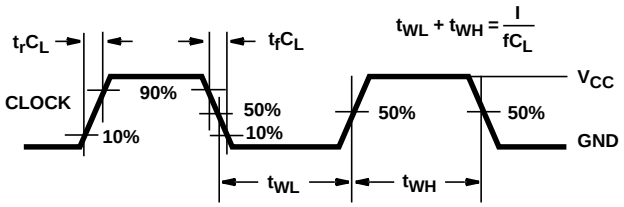
Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Three-State Disabling Time Bus to Output or Register to Output	t_{PLZ}, t_{PHZ}	C_L = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
			6	-	-	30	-	37	-	45	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
Three-State Enabling Time Bus to Output or Register to Output	t_{PZL}, t_{PZH}	C_L = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
			6	-	-	30	-	37	-	45	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
			6	-	-	10	-	13	-	15	ns
Three-State Output Capacitance	C_O	-	-	-	-	20	-	20	-	20	pF
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Maximum Frequency	f_{MAX}	C_L = 15pF	5	-	60	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 7, 8)	C_{PD}	-	5	-	52	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay, Store A Data to B Bus Store B Data to A Bus	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	44	-	55	-	66	ns
		C_L = 15pF	5	-	18	-	-	-	-	-	ns
Propagation Delay, A Data to B Bus B Data to A Bus	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	37	-	46	-	56	ns
		C_L = 15pF	5	-	15	-	-	-	-	-	ns
Propagation Delay, Select to Data	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	46	-	58	-	69	ns
		C_L = 15pF	5	-	19	-	-	-	-	-	ns
Three-State Disabling Time Bus to Output or Register to Output	t_{PLZ}, t_{PHZ}	C_L = 50pF	4.5	-	-	35	-	44	-	53	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
Three-State Enabling Time Bus to Output or Register to Output	t_{PZL}, t_{PZH}	C_L = 50pF	4.5	-	-	45	-	56	-	68	ns
		C_L = 15pF	5	-	19	-	-	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	12	-	15	-	18	ns
Three-State Output Capacitance	C_O	-	-	-	-	20	-	20	-	20	pF
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Maximum Frequency	f_{MAX}	C_L = 15pF	5	-	45	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 7, 8)	C_{PD}	-	5	-	52	-	-	-	-	-	pF

NOTES:

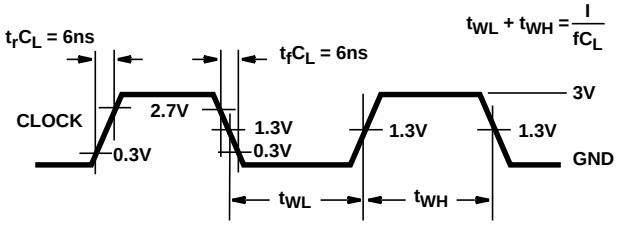
7. C_{PD} is used to determine the dynamic power consumption, per package.
8. $P_D = V_{CC}^2 C_{PD} f_i + \Sigma V_{CC}^2 C_L f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 2. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 3. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

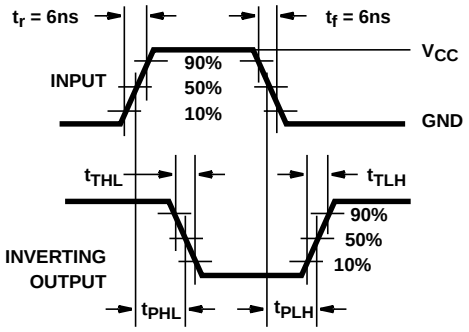


FIGURE 4. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

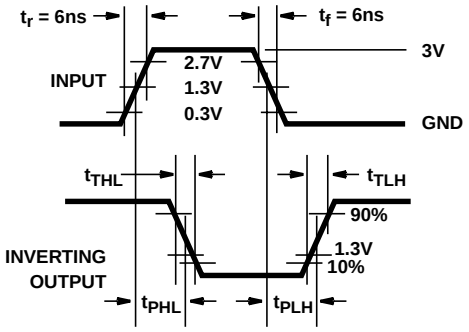


FIGURE 5. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Test Circuits and Waveforms (Continued)

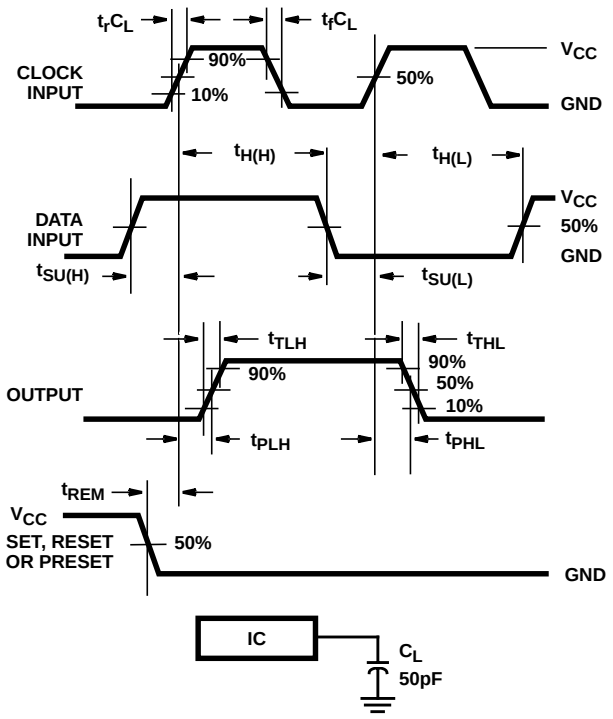


FIGURE 6. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

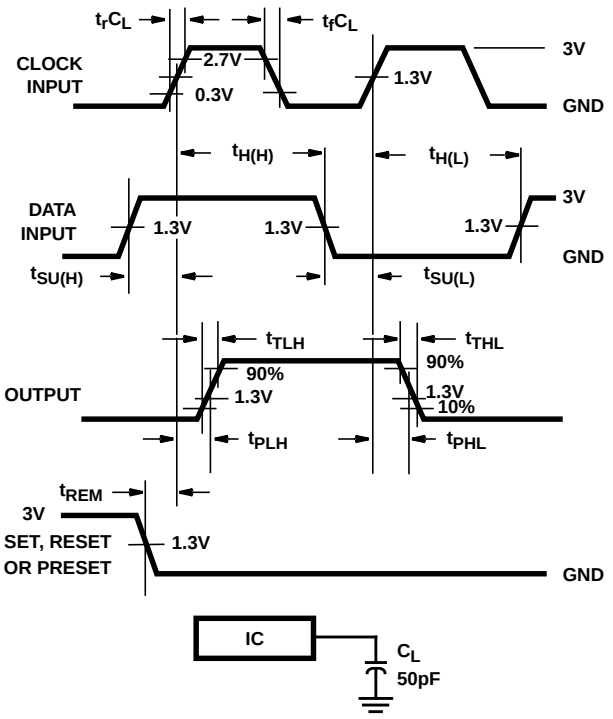


FIGURE 7. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

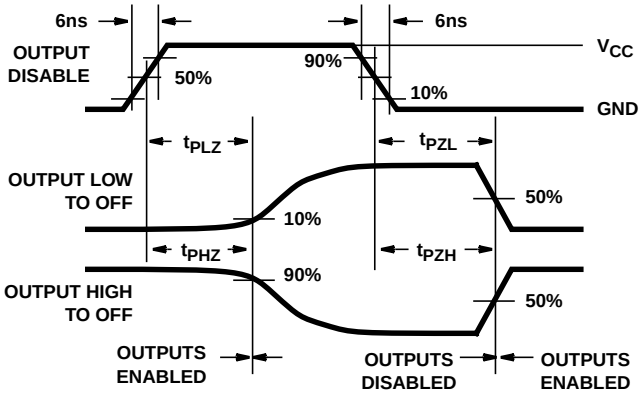


FIGURE 8. HC THREE-STATE PROPAGATION DELAY WAVEFORM

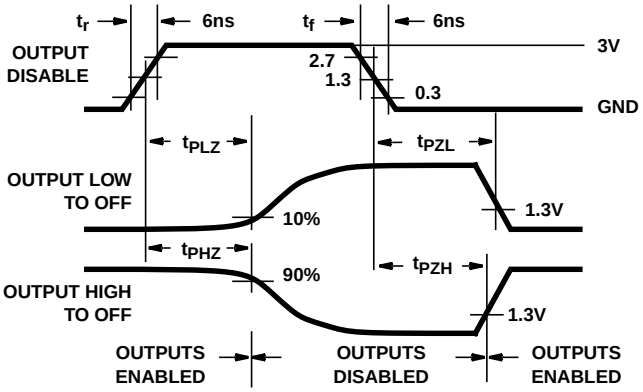
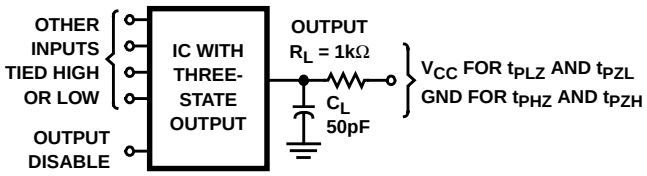


FIGURE 9. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

FIGURE 10. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT652M	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT652M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

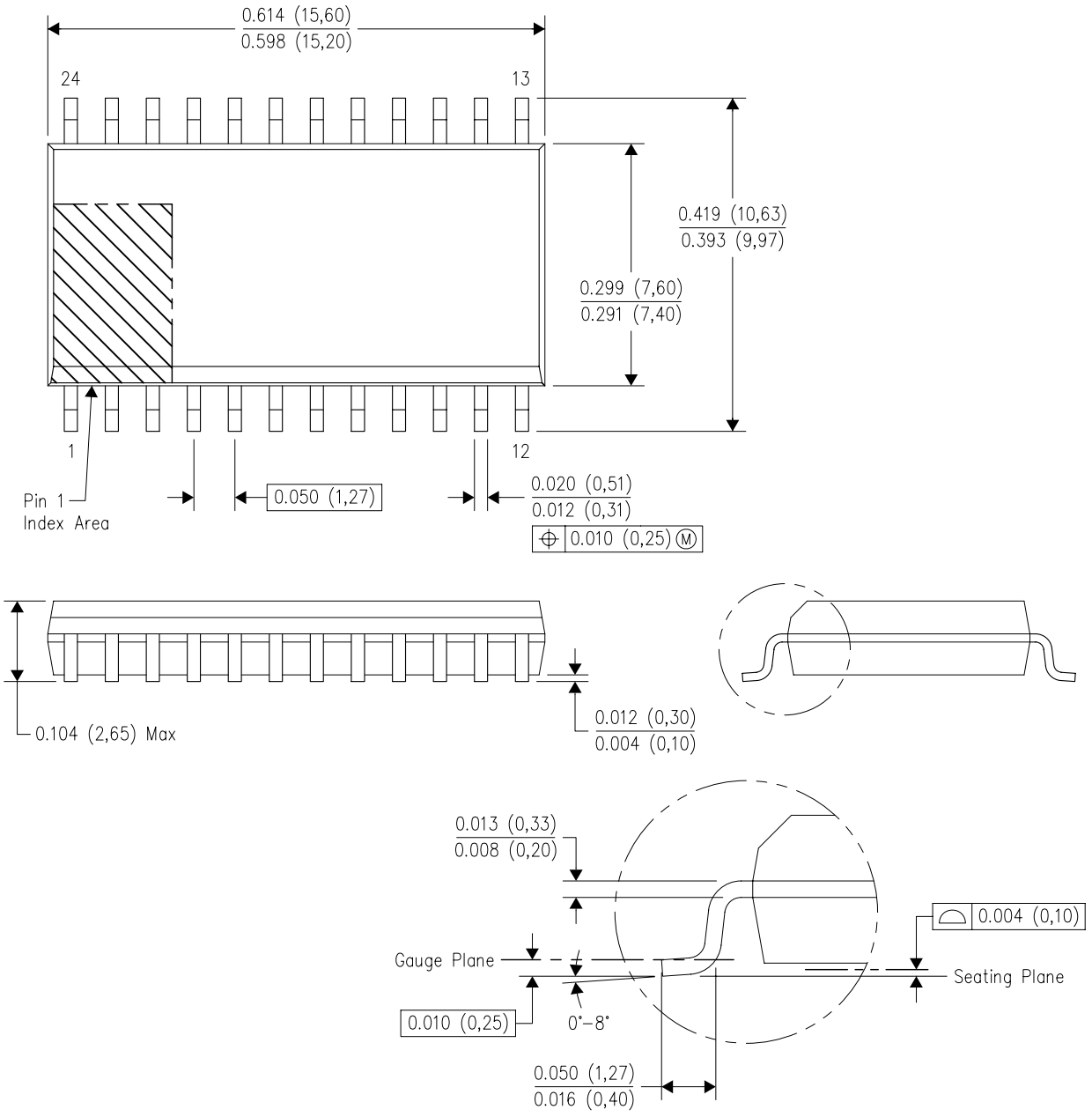
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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