MCP6141/2/3/4

600 nA, Non-Unity Gain Rail-to-Rail Input/Output Op Amps

Features

- Low Quiescent Current: 600 nA/Amplifier (typ.)
- Stable for gains of 10 V/V or higher
- Rail-to-Rail Input: -0.3V (min.) to V_{DD} + 0.3V (max.)
- Rail-to-Rail Output:
  - V_{SS}+10 mV (min.) to V_{DD}-10 mV (max.)
- Gain Bandwidth Product: 100 kHz (typ.)
- Wide Supply Voltage Range: 1.4V to 5.5V (max.)
- Available in Single, Dual and Quad
- Chip Select ($\overline{CS}$) with MCP6143

Applications

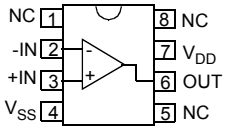
- Toll Booth Tags
- Wearable Products
- Temperature Measurement
- Battery-Powered

Available Tools

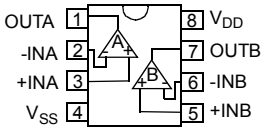
- Spice macro models (at www.microchip.com)
- FilterLab® Software (at www.microchip.com)

Package Types

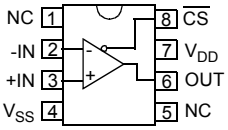
MCP6141
PDIP, SOIC, MSOP



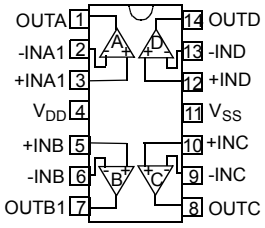
MCP6142
PDIP, SOIC, MSOP



MCP6143
PDIP, SOIC, MSOP



MCP6144
PDIP, SOIC, TSSOP



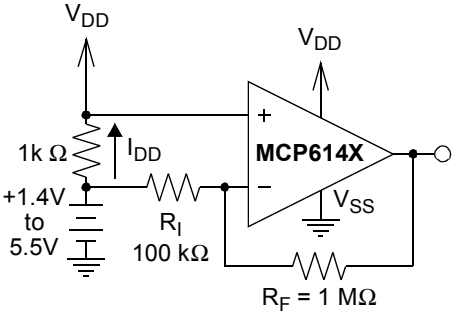
Description

The MCP6141/2/3/4 family of non-unity gain stable operational amplifiers (op amps) from Microchip Technology, Inc. operate with a single supply voltage as low as 1.4V, while drawing less than 1 µA (max.) of quiescent current per amplifier. These devices are also designed to support rail-to-rail input and output swing.

The MCP6141/2/3/4 op amps have a gain bandwidth product of 100 kHz (typ.) and are stable for gains of 10 V/V or higher. This specification makes these devices appropriate for battery-powered applications where higher frequency responses from the amplifier are required.

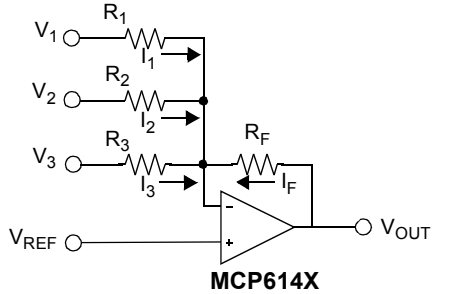
The MCP6141/2/3/4 family of op amps are offered in single (MCP6141), single with a Chip Select ($\overline{CS}$) feature (MCP6143), dual (MCP6142) and quad (MCP6144) configurations.

Typical Applications



High Side Battery Current Sensor

$$G_n = \left(1 + \frac{R_F}{R_I}\right) \geq 10 V/V$$



Summing Amplifier

$$G_n = 1 + R_F\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) \geq 10 V/V$$

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings†

V_{DD} - V_{SS} 7.0V
All inputs and outputs..... V_{SS} -0.3V to V_{DD} +0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....continuous
Current at Input Pins .....±2 mA
Current at Output and Supply Pins .....±30 mA
Storage temperature .....-65°C to +150°C
Junction Temperature, T_J .....+150°C
ESD protection on all pins (HBM:MM)..... ≥ 4 kV:200 V

†Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
+IN/+INA/+INB/+INC/+IND	Non-inverting Inputs
-IN/-INA/-INB/-INC/-IND	Inverting Inputs
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
OUT/OUTA/OUTB/OUTC/OUTD	Outputs
$\overline{CS}$	Chip Select
NC	No internal connection

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{DD} = +1.4V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, and V_{OUT} ~ V_{DD}/2.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						V_{CM} = V_{SS}
Input Offset Voltage	V_{OS}	-3.0	—	+3.0	mV	
Drift with Temperature	$\Delta V_{OS}/\Delta T$	—	±1.5	—	µV/°C	T_A= -40°C to +85°C
Power Supply Rejection	PSRR	70	85	—	dB	
Input Bias Current and Impedance						
Input Bias Current	I_B	—	1.0	—	pA	
Input Bias Current Over-Temperature	I_B	—	—	100	pA	T_A= -40°C to +85°C
Input Offset Current	I_{OS}	—	1.0	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF	
Common Mode						
Common-Mode Input Range	VCMR	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common-Mode Rejection Ratio	CMRR	62	80	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 5.3V
		60	75	—	dB	V_{DD} = 5V, V_{CM} = 2.5V to 5.3V
		60	80	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 2.5V
Open Loop Gain						
DC Open Loop Gain (large signal)	A_{OL}	95	115	—	dB	R_L = 50 kΩ to V_{DD}/2, 100 mV < V_{OUT} < (V_{DD} – 100 mV)
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 10	—	V_{DD} – 10	mV	R_L = 50 kΩ to V_{DD}/2
Output Short Circuit Current	I_O	—	21	—	mA	V_{OUT} = 2.5V, V_{DD} = 5 V
Power Supply						
Supply Voltage	V_{DD}	1.4	—	5.5	V	
Quiescent Current per amplifier	I_Q	0.3	0.6	1.0	µA	I_O = 0

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{DD} = +5V, V_{SS} = GND, T_A = 25 °C, $V_{CM} = V_{DD}/2$, R_L = 1 MΩ to $V_{DD}/2$, C_L = 60 pF, and $V_{OUT} \sim V_{DD}/2$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Gain Bandwidth Product	GBWP	—	100	—	kHz	
Slew Rate	SR	—	24	—	V/ms	
Phase Margin	PM	—	60	—	°	G = +10
Input Voltage Noise	E_n	—	5.0	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Voltage Noise Density	e_n	—	170	—	nV/√Hz	f = 1 kHz
Input Current Noise Density	i_n	—	0.6	—	fA/√Hz	f = 1 kHz

SPECIFICATIONS FOR MCP6143 CHIP SELECT FEATURE

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{DD} = +1.4V to +5.5V, V_{SS} = GND, T_A = 25 °C, $V_{CM} = V_{DD}/2$, R_L = 1 MΩ to $V_{DD}/2$, C_L = 60 pF, and $V_{OUT} \sim V_{DD}/2$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	V_{SS} + 0.3	V	For entire V_{DD} range
$\overline{CS}$ Input Current, Low	I_{CSL}	—	5.0	—	pA	$\overline{CS} = V_{SS}$
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	V_{DD} - 0.3	—	V_{DD}	V	For entire V_{DD} range
$\overline{CS}$ Input Current, High	I_{CSH}	—	5.0	—	pA	$\overline{CS} = V_{DD}$
$\overline{CS}$ Input High, GND Current	I_Q	—	20	—	pA	$\overline{CS} = V_{DD}$
Amplifier Output Leakage, $\overline{CS}$ High		—	20	—	pA	$\overline{CS} = V_{DD}$
Dynamic Specifications						
$\overline{CS}$ Low to Amplifier Output High Turn-on Time	t_{ON}	—	2.0	50	ms	$\overline{CS}$ low = V_{SS} + 0.3V, G = +1 V/V, V_{OUT} = 0.9 $V_{DD}/2$
$\overline{CS}$ High to Amplifier Output High Z	t_{OFF}	—	10	—	µs	$\overline{CS}$ high = V_{DD} - 0.3V, G = +1 V/V V_{OUT} = 0.1 $V_{DD}/2$
Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5V

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{DD} = +1.4V to +5.5V, V_{SS} = GND.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	108	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The MCP6141/2/3/4 family of op amps operates over this extended range, but with reduced performance.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = +5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

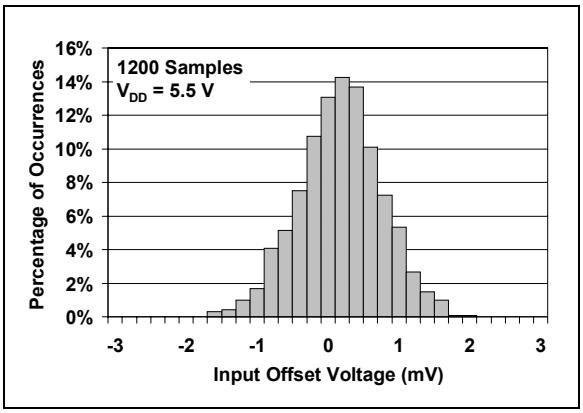


FIGURE 2-1: *Histogram of Input Offset Voltage with V_{DD} = 5.5V.*

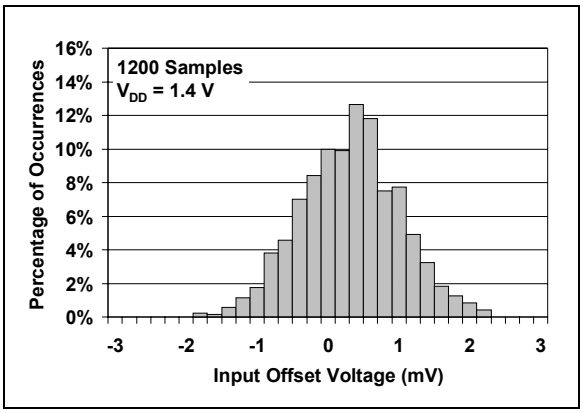


FIGURE 2-2: *Histogram of Input Offset Voltage with V_{DD} = 1.4V.*

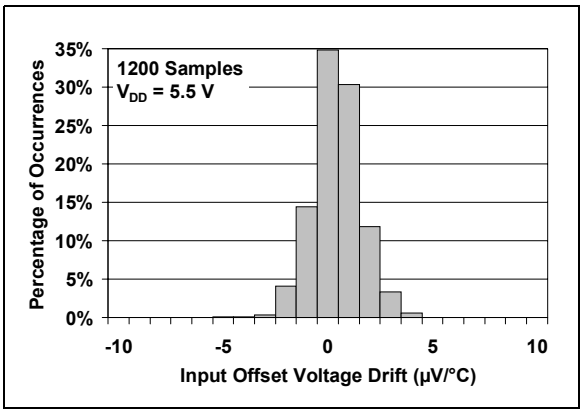


FIGURE 2-3: *Histogram of Input Offset Voltage Drift with V_{DD} = 5.5V.*

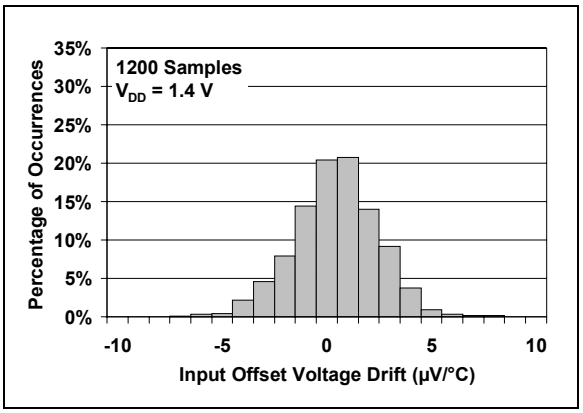


FIGURE 2-4: *Histogram of Input Offset Voltage Drift with V_{DD} = 1.4V.*

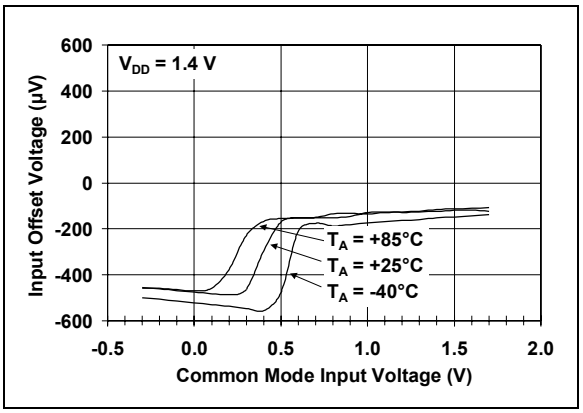


FIGURE 2-5: *Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with V_{DD} = 1.4V.*

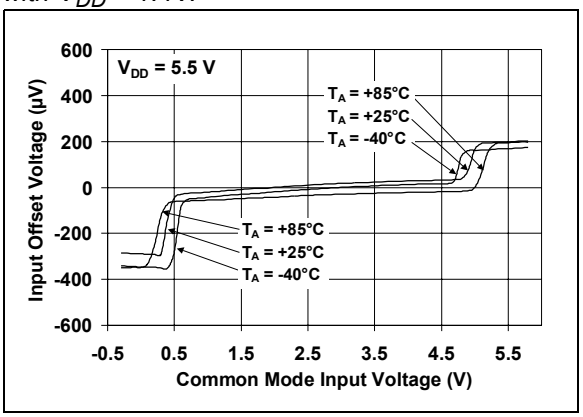


FIGURE 2-6: *Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with V_{DD} = 5.5V.*

Note: Unless otherwise indicated, V_{DD} = +5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

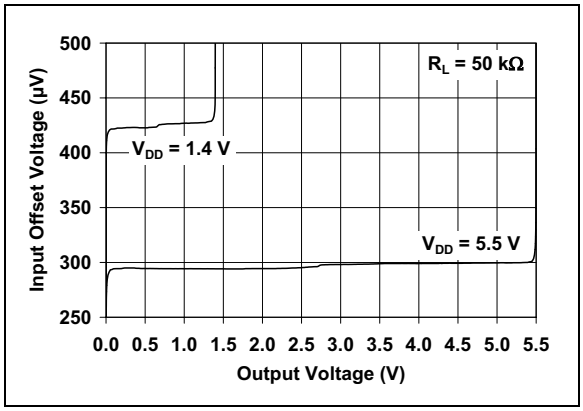


FIGURE 2-7: *Input Offset Voltage vs. Output Voltage vs. Power Supply Voltage.*

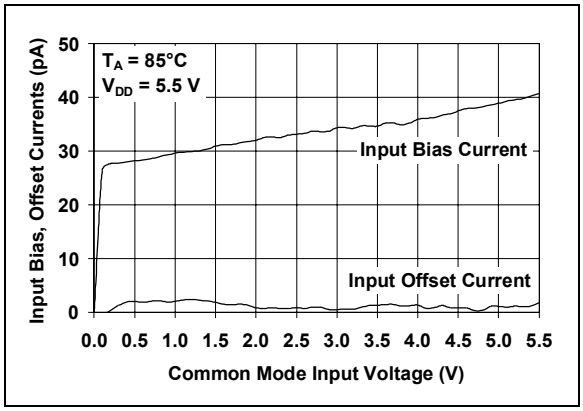


FIGURE 2-10: *Input Bias, Offset Currents vs. Common Mode Input Voltage with Temperature = 85°C.*

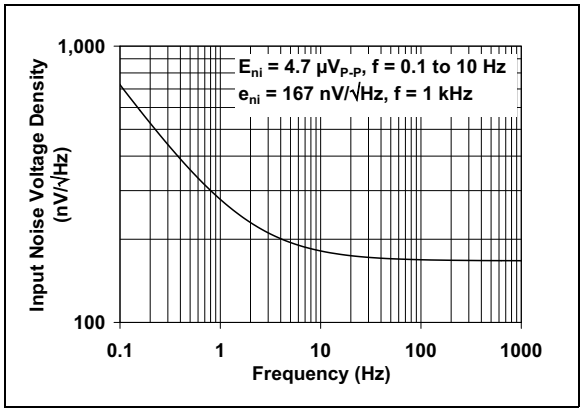


FIGURE 2-8: *Input Noise Voltage Density vs. Frequency.*

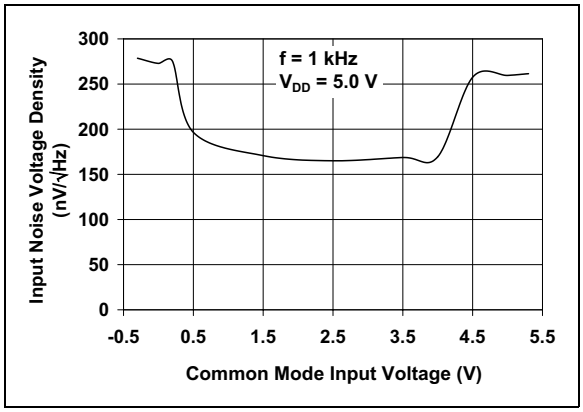


FIGURE 2-11: *Input Noise Voltage Density vs. Common Mode Input Voltage.*

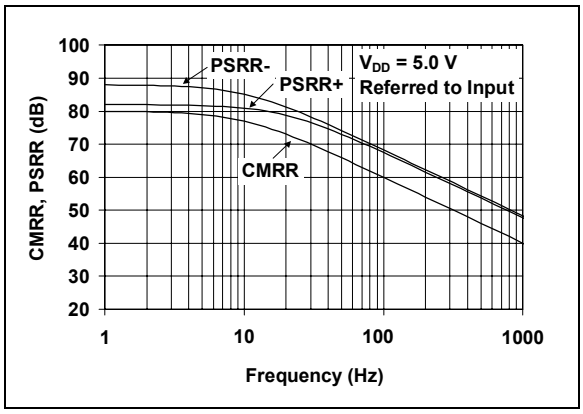


FIGURE 2-9: *Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Frequency.*

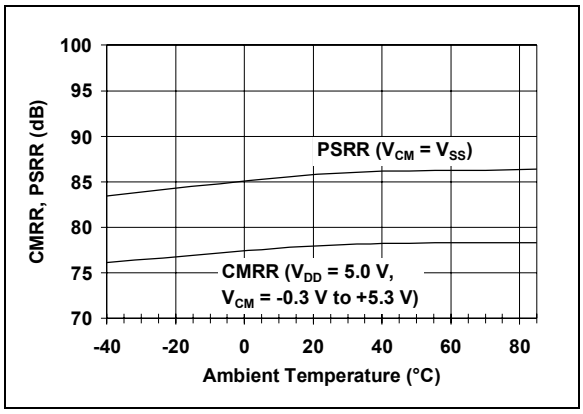


FIGURE 2-12: *Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Ambient Temperature.*

Note: Unless otherwise indicated, V_{DD} = +5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

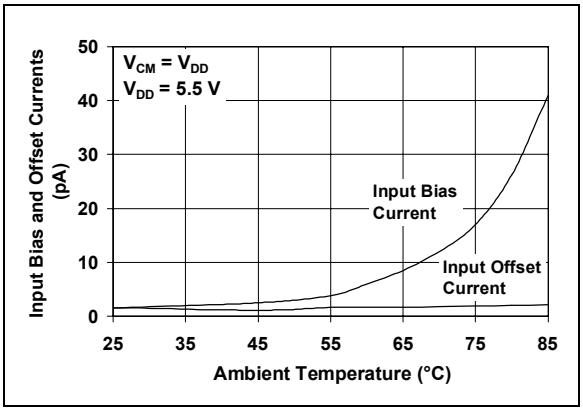


FIGURE 2-13: *Input Bias and Offset Currents vs. Ambient Temperature.*

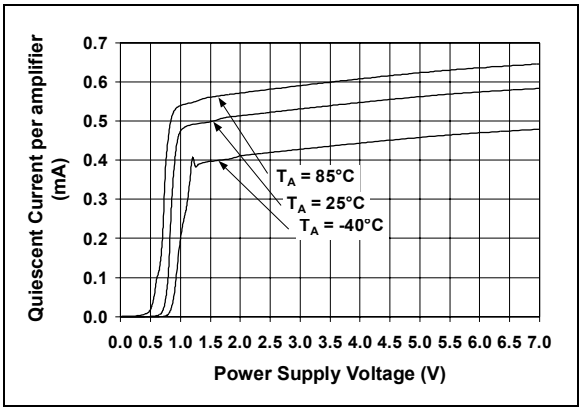


FIGURE 2-16: *Quiescent Current Vs. Power Supply Voltage vs. Temperature.*

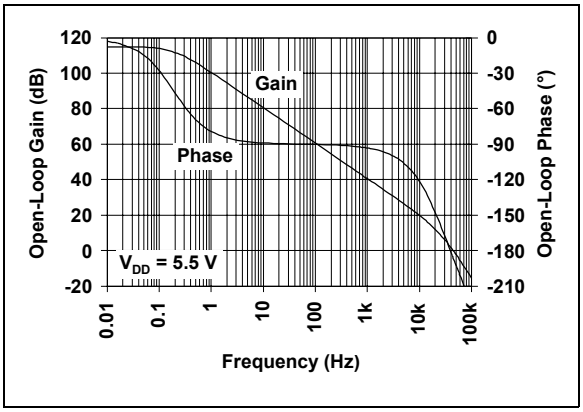


FIGURE 2-14: *Open Loop Gain, Phase vs. Frequency with V_{DD} = 5.5V.*

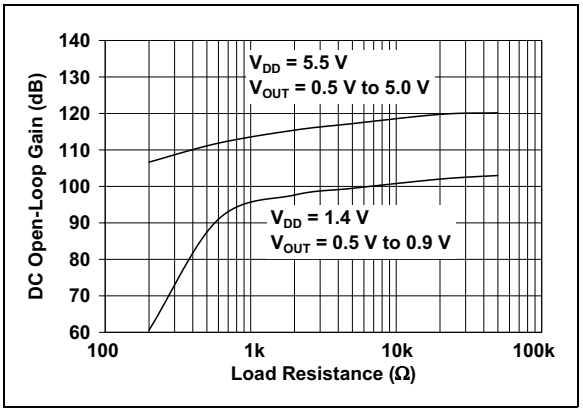


FIGURE 2-17: *DC Open Loop Gain vs. Load Resistance vs. Power Supply Voltage.*

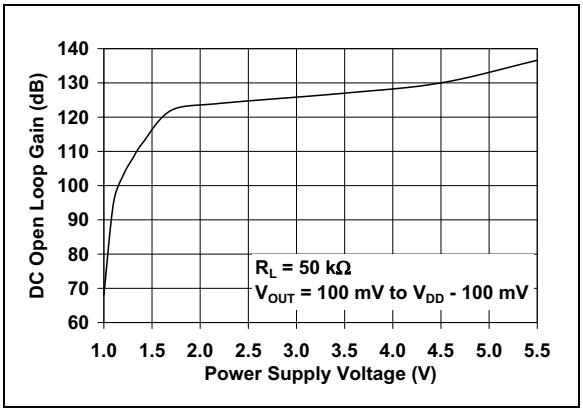


FIGURE 2-15: *DC Open Loop Gain vs. Power Supply Voltage.*

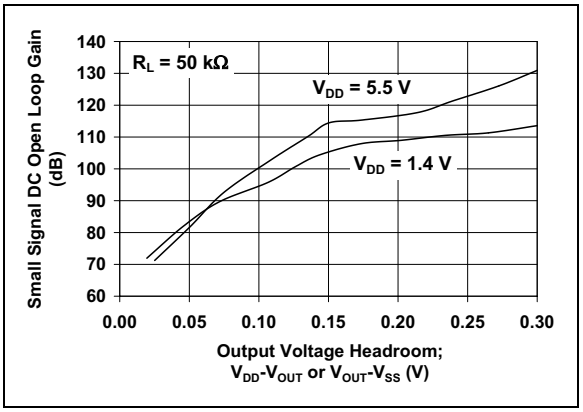


FIGURE 2-18: *Small Signal DC Open Loop Gain vs. Output Voltage Headroom vs. Power Supply.*

Note: Unless otherwise indicated, V_{DD} = +5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

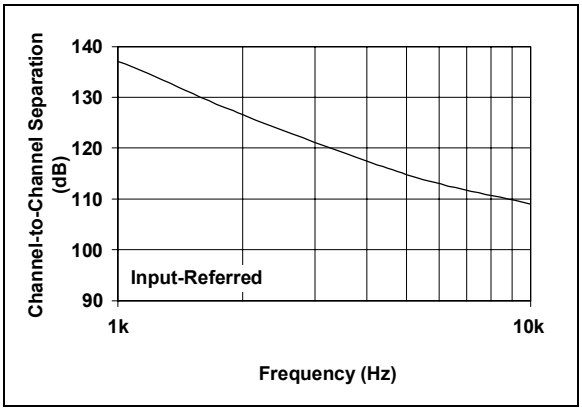


FIGURE 2-19: *Channel to Channel Separation vs. Frequency (MCP6142 and MCP6144 only).*

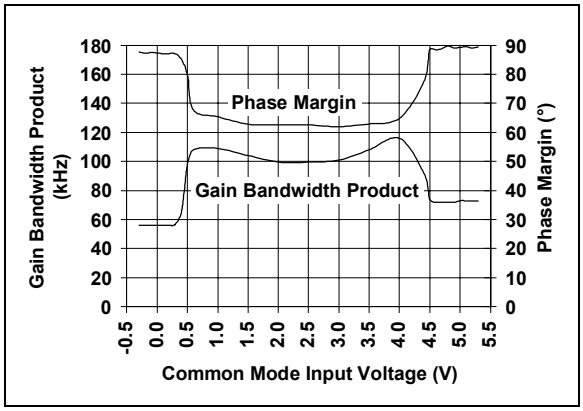


FIGURE 2-22: *Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage.*

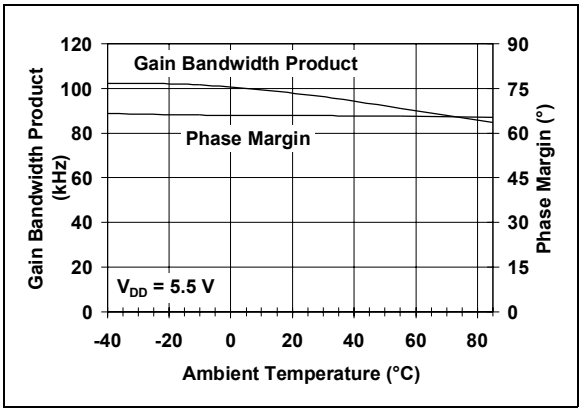


FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature with V_{DD} = 5.5V.*

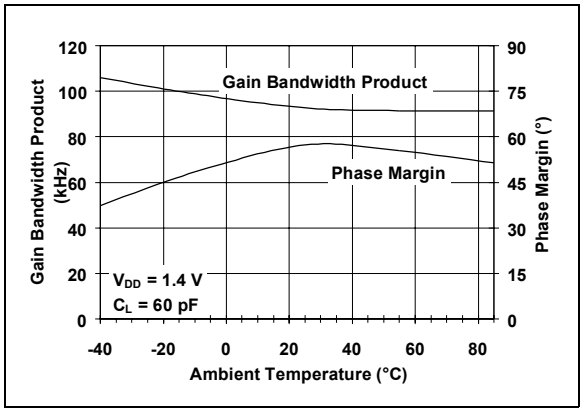


FIGURE 2-23: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature with V_{DD} = 1.4V.*

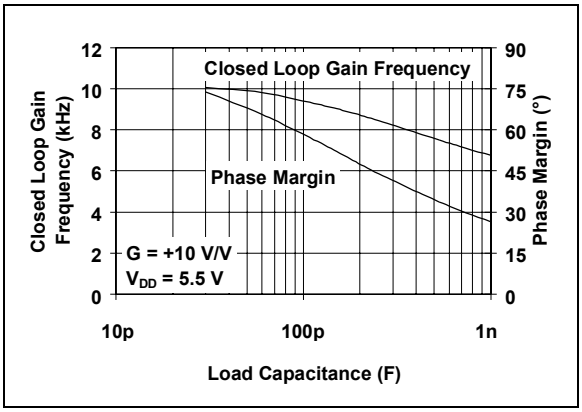


FIGURE 2-21: *Closed Loop Gain Frequency, Phase Margin vs. Load Capacitance with V_{DD} = 5.5V.*

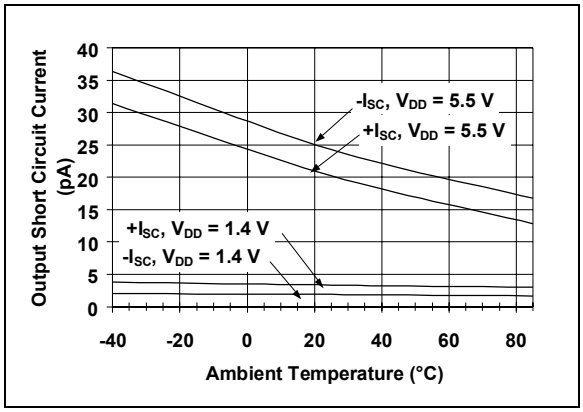


FIGURE 2-24: *Output Short Circuit Current vs. Ambient Temperature vs. Power Supply Voltage.*

Note: Unless otherwise indicated, V_{DD} = +5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

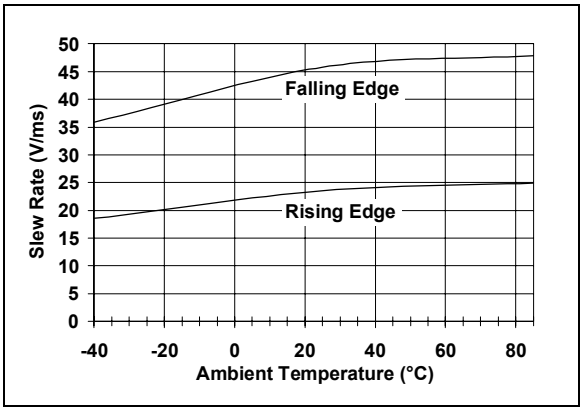


FIGURE 2-25: *Slew Rate vs. Ambient Temperature.*

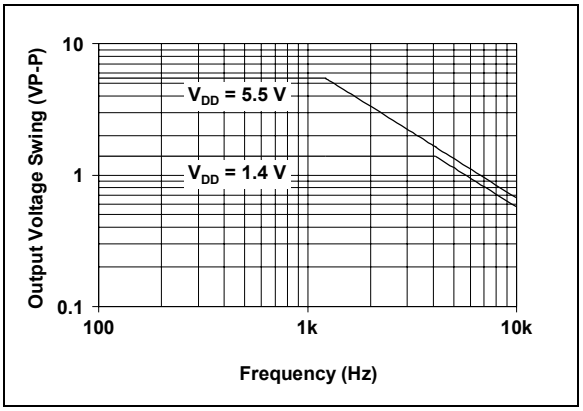


FIGURE 2-28: *Output Voltage Swing vs. Frequency vs. Power Supply Voltage.*

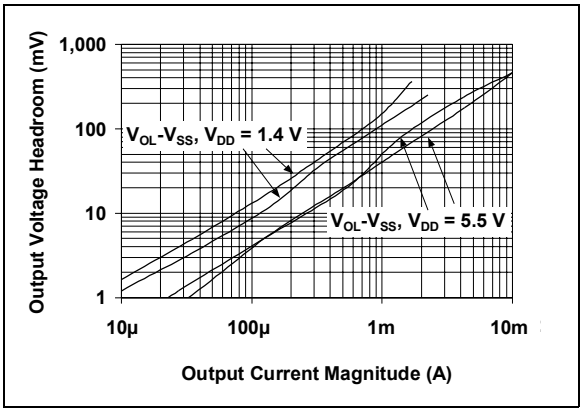


FIGURE 2-26: *Output Voltage Headroom vs. Output Current Magnitude vs. Power Supply Voltage.*

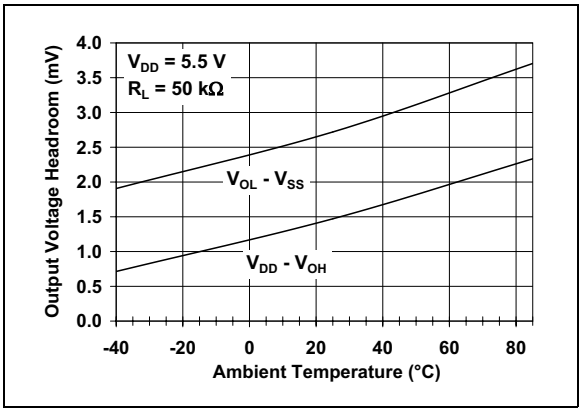


FIGURE 2-29: *Output Voltage Headroom vs. Ambient Temperature with V_{DD} = 5.5V.*

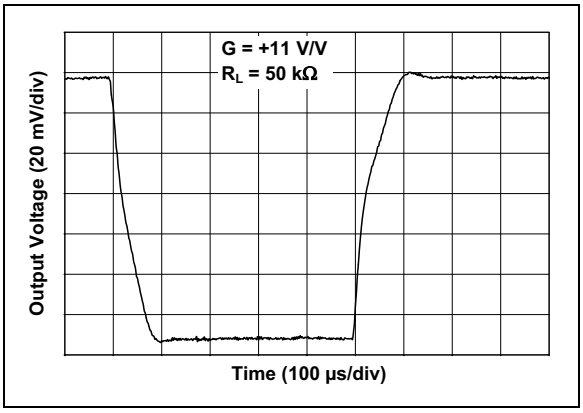


FIGURE 2-27: *Small Signal Non-Inverting Pulse Response vs. Time.*

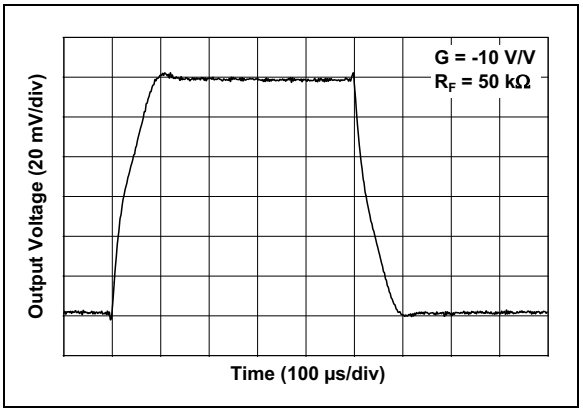


FIGURE 2-30: *Small Signal Inverting Pulse Response vs. Time.*

Note: Unless otherwise indicated, V_{DD} = +5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

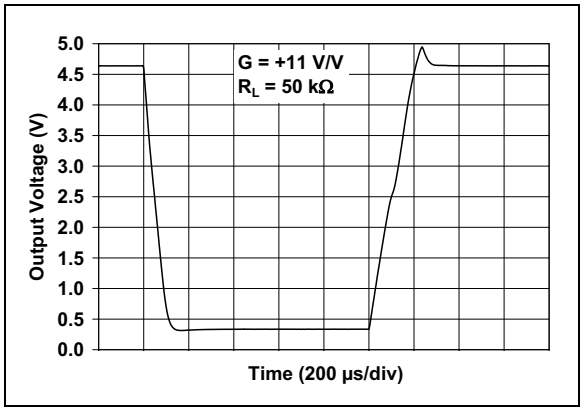


FIGURE 2-31: *Large Signal Non-Inverting Pulse Response vs. Time.*

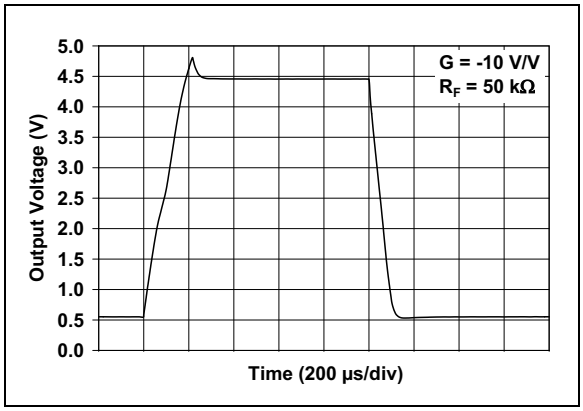


FIGURE 2-34: *Large Signal Inverting Pulse Response vs. Time.*

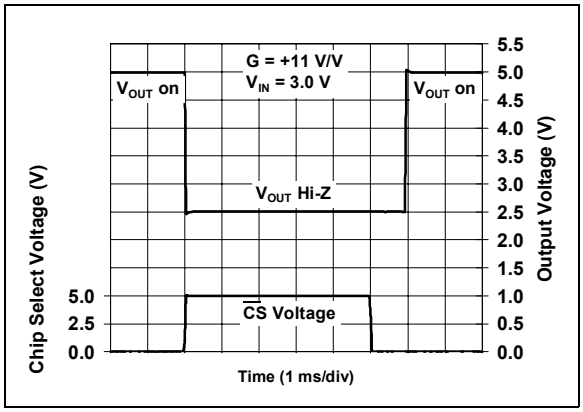


FIGURE 2-32: *Chip Select ($\overline{CS}$) to Amplifier Output Response Time (MCP6143 only).*

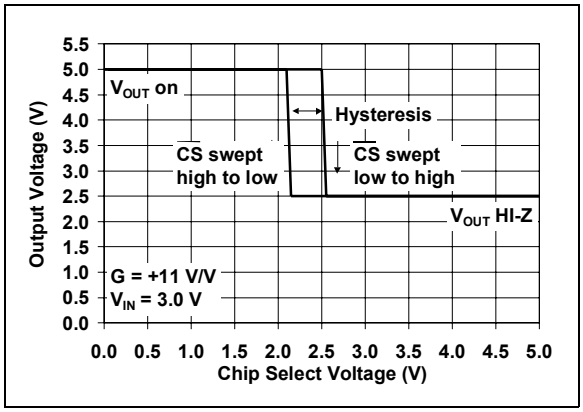


FIGURE 2-35: *Output Voltage vs. Chip Select ($\overline{CS}$) Voltage (MCP6143 only).*

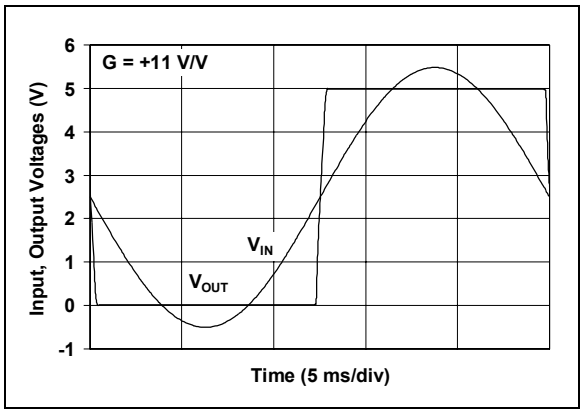


FIGURE 2-33: *The MCP6141/2/3/4 family shows no phase reversal (for information only– the Maximum Absolute Input Voltage is still V_{SS} - 0.3V and V_{DD} + 0.3V).*

3.0 APPLICATIONS INFORMATION

The MCP6141/2/3/4 family of operational amplifiers are fabricated on Microchip's state-of-the-art CMOS process. They are stable for noise gain of 10 V/V or higher. Microchip also produces a unity gain stable product, the MCP6041/2/3/4 family, which has similar specifications. The MCP6041/2/3/4 family has a bandwidth of 1.4 kHz at a noise gain of 10 V/V, while the MCP6141/2/3/4 family has a bandwidth of 10 kHz at a noise gain of 10 V/V. These devices are suitable for a wide range of applications requiring very low power consumption. With these op amps, the power supply pin needs to be bypassed with a 0.1 µF capacitor.

3.1 Rail-to-Rail Input

The input stage of these devices uses two differential input stages in parallel; one operates at low V_{CM} (common mode input voltage) and the other at high V_{CM}. With this topology, the MCP6141/2/3/4 family operates with V_{CM} up to 300 mV past either supply rail. The Input Offset Voltage is measured at both $V_{CM} = V_{SS}$ - 0.3V and V_{DD} + 0.3V to ensure proper operation.

3.2 Output Loads and Battery Life

The MCP6141/2/3/4 op amp family has low quiescent current, which supports battery-powered applications. There is minimal quiescent current glitch when chip select ($\overline{CS}$) is raised or lowered. This prevents excessive current draw and reduced battery life when the part is turned off or on.

Heavy resistive loads at the output can cause excessive battery drain. Driving a DC voltage of 2.5V across a 100 kΩ load resistor will cause the supply current to increase by 25 µA, depleting the battery 43 times as fast as I_Q (0.6 µA typ) alone.

High frequency signals (fast edge rate) across capacitive loads will also significantly increase supply current. For instance, a 0.1 µF capacitor at the output presents an AC impedance of 15.9 kΩ ($1/2\pi fC$) to a 100 Hz sinewave. It can be shown that the average power drawn from the battery by a 5.0 V_{p-p} sinewave (1.77 Vrms) under these conditions is:

EQUATION

$$\begin{aligned} P_{SUPPLY} &= (V_{DD} - V_{SS})(I_Q + V_{L(p-p)} f C_L) \\ &= (5V)(0.6\mu A + 5.0V_{p-p} \cdot 100Hz \cdot 0.1\mu F) \\ &= 3.0\mu W + 50\mu W \end{aligned}$$

This will drain the battery 18 times as fast as I_Q alone.

3.3 Rail-to-Rail Output

The MCP6141/2/3/4 family Maximum Output Voltage Swing defines the maximum swing possible under a particular output load. According to the specification table, the output can reach up to 10 mV of either supply rail with a 50 kΩ load.

3.4 Input Voltage and Phase Reversal

The MCP6141/2/3/4 op amp family uses CMOS transistors at the input. It is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-33 shows an input voltage exceeding both supplies without output phase reversal.

The maximum operating V_{CM} that can be applied to the inputs is V_{SS} -0.3V and V_{DD} + 0.3V. Voltage on the input that exceeds this absolute maximum rating can cause excessive current to flow in or out of the input pins. Current beyond ±2 mA can cause possible reliability problems. Applications that exceed this rating must be externally limited with an input resistor, as shown in Figure 3-1.

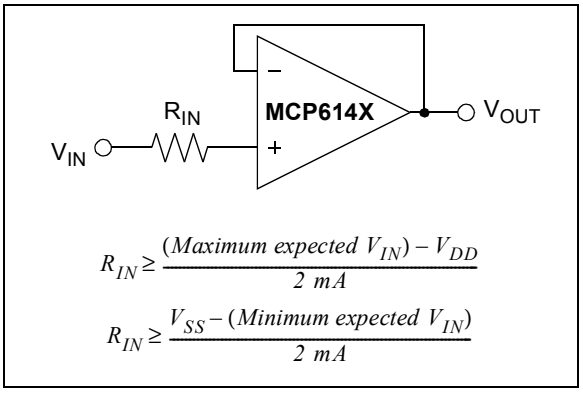


FIGURE 3-1: *An input resistor, R_{IN}, should be used to limit excessive input current if the inputs exceed the absolute maximum specification.*

3.5 Stability

The MCP6141/2/3/4 op amp family is designed to give high bandwidth and faster slew rate for circuits with high noise (G_n) or signal gain. The related unity-gain stable MCP6041/2/3/4 op amp family has lower AC performance, but it is preferable for low noise gain applications.

Noise gain is defined to be the gain from a voltage source at the non-inverting input to the output when all other voltage sources are zeroed (shorted out). Noise gain is independent of signal gain and depends only on components in the feedback loop.

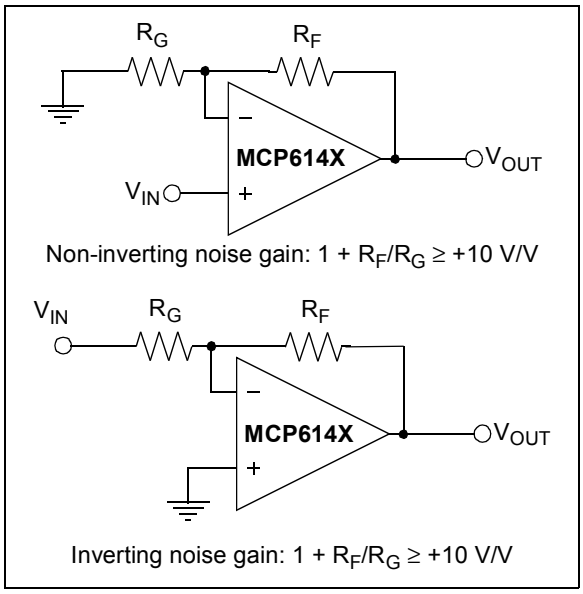


FIGURE 3-2: *Noise gain for inverting and non-inverting amplifier configuration.*

Figure 3-2 shows non-inverting and inverting amplifier circuits. In order for the amplifiers to be stable, the noise gain should meet the specified requirement:

EQUATION

$$G_n = 1 + \frac{R_F}{R_G} \geq 10V/V$$

Note that an inverting signal gain of G = -9 V/V corresponds to a noise gain G_n = +10 V/V.

Figure 3-3 shows a unity gain buffer and integrator that are unstable when used with the MCP6141/2/3/4 family. However, they are suitable for the MCP6041/2/3/4 family.

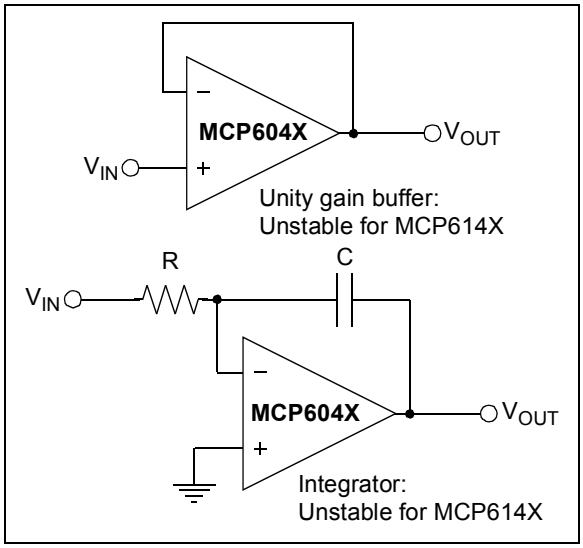


FIGURE 3-3: *Typical Circuits that are not suitable for the MCP6141/2/3/4 family.*

Note that the integrator circuit in Figure 3-3 becomes unity gain at high frequencies because of the capacitor. Therefore, this circuit is unstable for the MCP6141/2/3/4.

3.6 Capacitive Load and Stability

Driving capacitive loads can cause stability problems with voltage feedback op amps. Figure 2-21 shows how increasing the load capacitance will decrease the phase margin. While a phase margin above 60° is ideal, 45° is on the verge of instability. As can be seen, up to C_L = 150 pF can be placed on the MCP6141/2/3/4 op amp outputs without any problems, while 250 pF creates a 45° phase margin.

When the op amp is required to drive large capacitive loads (C_L >150 pF), a small series resistor (R_{ISO} in Figure 3-4) at the output of the amplifier improves the phase margin. This resistor makes the output load resistive at higher frequencies, which improves the phase margin. The bandwidth reduction caused by the capacitive load, however, is not changed. To select R_{ISO}, start with 1 kΩ, then use the MCP6141 SPICE macro model and bench testing to adjust R_{ISO} until there is a minimum frequency response peaking.

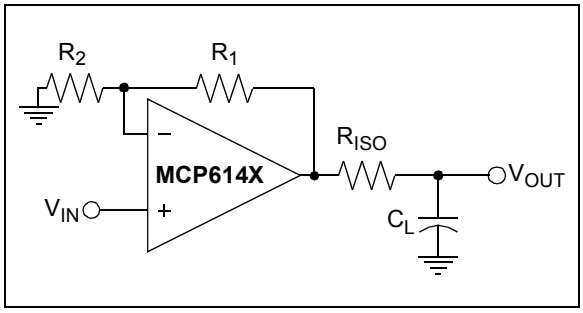


FIGURE 3-4: *Amplifier circuit for heavy capacitive loads.*

3.7 The MCP6143 Chip Select ($\overline{CS}$) Option

The MCP6143 is a single amplifier with a chip select ($\overline{CS}$) option. When $\overline{CS}$ is pulled high, the supply current drops to 20 pA (typ.) and goes through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier is put into a high impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the amplifier will not operate properly. Figure 3-5 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

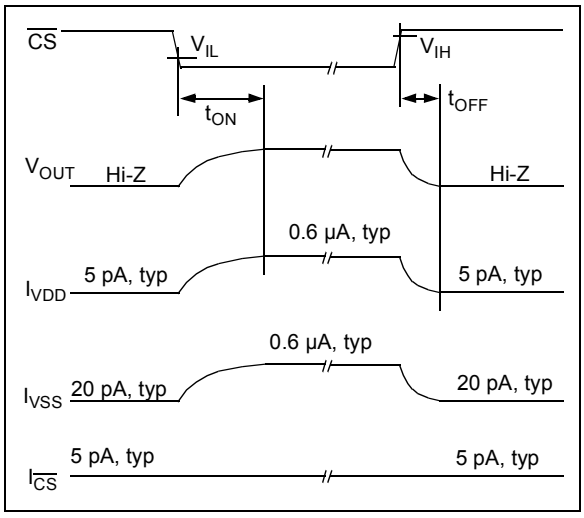


FIGURE 3-5: *Timing Diagram for the $\overline{CS}$ function on the MCP6143 op amp.*

3.8 Layout Considerations

Good PC board layout techniques will help you achieve the performance shown in the specifications and typical performance curves. It will also assist in minimizing Electro-Magnetic Compatibility (EMC) issues.

3.8.1 SURFACE LEAKAGE

In applications where low input bias current is critical, PC board surface leakage effects and signal coupling from trace to trace need to be considered.

Surface leakage is caused by a difference in voltage between traces, combined with high humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the input current of the MCP6141/2/3/4 family at 25°C (1 pA, typ).

The simplest technique to reduce surface leakage is using a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin or trace. Figure 3-6 shows an example of a typical layout.

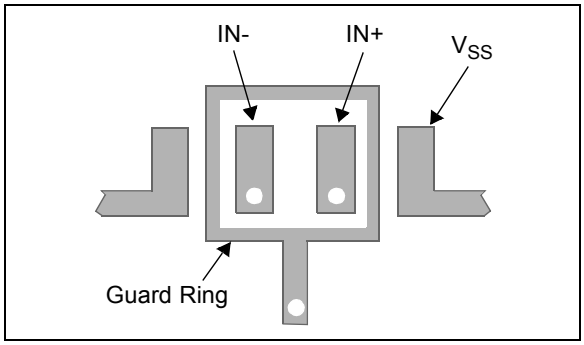


FIGURE 3-6: *Example of Guard Ring layout.*

Circuit schematics for different guard ring implementations are shown in Figure 3-7. Figure 3-7A biases the guard ring to the input common mode voltage, which is most effective for non-inverting gains. Figure 3-7B biases the guard ring to a reference voltage (V_{REF}, which can be ground), which is useful for inverting gains and precision photo sensing circuits.

Figure 3-7A

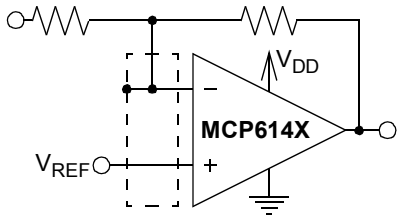


Figure 3-7B

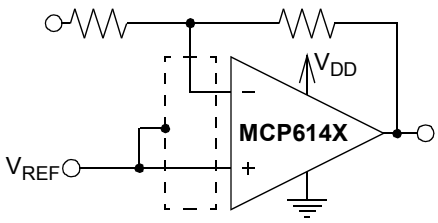


FIGURE 3-7: *Two possible guard ring connection strategies to reduce surface leakage effects.*

3.8.2 COMPONENT PLACEMENT

In order to help prevent crosstalk:

- Separate digital components from analog components, and low speed devices from high speed devices.
- Keep sensitive traces short and straight. Separate them from interfering components and traces. This is especially important for high frequency (low rise time) signals.
- Use a 0.1 µF supply bypass capacitor within 0.1" (2.5 mm) of the V_{DD} pin. It must connect directly to the ground plane.

3.8.3 SIGNAL COUPLING

The input pins of the MCP6141/2/3/4 family of op amps are high impedance, which allows noise injection. This noise can be capacitively or magnetically coupled. In either case, using a ground plane helps reduce noise injection.

When noise is coupled capacitively, the ground plane provides shunt capacitance to ground for high frequency signals (Figure 3-8 shows the equivalent circuit). The coupled current, I_M, produces a lower voltage ($V_{TRACE\ 2}$) on the victim trace when the trace to ground plane capacitance (C_{SH2}) is large and the terminating resistor (R_{T2}) is small. Increasing the distance between traces and using wider traces also helps.

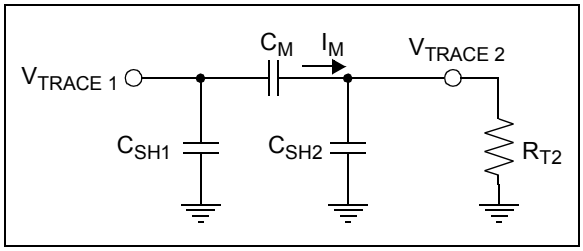


FIGURE 3-8: *Equivalent circuit for capacitive coupling between traces on a PC board (with ground plane).*

When noise is coupled magnetically, the ground plane reduces the mutual inductance between traces. This occurs because the ground return current at high frequencies will follow a path directly beneath the signal trace. Increasing the separation between traces makes a significant difference. Changing the direction of one of the traces can also reduce magnetic coupling.

If these techniques are not enough, it may help to place guard traces next to the victim trace. They should be on both sides of the victim trace and be as close as possible. Connect the guard traces to ground plane at both ends and in the middle for long traces.

3.9 Typical Applications

3.9.1 BATTERY CURRENT SENSING

The MCP6141/2/3/4 op amps' Common Mode Input Range, which goes 300 mV beyond both supply rails, supports their use in high side and low side battery current sensing applications. The very low quiescent current (0.6 µA, typ.) help prolong battery life, while the rail-to-rail output allows you to detect low currents.

Figure 3-9 shows a high side battery current sensor circuit. The feedback and input resistors are sized to minimize power losses. The battery current (I_{DD}) through the 1 kΩ resistor causes its top terminal to be more negative than the bottom terminal. This keeps the common mode input voltage of the op amp ≤ V_{DD}, which is within its allowed range. The output of the op amp can reach V_{DD} - 0.1 mV (see Figure 2-26), which is a smaller error than the offset voltage.

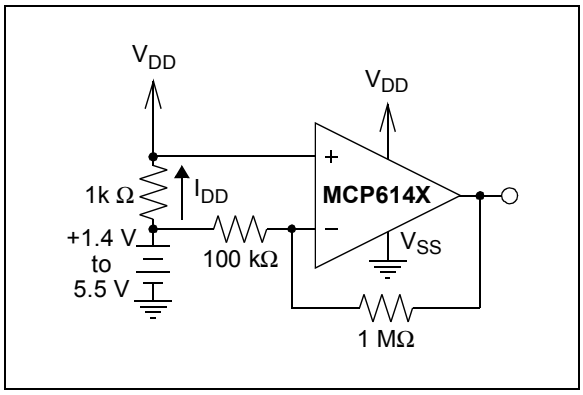


FIGURE 3-9: *High Side Battery Current Sensor.*

3.9.2 SUMMING AMPLIFIER

The rail-to-rail input and output, the 600 nA (typ.) quiescent current and the wide bandwidth make the MCP6141/2/3/4 family of operational amplifiers fit well in a summing amplifier circuit, as shown in Figure 3-10.

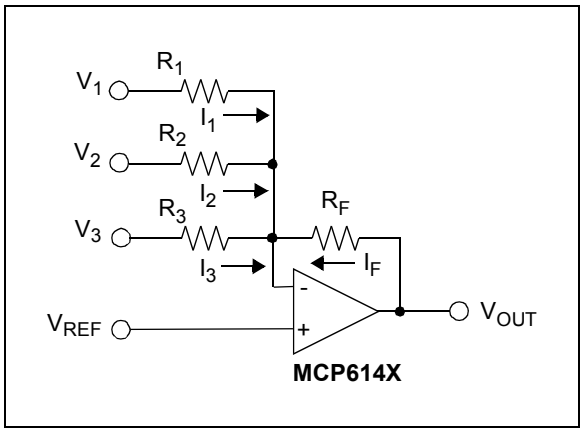


FIGURE 3-10: *Summing amplifier circuit.*

In this configuration, the amplifier outputs the sum of the three input voltages. The ratio of the sum and the output voltage is defined using the feedback and input resistors. V_{REF} is used to offset the output voltage. This family of amplifiers is stable for noise gain (G_n) of 10 V/V or higher. The G_n and the signal gain of the summing amplifier is calculated as shown below:

EQUATION

Noise Gain:

$$G_n = 1 + R_F\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) \geq 10\ V/V$$

Signal Gain:

$$V_{01} = \frac{-R_F}{R_1} \times V_1$$

$$V_{02} = \frac{-R_F}{R_2} \times V_2$$

$$V_{03} = \frac{-R_F}{R_3} \times V_3$$

$$V_{04} = \left(1 + \frac{R_F}{R_1} + \frac{R_F}{R_2} + \frac{R_F}{R_3}\right) \times V_{REF}$$

$$V_{OUT} = V_{01} + V_{02} + V_{03} + V_{04}$$

$$V_{OUT} = R_F\left[\frac{V_{REF} - V_1}{R_1} + \frac{V_{REF} - V_2}{R_2} + \frac{V_{REF} - V_3}{R_3}\right] + V_{REF}$$

At a noise gain of 10 V/V, the amplifier bandwidth is approximately 10 kHz. The bandwidth to quiescent current ratio of MCP6141/2/3/4 makes this device an appropriate choice for battery-powered applications.

4.0 SPICE MACRO MODEL

The Spice macro model for the MCP6141, MCP6142, MCP6143 and MCP6144 simulates the typical amplifier performance of offset voltage, DC power supply rejection, input capacitance, DC common mode rejection, open loop gain over frequency, phase margin, output swing, DC power supply current, power supply current change with supply voltage, input common mode range, output voltage range vs. load and input voltage noise.

The characteristics of the MCP6141, MCP6142, MCP6143 and MCP6144 amplifiers are similar in terms of performance and behavior. This single op amp macro model supports all four devices, with the exception of the chip select function of the MCP6143, which is not modeled.

The listing for this macro model is shown on the next page. The most recent revision of the model can be downloaded from Microchip's web site at www.microchip.com.

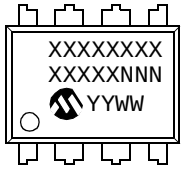
```
.SUBCKT MCP6141 1 2 3 4 5
*               | | | | |
*               | | | | Output
*               | | | Negative Supply
*               | | Positive Supply
*               | Inverting Input
*               Non-inverting Input
*
* Macromodel for the MCP6141/2/3/4 op amp family:
*   MCP6141 (single)
*   MCP6142 (dual)
*   MCP6143 (single w/ CS; chip select is not modeled)
*   MCP6144 (quad)
*
* Revision History:
*   REV A: 06-Sep-02, KEB (created model)
*
* Recommendations:
*   Use PSPICE (or SPICE 2G6; other simulators may require translation)
*   For a quick, effective design, use a combination of: data sheet
*     specs, bench testing, and simulations with this macromodel
*   For high impedance circuits, set GMIN=100F in the .OPTIONS
*     statement
*
* Supported:
*   Typical performance at room temperature (25 degrees C)
*   DC, AC, Transient, and Noise analyses.
*   Most specs, including: offsets, DC PSRR, DC CMRR, input impedance,
*     open loop gain, voltage ranges, supply current, ... , etc.
*
* Not Supported:
*   Chip select (MCP6143)
*   Variation in specs vs. Power Supply Voltage
*   Distortion (detailed non-linear behavior)
*   Temperature analysis
*   Process variation
*   Behavior outside normal operating region
*
* Input Stage
V10  3 10 -300M
R10 10 11 258K
R11 10 12 258K
C11 11 12 3.53P
C12  1  0 6.00P
E12  1 14 POLY(4) 20 0 21 0 26 0 27 0   1.00M 117 117 1 1
I12 14  0 1.50P
M12 11 14 15 15 NMI L=2.00U W=5.00U
C13 14  2 6.00P
M14 12  2 15 15 NMI L=2.00U W=5.00U
I14  2  0 500E-15
C14  2  0 6.00P
```

```
I15 15  4 300N
V16 16  4 200M
D16 16 15 DL
V13  3 13 50.0M
D13 14 13 DL
*
* Noise, PSRR, and CMRR
I20 21 20 423U
D20 20  0 DN1
D21  0 21 DN1
G26  0 26 POLY(1) 3 4   308U -56.0U
R26 26  0 1
G27  0 27 POLY(2) 1 3 2 4   -979U 178U 178U
R27 27  0 1
*
* Open Loop Gain, Slew Rate
G30  0 30 POLY(1) 12 11   0 1.00K
R30 30  0 1
E31 31  0 POLY(1) 3 4   29.3 1.05
D31 30 31 DL
E32  0 32 POLY(1) 3 4   57.0 2.04
D32 32 30 DL
G33  0 33 POLY(1) 30 0   0 562
R33 33  0 1
C33 33  0 838M
G34  0 34 POLY(1) 33 0   0 1.00
R34 34  0 1.00
C34 34  0 8.53U
G35  0 35 POLY(2) 34 0 33 34   0 1.00 1.22
R35 35  0 1.00
*
* Output Stage
G50  0 50 POLY(1) 57 5   0 1.00
D51 50 51 DL
R51 51  0 1K
D52 52 50 DL
R52 52  0 1K
G53  3  0 POLY(1) 51 0   300N  1M
G54  0  4 POLY(1) 52 0   300N  -1M
E55 55  0 POLY(2) 3 0 51 0   -10M 1 -100M
D55 57 55 DLS
E56 56  0 POLY(2) 4 0 52 0    10M 1 -100M
D56 56 57 DLS
G57  0 57 POLY(3) 3 0 4 0 35 0   0 17.8U 17.8U 35.5U
R57 57  0 28.2K
R58 57  5 1.00
C58  5  0 2.00P
*
* Models
.MODEL NMI NMOS
.MODEL DL  D   N=1   IS=1F
.MODEL DLS D   N=10M IS=1F
.MODEL DN1 D   IS=1F KF=1.17E-18 AF=1
*
.ENDS MCP6141
```

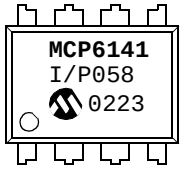
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

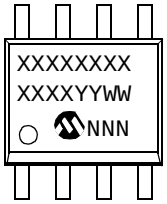
8-Lead PDIP (300 mil)



Example:



8-Lead SOIC (150 mil)



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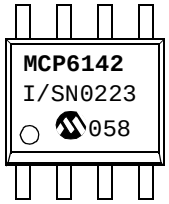
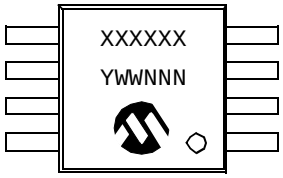


8-Lead MSOP



Example:

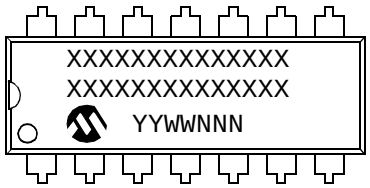
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

5.1 Package Marking Information (Continued)

14-Lead PDIP (300 mil) (MCP6144)



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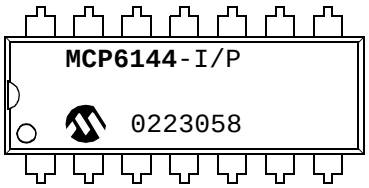
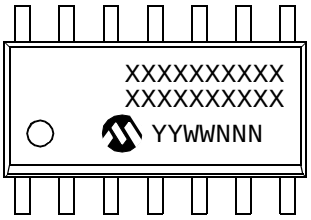
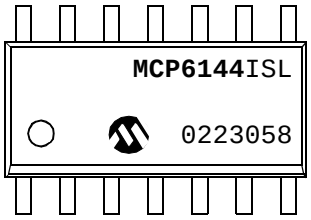


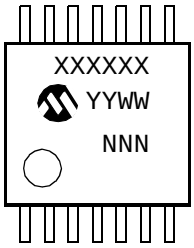
14-Lead SOIC (150 mil) (MCP6144)



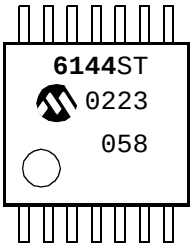
Example:



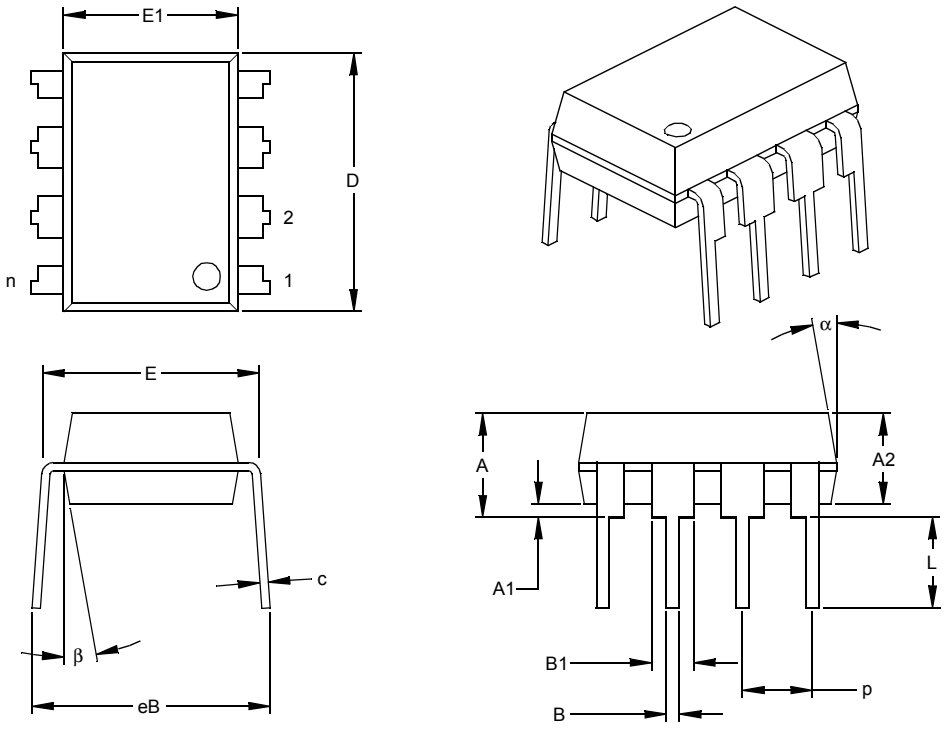
14-Lead TSSOP (MCP6144)



Example:



8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

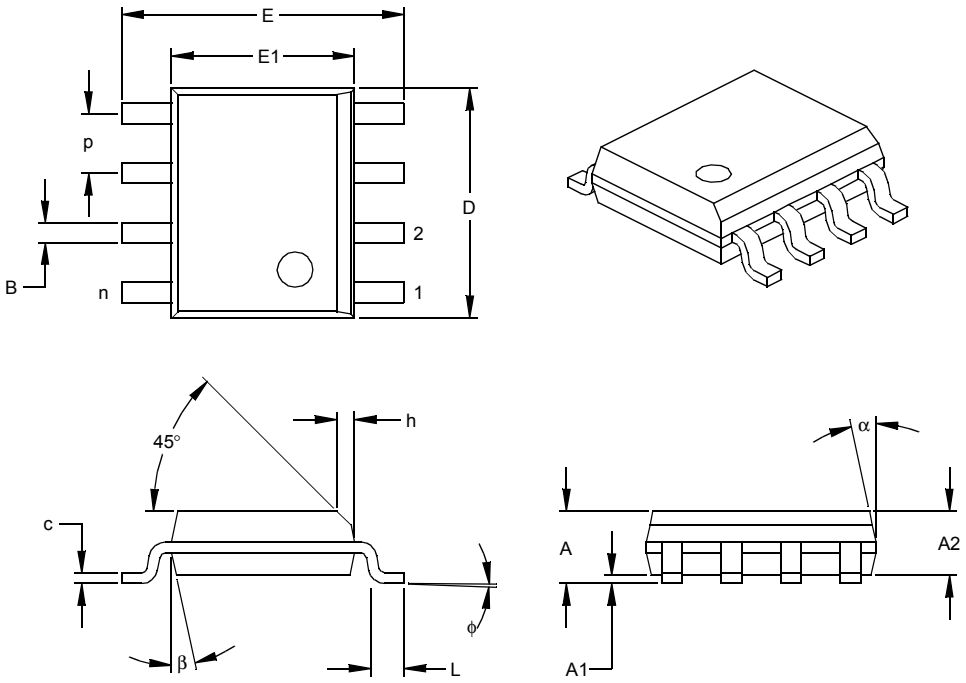


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

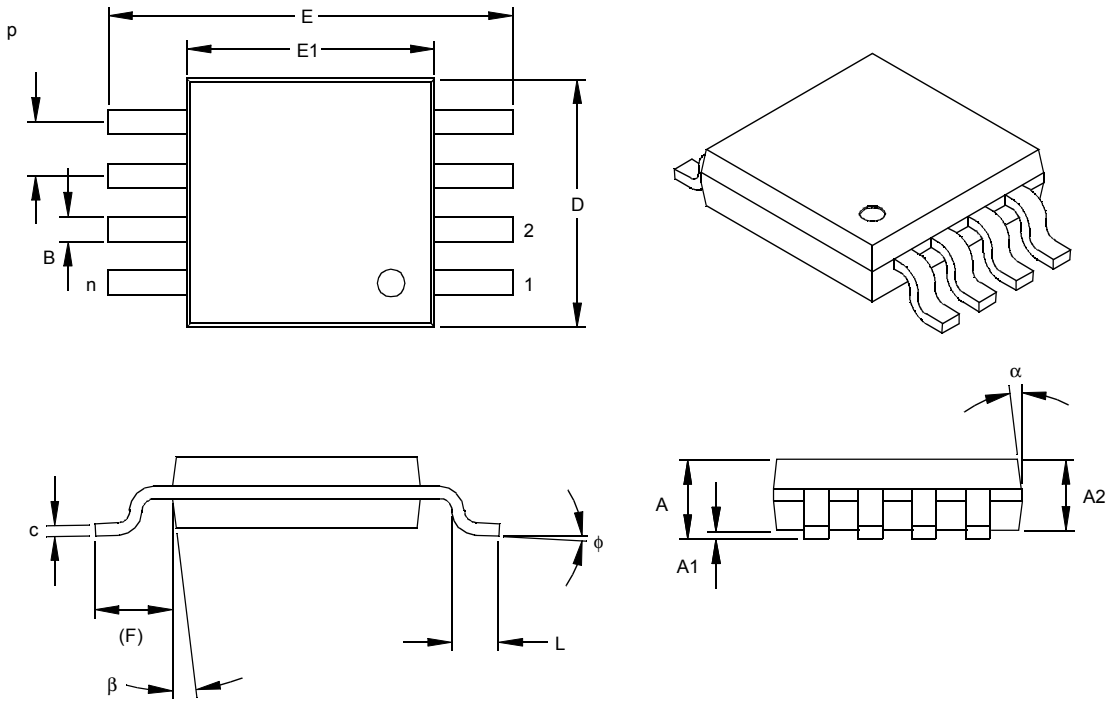


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



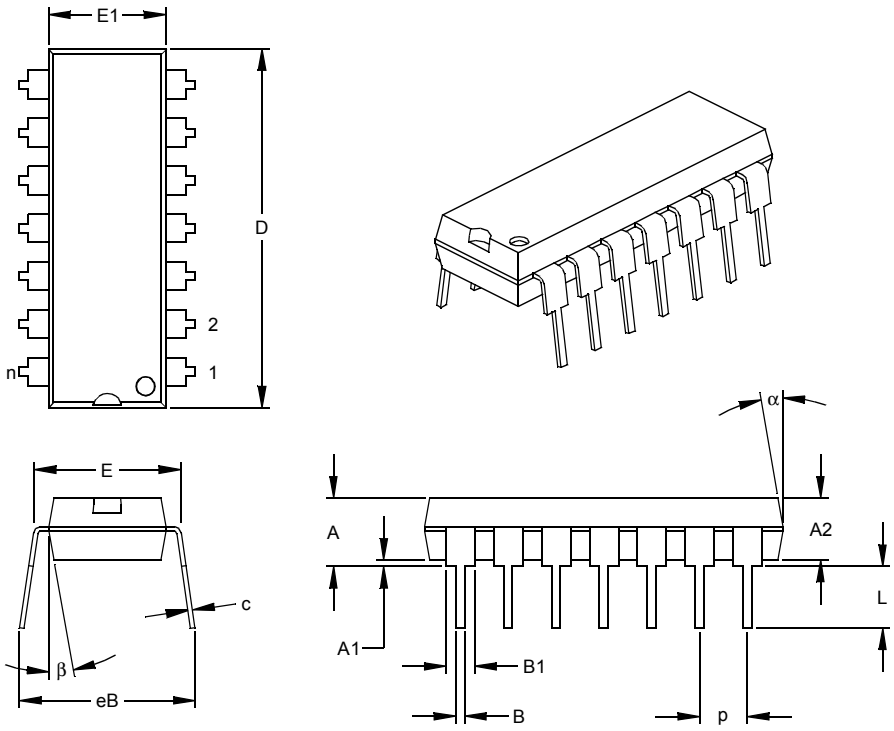
Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p		.026			0.65	
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	.5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

*Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
Drawing No. C04-111

14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

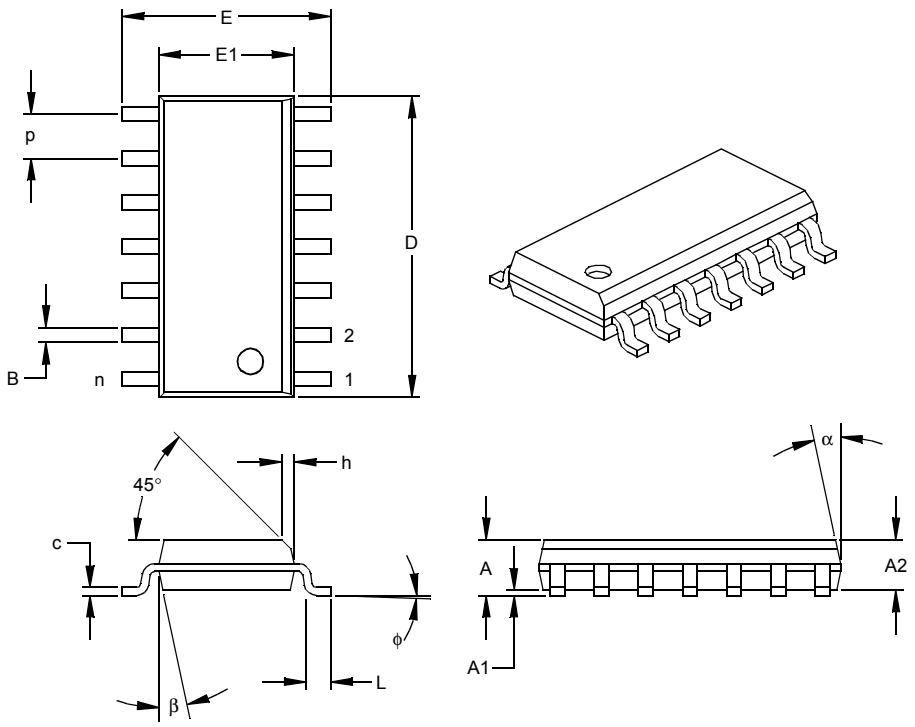


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

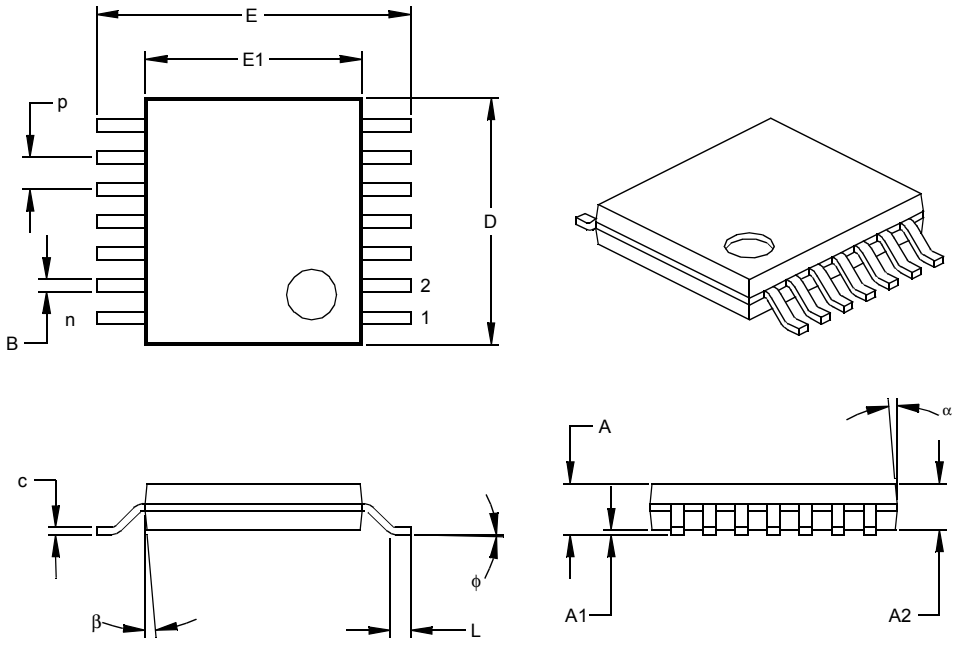


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

NOTES:

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Device: MCP6141/2/3/4 Literature Number: DS21668A

Questions:

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3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP6141:	CMOS Single Op Amp
	MCP6141T:	CMOS Single Op Amp (Tape and Reel for SOIC, MSOP)
	MCP6142:	CMOS Dual Op Amp
	MCP6142T:	CMOS Dual Op Amp (Tape and Reel for SOIC and TSSOP)
	MCP6143:	CMOS Single Op Amp w/$\overline{CS}$ Function
	MCP6143T:	CMOS Single Op Amp w/$\overline{CS}$ Function (Tape and Reel for SOIC and MSOP)
	MCP6144:	CMOS Quad Op Amp
	MCP6144T:	CMOS Quad Op Amp (Tape and Reel for SOIC and TSSOP)
Temperature Range:	I =	-40°C to +85°C
Package:	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	ST =	Plastic TSSOP (4.4mm Body), 14-lead

Examples:

a) MCP6141-I/P: Industrial temperature, PDIP package.

b) MCP6141T-I/SN: Tape and Reel, Industrial temperature, SOIC package.

a) MCP6142-I/SN: Industrial temperature, SOIC package.

b) MCP6142-I/MS: Industrial temperature, MSOP package.

a) MCP6143-I/MS: Industrial temperature, MSOP package.

b) MCP6143-I/P: Industrial temperature, PDIP package.

a) MCP6144-I/SL: Industrial temperature, SIOC package.

b) MCP6144T-I/ST: Tape and Reel, Industrial temperature, TSSOP package.

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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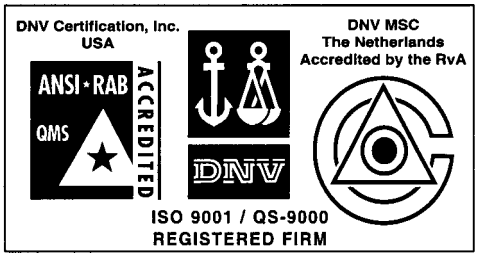
NOTES:



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