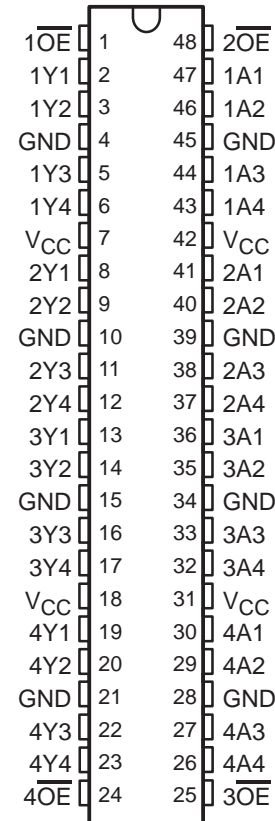


SN54ALVTH162244, SN74ALVTH162244 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCES074E – JUNE 1996 - REVISED JANUARY 1999

- State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus*™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- High-Impedance State During Power Up and Power Down Prevents Driver Conflict
- Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Output Ports Have Equivalent $30\text{-}\Omega$ Series Resistors, So No External Resistors Are Required
- Auto3-State Eliminates Bus Current Loading When Output Exceeds $V_{CC} + 0.5$ V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model; and Exceeds 1000 V Using Charged-Device Model, Robotic Method
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package

SN54ALVTH162244 . . . WD PACKAGE
SN74ALVTH162244 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NOTE: For order entry:
The DGG package is abbreviated to G, and
the DGV package is abbreviated to V.

description

The 'ALVTH162244 devices are 16-bit buffers/line drivers designed for low-voltage 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.



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Widebus is a trademark of Texas Instruments Incorporated.

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SN54ALVTH162244, SN74ALVTH162244

2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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description (continued)

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

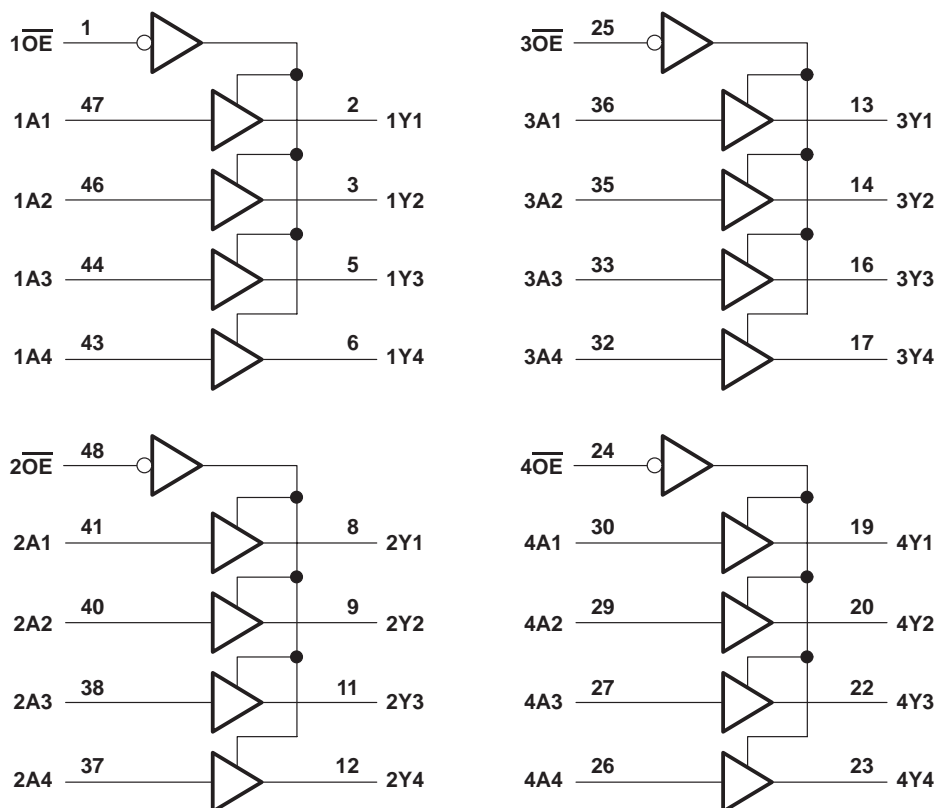
All outputs are designed to sink up to 12 mA and include equivalent 30- Ω resistors to reduce overshoot and undershoot.

The SN54ALVTH162244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALVTH162244 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 4-bit buffer)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

logic diagram (positive logic)



SN54ALVTH162244, SN74ALVTH162244

2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54ALVTH162244 | | SN74ALVTH162244 | | UNIT |
|-----------------------|--|---|------------------|------|-----------------|-----|---------------|
| | | | MIN | TYP† | MAX | MIN | |
| V_{IK} | $V_{CC} = 2.3 \text{ V}$, $I_I = -18 \text{ mA}$ | | -1.2 | | -1.2 | | V |
| V_{OH} | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$, $I_{OH} = -100 \mu\text{A}$ | | $V_{CC}-0.2$ | | $V_{CC}-0.2$ | | V |
| | $V_{CC} = 2.3 \text{ V}$ | $I_{OH} = -6 \text{ mA}$ | 1.7 | | 1.7 | | |
| V_{OL} | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$, $I_{OL} = 100 \mu\text{A}$ | | 0.2 | | 0.2 | | V |
| | $V_{CC} = 2.3 \text{ V}$ | $I_{OL} = 8 \text{ mA}$ | 0.7 | | 0.7 | | |
| | | $I_{OL} = 12 \text{ mA}$ | | | 0.7 | | |
| I_I | Control inputs | $V_{CC} = 2.7 \text{ V}$, $V_I = V_{CC} \text{ or GND}$ | ± 1 | | ± 1 | | μA |
| | | $V_{CC} = 0 \text{ or } 2.7 \text{ V}$, $V_I = 5.5 \text{ V}$ | 10 | | 10 | | |
| | Data inputs | $V_{CC} = 2.7 \text{ V}$, $V_I = 5.5 \text{ V}$ | 10 | | 10 | | |
| | | $V_{CC} = 2.7 \text{ V}$, $V_I = V_{CC}$ | 1 | | 1 | | |
| | $V_{CC} = 2.7 \text{ V}$, $V_I = 0$ | -5 | | -5 | | | |
| I_{off} | $V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$ | | | | ± 100 | | μA |
| I_{BHL}^\ddagger | $V_{CC} = 2.3 \text{ V}$, $V_I = 0.7 \text{ V}$ | | 115 | | 115 | | μA |
| I_{BHH}^\S | $V_{CC} = 2.3 \text{ V}$, $V_I = 1.7 \text{ V}$ | | -10 | | -10 | | μA |
| I_{BHLO}^\P | $V_{CC} = 2.7 \text{ V}$, $V_I = 0 \text{ to } V_{CC}$ | | 300 | | 300 | | μA |
| $I_{BHHO}^\#$ | $V_{CC} = 2.7 \text{ V}$, $V_I = 0 \text{ to } V_{CC}$ | | -300 | | -300 | | μA |
| I_{EX}^\parallel | $V_{CC} = 2.3 \text{ V}$, $V_O = 5.5 \text{ V}$ | | 125 | | 125 | | μA |
| $I_{OZ(PU/PD)}^\star$ | $V_{CC} \leq 1.2 \text{ V}$, $V_O = 0.5 \text{ V to } V_{CC}$, $V_I = \text{GND or } V_{CC}$, $\overline{OE} = \text{don't care}$ | | ± 100 | | ± 100 | | μA |
| I_{OZH} | $V_{CC} = 2.7 \text{ V}$ | $V_O = 2.3 \text{ V}$, $V_I = 0.7 \text{ V or } 1.7 \text{ V}$ | 5 | | 5 | | μA |
| I_{OZL} | $V_{CC} = 2.7 \text{ V}$ | $V_O = 0.5 \text{ V}$, $V_I = 0.7 \text{ V or } 1.7 \text{ V}$ | -5 | | -5 | | μA |
| I_{CC} | $V_{CC} = 2.7 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$ | | Outputs high | | 0.04 | 0.1 | mA |
| | | | Outputs low | | 2.3 | 4.5 | |
| | | | Outputs disabled | | 0.04 | 0.1 | |
| C_i | $V_{CC} = 2.5 \text{ V}$, $V_I = 2.5 \text{ V or } 0$ | | 3 | | 3 | | pF |
| C_o | $V_{CC} = 2.5 \text{ V}$, $V_O = 2.5 \text{ V or } 0$ | | 6 | | 6 | | pF |

† All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at $V_{IL} \text{ max}$. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to $V_{IL} \text{ max}$.

§ The bus-hold circuit can source at least the minimum high sustaining current at $V_{IH} \text{ min}$. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to $V_{IH} \text{ min}$.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when $V_O > V_{CC}$

☆ High-impedance state during power up or power down

SN54ALVTH162244, SN74ALVTH162244
2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN54ALVTH162244 | | SN74ALVTH162244 | | UNIT | | |
|-------------------------|---|---|------------------|------|-----------------|-----|---------------|---------------|-----|
| | | | MIN | TYP† | MAX | MIN | | TYP† | MAX |
| V_{IK} | | $V_{CC} = 3 \text{ V}$, $I_I = -18 \text{ mA}$ | | | -1.2 | | -1.2 | V | |
| V_{OH} | | $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$ | $V_{CC}-0.2$ | | $V_{CC}-0.2$ | | | V | |
| | | $V_{CC} = 3 \text{ V}$, $I_{OH} = -8 \text{ mA}$ | 2 | | | | | | |
| V_{OL} | | $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, $I_{OL} = 100 \mu\text{A}$ | | | 0.2 | | 0.2 | V | |
| | | $V_{CC} = 3 \text{ V}$, $I_{OL} = 8 \text{ mA}$ | | | 0.8 | | | | |
| | | $V_{CC} = 3 \text{ V}$, $I_{OL} = 12 \text{ mA}$ | | | | | 0.8 | | |
| I_I | Control inputs | $V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$ | | | ± 1 | | ± 1 | μA | |
| | | $V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$ | | | 10 | | 10 | | |
| | Data inputs | $V_{CC} = 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$ | | | 10 | | 10 | | |
| | | $V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$ | | | 1 | | 1 | | |
| | $V_{CC} = 3.6 \text{ V}$, $V_I = 0$ | | | -5 | | -5 | | | |
| I_{off} | | $V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$ | | | | | ± 100 | μA | |
| I_{BHL}^\ddagger | | $V_{CC} = 3 \text{ V}$, $V_I = 0.8 \text{ V}$ | 75 | | 75 | | μA | | |
| I_{BHH}^\S | | $V_{CC} = 3 \text{ V}$, $V_I = 2 \text{ V}$ | -75 | | -75 | | μA | | |
| I_{BHLO}^\P | | $V_{CC} = 3.6 \text{ V}$, $V_I = 0 \text{ to } V_{CC}$ | 500 | | 500 | | μA | | |
| $I_{BHHO}^\#$ | | $V_{CC} = 3.6 \text{ V}$, $V_I = 0 \text{ to } V_{CC}$ | -500 | | -500 | | μA | | |
| I_{EX}^{\parallel} | | $V_{CC} = 3 \text{ V}$, $V_O = 5.5 \text{ V}$ | | | 125 | | 125 | μA | |
| $I_{OZ(PU/PD)}^\star$ | | $V_{CC} \leq 1.2 \text{ V}$, $V_O = 0.5 \text{ V to } V_{CC}$, $V_I = \text{GND or } V_{CC}$, $\overline{OE} = \text{don't care}$ | | | ± 100 | | ± 100 | μA | |
| I_{OZH} | | $V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$, $V_I = 0.8 \text{ V or } 2 \text{ V}$ | | | 5 | | 5 | μA | |
| I_{OZL} | | $V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$, $V_I = 0.8 \text{ V or } 2 \text{ V}$ | | | -5 | | -5 | μA | |
| I_{CC} | | $V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$ | Outputs high | | 0.07 | 0.1 | 0.07 | 0.1 | mA |
| | | | Outputs low | | 3.2 | 5 | 3.2 | 5 | |
| | | | Outputs disabled | | 0.07 | 0.1 | 0.07 | 0.1 | |
| ΔI_{CC}^\square | | $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$ | | | 0.4 | | 0.4 | mA | |
| C_i | | $V_{CC} = 3.3 \text{ V}$, $V_I = 3.3 \text{ V or } 0$ | | | 3 | | 3 | pF | |
| C_o | | $V_{CC} = 3.3 \text{ V}$, $V_O = 3.3 \text{ V or } 0$ | | | 6 | | 6 | pF | |

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when $V_O > V_{CC}$

☆ High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54ALVTH162244, SN74ALVTH162244
2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ALVTH162244 | | SN74ALVTH162244 | | UNIT |
|-----------|-----------------|-------------|-----------------|-----|-----------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 1 | 4.3 | 1 | 4.2 | ns |
| t_{PHL} | | | 1.4 | 3.8 | 1.5 | 3.7 | |
| t_{PZH} | \overline{OE} | Y | 1.3 | 6.9 | 1.4 | 6.8 | ns |
| t_{PZL} | | | 1.3 | 5.2 | 1.4 | 5.1 | |
| t_{PHZ} | \overline{OE} | Y | 1 | 4.7 | 1 | 4.6 | ns |
| t_{PLZ} | | | 1 | 3.6 | 1 | 3.5 | |

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ALVTH162244 | | SN74ALVTH162244 | | UNIT |
|-----------|-----------------|-------------|-----------------|-----|-----------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 1 | 3.4 | 1 | 3.3 | ns |
| t_{PHL} | | | 1 | 3.4 | 1 | 3.3 | |
| t_{PZH} | \overline{OE} | Y | 1.4 | 5 | 1.5 | 4.9 | ns |
| t_{PZL} | | | 1.3 | 3.4 | 1.4 | 3.3 | |
| t_{PHZ} | \overline{OE} | Y | 1.4 | 5 | 1.5 | 4.9 | ns |
| t_{PLZ} | | | 1.4 | 4.4 | 1.5 | 4.3 | |

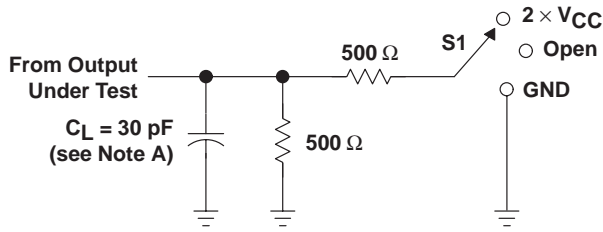
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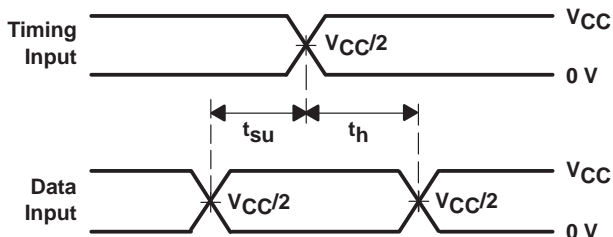
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

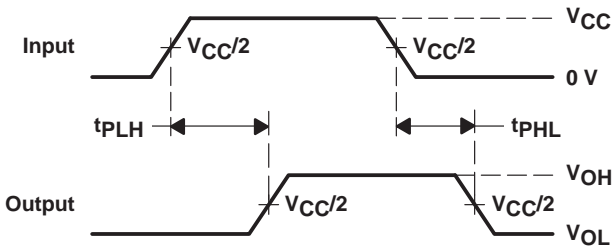


LOAD CIRCUIT

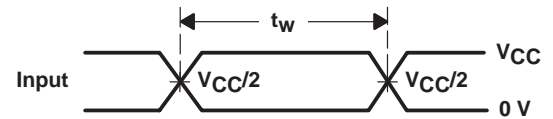
| TEST | S1 |
|-------------------|---------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 2 \times V_{CC} |
| t_{PHZ}/t_{PZH} | GND |



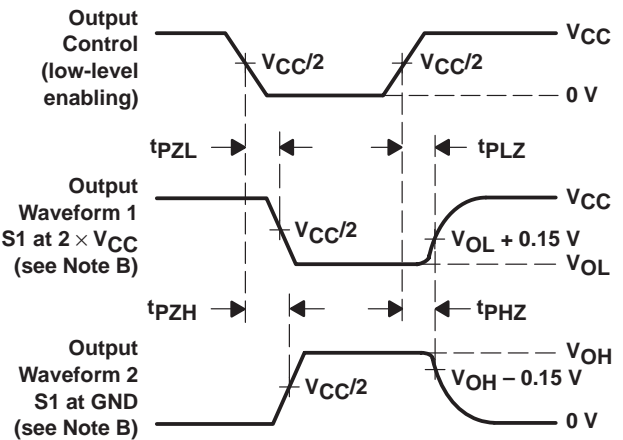
VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

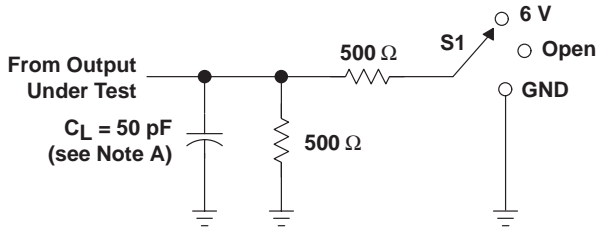
Figure 1. Load Circuit and Voltage Waveforms

SN54ALVTH162244, SN74ALVTH162244
2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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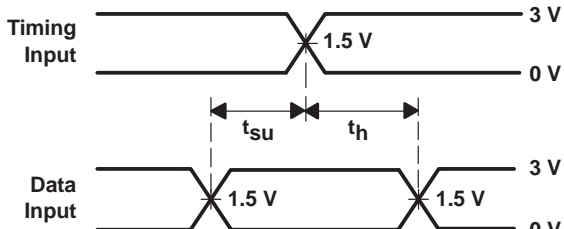
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

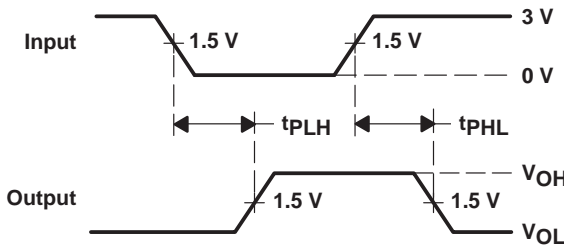


| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |

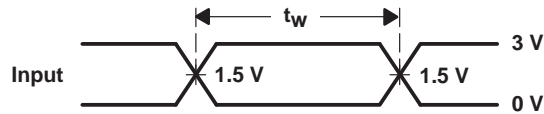
LOAD CIRCUIT



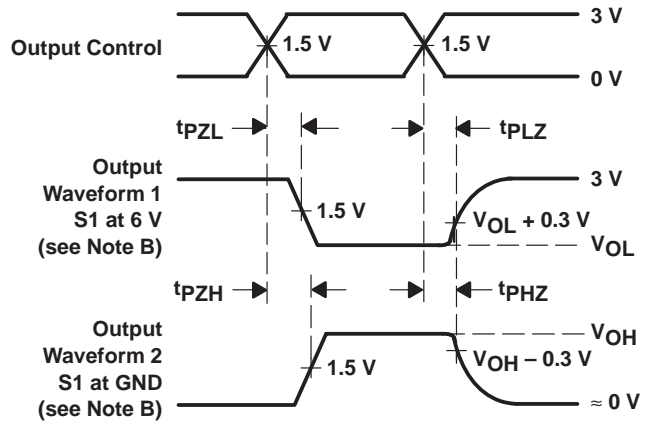
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
 PULSE DURATION**



**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74ALVTH162244DL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVTH162244 | Samples |
| SN74ALVTH162244GR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVTH162244 | Samples |
| SN74ALVTH162244LR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVTH162244 | Samples |
| SN74ALVTH162244VR | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VT2244 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

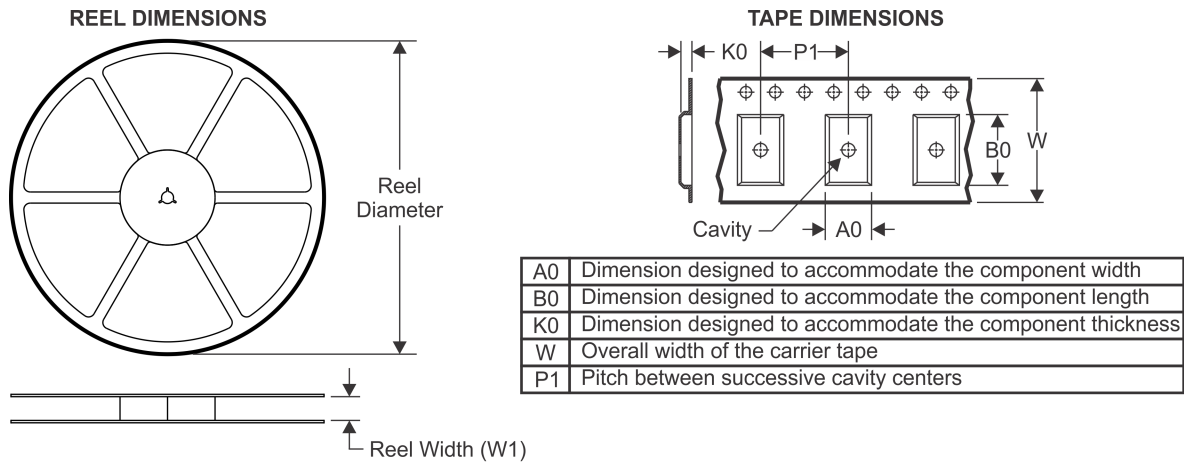
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALVTH162244GR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74ALVTH162244LR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |
| SN74ALVTH162244VR | TVSOP | DGV | 48 | 2000 | 330.0 | 16.4 | 7.1 | 10.2 | 1.6 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALVTH162244GR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ALVTH162244LR | SSOP | DL | 48 | 1000 | 367.0 | 367.0 | 55.0 |
| SN74ALVTH162244VR | TVSOP | DGV | 48 | 2000 | 367.0 | 367.0 | 38.0 |

MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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