TEXAS INSTRUMENTS

PGA4311
Evaluation Module

User's Guide

2002 Data Acquisition Products

SBOU013

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EVM WARNINGS AND RESTRICTIONS

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Read This First

About This Manual

This document provides information pertinent to the setup and operation of the PGA4311 evaluation module. This includes hardware configuration, as well as software installation. For a more detailed description of the PGA4311 4-channel volume control product, the user is referred to the Related Documentation from Texas Instruments section of this manual.

How to Use This Manual

This manual is divided into three chapters. Chapters 1 and 2 provide information relevant to the hardware setup and configuration for the evaluation module. A complete schematic is also provided at the end of Chapter 2. Chapter 3 focuses on the installation and usage of the PC-based software used to control the PGA4311 for evaluation purposes.

For a more detailed topical breakdown and quick reference, please refer to the Contents, Figures, and Tables sections located just prior to Chapter 1 in this manual.

Related Documentation From Texas Instruments

Data Sheets	Literature Number
PGA4311 Data Sheet	SBOS230
PGA2310-EVM	SBOU012

If You Need Assistance

If you have questions about this or other Texas Instruments data converter evaluation modules, feel free to e-mail the data converter application team at dataconvapps@list.ti.com. Include the product name in the subject heading.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Trademarks

Windows is a registered trademark of Microsoft Corporation.

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Chapter 1

Operating Conditions and Block Diagram

This chapter provides a brief listing of the reccommended operating conditions for the PGA4311 evaluation module. A simplified functional block diagram is also provided for reference when reading through Chapter 2.

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1.1 Recommended Operating Conditions

Analog Supplies
- VA+ ..... +5.0V DC
- VA– ..... –5.0V DC

Digital Supply
- VD+ ..... +5.0V DC

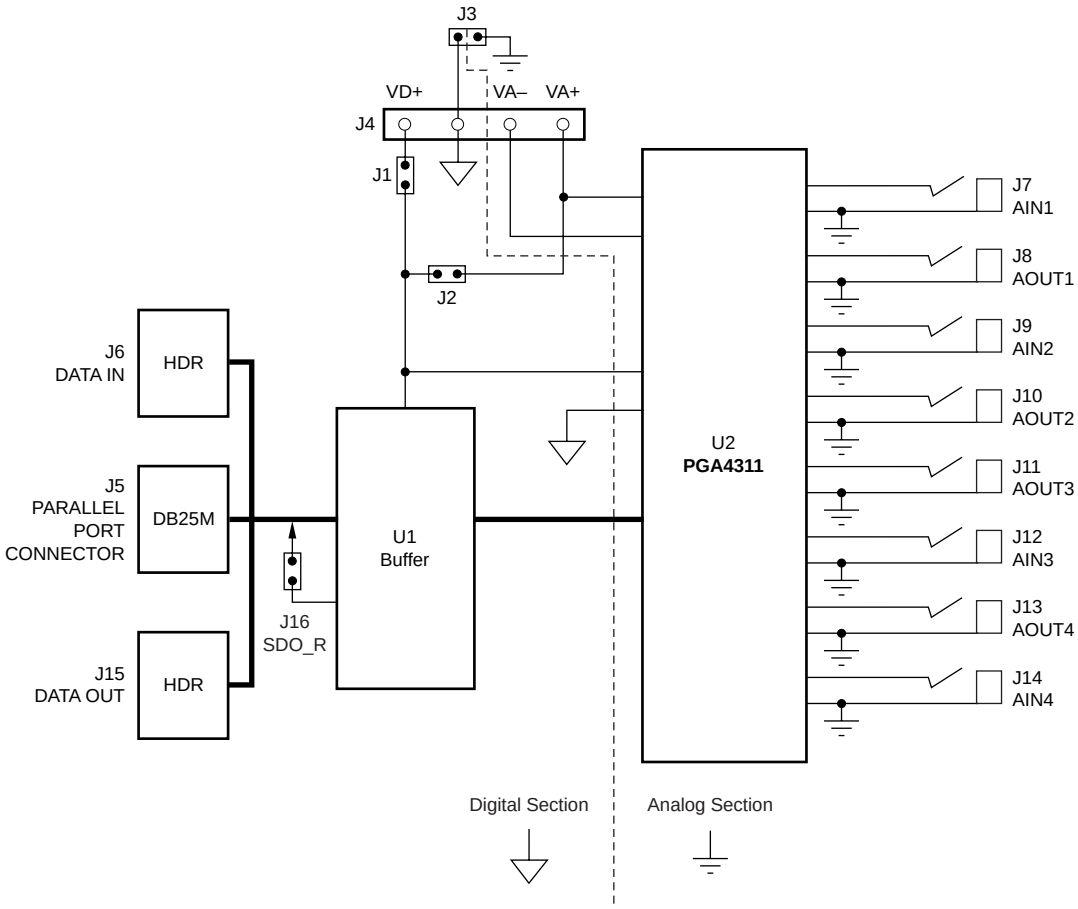
Ambient Temperature ..... 0°C to +40°C

Input Voltage, AIN1 through AIN4 ..... 7.5Vp-p max

Output Voltage, AOUT1 through AOUT4 ..... 7.5Vp-p max

1.2 PGA4311-EVM Block Diagram

Figure 1. EVM Block Diagram.



Chapter 2

Hardware Guide

This chapter provides hardware setup and configuration information for the PGA4311 evaluation module. A complete schematic is also provided at the end of this chapter.

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2.1 Power Supplies

The PGA4311-EVM includes a power supply connector, labeled J4 on the circuit board. Four locking terminals are provided for the analog power supplies (VA+ and VA–), a digital power supply (VD+), and a common ground (GND). There are two configuration modes for the power supplies: Three-Supply operation and Two-Supply operation.

In the case of Three-Supply operation, jumper J1 is installed while jumper J2 is an open circuit. Separate supplies are required for VD+, VA+, and VA–. The supplies share a common ground connection at the GND terminal. Table 1 shows the supply configuration details.

Table 1. Requirements for Three-Supply Operation.

Supply Designator	Recommended Supply Voltage	Supply Voltage Range
VD+	+5V	+4.5V to +5.5V
VA+	+5V	+4.5V to +5.5V
VA–	–5V	–4.5V to –5.5V

NOTE: Install jumper at J1. Remove jumper from J2 (open circuit).

In the case of Two-Supply operation, jumpers are installed at both J1 and J2. The J2 jumper connects the VA+ terminal to the VD+ terminal, with VA+ providing both the positive analog and digital supplies. Separate supplies are required for VA+ and VA-. The supplies share a common ground connection at the GND terminal. Table 2 shows the supply configuration details.

Table 2. Requirements for Two-Supply Operation.

Supply Designator	Recommeded Supply Voltage	Supply Voltage Range
VA+	+5V	+4.5V to +5.5V
VA–	–5V	–4.5V to –5.5V

NOTE: Jumpers J1 and J2 need to be installed.

2.2 PC Parallel Port Interface

The evaluation module includes a DB-25 connector, labeled J5, which is used to interface the PGA4311-EVM with a PC parallel (printer) port. The evaluation module software utilizes the parallel port to communicate with the PGA4311's serial interface. An interface cable is supplied as part of the evaluation module package.

2.3 DATA IN and DATA OUT Headers

Two 14-pin headers are included on the evaluation module. They are labeled DATA IN and DATA OUT. The DATA IN header provides an alternative connection for host communications with the PGA4311's serial interface. It also provides a means for interfacing to another PGA4311-EVM when using a daisy-chain configuration. The DATA OUT header is used for connection to the DATA IN header of another PGA4311-EVM when implementing a daisy-chain configuration.

2.4 Analog Input and Output Connectors

The evaluation module includes RCA jacks for connection to waveform generators, signal analyzers, and commercial audio equipment. The input jacks are labeled AIN1 through AIN4, while the output jacks are labeled AOUT1 through AOUT4. The analog inputs and outputs are unbalanced (referenced to ground). The analog input or output swing at these terminals must not exceed 7.5Vp-p when powered from ±5V analog power supplies.

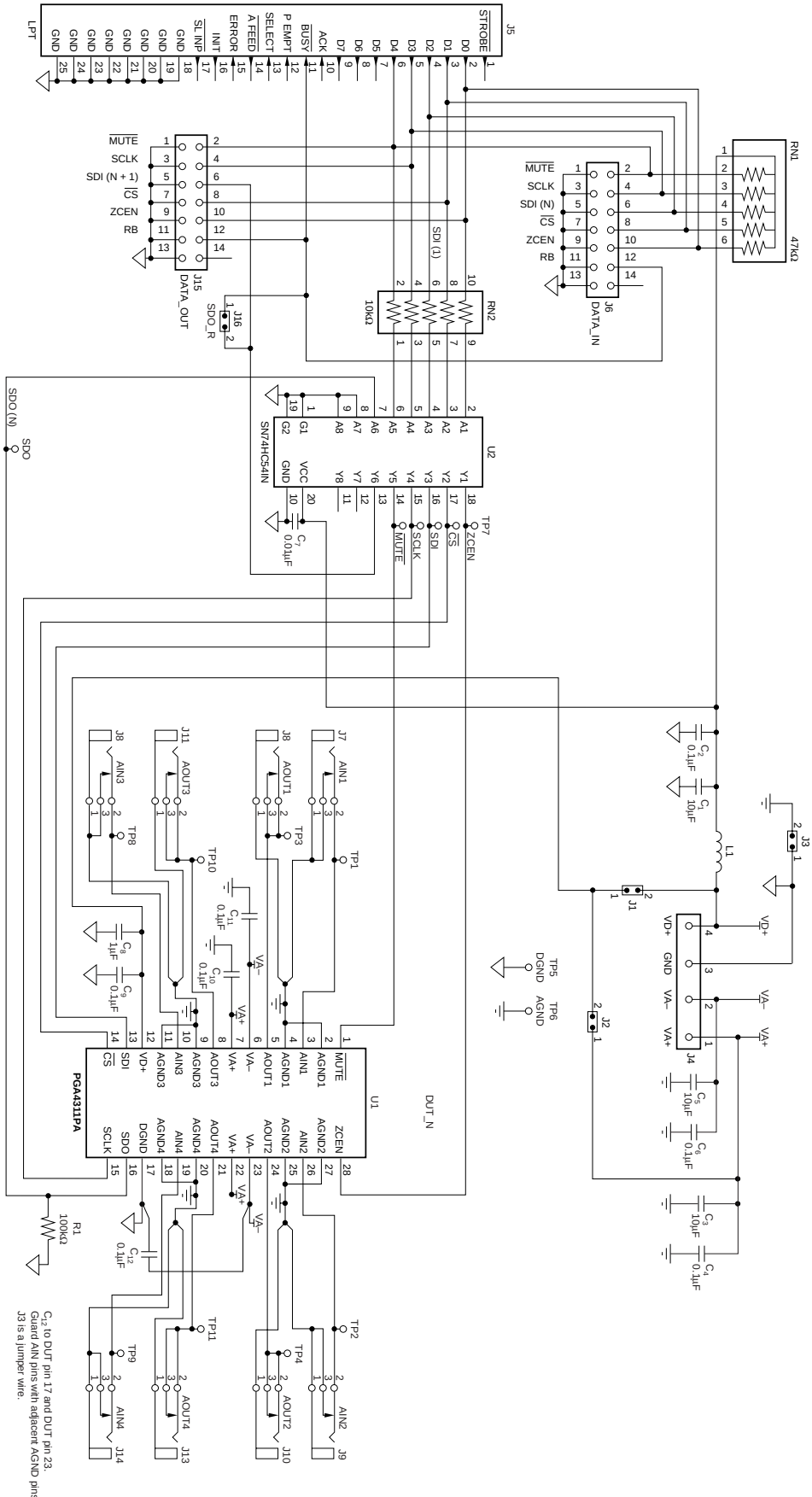
2.5 Register Loop-Back Jumper

The evaluation module contains a loop-back jumper, labeled SDO_R. The purpose of this jumper is to allow read back of the gain register values. This is helpful when diagnosing problems with the PC parallel port interface or host controller communications.

The serial interface is basically a 32 bit serial IN, serial OUT shift register. The SDI pin is the input, while SDO is the output. As 32 bits of new data are shifted into the PGA4311, the previously programmed 32-bits are being shifted out. This allows the user to read back the values to determine if the device is being programmed correctly. It also allows multiple PGA4311 devices to be cascaded, or daisy-chained, to form a 32 • N-bit long shift register, where N is the number of devices included in the chain. This arrangement allows a 3-wire interface to program multiple PGA4311 devices connected in a daisy-chain fashion.

2.6 Schematic

Figure 2. EVM Schematic.



Chapter 3

Software Guide

This chapter provides information regarding evaluation software installation and application. Software control panel operation is described in detail, with graphics of each panel providing a visual reference.

Note: The PGA4311-EVM utilizes the applications software created for the PGA2310-EVM. Where needed, differences in operation between the PGA4311-EVM and PGA2311-EVM will be explained in more detail.

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3.1 System Requirements

The supplied software will operate on personal computers designed for use with Windows 95 and 98. A CD-ROM drive is required for installation of program files and access to support documents. Approximately 4MB of hard disk space is required for installation.

3.2 Installation Procedure

The following procedure assumes familiarity with navigating the Windows desktop to find folders and files located on mounted volumes. Should you need assistance with this, please consult the Windows Help system.

Step 1: Insert the accompanying CD into your CD-ROM drive.

Step 2: Locate the **PGA2310-EVM** folder on the CD, using either My Computer or Windows Explorer.

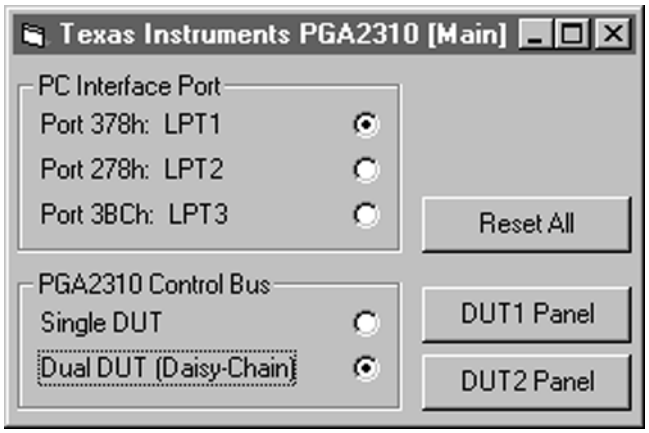
Step 3: Double-click the **PGA2310-EVM** folder icon, and then locate the **Package** folder. Double-click on the **Package** folder icon to open the folder. Locate the file named **Setup.exe**. Double-click the **Setup.exe** icon to start the installation process. Follow the on-screen instructions to complete the installation procedure.

3.3 Getting Started: The Main Panel

The setup program installs a Texas Instruments folder in the Programs folder of the Start menu. Within the Texas Instruments folder is the PGA2310 EVM program. Selecting this program will startup the applications software.

Once the program is started, the Main panel will be displayed, as shown in Figure 3. The Main panel allows the user to select the parallel (or printer) port address, and either Single or Dual DUT operation. The 'Reset All' button will revert all settings to their startup defaults. Pressing the DUT1 Panel and DUT2 Panel buttons will open panels containing the PGA4311 control objects, as shown in Figures 4 and 5.

Figure 3. The Main Panel.



3.4 Determining and Setting the Printer Port Address

The parallel port address for your PC can be found by going to the Start menu and selecting the Control Panel item in the Settings menu. When the Control Panels window opens, find the System icon and double click it. From the System window, select the Device Manager tab by clicking on it once. Scroll down the list of devices until you see the Ports entry. Double click on the Ports entry to list the PC ports. One of the ports should be a Printer Port. Double click on the Printer Port entry to open the Printer Port window. From the Printer Port window, select the Resources tab by clicking on it once. The Input/Output Range is displayed (ex/ 0378 – 037F). Write down the starting number in the range (ex/ 0378), and go to the Main panel of the evaluation module program and select the port address that matches this number.

3.5 Programming the PGA4311: The DUT Panels

All controls for the PGA4311 are contained within the DUT1 and DUT2 control panels, as shown in Figures 4 and 5. This section describes the functions contained within these panels.

Figure 4. The DUT1 Control Panel.

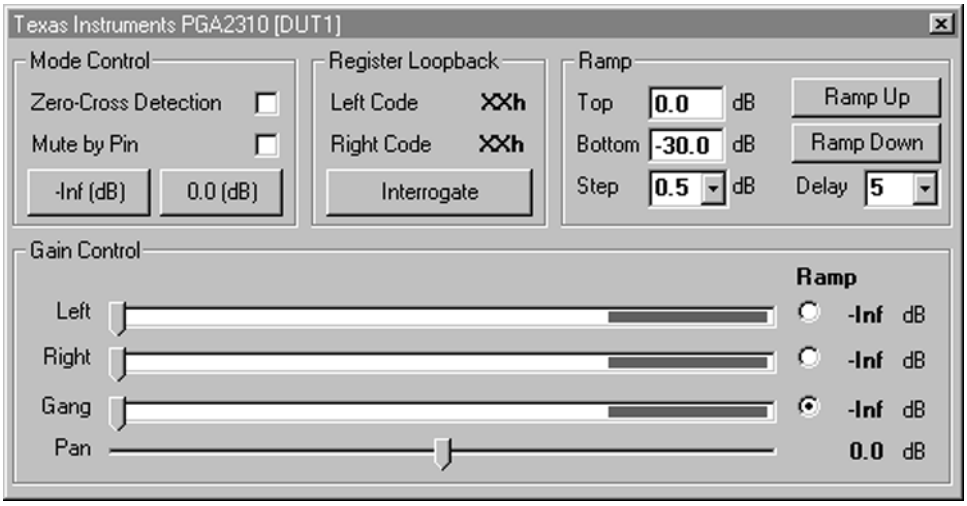
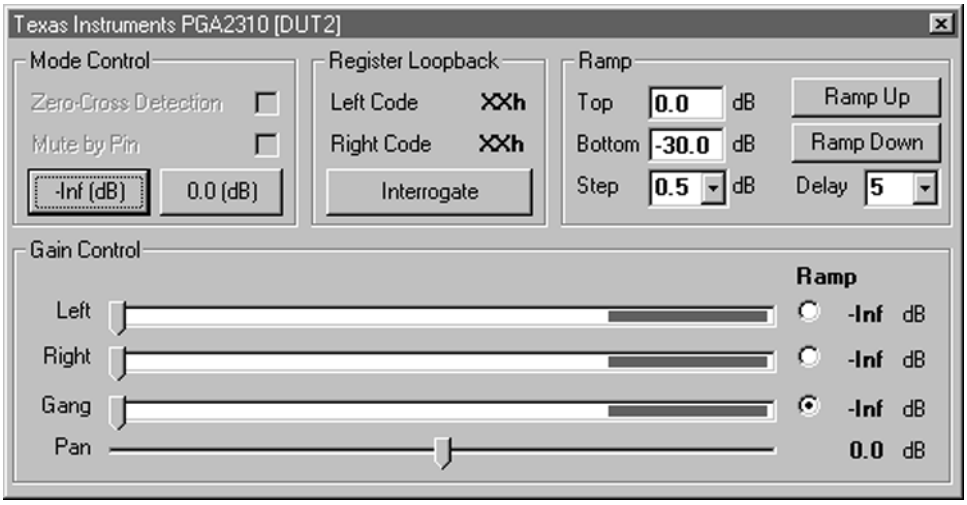


Figure 5. The DUT2 Control Panel.



3.6 Gain Controls

The Gain Controls occupy the bottom half of each DUT panel. There are three gain sliders, including one each for left and right channel, and a Gang slider for controlling both channels simultaneously. The DUT1 panel controls Channels 1 and 2 of the PGA4311, with Channel 2 corresponding to the right channel, and Channel 1 corresponding to the left channel. The DUT2 panel controls Channels 3 and 4 of the PGA4311, with Channel 4 corresponding to the right channel, and Channel 3 corresponding to the left channel.

When the PGA4311 first powers up, all channels will reset to maximum attenuation (or mute). The software also defaults to maximum attenuation at startup (shown as –Inf to the right of the sliders). A display to the right of each slider displays the currently selected gain setting.

The Ramp radio buttons to the right of each slider are used to select the gain slider to be automated when using the Ramp controls in the upper right-hand corner of the DUT panel.

The Pan slider functions as a Balance control, simultaneously gaining one channel while attenuating the other. It's behaves just like the balance control on your home or car stereo system.

3.7 Mode Controls

The Mode control section resides in the upper left-hand corner of each DUT panel. Only the mode controls in the DUT1 control panel are enabled. Several functions are accessible from this section. The Zero-Cross Detection checkbox is used to enable and disable the zero crossing detector circuit inside the PGA4311 device. The default setting is zero crossing detection disabled.

The Mute by Pin checkbox is used to enable or disable the $\overline{\text{MUTE}}$ pin function of the PGA4311. When $\overline{\text{MUTE}}$ is LOW, the PGA4311 sets both left and right channel attenuation to maximum (or mute). The default setting is mute disabled.

Two buttons allow the user to quickly set the gain of both left and right channels to either 0dB or –Inf dB (or mute). The –Inf dB button differs from the Mute by Pin checkbox in that it programs maximum attenuation for both left and right channels using the PGA4311's gain control registers, as opposed to using the $\overline{\text{MUTE}}$ pin.

3.8 Register Loop-Back Controls

With the SDO_R jumper installed, the user can test the function of the PGA4311 serial interface by using the Register Loop-Back control available in each DUT panel. Simply press the Interrogate button to read back the values being programmed for each channel. This function is included primarily for diagnostics, to ensure that the PC parallel port and the PGA4311 are communicating properly.

3.9 Ramp Function Controls

The Ramp controls allow automation of the gain settings for the PGA4311. The user enters the top and bottom points for the ramp, along with the desired step size and delay between steps. The ramp may be generated from bottom to top (Ramp Up) or from top to bottom (Ramp Down) for the given range. The ramp step size may be set from 0.5dB to 3.0dB in 0.5dB increments. The ramp step delay may be set using relative delay settings of 0, 1, 2, 5, 10, 20, or 50.

The channel selection for the automated ramp is selected using the radio buttons located to the right of the gain sliders in the Gain Control section of each DUT panel.