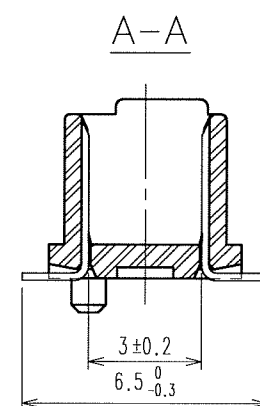
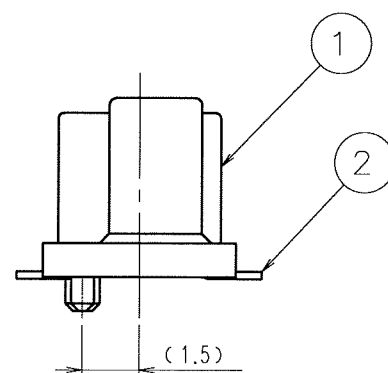
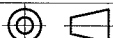


in cas	TO		
	PCK		



NOTE 1 LEAD CO-PLANARITY SHALL BE 0.1mm MAX.
2 FOR MODIFICATION, ETC., PREVENTIVE HOLE FOR SINK MARK
MAY BE ADDED ACCORDING TO CIRCUMSTANCES.
3 THE DIMENSIONS IN PARENTHESES ARE FOR REFERENCE.

Technical drawing of a 1000 nm VCSEL chip layout. The drawing shows a rectangular chip with a central dashed line. Dimensions are given in micrometers (μm). The total width is 34.2 ± 0.05 , with 2.4 ± 0.03 margins on both sides. The central active region is 29.4 ± 0.05 wide. There are two sets of four parallel lines on each side of the center, with a 0.6 ± 0.05 gap between them and a 0.35 ± 0.03 gap from the outer edge. The total height is 6.9 , with a 2 ± 0.05 gap between the two sets of lines and a 1.5 ± 0.05 gap from the bottom edge. Two circular features are shown, one on each side, with diameters of $\phi 1.1 \pm 0.05$ and $\phi 0.7 \pm 0.05$. A label "POLARIZATION MARK" points to the central dashed line.

1	POLYPHENYLENE SULFIDE	LIGHT BROWN UL94V-0	2	PHOSPHOR BRONZE	CONTACT AREA:GOLD 0.1μ m min.		
					LEAD AREA:GOLD PLATING FLASH		
					UNDER PLATING:NICKEL 1μ m min.		
NO.	MATERIAL	FINISH, REMARKS	NO.	MATERIAL	FINISH, REMARKS		
CODE NO. (OLD) CL			DRAWN	DESIGNED	CHECKED	APPROVED	RELEASED
			A. SUZUKAWA 05.11.05	H. Doi '05.11.09	H. Ogawa '05.11.09	H. Okawa '05.11.09	
			DRAWING NO.		PART NO.		
SCALE 5 : 1			EDC3-150823-25		FX8C-100P-SV(71)		
UNITS mm			HRS HIROSE ELECTRIC CO.,LTD.		CODE NO. CL578-0505-0-71		1/1