TEXAS INSTRUMENTS

LMV341, LMV342, LMV344

SLOS447I – SEPTEMBER 2004 – REVISED MAY 2016

# LMV34x Rail-to-Rail Output CMOS Operational Amplifiers With Shutdown

## 1 Features

- 2.7-V and 5-V Performance
- Rail-to-Rail Output Swing
- Input Bias Current:1 pA (Typical)
- Input Offset Voltage: 0.25 mV (Typical)
- Low Supply Current: 100 µA (Typical)
- Low Shutdown Current: 45 pA (Typical)
- Gain Bandwidth of 1 MHz (Typical)
- Slew Rate: 1 V/µs (Typical)
- Turnon Time From Shutdown: 5 µs (Typical)
- Input Referred Voltage Noise (at 10 kHz): 20 nV/√Hz
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (HBM)
  - 750-V Charged-device model (CDM)

## 2 Applications

- Cordless and Cellular Phones
- Consumer Electronics (Laptops, PDAs)
- Audio Preamplifiers for Voice
- Portable, Battery-Powered Electronic Equipment
- Supply-Current Monitoring
- Battery Monitoring
- Buffers
- Filters
- Drivers

## 3 Description

The LMV34x devices are single, dual, and quad CMOS operational amplifiers, respectively, with low voltage, low power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultra-low input bias current of 1 pA (typical) and an offset voltage of 0.25 mV (typical). The single-supply amplifier is designed specifically for low-voltage (2.7 V to 5 V) operation, with a wide common-mode input voltage range that typically extends from –0.2 V to 0.8 V from the positive supply rail. The LMV341 (single) also offers a shutdown ($\overline{SHDN}$) pin that can be used to disable the device. In shutdown mode, the supply current is reduced to 33 nA (typical). Additional features of the family are a 20-nV/√Hz voltage noise at 10 kHz, 1-MHz unity-gain bandwidth, 1-V/µs slew rate, and 100-µA current consumption per channel.

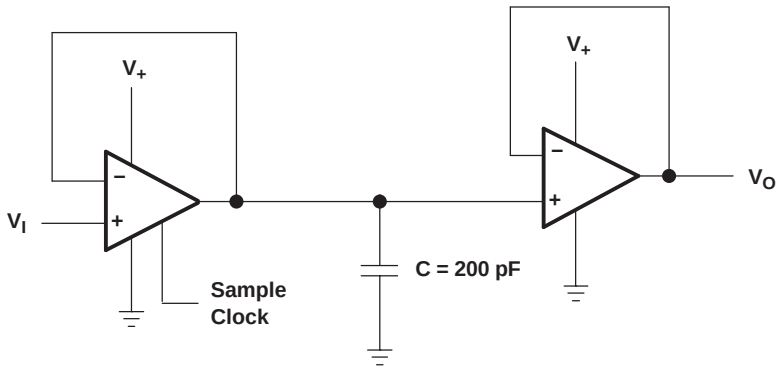
Offered in both the SOT-23 and smaller SC70 packages, the LMV341 is suitable for the most space-constraint applications. The LMV342 dual device is offered in the standard SOIC and VSSOP packages. An extended industrial temperature range from –40°C to 125°C makes these devices suitable in a wide variety of commercial and industrial environments.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LMV341IDCK | SC70 (6) | 2.00 mm × 1.25 mm |
| LMV341IDBV | SOT-23 (6) | 2.90 mm ×1.60 mm |
| LMV342ID | SOIC (8) | 4.90 mm × 3.91 mm |
| LMV342IDGK | VSSOP (8) | 3.00 mm × 3.00 mm |
| LMV344ID | SOIC (14) | 8.65 mm × 3.91 mm |
| LMV344IPW | TSSOP (14) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Sample-and-Hold Circuit**



# Table of Contents



## 4 Revision History

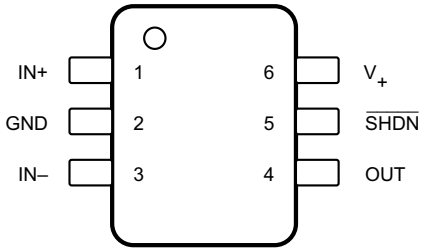
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision H (June 2012) to Revision I** **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed *Ordering Information* table ... 1

# 5 Pin Configuration and Functions

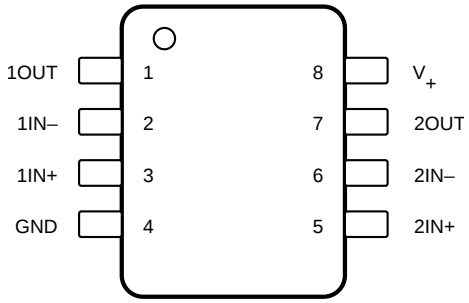
**DBV or DCK Package**
**6-Pin SOT-23 or SC70**
**Top View**




### Pin Functions: LMV341

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | SOT-23, SC70 | | |
| IN+ | 1 | I | Noninverting input on channel 1 |
| IN– | 3 | I | Inverting input on channel 1 |
| OUT | 4 | O | Output on channel 1 |
| GND | 2 | — | Ground |
| $\overline{SHDN}$ | 5 | I | Shutdown active low |
| $V_+$ | 6 | — | Positive power supply |

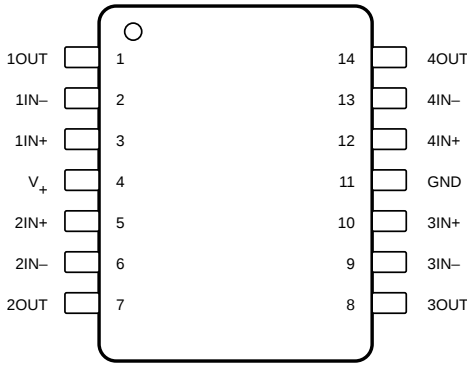
**D or DGK Package**
**8-Pin SOIC or VSSOP**
**Top View**




### Pin Functions: LMV342

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | SOIC, VSSOP | | |
| 1IN+ | 3 | I | Noninverting input on channel 1 |
| 1IN– | 2 | I | Inverting input on channel 1 |
| 1OUT | 1 | O | Output on channel 1 |
| 2IN+ | 5 | I | Noninverting input on channel 2 |
| 2IN– | 6 | I | Inverting input on channel 2 |
| 2OUT | 7 | O | Output on channel 2 |
| GND | 4 | — | Ground |
| $V_+$ | 8 | — | Positive power supply |

**D or PW Package**
**14-Pin SOIC or TSSOP**
**Top View**




**Pin Functions: LMV344**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | SOIC, TSSOP | | |
| 1IN+ | 3 | I | Noninverting input on channel 1 |
| 1IN– | 2 | I | Inverting input on channel 1 |
| 1OUT | 1 | O | Output on channel 1 |
| 2IN+ | 5 | I | Noninverting input on channel 2 |
| 2IN– | 6 | I | Inverting input on channel 2 |
| 2OUT | 7 | O | Output on channel 2 |
| 3IN+ | 10 | I | Noninverting input on channel 3 |
| 3IN– | 9 | I | Inverting input on channel 3 |
| 3OUT | 8 | O | Output on channel 3 |
| 4IN+ | 12 | I | Noninverting input on channel 4 |
| 4IN– | 13 | I | Inverting input on channel 4 |
| 4OUT | 14 | O | Output on channel 4 |
| GND | 11 | — | Ground |
| $V_+$ | 4 | — | Positive power supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_+$ | Supply voltage(2) | –0.3 | 5.5 | V |
| $V_{ID}$ | Differential input voltage(3) | | ±5.5 | V |
| $V_I$ | Input voltage (either input) | –0.3 | 5.5 | V |
| $V_O$ | Output voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $T_J$ | Operating virtual junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN−.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_+$ | Supply voltage (single-supply operation) | 2.5 | 5.5 | V |
| $T_A$ | Operating free-air temperature | –40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | LMV342 | LMV344 | LMV341 | | LMV342 | LMV344 | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | D (SOIC) | | DBV (SOT-23) | DCK (SC70) | DGK (VSSOP) | PW (TSSOP) | |
| | | 8 PINS | 14 PINS | 6 PINS | 6 PINS | 8 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (2) (3) | 123.9 | 88.7 | 193.4 | 196.8 | 192.3 | 118 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 70.2 | 49 | 145.6 | 82.4 | 78.2 | 46.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 64.1 | 43 | 44.1 | 95.2 | 112.6 | 59.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 25 | 16.9 | 34.1 | 1.8 | 15.2 | 5.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 63.6 | 42.7 | 43.4 | 93.2 | 111.2 | 59.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of $T_J(max)$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/R_{\theta JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics: $V_+ = 2.7$ V

$V_+ = 2.7$ V, GND = 0 V, $V_{IC} = V_O = V_+/2$, $R_L > 1$ MΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP (1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | | 25°C | | 0.25 | 4 | mV |
| | | | Full range | | | 4.5 | |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | | Full range | | 1.7 | | µV/°C |
| $I_{IB}$ | Input bias current | | 25°C | | 1 | 120 | pA |
| | | | –40°C to 85°C | | | 250 | |
| | | | –40°C to 125°C | | | 3 | nA |
| $I_{IO}$ | Input offset current | | 25°C | | 6.6 | | fA |
| CMRR | Common-mode rejection ratio | $0 \le V_{ICR} \le 1.7$ V | 25°C | 56 | 80 | | dB |
| | | $0 \le V_{ICR} \le 1.6$ V | Full range | 50 | | | |
| $k_{SVR}$ | Supply-voltage rejection ratio | 2.7 V ≤ $V_+$ ≤ 5 V | 25°C | 65 | 82 | | dB |
| | | | Full range | 60 | | | |
| $V_{ICR}$ | Common-mode input voltage range | Lower range, CMRR ≥ 50 dB | 25°C | | –0.2 | 0 | V |
| | | Upper range, CMRR ≥ 50 dB | 25°C | 1.7 | 1.9 | | |
| $A_V$ | Large-signal voltage gain (2) | $R_L$ = 10 kΩ to 1.35 V | 25°C | 78 | 113 | | dB |
| | | | Full range | 70 | | | |
| | | $R_L$ = 2 kΩ to 1.35 V | 25°C | 72 | 103 | | |
| | | | Full range | 64 | | | |

(1) Typical values represent the most likely parametric norm.
(2) GND + 0.2 V ≤ $V_O$ ≤ $V_+$ – 0.2 V

## Electrical Characteristics: $V_+$ = 2.7 V (continued)

$V_+$ = 2.7 V, GND = 0 V, $V_{IC}$ = $V_O$ = $V_+$/2, $R_L$ > 1 MΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_O$ | Output swing (delta from supply rails) | $R_L$ = 2 kΩ to 1.35 V | Low level | 25°C | | 24 | 60 | mV |
| | | | | Full range | | | 95 | |
| | | | High level | 25°C | | 26 | 60 | |
| | | | | Full range | | | 95 | |
| | | $R_L$ = 10 kΩ to 1.35 V | Low level | 25°C | | 5 | 30 | |
| | | | | Full range | | | 40 | |
| | | | High level | 25°C | | 5.3 | 30 | |
| | | | | Full range | | | 40 | |
| $I_{CC}$ | Supply current (per channel) | | | 25°C | | 100 | 170 | µA |
| | | | | Full range | | | 230 | |
| $I_{OS}$ | Output short-circuit current | Sourcing | LMV341, LMV342 | 25°C | 20 | 32 | | mA |
| | | | LMV344 | | 18 | 24 | | |
| | | Sinking | | | 15 | 24 | | |
| SR | Slew rate | $R_L$ = 10 kΩ(3) | | 25°C | | 1 | | V/µs |
| GBM | Unity-gain bandwidth | $R_L$ = 10 kΩ, $C_L$ = 200 pF | | 25°C | | 1 | | MHz |
| $\Phi_m$ | Phase margin | $R_L$ = 100 kΩ | | 25°C | | 72 | | ° |
| $G_m$ | Gain margin | $R_L$ = 100 kΩ | | 25°C | | 20 | | dB |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz | | 25°C | | 40 | | nV/√Hz |
| $I_n$ | Equivalent input noise current | f = 1 kHz | | 25°C | | 0.001 | | pA/√Hz |
| THD | Total harmonic distortion | f = 1 kHz, $A_V$ = 1, $R_L$ = 600 Ω, $V_I$ = 1 $V_{PP}$ | | 25°C | | 0.017% | | |

(3) Connected as voltage follower with 2-$V_{PP}$ step input. Number specified is the slower of the positive and negative slew rates.

## 6.6 Electrical Characteristics: $V_+$ = 5 V

$V_+$ = 5 V, GND = 0 V, $V_{IC}$ = $V_O$ = $V_+$/2, $R_L$ > 1 MΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | | 25°C | | 0.25 | 4 | mV |
| | | | Full range | | | 4.5 | |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | | Full range | | 1.9 | | µV/°C |
| $I_{IB}$ | Input bias current | | 25°C | | 1 | 200 | pA |
| | | | –40°C to 85°C | | | 375 | |
| | | | –40°C to 125°C | | | 5 | nA |
| $I_{IO}$ | Input offset current | | 25°C | | 6.6 | | fA |
| CMRR | Common-mode rejection ratio | 0 ≤ $V_{ICR}$ ≤ 4 V | 25°C | 56 | 86 | | dB |
| | | 0 ≤ $V_{ICR}$ ≤ 3.9 V | Full range | 50 | | | |
| $k_{SVR}$ | Supply-voltage rejection ratio | 2.7 V ≤ $V_+$ ≤ 5 V | 25°C | 65 | 82 | | dB |
| | | | Full range | 60 | | | |
| $V_{ICR}$ | Common-mode input voltage range | Lower range, CMRR ≥ 50 dB | 25°C | | –0.2 | 0 | V |
| | | Upper range, CMRR ≥ 50 dB | 25°C | 4 | 4.2 | | |
| $A_V$ | Large-signal voltage gain(2) | $R_L$ = 10 kΩ to 2.5 V | 25°C | 78 | 116 | | dB |
| | | | Full range | 70 | | | |
| | | $R_L$ = 2 kΩ to 2.5 V | 25°C | 72 | 107 | | |
| | | | Full range | 64 | | | |

(1) Typical values represent the most likely parametric norm.
(2) GND + 0.2 V ≤ $V_O$ ≤ $V_+$ – 0.2 V

## Electrical Characteristics: $V_+$ = 5 V (continued)

$V_+$ = 5 V, GND = 0 V, $V_{IC}$ = $V_O$ = $V_+$/2, $R_L$ > 1 MΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_O$ | Output swing (delta from supply rails) | $R_L$ = 2 kΩ to 2.5 V | Low level | 25°C | | 32 | 60 | mV |
| | | | | Full range | | | 95 | |
| | | | High level | 25°C | | 34 | 60 | |
| | | | | Full range | | | 95 | |
| | | $R_L$ = 10 kΩ to 2.5 V | Low level | 25°C | | 7 | 30 | |
| | | | | Full range | | | 40 | |
| | | | High level | 25°C | | 7 | 30 | |
| | | | | Full range | | | 40 | |
| $I_{CC}$ | Supply current (per channel) | | | 25°C | | 107 | 200 | µA |
| | | | | Full range | | | 260 | |
| $I_{OS}$ | Output short-circuit current | Sourcing | LMV341, LMV342 | 25°C | 85 | 113 | | mA |
| | | | LMV344 | | 85 | 113 | | |
| | | Sinking | | | 50 | 75 | | |
| SR | Slew rate | $R_L$ = 10 kΩ(3) | | 25°C | | 1 | | V/µs |
| GBM | Unity-gain bandwidth | $R_L$ = 10 kΩ, $C_L$ = 200 pF | | 25°C | | 1 | | MHz |
| $\Phi_m$ | Phase margin | $R_L$ = 100 kΩ | | 25°C | | 70 | | ° |
| $G_m$ | Gain margin | $R_L$ = 100 kΩ | | 25°C | | 20 | | dB |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz | | 25°C | | 39 | | nV/√Hz |
| $I_n$ | Equivalent input noise current | f = 1 kHz | | 25°C | | 0.001 | | pA/√Hz |
| THD | Total harmonic distortion | f = 1 kHz, $A_V$ = 1, $R_L$ = 600 Ω, $V_I$ = 1 $V_{PP}$ | | 25°C | | 0.012% | | |

(3) Connected as voltage follower with 2-$V_{PP}$ step input. Number specified is the slower of the positive and negative slew rates.

## 6.7 Shutdown Characteristics: $V_+$ = 2.7 V

$V_+$ = 2.7 V, GND = 0 V, $V_{IC}$ = $V_O$ = $V_+$/2, $R_L$ > 1 MΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC(SHDN)}$ | Supply current in shutdown mode | $V_{SD}$ = 0 V | 25°C | | 0.045 | 1000 | nA |
| | | | Full range | | | 1.5 | µA |
| $t_{(on)}$ | Amplifier turnon time | | 25°C | | 5 | | µs |
| $V_{SD}$ | Recommended shutdown pin voltage range | ON mode | 25°C | 2.4 | | 2.7 | V |
| | | Shutdown mode | | 0 | | 0.8 | |

## 6.8 Shutdown Characteristics: $V_+$ = 5 V

$V_+$ = 5 V, GND = 0 V, $V_{IC}$ = $V_O$ = $V_+$/2, $R_L$ > 1 MΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC(SHDN)}$ | Supply current in shutdown mode | $V_{SD}$ = 0 V | 25°C | | 0.033 | 1 | µA |
| | | | Full range | | | 1.5 | |
| $t_{(on)}$ | Amplifier turnon time | | 25°C | | 5 | | µs |
| $V_{SD}$ | Recommended shutdown pin voltage range | ON mode | 25°C | 4.5 | | 5 | V |
| | | Shutdown mode | | 0 | | 0.8 | |

## 6.9 Typical Characteristics

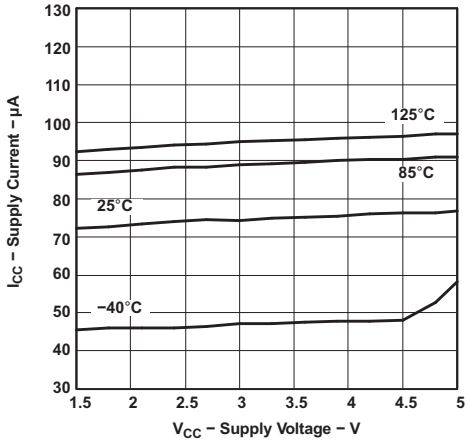



**Figure 1. Supply Current vs Supply Voltage**

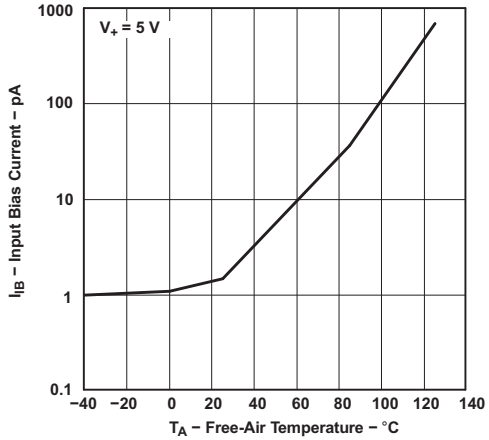



**Figure 2. Input Bias Current vs Temperature**

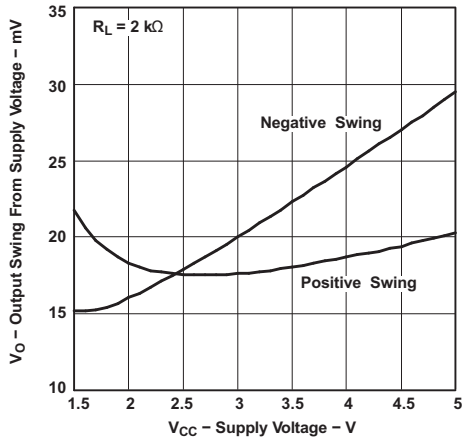



**Figure 3. Output Voltage Swing vs Supply Voltage**

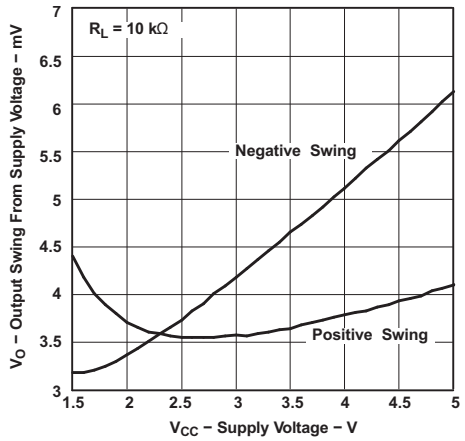



**Figure 4. Output Voltage Swing vs Supply Voltage**

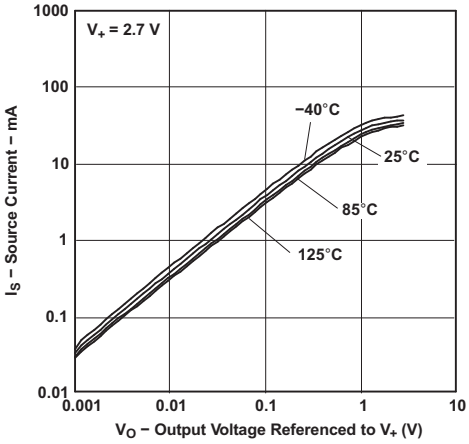



**Figure 5. Source Current vs Output Voltage**

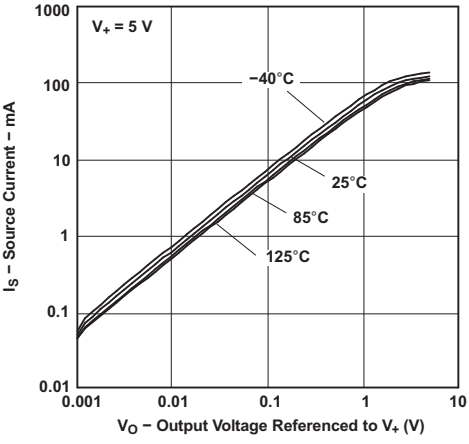



**Figure 6. Source Current vs Output Voltage**

## Typical Characteristics (continued)

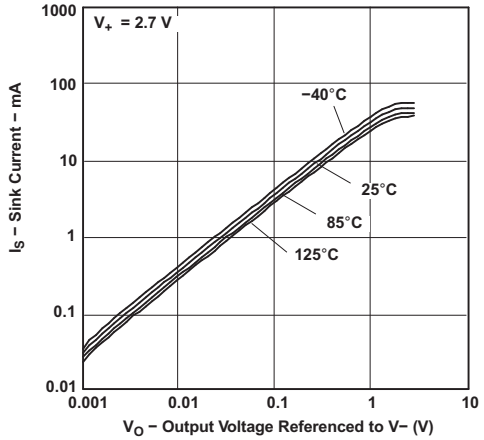



**Figure 7. Sink Current vs Output Voltage**

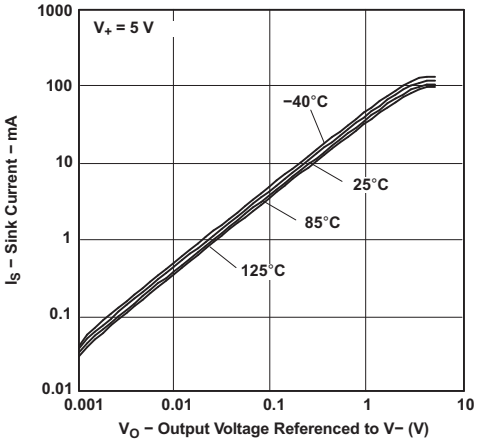



**Figure 8. Sink Current vs Output Voltage**

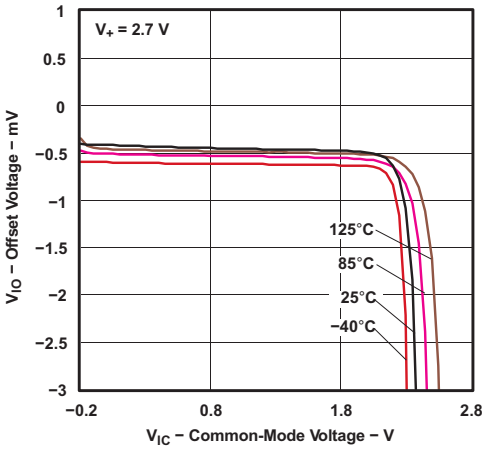



**Figure 9. Offset Voltage vs Common-Mode Voltage**

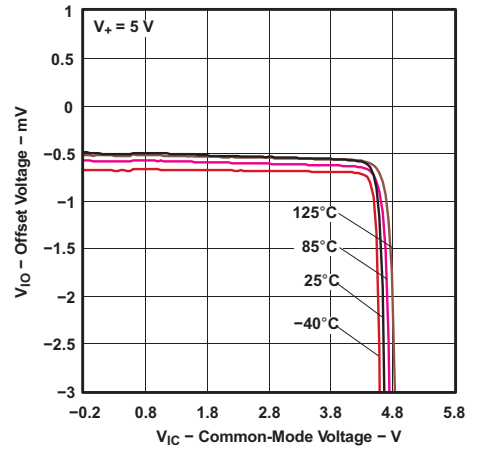



**Figure 10. Offset Voltage vs Common-Mode Voltage**

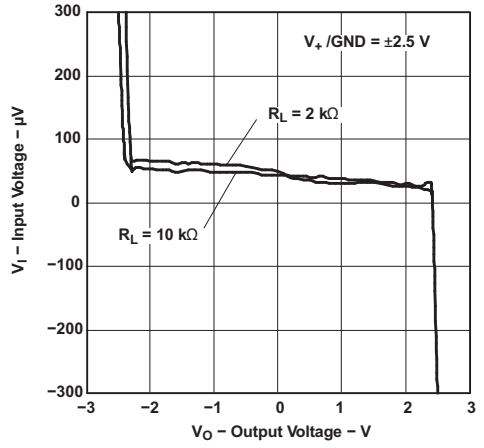



**Figure 11. Input Voltage vs Output Voltage**

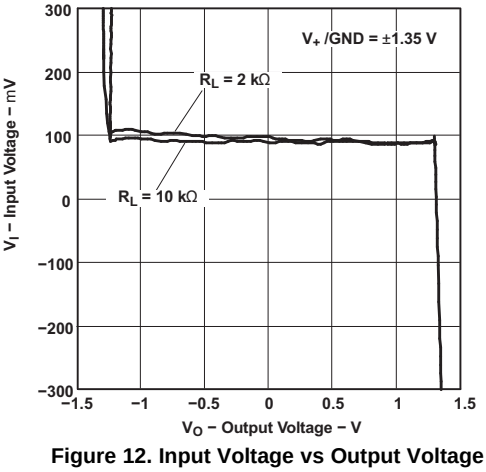



**Figure 12. Input Voltage vs Output Voltage**

## Typical Characteristics (continued)

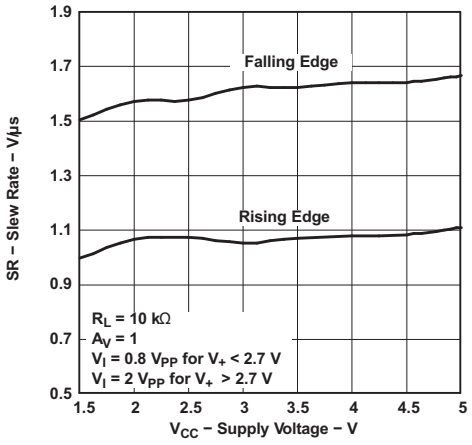



**Figure 13. Slew Rate vs Supply Voltage**

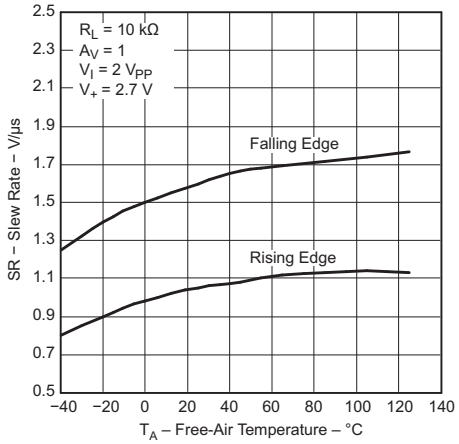



**Figure 14. Slew Rate vs Temperature**

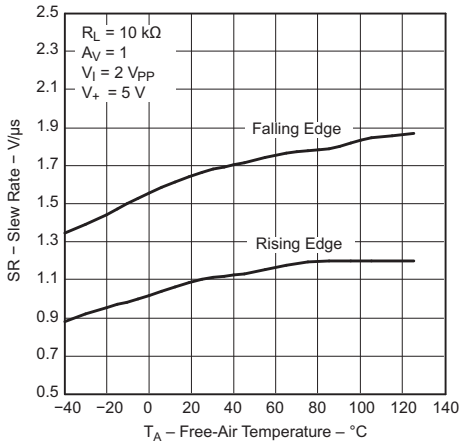



**Figure 15. Slew Rate vs Temperature**

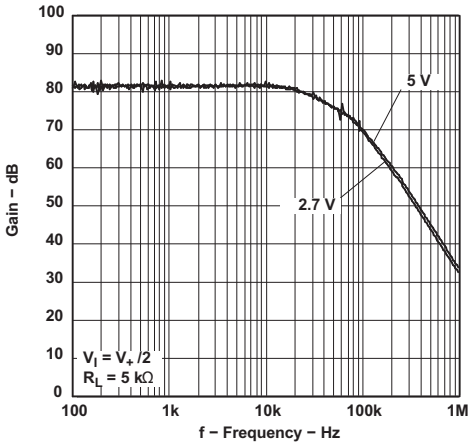



**Figure 16. CMRR vs Frequency**

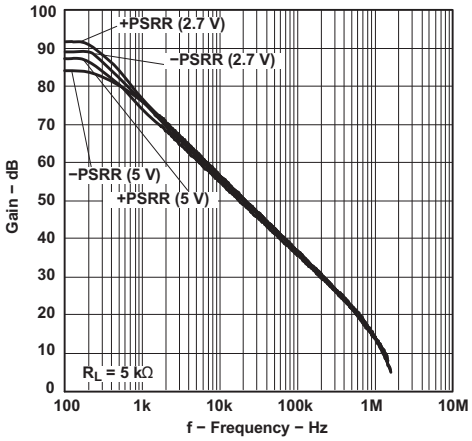



**Figure 17. PSRR vs Frequency**

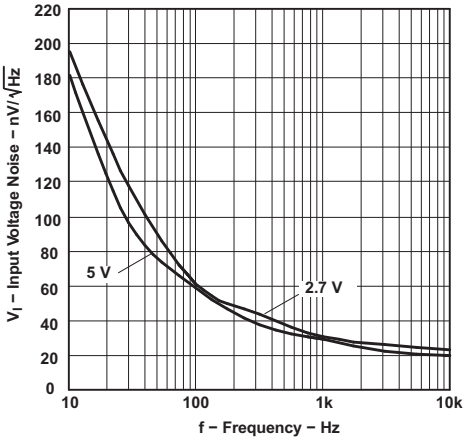



**Figure 18. Input Voltage Noise vs Frequency**

## Typical Characteristics (continued)

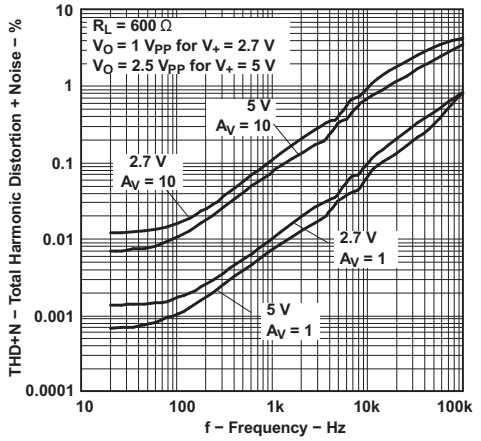



**Figure 19. Total Harmonic Distortion + Noise vs Frequency**

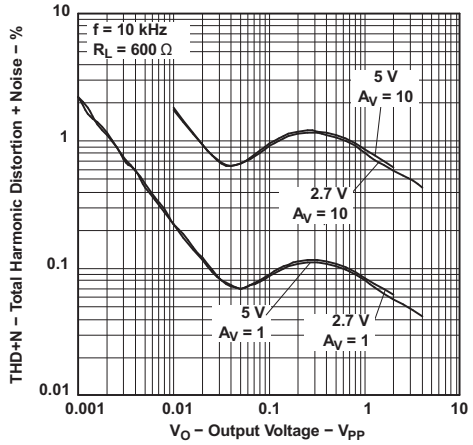
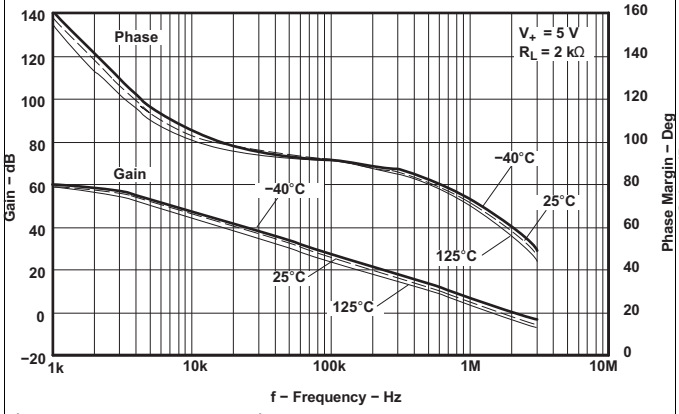
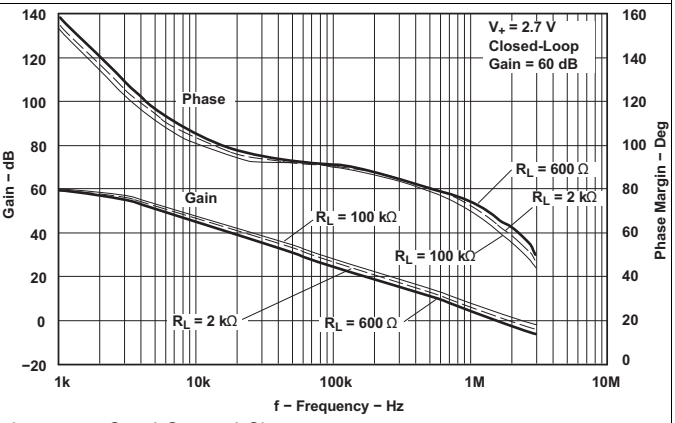



**Figure 20. Total Harmonic Distortion + Noise vs Output Voltage**



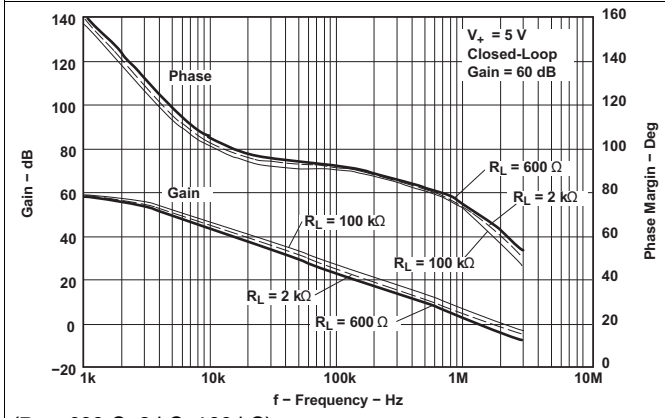

($T_A$ = –40°C, 25°C, 125°C)

**Figure 21. Gain and Phase Margin vs Frequency**



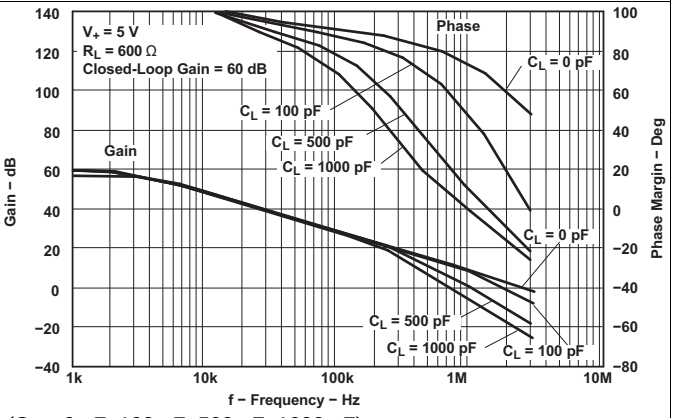

($R_L$ = 600 Ω, 2 kΩ, 100 kΩ)

**Figure 22. Gain and Phase Margin vs Frequency**




($R_L$ = 600 Ω, 2 kΩ, 100 kΩ)

**Figure 23. Gain and Phase Margin vs Frequency**




($C_L$ = 0 pF, 100 pF, 500 pF, 1000 pF)

**Figure 24. Gain and Phase Margin vs Frequency**

## Typical Characteristics (continued)

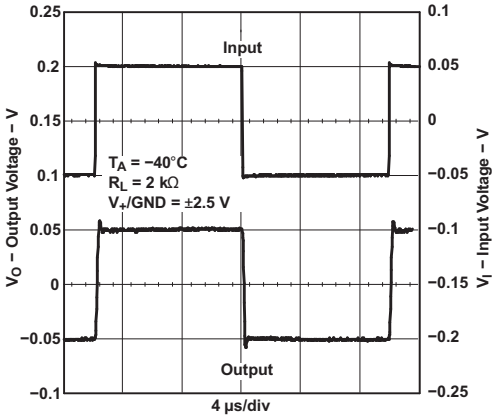



**Figure 25. Small-Signal Noninverting Response**

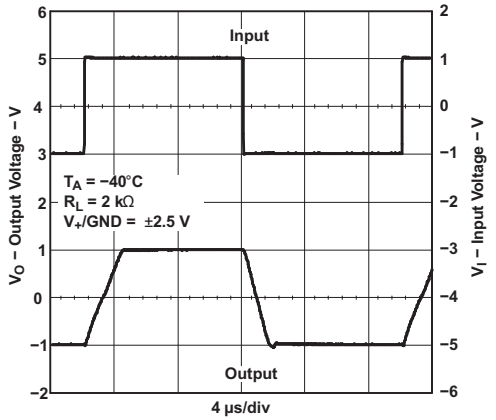



**Figure 26. Large-Signal Noninverting Response**

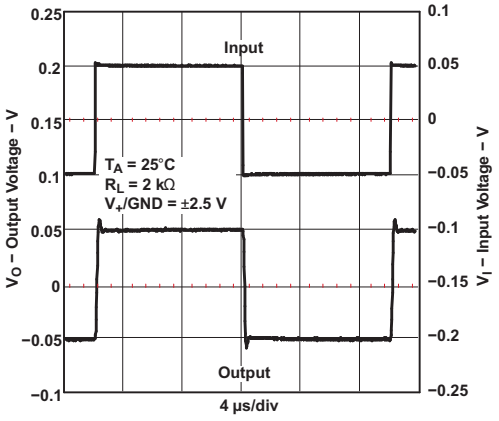



**Figure 27. Small-Signal Noninverting Response**

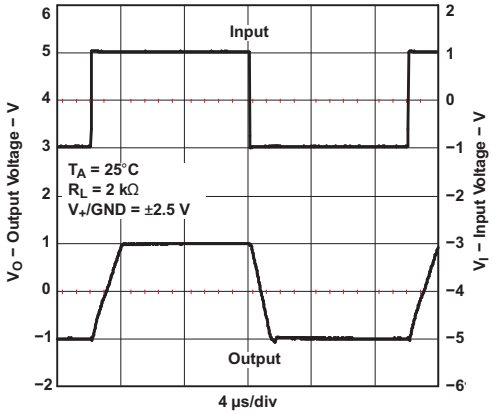



**Figure 28. Large-Signal Noninverting Response**

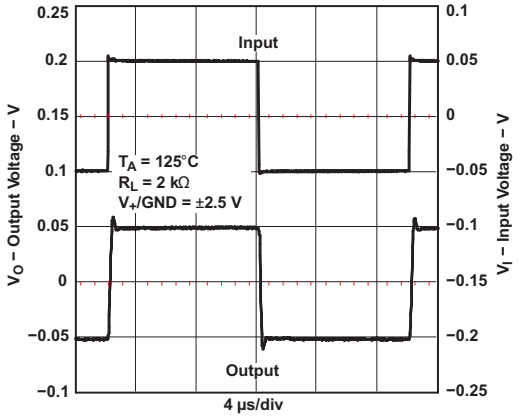



**Figure 29. Small-Signal Noninverting Response**

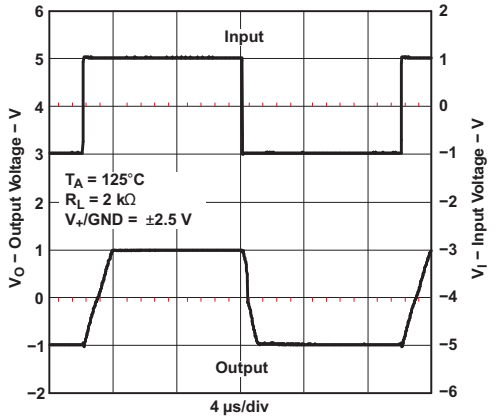



**Figure 30. Large-Signal Noninverting Response**

## Typical Characteristics (continued)

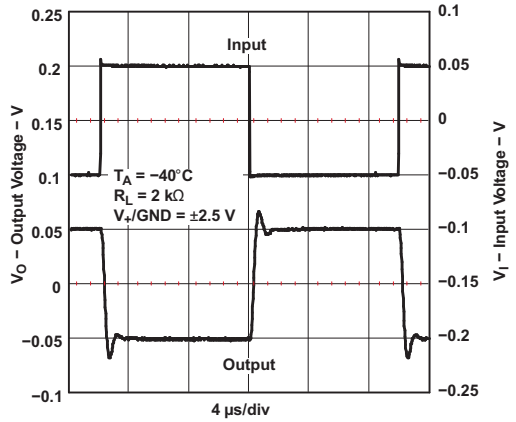



**Figure 31. Small-Signal Inverting Response**

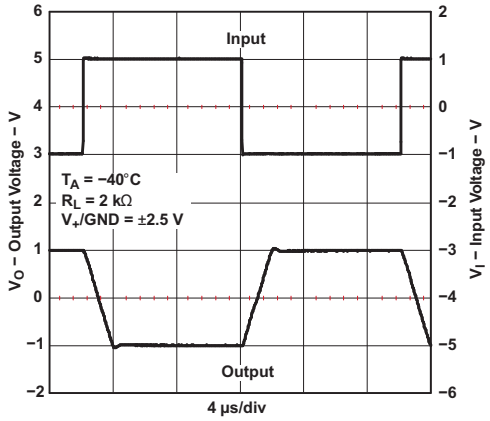



**Figure 32. Large-Signal Inverting Response**

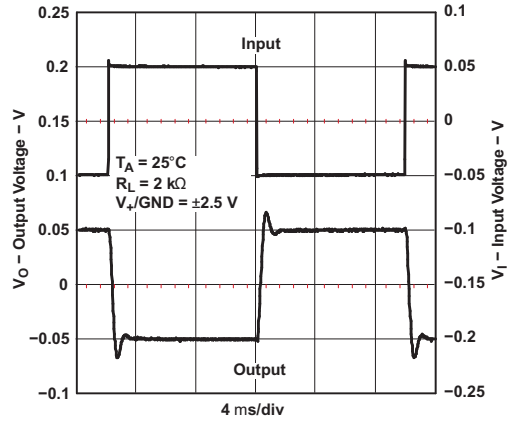



**Figure 33. Small-Signal Inverting Response**

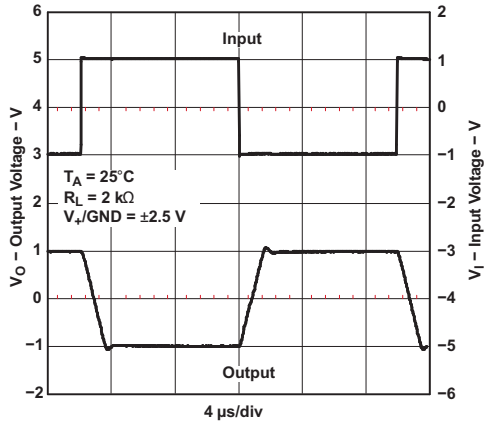



**Figure 34. Large-Signal Inverting Response**

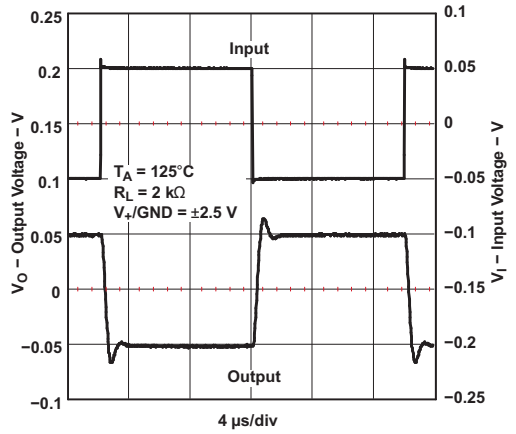



**Figure 35. Small-Signal Inverting Response**

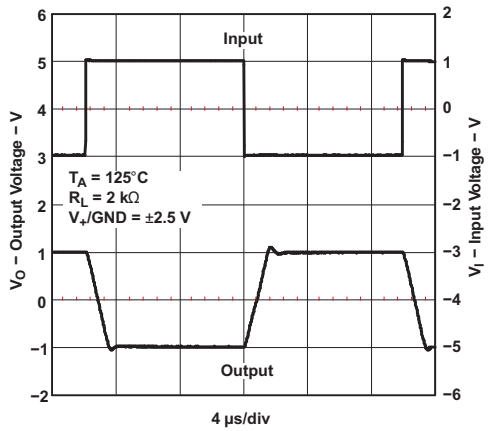


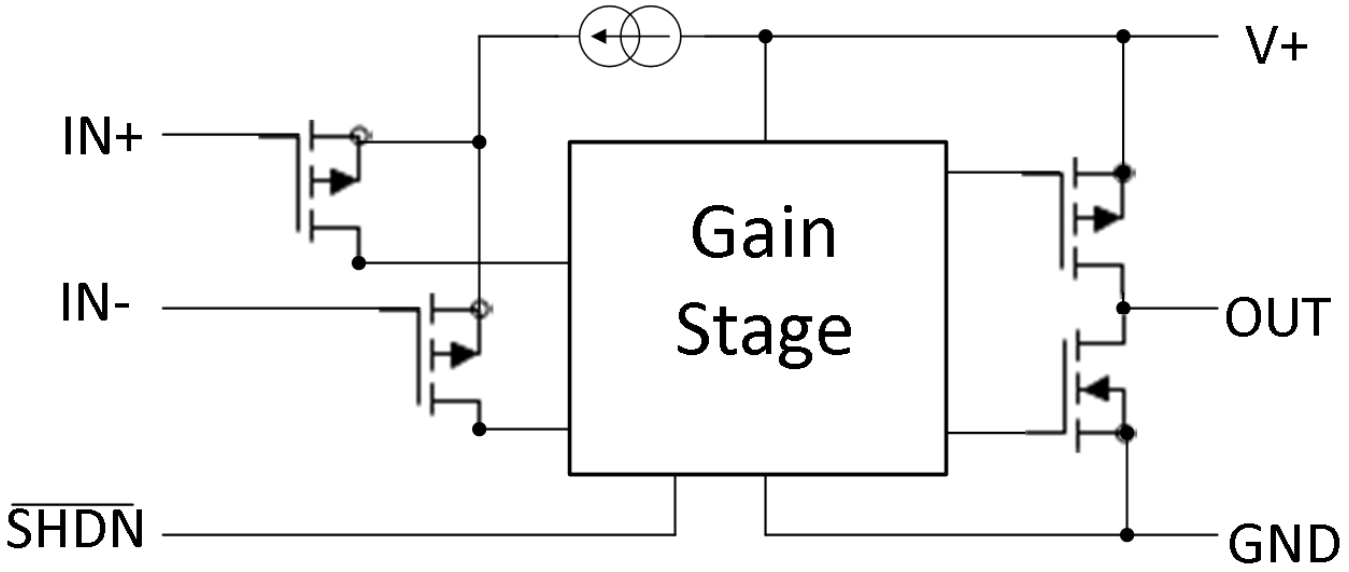

**Figure 36. Large-Signal Inverting Response**

# 7 Detailed Description

## 7.1 Overview

The LMV34x devices are precision operational amplifiers with CMOS inputs for very low input bias current. Output is rail-to-rail and input common-mode includes ground. LMV341 has a shutdown mode for very low supply current.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 PMOS Input Stage

PMOS Input Stage supports a lower input range that includes ground. Upper range limit is $V_+$ – 1 V.

### 7.3.2 CMOS Output Stage

The CMOS drain output topology allows rail-to-rail output swing.

### 7.3.3 Shutdown

LMV341 includes a shutdown pin. During shutdown, $I_{CC}$ is nearly zero and the output becomes high impedance. The typical turnon time coming out of shutdown is 5 µs.

## 7.4 Device Functional Modes

The LMV34x devices have two modes of operation:

- Normal operation when $\overline{SHDN}$ pin is at $V_+$ level or the $\overline{SHDN}$ pin is not present
- Shutdown mode when $\overline{SHDN}$ is at GND level; $I_{CC}$ is very low and output is high impedance.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

LMV34x devices have rail-to-rail output and input range from ground to VCC – 1 V. CMOS inputs provide very low input current. Shutdown capability is an option in dual amplifier version. Operation from 2.5-V to 5.5-V is possible.

## 8.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

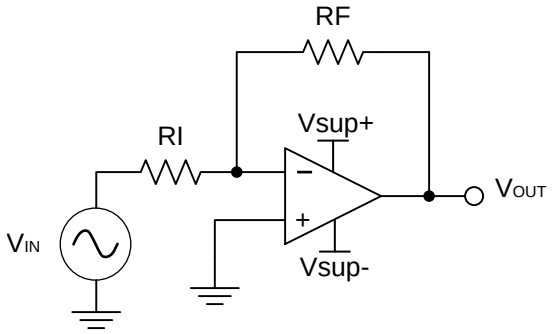





**Figure 37. Application Schematic**

### 8.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ± 2 V is sufficient to accommodate this application. The supplies can power up in any order; however, neither supply can be of opposite polarity relative to ground at any time; otherwise, a large current can flow though the input ESD diodes. To limit current in such an occurrence, TI highly recommends adding a series resistor to the grounded input. Vsup+ must be more positive than Vsup– at all times; otherwise, a large reverse supply current may flow.

### 8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2.

$$A_v = \frac{VOUT}{VIN} \tag{1}$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit uses currents in the mA range. This ensures the part does not draw too much current. For this example, choose 10 kΩ for RI, which means 36 kΩ is used for RF. This was determined by Equation 3.

$$A_v = -\frac{RF}{RI} \tag{3}$$

## Typical Application (continued)

### 8.2.3 Application Curve

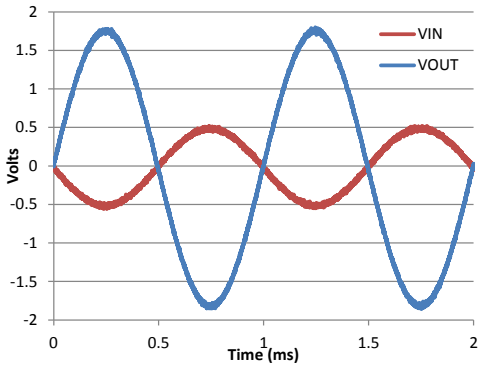



**Figure 38. Input and Output Voltages of the Inverting Amplifier**

## 9 Power Supply Recommendations

**CAUTION**

Supply voltages larger than 5.5 V for a single supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

# 10 Layout

## 10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from $V_+$ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, and pay attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Examples*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 10.2 Layout Examples

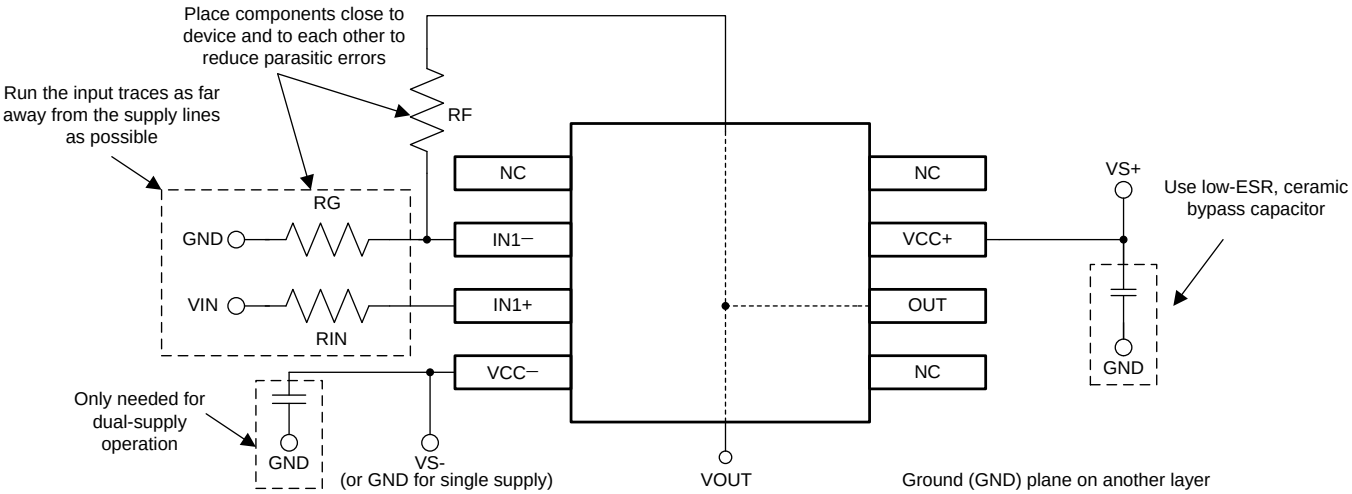



**Figure 39. Operational Amplifier Layout for Noninverting Configuration**

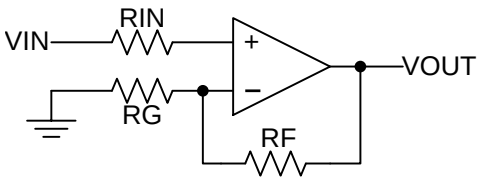



**Figure 40. Operational Amplifier Schematic for Noninverting Configuration**

# 11 Device and Documentation Support

## 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| LMV341 | Click here | Click here | Click here | Click here | Click here |
| LMV342 | Click here | Click here | Click here | Click here | Click here |
| LMV344 | Click here | Click here | Click here | Click here | Click here |

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMV341IDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC9A, RC9E, RC9S) | Samples |
| LMV341IDBVRE4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC9A, RC9E, RC9S) | Samples |
| LMV341IDBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC9A, RC9E, RC9S) | Samples |
| LMV341IDCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (R4A, R4E) | Samples |
| LMV341IDCKRG4 | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (R4A, R4E) | Samples |
| LMV342ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV342I | Samples |
| LMV342IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | RPA | Samples |
| LMV342IDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | RPA | Samples |
| LMV342IDGKT | PREVIEW | VSSOP | DGK | 8 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |
| LMV342IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV342I | Samples |
| LMV342IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV342I | Samples |
| LMV344ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV344I | Samples |
| LMV344IDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV344I | Samples |
| LMV344IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV344I | Samples |
| LMV344IPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV344I | Samples |
| LMV344IPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV344I | Samples |
| LMV344IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV344I | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMV344IPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV344I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF LMV341, LMV344 :**

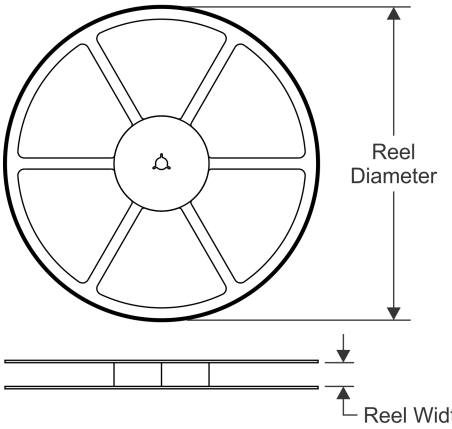
- Automotive: LMV341-Q1, LMV344-Q1

NOTE: Qualified Version Definitions:

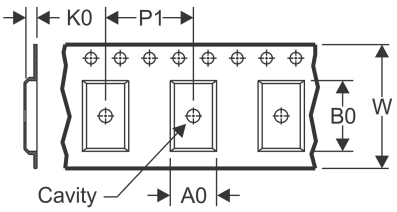
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

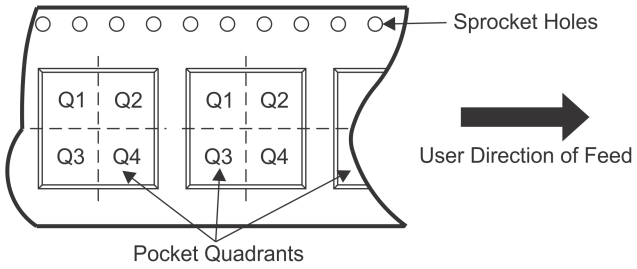



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

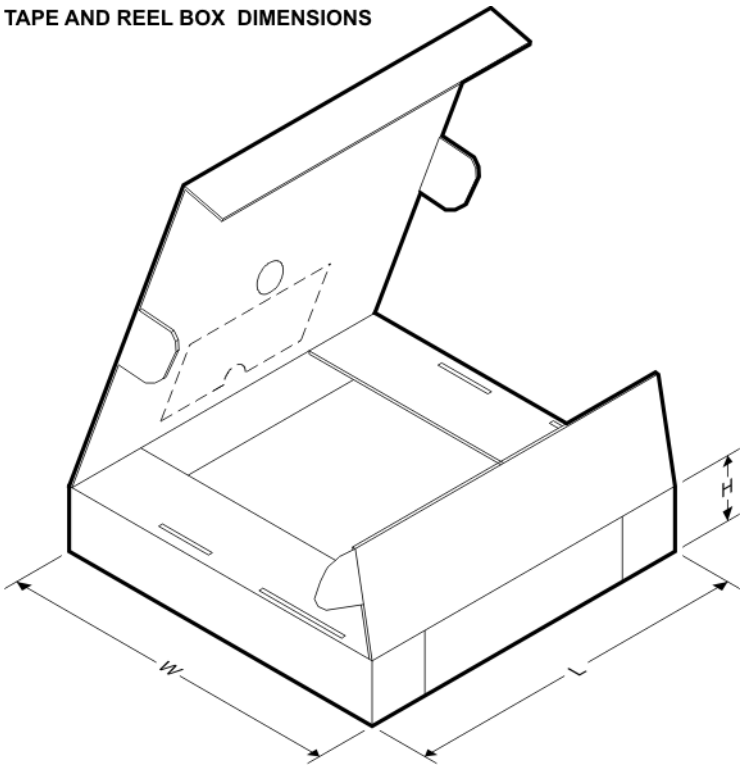
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMV341IDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| LMV341IDCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| LMV342IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMV342IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LMV344IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LMV344IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

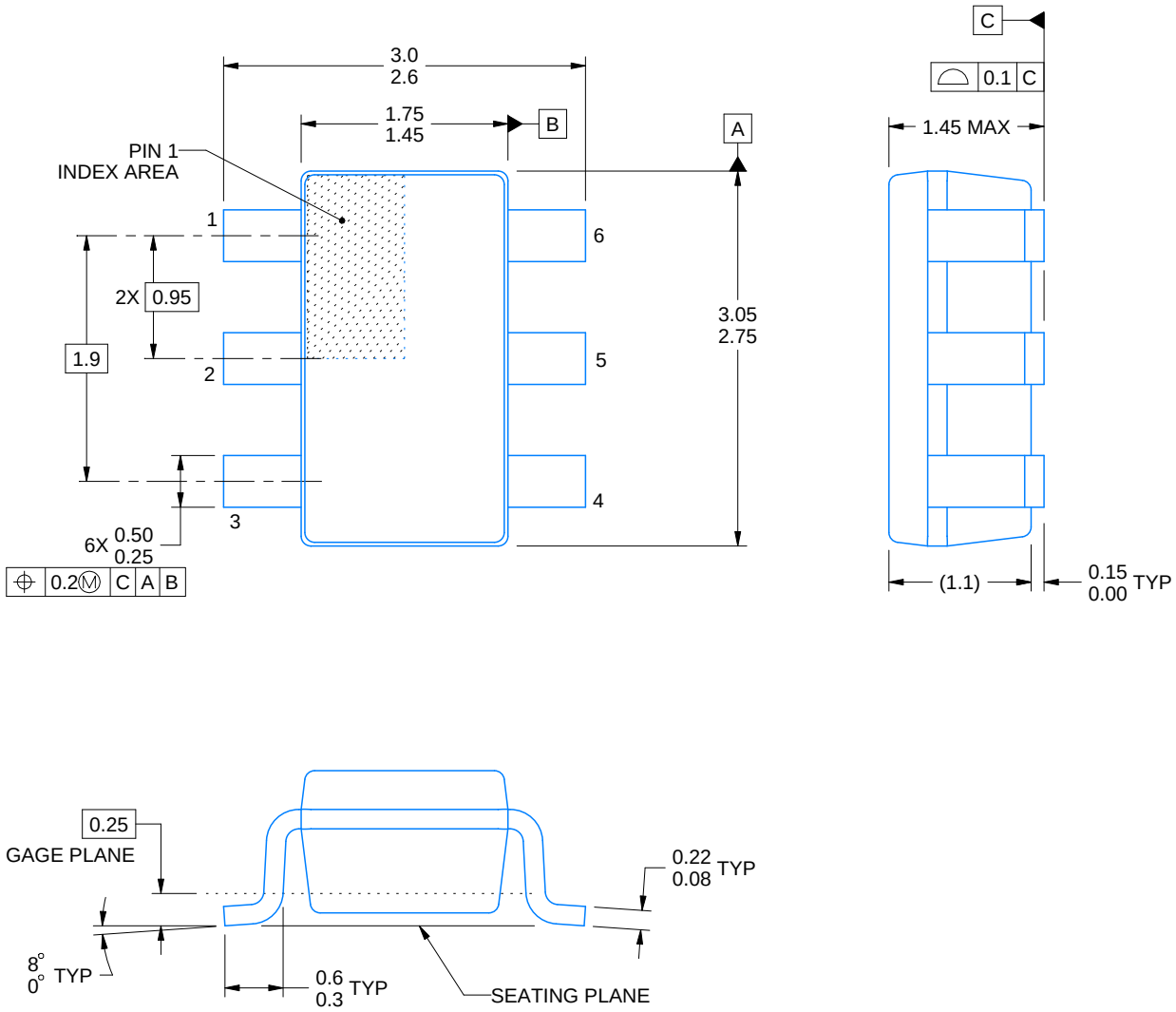
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMV341IDBVR | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| LMV341IDCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| LMV342IDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| LMV342IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| LMV344IDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| LMV344IPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

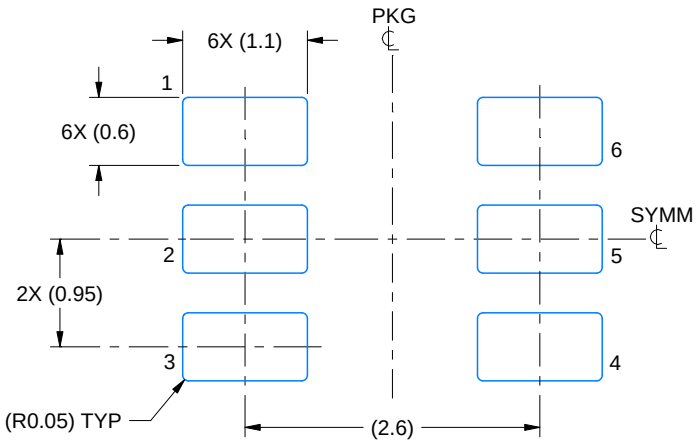
SMALL OUTLINE TRANSISTOR



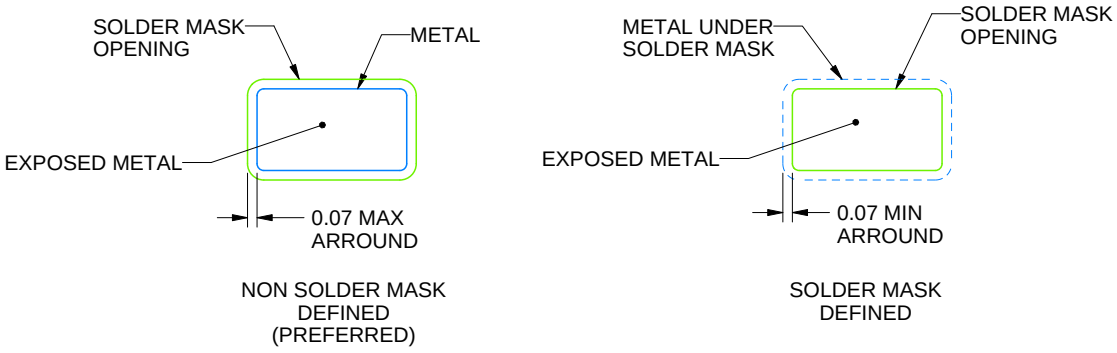

4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

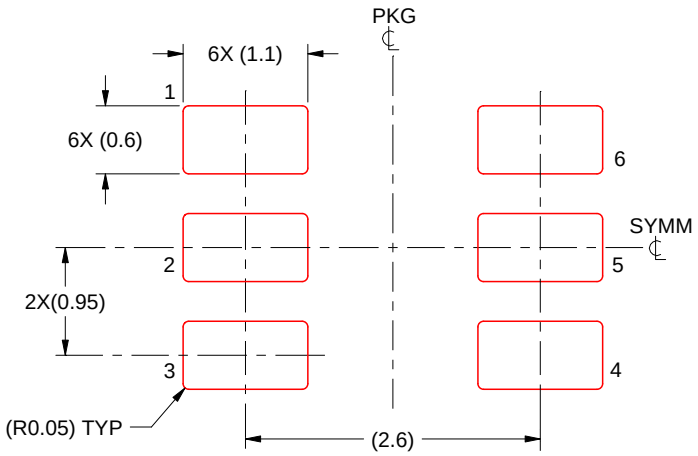



SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



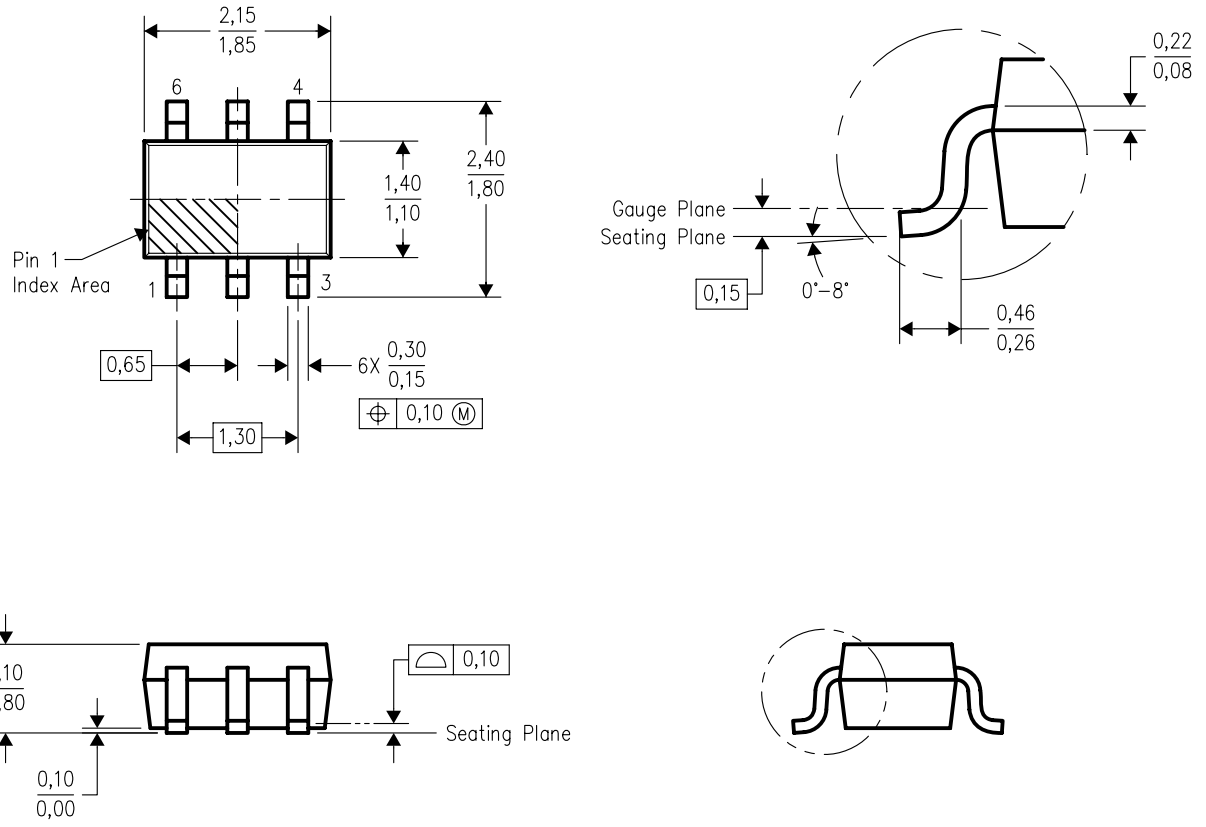

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

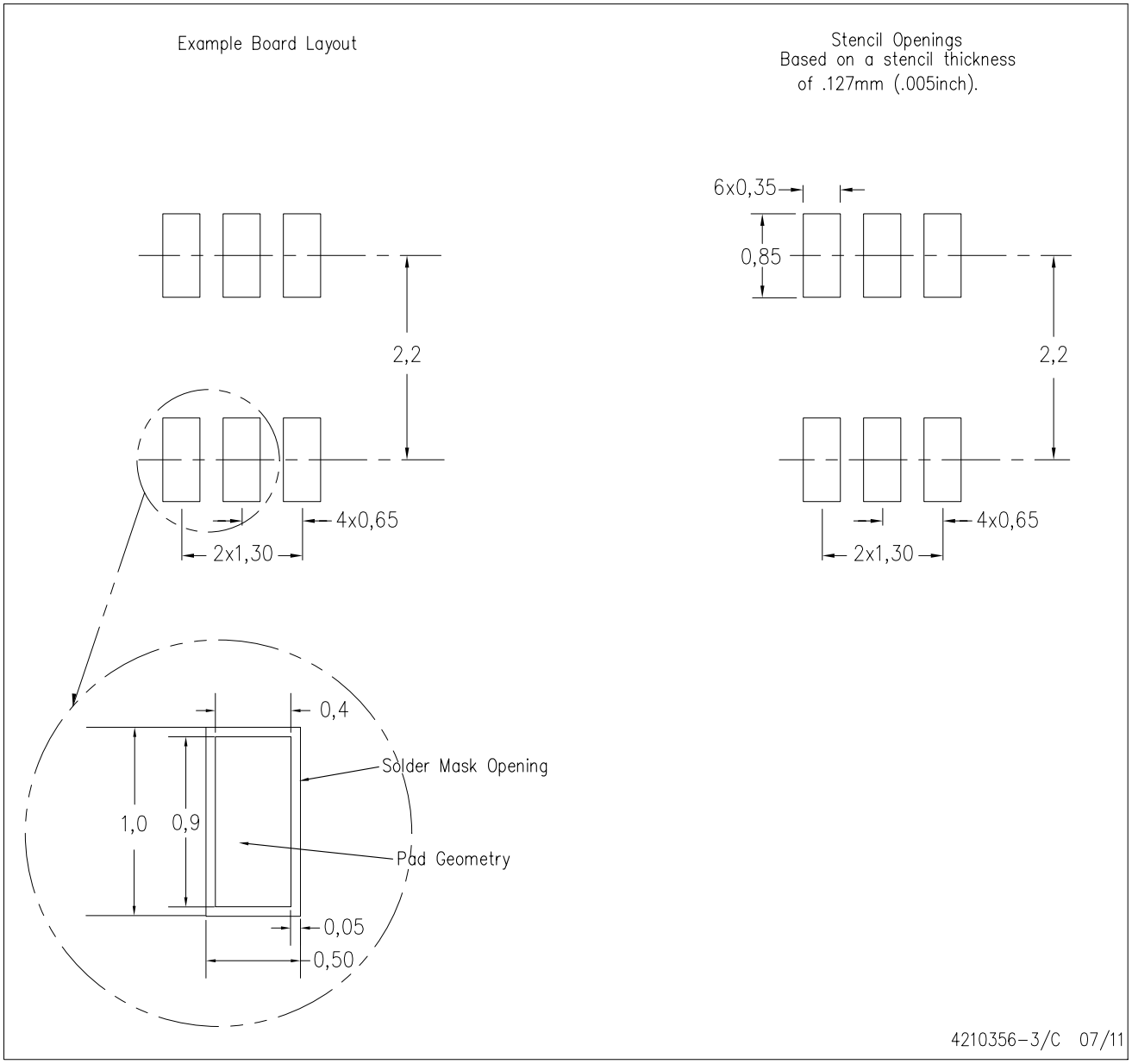
## DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




4093553–4/G 01/2007

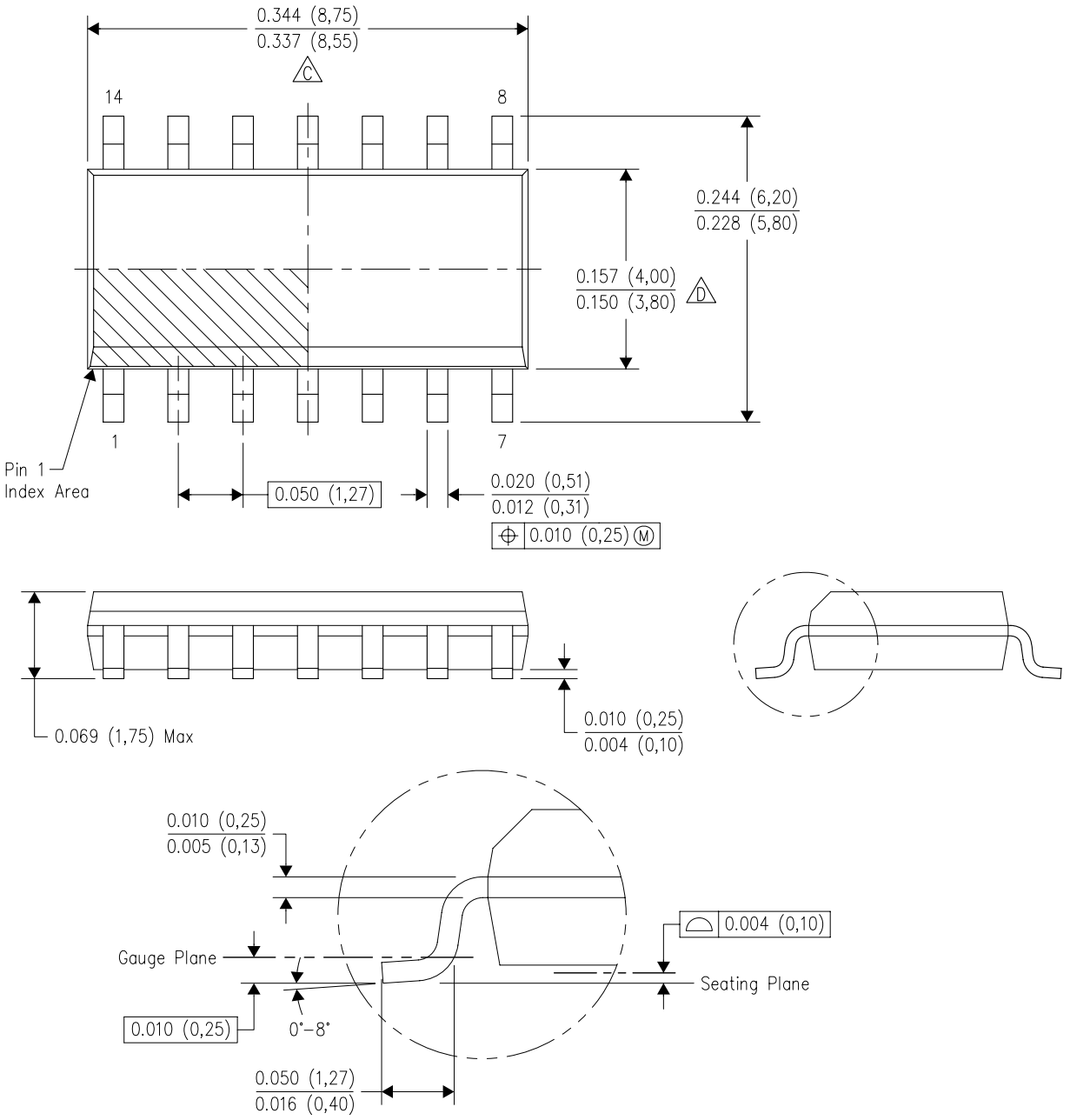
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

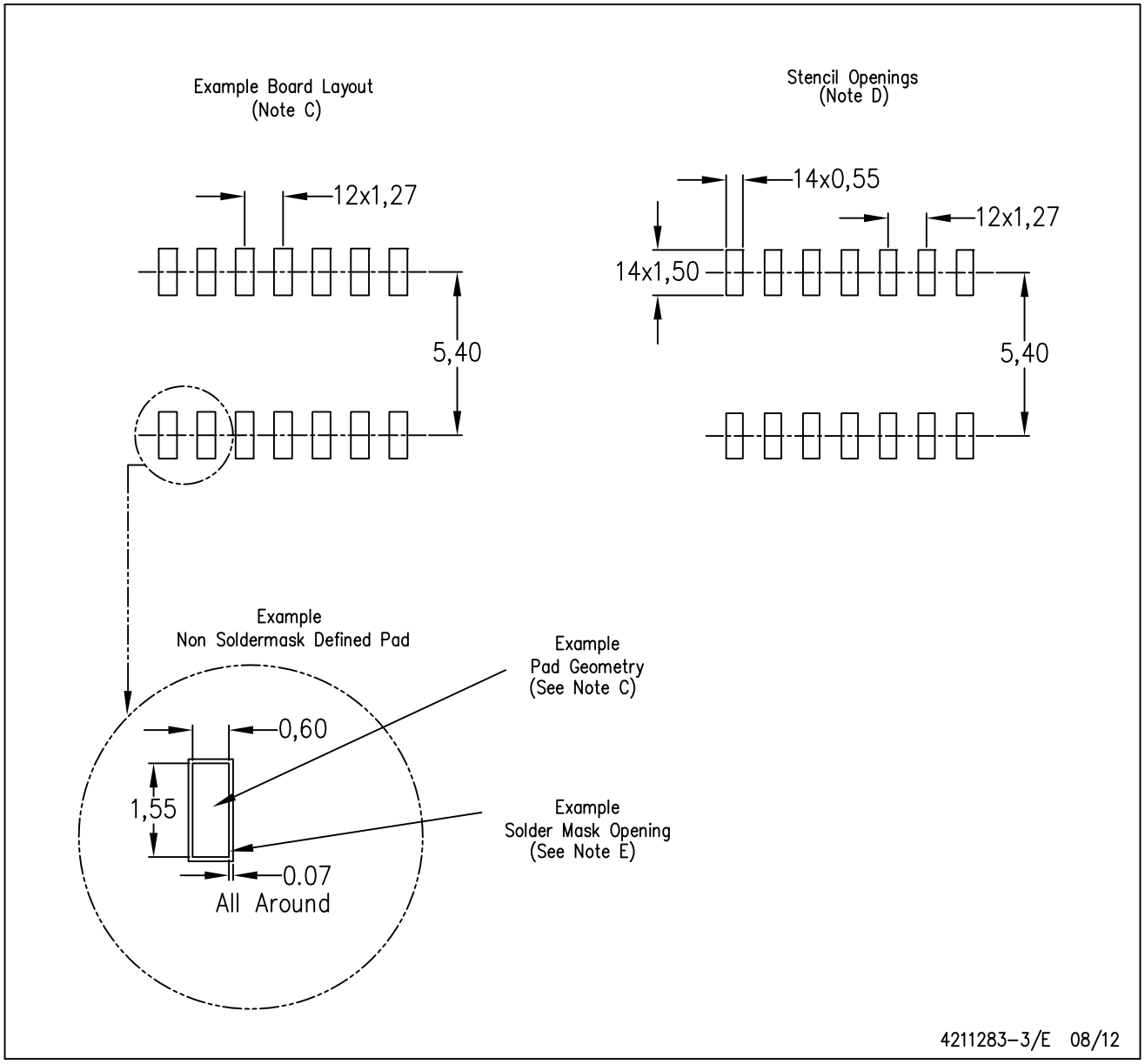
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

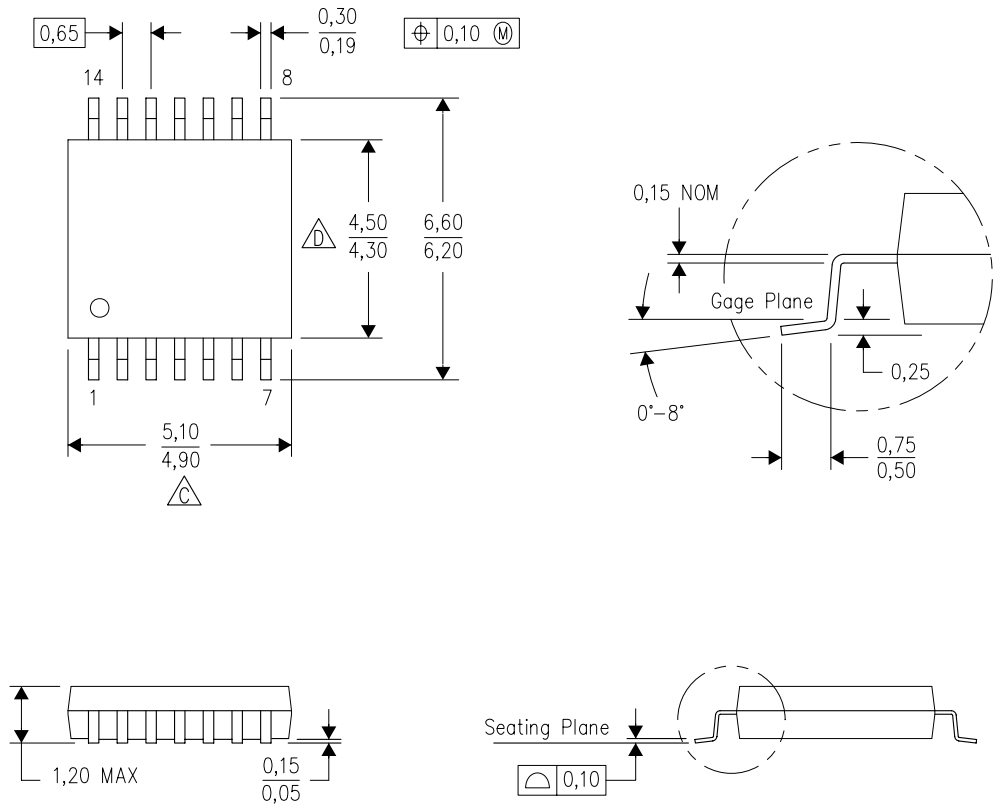
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

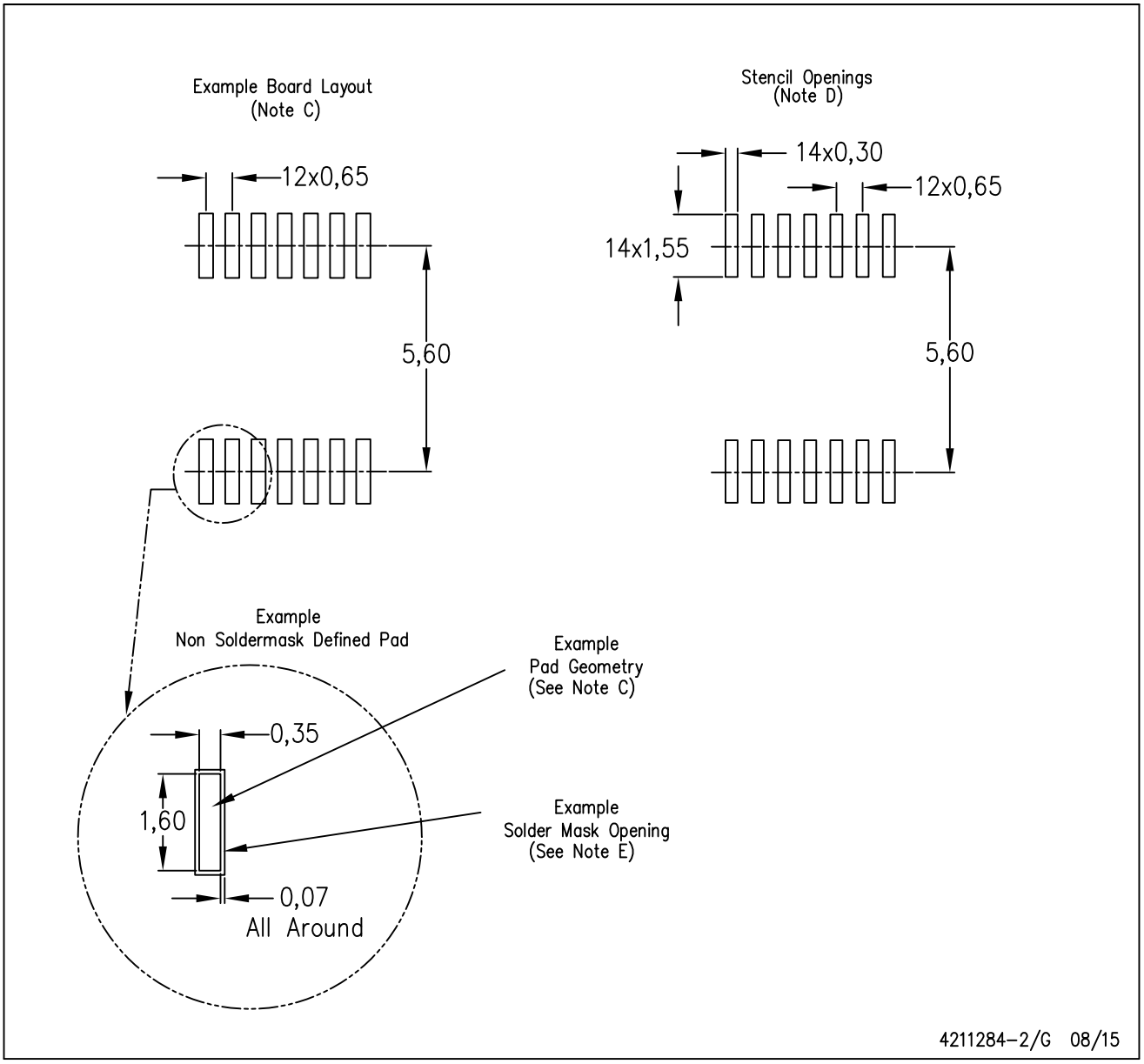
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



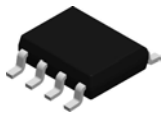

4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

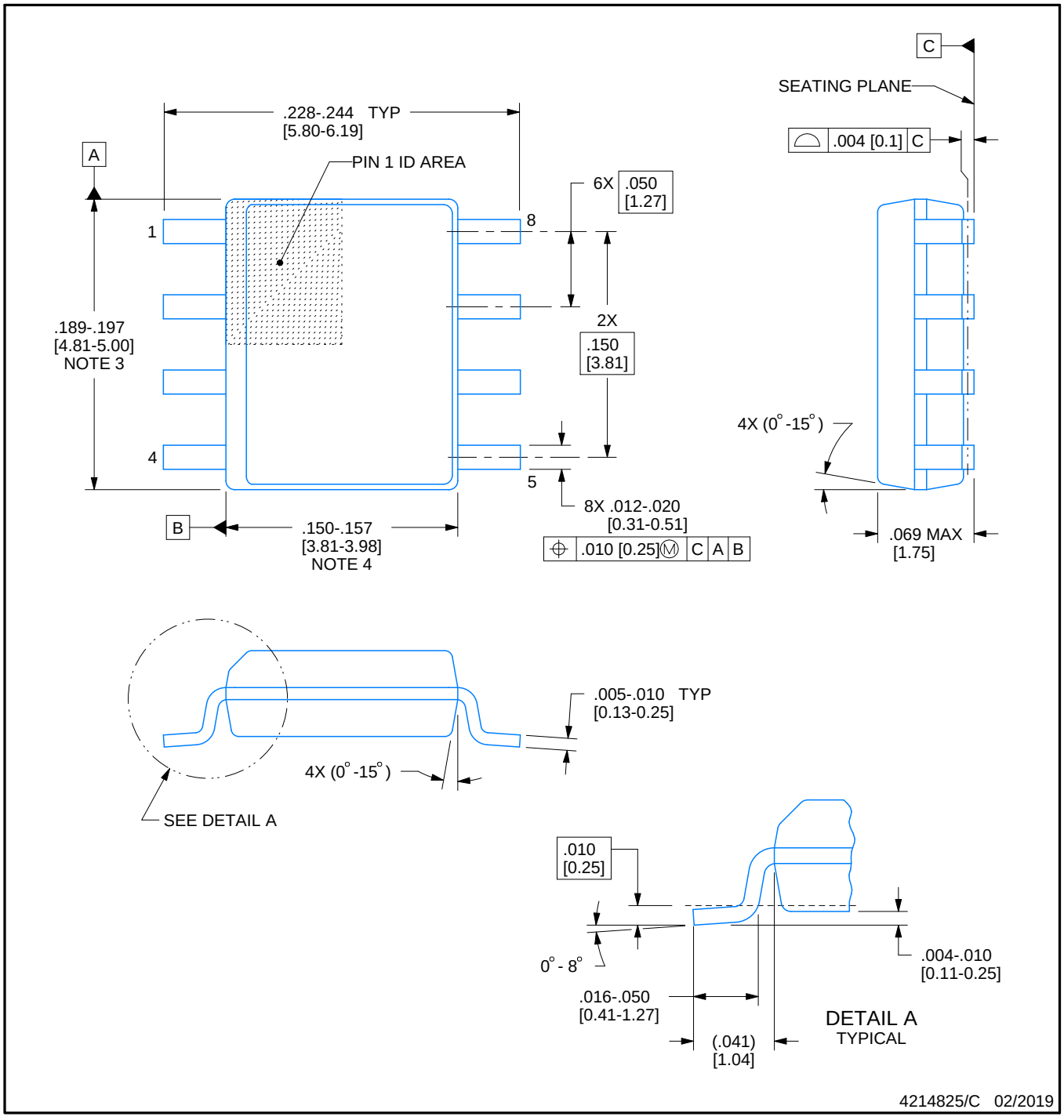


# PACKAGE OUTLINE

## D0008A

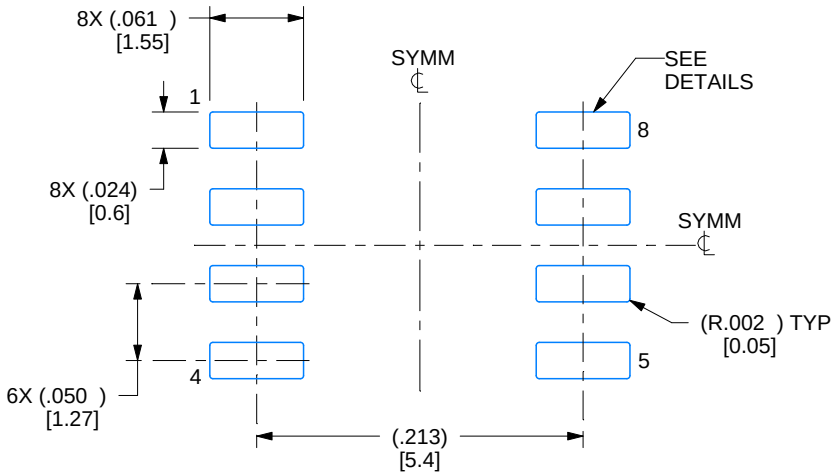
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

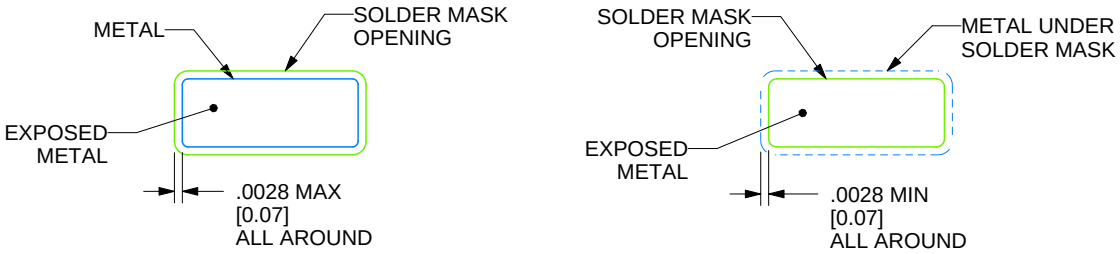



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

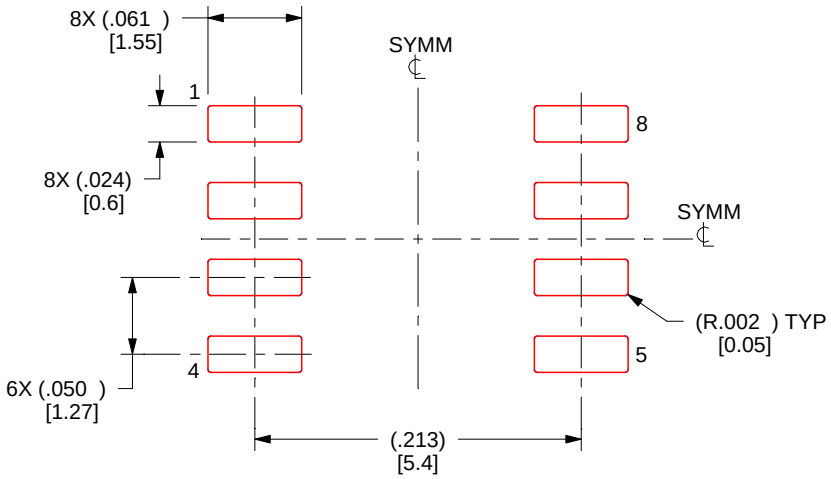
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



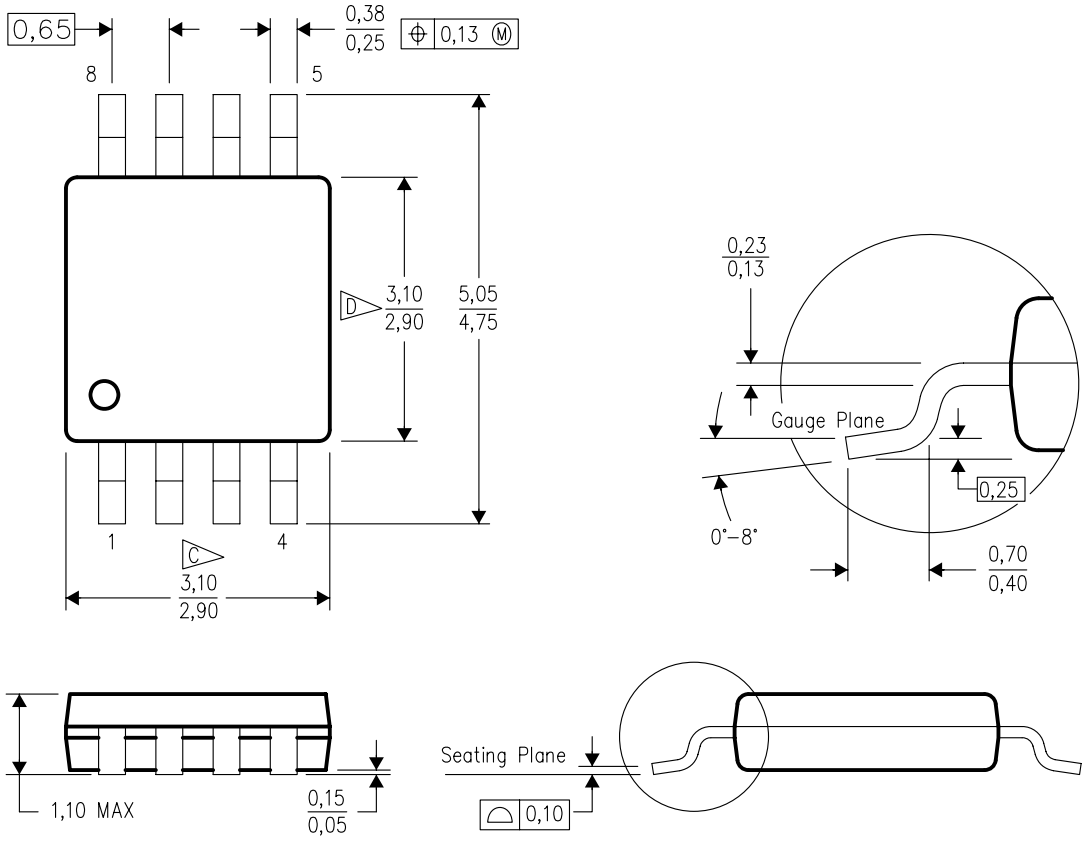

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

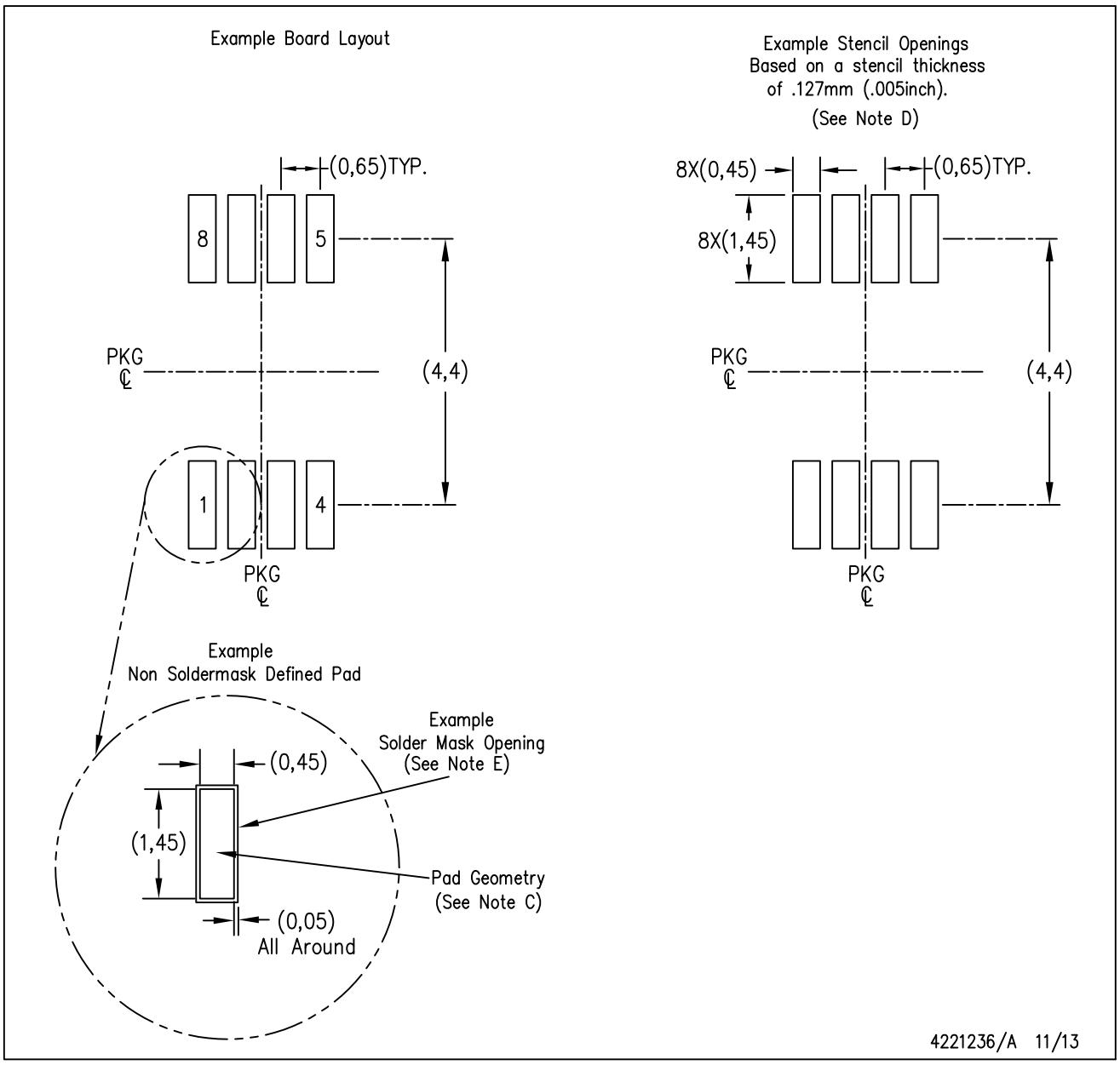
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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