

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT153** Dual 4-input multiplexer

Product specification  
File under Integrated Circuits, IC06

December 1990

## Dual 4-input multiplexer

## 74HC/HCT153

## FEATURES

- Non-inverting output
- Separate enable for each output
- Common select inputs
- See '253' for 3-state version
- Permits multiplexing from n lines to 1 line
- Enable line provided for cascading (n lines to 1 line)
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT153 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT153 have two identical 4-input multiplexers which select two bits of data from up to four sources selected by common data select inputs ( $S_0, S_1$ ). The two 4-input multiplexer circuits have individual active LOW output enable inputs ( $1\bar{E}$ ,  $2\bar{E}$ ) which can be used to strobe the outputs independently. The outputs ( $1Y, 2Y$ ) are forced LOW when the corresponding output enable inputs are HIGH.

The "153" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to  $S_0$  and  $S_1$ .

The logic equations for the outputs are:

$$1Y = 1\bar{E} \cdot (1I_0 \cdot \bar{S}_1 \cdot \bar{S}_0 + 1I_1 \cdot \bar{S}_1 \cdot S_0 + 1I_2 \cdot S_1 \cdot \bar{S}_0 + 1I_3 \cdot S_1 \cdot S_0)$$

$$2Y = 2\bar{E} \cdot (2I_0 \cdot \bar{S}_1 \cdot \bar{S}_0 + 2I_1 \cdot \bar{S}_1 \cdot S_0 + 2I_2 \cdot S_1 \cdot \bar{S}_0 + 2I_3 \cdot S_1 \cdot S_0)$$

The "153" can be used to move data to a common output bus from a group of registers. The state of the select inputs would determine the particular register from which the data came. An alternative application is a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

The "153" is similar to the "253" but has standard outputs.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> , 2I <sub>n</sub> to nY S <sub>n</sub> to nY n $\bar{E}$ to nY	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	14 15 10	16 17 11	ns ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per multiplexer	notes 1 and 2	30	30	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}, 2\overline{E}$	output enable inputs (active LOW)
14, 2	$S_0, S_1$	common data select inputs
6, 5, 4, 3	$1I_0$ to $1I_3$	data inputs from source 1
7	$1Y$	multiplexer output from source 1
8	GND	ground (0 V)
9	$2Y$	multiplexer output from source 2
10, 11, 12, 13	$2I_0$ to $2I_3$	data inputs from source 2
16	$V_{CC}$	positive supply voltage

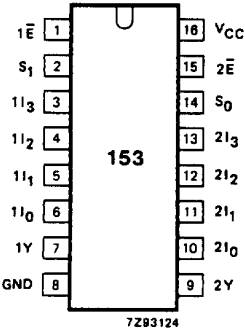


Fig.1 Pin configuration.

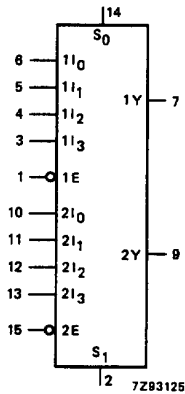


Fig.2 Logic symbol.

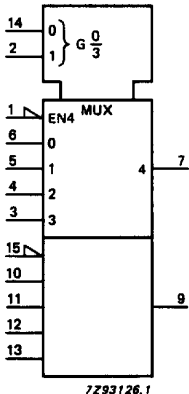


Fig.3 IEC logic symbol.

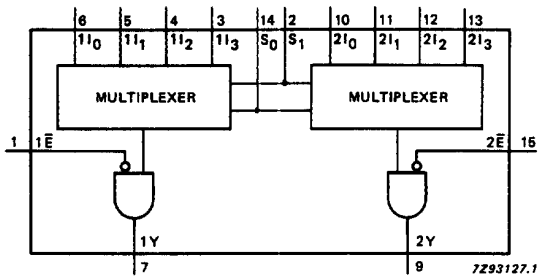


Fig.4 Functional diagram.

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FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S <sub>0</sub>	S <sub>1</sub>	nI <sub>0</sub>	nI <sub>1</sub>	nI <sub>2</sub>	nI <sub>3</sub>	n $\overline{\text{E}}$	nY
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Note

1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care

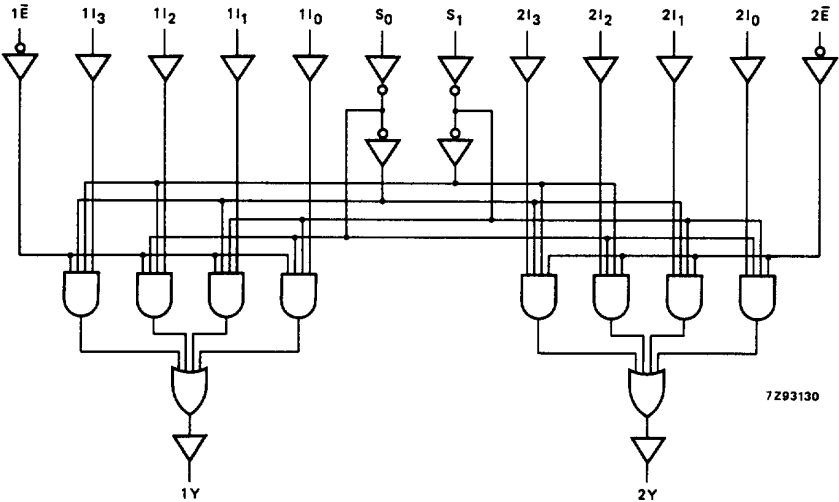


Fig.5 Logic diagram.

## Dual 4-input multiplexer

## 74HC/HCT153

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to+85		−40 to+125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> to nY; 2I <sub>n</sub> to nY		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to nY		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\overline{E}$ to nY		33 12 10	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1I_n, 2I_n$	0.45
$n\bar{E}$	0.60
$S_n$	1.35

**AC CHARACTERISTICS FOR 74HCT**

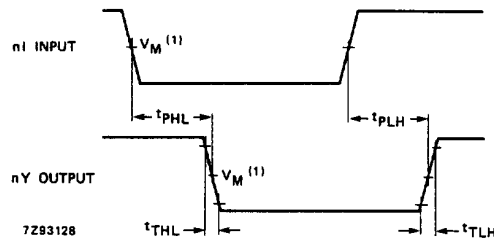
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to+85		−40 to+125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub>	propagation delay 1I <sub>n</sub> to nY; 2I <sub>n</sub> to nY		19	34		43		51	ns	4.5	Fig.6
t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> to nY; 2I <sub>n</sub> to nY		13	24		30		36	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to nY		20	34		43		51	ns	4.5	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\overline{E}$ to nY		14	27		34		41	ns	4.5	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

## Dual 4-input multiplexer

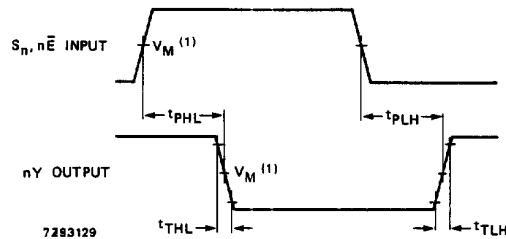
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## AC WAVEFORMS



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.6 Waveforms showing the input ( $1I_n, 2I_n$ ) to output ( $1Y, 2Y$ ) propagation delays and the output transition times.



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the select input ( $S_0, S_1$ ) and the output enable input ( $\bar{E}$ ) to output ( $1Y, 2Y$ ) propagation delays and the output transition times.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

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