ISLA112P50/55210EV1Z

Ultra Low Power Broadband 8 to 14-Bit Data Acquisition Platform

AN1725
Rev 0.00
March 8, 2012

ISLA112P50/55210EV1Z High Speed ADC/AMP Evaluation Board

- ISLA112P50 High Speed, Low Power ADC [12Bits,500MSPS]
- ISL55210 High Performance, Low Power, Differential Amplifier
- Compatible with Existing Intersil High-Speed ADC Evaluation Platform
- Optional Measurement Port to ADC Inputs
- Pin Compatible Family of 8- to 14-bit ADCs can be used.

Performance

- Clock Rate Range: 200MSPS to 500MSPS
- 200mV$_{P-P}$ Input (-10dBm) for -1dBFS ADC Input
- ±0.5dB flat response: 100kHz to 100MHz
- Typical SNR: 65dBFS
- Typical SFDR: 82dBC @ -1dBFS Input [10MHz to 100MHz Analog Input]

System Requirements

- ISLA112P50/55210EV1Z Evaluation Board
- KMB-001LEVALZ Intersil Motherboard (5V Supply Provided with Motherboard)
- Intersil Konverter Software http://www.intersil.com/converters/adc_eval_platform/
- Low Jitter Clock Source
- Bandpass Filter(s)

Evaluation Platform Overview

The ISLA112P50/55210EV1Z is an evaluation platform featuring Intersil's high-speed FDA (Fully Differential Amplifier) (ISL55210) and High Speed, Low Power 12-bit, 500Msps ADC (ISLA112P50). The PCB is compatible with Intersil's existing high speed ADC evaluation platform allowing for easy performance measurement and analysis. (*See* Intersil's Application Notes AN1433, AN1434 for more information). The ADC evaluation platform consists of custom designed hardware and software. The function of the hardware is to provide power to the ADC and to excite and/or measure the appropriate analog and digital inputs and outputs. The software is required to configure the device for initial operation, to modify the device functionality or parameters, and to process and display the output data. Konverter software version 1.22c (or later) supports the ISLA11XP50 family and the ISLA112P50/55210EV1Z PCB.

CONTACT THE FACTORY FOR ASSISTANCE IN USING THE KONVERTER SOFTWARE TO MODIFY THIS BOARD TO A DIFFERENT ADC.

Operating Precautions

IT IS STRONGLY RECOMMENDED TO INSERT THE +5V PLUG AT THE MOTHERBOARD PRIOR TO PLUGGING IN THE AC ADAPTER TO REDUCE THE POSSIBILITY OF POWER SURGES WHICH CAN DAMAGE THE PCB. PROBING ON THE PCB SHOULD BE DONE WITH CARE USING PROPER ESD TECHNIQUES WHILE HANDLING.

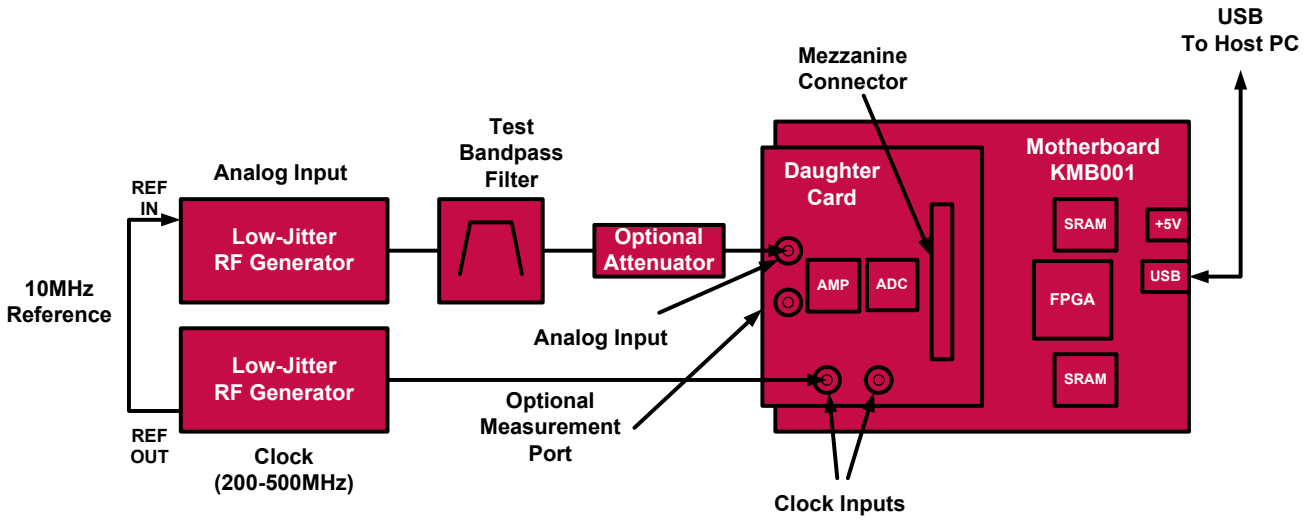

FIGURE 1. TYPICAL CHARACTERIZATION SETUP

Hardware

There are two components in the hardware portion of the evaluation platform: the daughter card and the motherboard (Figure 1). The FDA and ADC are contained on the daughter card, which routes power from the motherboard and contains the analog input circuitry, clock drive and decoupling. The daughter card interfaces to the motherboard through a mezzanine connector. The motherboard contains a USB interface, an FPGA and SRAM. The motherboard serves as the interface between the host PC and the ADC daughter card. Most of the ADC functionality is controlled through the motherboard by the Konverter software. The FPGA accepts output data from the ADC and buffers it in the SRAMs before passing it to the PC at a lower speed for post-processing. The maximum buffer depth is approximately one million words.

The user must supply a low-jitter RF generator for the clock input to achieve the SNR shown here. Recommendations of suitable generators can be found in “Appendix A: RF Generators” on page 13. Note, a low cost, low jitter 500MHz clock source also is available from Crystek - the RFPRO33-500.

Many low-jitter RF generators exhibit high harmonic spectral content relative to the ADC performance. A band-pass filter is recommended to attenuate the harmonics when testing the analog path.

Software

The software component is a Konverter Analyzer, a graphical user interface (GUI) created with MATLAB™. A MATLAB Component Runtime engine is supplied, which executes a compiled version of the m-files. Therefore, a stand-alone version of MATLAB is not required to run the Konverter Analyzer.

The GUI controls the ADC configuration through the SPI port, reads data from the motherboard and performs post-processing and display of the output data. Data can be viewed in the time or frequency domain, and can be saved for later processing. Critical performance parameters such as SNR, SFDR, harmonic distortion, etc. are calculated and displayed on-screen when viewing in the frequency domain. Different regions of the FFT output may be easily viewed by zooming in using the settings available in the Konverter software.

Initial Start-Up

Referring to Figure 1, connect the daughter card to the motherboard by aligning the two matching mezzanine connectors. Four screws on the motherboard (not shown) align with mounting holes in the daughter card. Next, connect the clock source (~10dBm) which is required for communication to the Konverter software, then connect a test source or signal of interest coming from your signal channel at a maximum V_{P-P} < 200mV (-10dBm). With the RF generators on, apply +5V power (minimum 5W supply) to the motherboard. The daughter card is powered by linear regulators on the motherboard. A USB cable should then be connected after +5V power has been applied. (Use the same USB port that was used when Konverter was initially installed so the hardware is recognized).

Motherboard

The only connections required for the motherboard are +5V power and a USB connection to the PC running Konverter Analyzer. No additional configuration of the motherboard is required. *IT IS STRONGLY RECOMMENDED TO INSERT THE +5V PLUG AT THE MOTHERBOARD PRIOR TO PLUGGING IN THE AC ADAPTER TO REDUCE THE POSSIBILITY OF POWER SURGES, WHICH CAN DAMAGE THE PCB. PROBING ON THE PCB SHOULD BE DONE WITH CARE USING PROPER ESD TECHNIQUES WHILE HANDLING.*

Software Start-Up

The FPGA clock is derived from the ADC output clock, and the FPGA clock must be active for the software to run properly. Therefore, it’s important that the evaluation platform is powered and receiving a conversion clock prior to initializing the Konverter Analyzer Software.

The compressed MATLAB files are unpacked the first time the GUI is invoked after installation. Subsequently, the graphical window will open more quickly. Complete information can be found in the KMB-001 Installer manual.

http://www.intersil.com/converters/adc_eval_platform/

The main Konverter Analyzer window is shown in Figure 4. The application opens in FFT mode by default, but other modes can be selected using the radio buttons in the lower left corner. In each mode, relevant parameters are displayed in the data box on the left side of the window.

The following parameters are displayed in the data box in all operating modes:

- Fsamp: Sample clock frequency, automatically detected
- Ffund: Input frequency, automatically detected (assumes sine wave single tone input)
- Fund: Input amplitude (in dBFS)
- Samples: Record length
- Power: Total ADC power dissipation (FDA Power is in addition to this), as well as the voltage and current of each ADC supply

Data Acquisition

Press the Run button in the lower left corner of the screen to produce a single FFT plot. The Continuous check box can be selected to capture and display successive FFT plots. Multiple acquisitions can be averaged by selecting the Average check box. The number of averaged acquisitions defaults to 10, but can be changed in the Setup Conditions dialog. The FFT window also allows for tuning the number of frequency bins used in the FFT calculations.

Menu items and the toolbar buttons may not function properly if data is being captured in Continuous mode. Stop the acquisition before selecting a menu item or using a toolbar button.

FIGURE 2. ISLA112P50/55210 DAUGHTERBOARD

.

FIGURE 3. DAUGHTERBOARD WITH KMB MOTHERBOARD

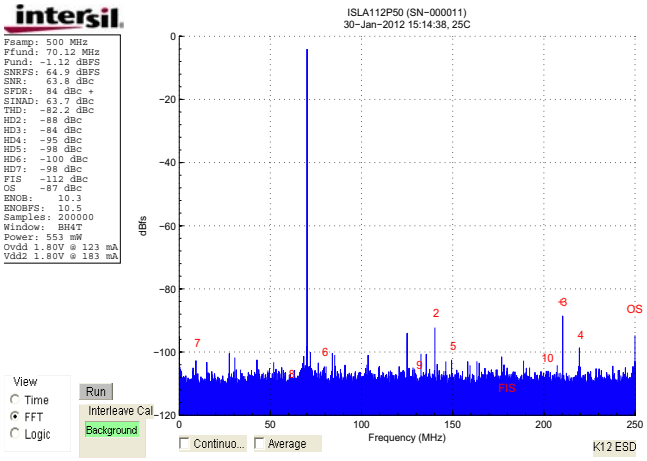

FIGURE 4. FFT OUTPUT WITH 70MHZ ANALOG INPUT

Figure 4 shows a typical FFT for the PCB with a 70MHz Analog Input with the drive level adjusted to ~ -9.4dBm at the card edge resulting in a -1dBFS signal for the ADC. The ISLA112P50 is a low power 500Msps 12-bit ADC, more detailed information on the ADC can be found in the datasheet (http://www.intersil.com/data/fn/fn7604.pdf)

Menus

AN1433 should be consulted for more information on the File, Setup, and Help software menus. AN1434 has information on software installation if needed.

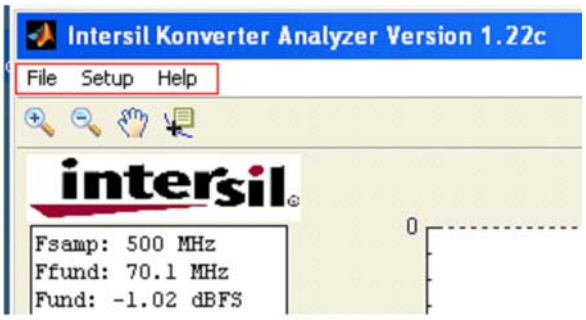

FIGURE 5. KONVERTER MENUS

Analog Signal Path Description

The amplifier implementation on this daughterboard is intended to:

1. Terminate a single-ended input source with an AC-coupled broadband 50Ω impedance.
2. Convert the single-ended source to differential inputs for the ADC.
3. Provide extremely low noise and distortion amplification from a nominal -10dBm (200mV$_{P-P}$ single tone) input to a differential V$_{P-P}$ at the ADC inputs of approximately 1.3V$_{P-P}$. This 6.45V/V gain (16.2dB) gain is a combination of input transformer step up, amplifier gain, and interstage filter insertion loss.
4. The interstage filter between the amplifier's differential outputs and the ADC, also level shifts the Vcm output voltage from the amplifier to a lower Vcm voltage required by the ADC.

The signal path circuit can be broken into an input side operation and then an output interstage filter.

Figure 6 shows the input circuit for this daughterboard. Elements in green are optional and not populated for the nominal design board as delivered.

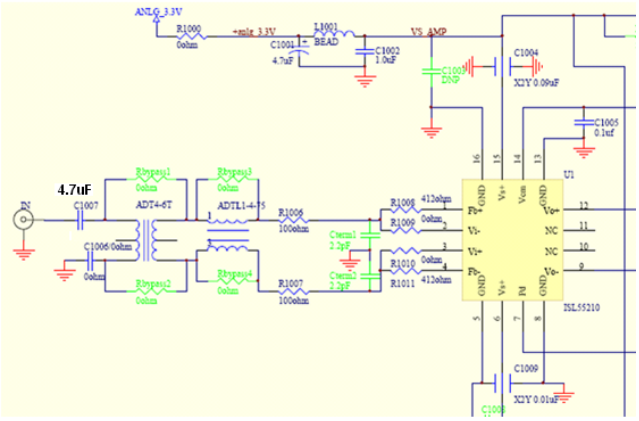

FIGURE 6. POWER SUPPLY DECOUPLING AND INPUT SIDE TRANSFORMER/FILTER BEFORE ADC

The input is AC-coupled through a 4.7µF blocking cap into the primary side of a 1:2 turns ratio step-up transformer; a Minicircuits ADT4-6T device. The blocking cap protects the source from accidental DC shorts while adding a 1.4kHz high-pass pole (if the source is 50Ω). The 2nd transformer (ADTL1-4-75) acts as a common mode choke improving the differential balance for the amplifier stage. Ignoring it for a moment, the two 100Ω resistors (R1006 and R1007) act as both the gain resistors for the ISL55210 Fully Differential Amplifier (FDA) and the input termination elements. They drive into the differential summing junction of the FDA, which will appear as a broadband virtual ground for the differential signal. Since the input transformer is a 1:4 ohms ratio step up, those two 100Ω elements will add together to look like a 200Ω termination. They input refer through the transformer to appear as a 50Ω termination to the source. Detailed specifications on the 4GHz, 0.85nV/√Hz input noise ISL55210 may be found at – http://www.intersil.com/data/fn/fn7811.pdf

The purely differential signal at the output side of 2nd transformer then gets through to the amplifier differential output gained up by the two 412Ω feedback resistors. A complete description of the noise, loop gain, and signal path balance of this implementation may be found in this series of 4 articles.

- **Part 1. Advantages to transformer input in a single to differential AC-coupled application.**

http://www.eetimes.com/design/analog-design/4215415/Deliver-the-lowest-distortion-and-noise-in-a-low-power--wideband--ADC-interface--Part-1-of-4-

- **Part 2. Calculating integrated noise at the ADC for different filters and input pin SNR with the ADC for a net result.**

http://www.eetimes.com/design/analog-design/4215416/Deliver-the-lowest-distortion-and-noise-in-a-low-power--wideband--ADC-interface--Part-2-of-4-

- **Part3. Distortion issues and combining SFDR at input pins with ADC for a net result.**

http://www.eetimes.com/design/analog-design/4215417/Deliver-the-lowest-distortion-and-noise-in-a-low-power--wideband--ADC-interface--Part-3-of-4-

- **Part 4. Summary amplifier + ADC data on the Rev. A daughterboard and transformer modeling.**

http://www.eetimes.com/design/analog-design/4215418/Deliver-the-lowest-distortion-and-noise-in-a-low-power--wideband--ADC-interface--Part-4-of-4-?Ecosystem=analog-design

This article series was not including the 2nd common mode choke transformer (T2). Significant HD2 improvement at higher frequencies was found in adding this to the design. Thus, going from the Rev. A board described in the article series to the Rev. C final implementation, added that component. One of the options on this board is to eliminate that transformer and short across its pins with 0Ω resistors.

Frequency Response Flatness Issues

Each of the elements in the signal path have fine scale rolloffs that need to be considered to achieve the final ±0.5dB flatness through the 100kHz to 100MHz range.

The ADT4-6T input transformer was selected mainly for its low frequency performance. While specified as -1dB flat from 150kHz to 200MHz, it actually does better than this in lab tests. Figure 7 shows the measured S21 response for several of the transformer options (for 1:2 turns ratio) possible on this board. Here, the ADT4-6T is clearly very flat down to 100kHz while hitting about -1dB at its specified 200MHz on this 2dB/div plot. These measurements included a resistor output network that looks like 200Ω to the transformer but 50Ω to the network analyzer – giving an insertion loss to the measurement but more accurately measuring the S21 flatness.

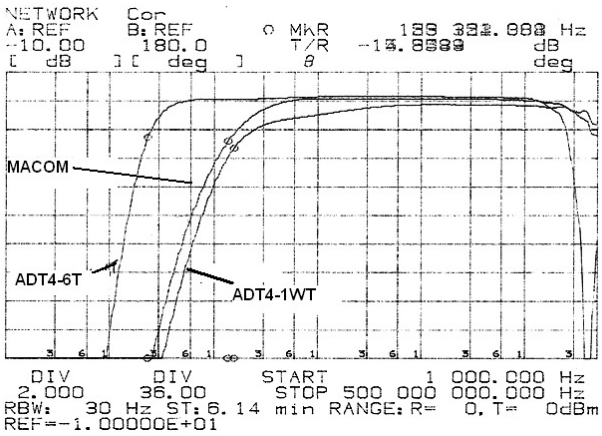

FIGURE 7. OPTIONAL INPUT 1:2 TURNS RATIO TRANSFORMERS MEASURED IN 50Ω SYSTEM

The ADT4-6T is a good match to this 100kHz to 100MHz design. To modify this board to higher frequencies, the Macom MABA0096-CF48A0 seems to give a little better flatness range vs the ADT4-1WT from Mini-circuits. The Macom device measures very flat over a 1MHz to 200MHz range.

The 2nd common mode choke transformer (ADTL-4-75, T2 in Figure 6) is extremely broadband, showing < 0.25dB insertion loss from DC to 100MHz. While not specified by MiniCircuits, since these elements are in fact a DC short, the loss below the minimum specified frequency of 500kHz actually decreases. For higher frequency designs, the pin compatible ADTL1-12 holds lower insertion loss through 200MHz.

The amplifier will have its own frequency response from these source impedances and gain settings. One of the subtle advantages of this configuration is that the signal gain is higher than the amplifier noise gain. In the default circuit, the amplifier is operating at a signal gain from the output of the transformer that is simply the ratio of the feedback to gain setting resistors (4.12V/V here). However, looking at the noise gain for this Voltage Feedback Amplifier (VFA) implementation will also see the source element coming through the transformers as another 100Ω element on each side if the source signal is coming from a 50Ω impedance. Thus, the amplifier believes it is in a 1+ 412/200 = 3.06V/V noise gain while delivering a signal gain of

4.12V/V. These issues are described and explored in detail in the ISL55210 EVM board users guide available at - http://www.intersil.com/data/an/an1649.pdf

From that, a series of bandwidth vs Rf value curves were taken. These are using a different input transformer, ADT2-1T, that has a bit broader response on the high end. Stepping Rf is stepping the gain, with fixed 50Ω Rg resistors, which provide the match for the 1:2 ohms ratio input transformer used for this data. The Rf = 300Ω curve (between the 200Ω and 400Ω curves in Figure 8) is the same noise gain as that described on the ADC daughterboard where we see a very flat response through 100MHz.

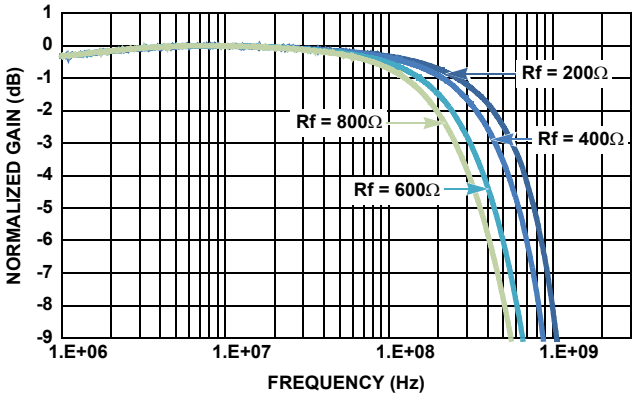

FIGURE 8. MEASURED AMPLIFIER FREQUENCY RESPONSE vs GAIN SETTING ($1V_{P-P}$ OUTPUT)

Increasing the amplifier gain does of course start to rolloff the frequency response as you move higher for the VFA design. The two input node capacitors in Figure 6 on page 3 (green, not populated 2.2pF), can be used as a fine tune on the output rolloff to the amplifier output pins. They were not used here as the response using the ADT4-6T and this relatively low gain setting on the ISL55210 did not require any equalization. This technique should be used with caution as it is also peaking up the output spot noise, which can quickly degrade the overall SNR for the solution. The ISL55210 Device information page includes a Spice Model that can be used to test these issues.

http://www.intersil.com/products/deviceinfo.asp?pn=ISL55210

Power Supply Decoupling Issues

The Daughterboard schematic of Figure 6 shows one example of good power supply decoupling for this single 3.3V supply device. Where possible, a large valued capacitor isolated towards this 4GHz amplifier with a high frequency ferrite and then another 1µF element provides a Pi filter on the board. Right at the device pins, the daughterboard uses two X2Y capacitors on each side of the package to get the best high frequency decoupling. Standard 0.01µF can also be used, which may reduce the HD2 performance at higher frequencies.

Amplifier to ADC Interstage Circuit and Vcm Issues

Figure 9 shows the signal path from the amplifier outputs to the ADC inputs.

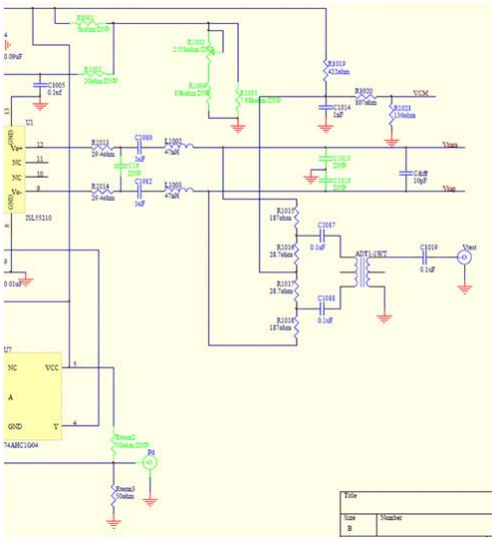

FIGURE 9. INTERSTAGE CONNECTIONS FROM THE AMPLIFIER TO THE ADC

The basic signal path is from the two amplifier output pins on the left through the differential RLC filter to the two ADC input pins on the right (Vinp and Vinm). The circuit here looks a little more involved than an actual end equipment implementation as it includes some optional features.

The ISL55210 includes an internally regulated 1.2V common mode voltage generator. The circuit implemented here uses that and no connection to the external Vcm adjustment pin on the ISL55210 is required. These are the resistor and pot elements at the top of Figure 9. If a very high insertion loss filter needs to be tested on this board, where the required V_{P-P} at the amplifier outputs exceeds $3V_{P-P}$, moving the default amplifier Vcm up will give more output swing range. This can be done by populating the optional amplifier Vcm adjustment elements (R1001 and R1005).

On the lower part of Figure 9 is a logic gate to drive the disable line on the ISL55210. With the 50Ω termination tied to ground with no input signal, this 74AHC1G04 single inverter holds the amplifier enable line high (keeping it turned on) but it can certainly be connected to control signal input to test this feature.

Interstage Filter Design and Vcm Bias

Figure 10 shows an iSim PE simulation circuit for the filter and Vcm bias circuit implemented on the board as shown in Figure 9. This is a free Spice and Power simulator available in the Intersil web site at

http://web.transim.com/intersil/iSimPE.aspx

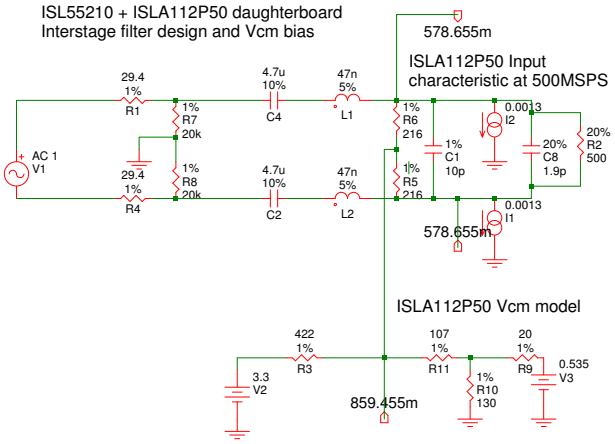

FIGURE 10. SIMULATION MODEL FOR THE INTERSTAGE FILTER AND VCM SETUP

The numbering does not follow Figure 9, but this is the same circuit with the ADC input and Vcm terms added. The amplifier output shows up as AC1 and the R7 and R8 elements are simulation artifacts to get DC operation points set. Aside from simply implementing a 2nd order differential RLC filter, this circuit also provides the bias voltage for the ADC input Vcm pins. The ISLA112P50 has a clock rate dependent common input current (shown in Figure 10 as two 1.3mA current sources). The network on the lower part of Figure 10 generates a DC bias voltage as a Thevenin equivalent from the converter's Vcm output pin (modeled above as a 0.535V and 20Ω internal element) and the +3.3V supply. This voltage ends up being greater than the required voltage at the ADC inputs and it is pulled down through the two 216Ω resistors that are part of the filter design to be in range for the ADC. It is important to recognize that the filter design must be including the differential input impedance of the ADC – shown in Figure 10 as 500Ω in parallel with 1.9pF.

Running the simulation with the DC probes included, shows this circuit provides a Vcm at the ADC of approximately 0.578V for this 500MSPS Icm. Remember the actual amplifier outputs are sitting at approx. 1.2Vcm and that is being level shifted to this ADC voltage through the two 4.7µF blocking caps. Figure 11 shows the simulated response for this design.

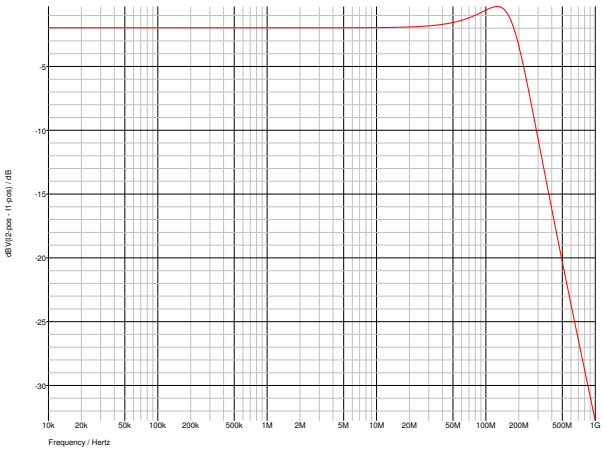

FIGURE 11. SIMULATED DIFFERENTIAL FILTER RESPONSE

The key information in this response is the midband insertion loss of only 2dB and the moderate peaking in the nominal response. It is very desirable to limit the insertion loss as this will reduce the maximum amplifier output V_{P-P} to reach -1dBFS at the ADC. For instance, here we need $1.3V_{P-P}$ at the ADC to be delivering a -1dBFS signal, which moves back through this filter to be a $(10^{(2/20)})*1.3V = 1.63V_{P-P}$ at the amplifier outputs. This simulated response is peaking approximately 1.5dB but in the actual board, there are parasitic C's in the interstage path that rolls this off to be perfectly flat.

Measurement Port Option

The Vcm bias setup resistors in the simulation circuit (216Ω) are actually implemented on the board as a passive sense path for the signal response right up to the ADC input pins. Going back to Figure 9 on page 5, those resistors are split into 4 elements that show the correct differential impedance for the filter, but divide down the differential signal at the ADC inputs while presenting two 25Ω source impedance elements into a very broadband 1:1 transformer (ADT1-1WT), where it is converted back to single-ended and delivered to a measurement port on the board. Using this technique, a direct network analyzer measurement of the response to the ADC inputs can be made. End equipment implementations would not use this feature and the sense path transformer can be eliminated from the design. However, this provides a relatively quick and easy way to measure the frequency response to the ADC inputs. Figure 12 shows a typical small signal measurement with the ADC clocking at 500MSPS, while Figure 13 shows the same thing running the ADC at 200MSPS. Note that the board as shipped does not have the measurement path populated; to install it add 0.1µF input capacitors C1017, C1018, the transformer and the transformer output DC blocking capacitor C1019, as shown in the schematic at Figure 39.

Nearly identical results occur at the minimum clock rate of 200MSPS.

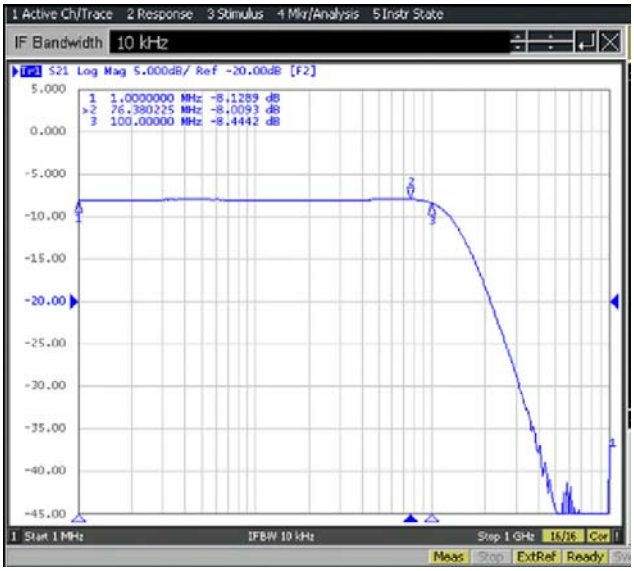

FIGURE 12. AMPLIFIER FREQUENCY RESPONSE AT 500MSPS

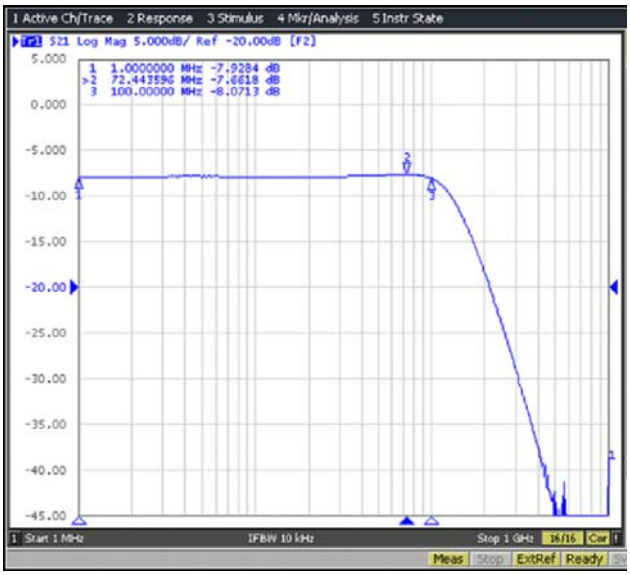

FIGURE 13. AMPLIFIER FREQUENCY RESPONSE AT 200MSPS

The markers show very small deviation from 1MHz gain through this 100MHz span. These measured responses are from the board input SMA to the sense port output SMA.

While not shown in Figures 12 & 13, the response going down to 100kHz remains flat to within 0.5dB to the 1MHz gain. The total insertion loss in the 4 resistor network, including two 50Ω impedance reflected through from the output pin load, is approximately 23.5dB for the resistor divider and then another 0.5dB insertion loss for the ADT1-1WT transformer. Adding this 24dB insertion loss to the -8.0dB 1MHz number measured above, gives a nominal gain from the input of the board to the ADC inputs of 16.0dB. Going from the input SMA to the ADC inputs, we should be seeing:

1. +6dB for the input ADT4-6T
2. -0.3dB midband insertion loss for the ADT4-6T
3. -0.25dB Insertion Loss for the ADT1-4-75
4. +12.3dB amplifier gain from the transformer outputs to the amplifier outputs
5. -2dB interstage filter insertion loss, which comes to 15.75dB nominal gain – very close to the measured 16.0dB result.

Figures 14 and 15 show typical AC performance for the ADC alone as a function of analog input frequency. These figures are from the ISLA112P50 datasheet.

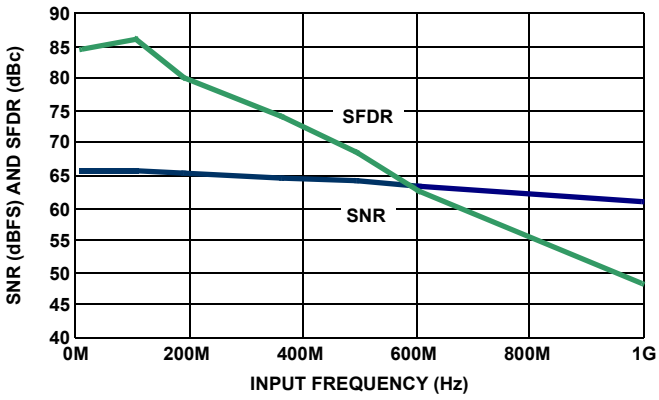

FIGURE 14. SNR and SFDR vs ANALOG INPUT FREQUENCY AT 500MSPS (ADC ONLY)

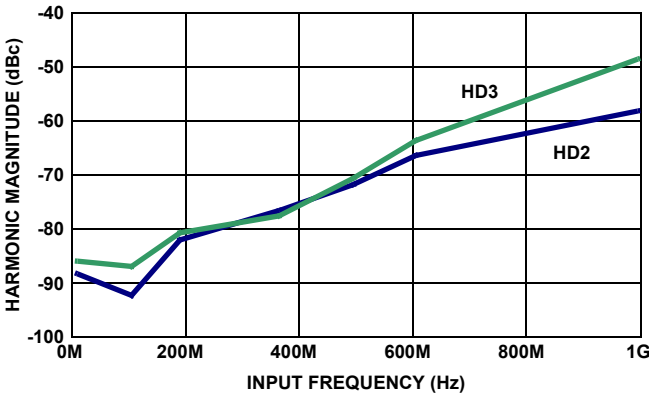

FIGURE 15. H2 and H3 vs ANALOG INPUT FREQUENCY AT 500MSPS (ADC ONLY)

The SNR curves are always referenced to full scale. Thus, if an SNR is developed at -1dBFS, the resulting number is increased by 1dB to project the SNR if the exact full scale input swing was being delivered.

Generally, up through 100MHz, the ISLA112P50 typical data shows:

1. SNR of about 65.5dBFS
2. HD2 of about -90dBc
3. HD3 of about -86dBc

These are remarkable numbers for an ADC consuming < 500mW at this maximum 500MSPS clock rate.

Amplifier/ADC PCB AC Performance

The frequency response achieved here has exceptional flatness over this 100kHz to 100MHz range and then rolls off with a bit more than a 2nd order rolloff above that. This filtering is very important to:

1. Control the integrated noise power bandwidth for the noise out of the amplifier stage.
2. Help attenuate the HD terms present at the amplifier outputs. For instance, the filter shows about 10dB attenuation at 200MHz. This will be knocking down the amplifier HD2 by 10dB for a 100MHz input signal while the HD3 will be getting >10dB attenuation for frequencies above 67MHz.

The board supports a 3rd order filter design as well with the C16 element shown in Figure 9. The measurement port path provides an easy way to build and test alternate interstage filter designs. Contact the factory for assistance in redesigning this filter.

It is of course also possible to use the ADC to measure the frequency response through the FFT. A splitter is used at the input to measure the change in input signal power required over frequency to hold the output FFT amplitude for the single tone input constant over frequency.

Tested SNR and SFDR at 500MSPS

The goal for this analog signal path before the ADC is to greatly reduce the required input signal level while suffering minimal degradation from lab tested ADC performance and provide a very broadband solution from 100kHz to 100MHz inputs. The ISLA112P50 shows an SNR over frequency (and these are always -1dBFS single tone test curves) in Figure 14 and HD2 and HD3 curves in Figure 15. These are normally taken with a 2 transformer input circuit using the ADTL1-12. Thus, the signal source is driving a very high amplitude single-ended test signal but is heavily filtered by narrow bandpass filters for each data point in Figure 15. The performance numbers shown are implicitly very narrowband due to the bandpass filter used in ADC characterization.

Figures 16 through 18 show tested SNRFS, HD2 and HD3 for 3 example amplifier + ADC daughterboards tested at 500MSPS.

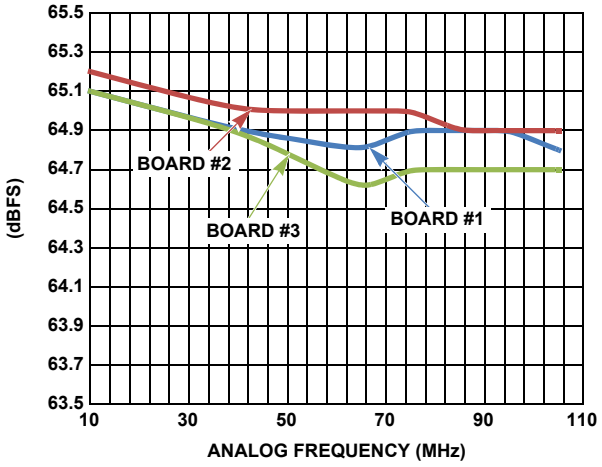

FIGURE 16. TESTED SNRFS FOR 3 BOARDS AT -10dBm BOARD EDGE SINGLE TONE POWER

Very little degradation in ADC SNR is observed here. This is the combined result of very low output spot noise from this low input noise (0.85nV/√Hz) wideband FDA and good noise power bandwidth control in the interstage filter.

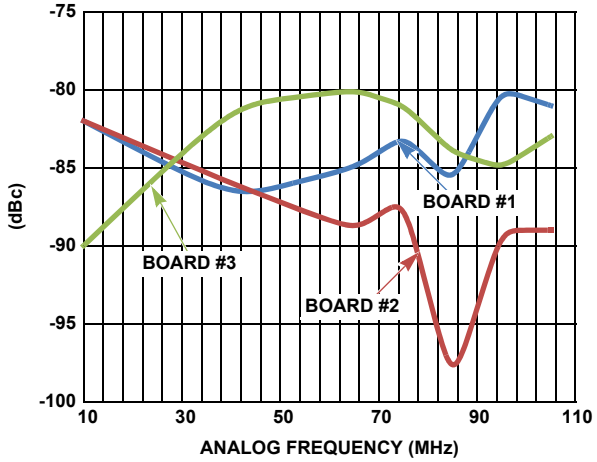

FIGURE 17. TESTED HD2 FOR 3 BOARDS AT -10dBm BOARD EDGE SINGLE TONE POWER

Quite a bit of variability in the measured HD2 is seen in Fig. 17 and should be expected due to the cancellation nature of HD2. However in any case, all 3 boards over 10MHz to 100MHz hold lower than the -80dBc combined performance. This is exceptional performance for a 115mW signal path solution.

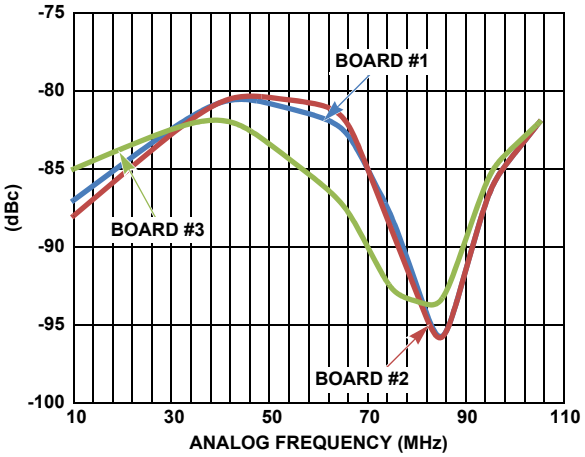

FIGURE 18. TESTED HD3 FOR 3 BOARDS AT -10dBm BOARD EDGE SINGLE TONE POWER

Figure 18 shows that the boards are much closer in HD3 performance and we can detect a clear pattern in the response shape. As the frequency moves above 60MHz, the filter rolloff above 180MHz is really starting to attenuate the HD3 at the ADC inputs. Above 85MHz, the HD3 out of the amplifier appears to be coming up faster than the filter is rolling it off. In any case, all 3 boards hold about -80dBc worst case over this 10MHz to 100MHz span.

Thus, the amplifier interface has degraded the SNRFS by about 0.5dB and the HD2 a varying amount but no more than 9dB, while the HD3 has been degraded by no more than 6dB.

Tested Performance at Lower ADC Clock Rates

As the clock rate is reduced on the ADC, many fine scale changes in performance will be observed. The very simple interface of Figure 9 on page 5 develops the Vcm voltage for the ADC as a fixed Thevenin source that is then adjusted down by the common mode input current of the ADC. Measured results on this board show a 2.8µA/MSPS common mode current into each input of the ISLA112P50 ADC. As the clock rate decreases, the resulting Vcm voltage at the ADC inputs will be shifting up. This also has a lot of fine scale interaction with the ADC performance. Figure 19 shows a typical ADC Vcm vs Clock rate curve for the design shown here.

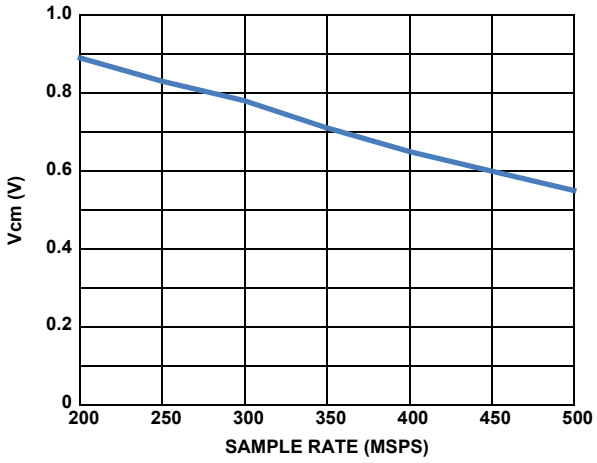

FIGURE 19. ADC Vcm vs CLOCK RATE

The goal here was to keep the interface as simple as possible while holding performance. A more sophisticated approach would be to include a Vcm servo loop to target a fixed ADC Vcm vs clock rate. It is, however, this increase in Vcm that limits the lower end of operation to 200MSPS before the ADC common mode voltage goes out of range for this particular set of values. However, 200MSPS also matches up with this 100MHz maximum application bandwidth for a 1st Nyquist zone implementation.

Figures 20 through 37 give the typical SNRFS, HD2 and HD3 as the clock is stepped down in 50MHz steps for 3 different boards. And remember, all of these require a very low phase noise (or jitter) clock to get these results.

These plots are mainly showing the variation coming from the ADC performance as the clock rate and input Vcm voltage is changing. The signal path up to the ADC inputs is not changing at all as the clockrate is being swept. These seem to show the SNR degrading more at low clock rates while the HD performance actually improves significantly.

450MSPS

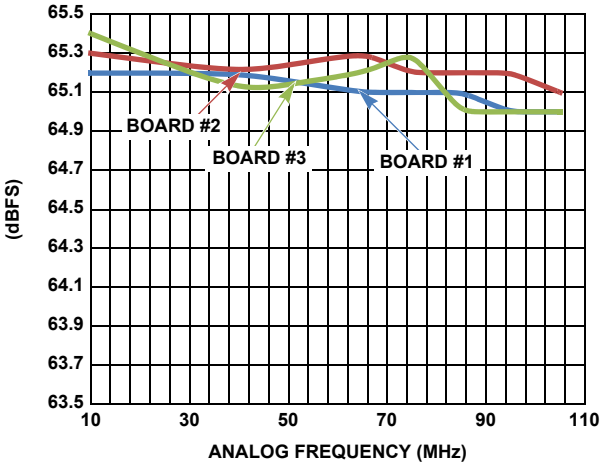

FIGURE 20. SNR at 450MSPS

400MSPS

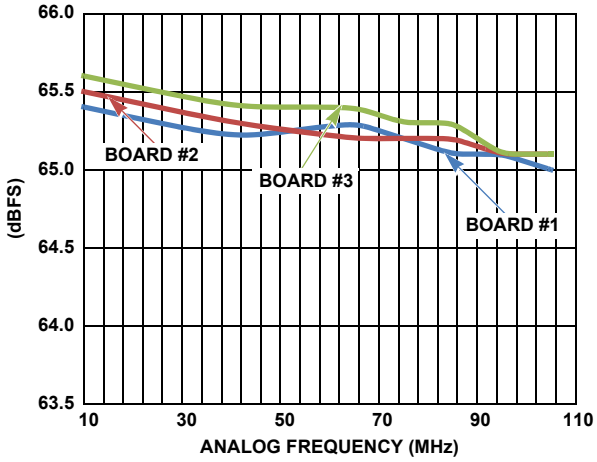

FIGURE 21. SNR at 400MSPS

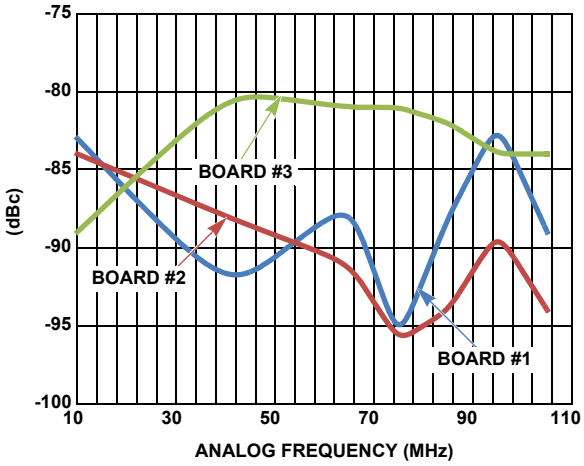

FIGURE 22. HD2 at 450MSPS

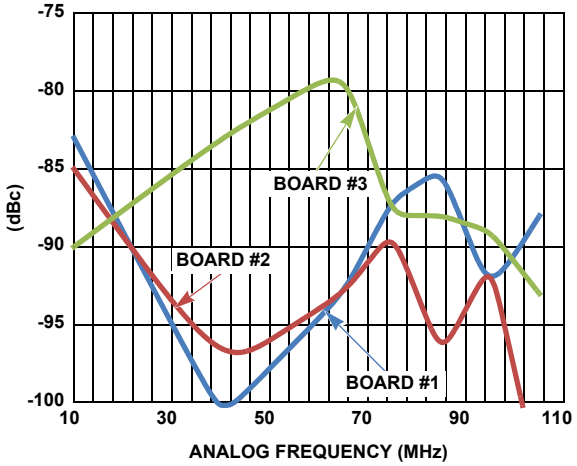

FIGURE 23. HD2 at 400MSPS

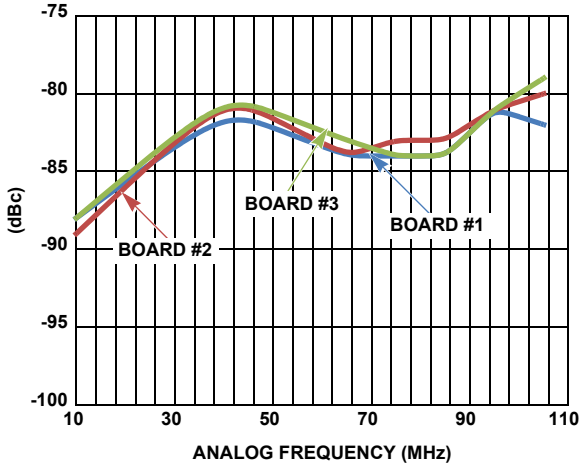

FIGURE 24. HD3 at 450MSPS)

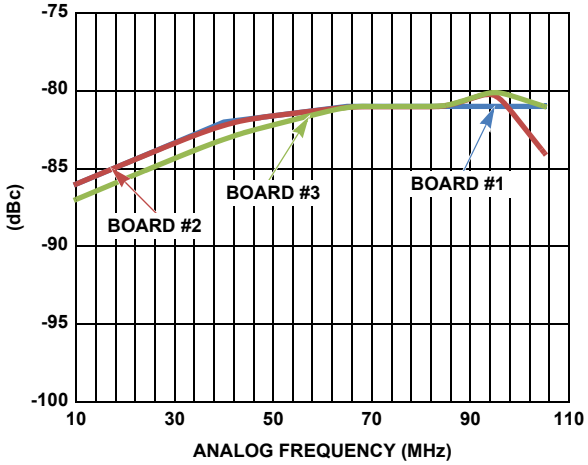

FIGURE 25. HD3 at 400MSPS

350MSPS

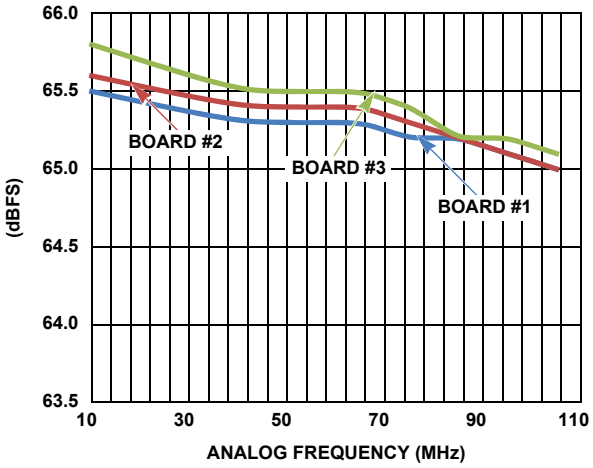

FIGURE 26. SNR at 350

300MSPS

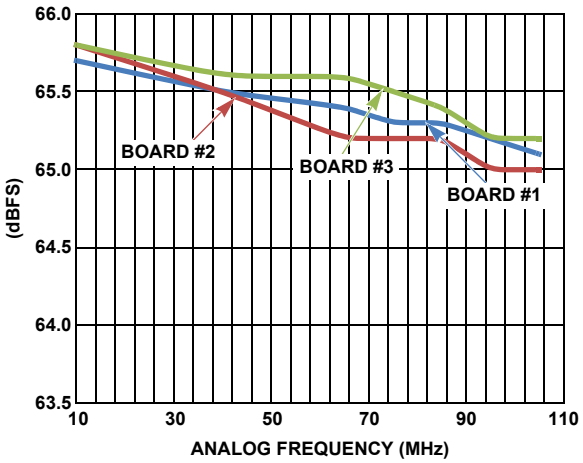

FIGURE 27. SNR at 300MSPS

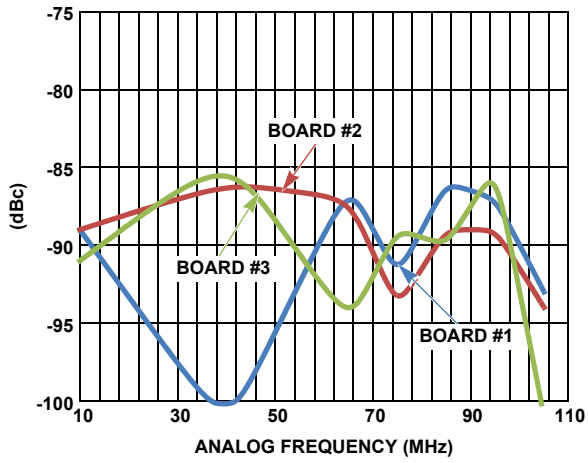

FIGURE 28. HD2 at 350MSPS

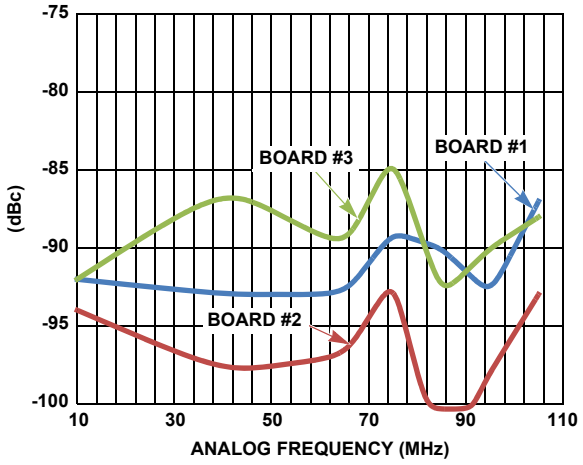

FIGURE 29. HD2 at 300MSPS

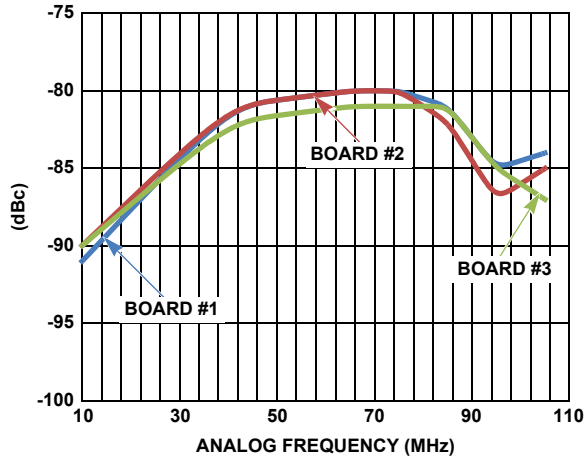

FIGURE 30. HD3 at 350MSPS

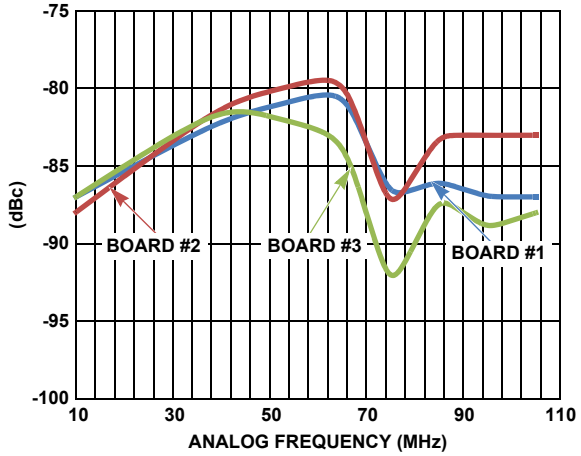

FIGURE 31. HD3 at 300MSPS

250MSPS

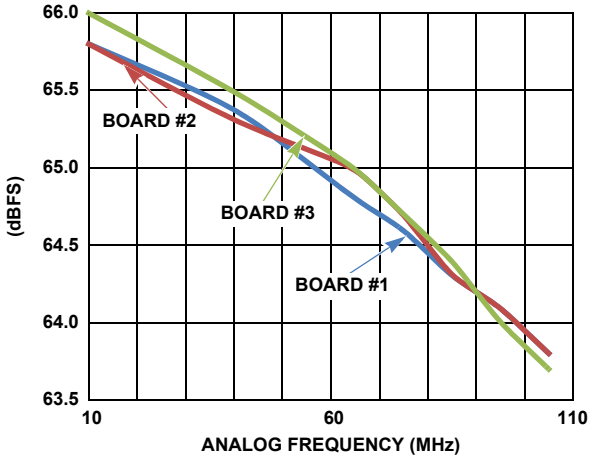

FIGURE 32. SNR at 250MSPS

200MSPS

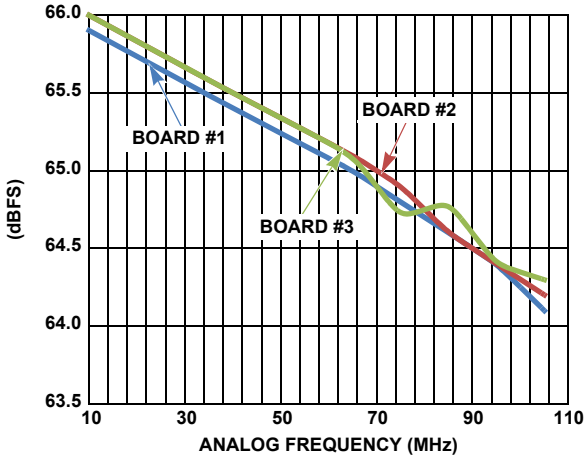

FIGURE 33. SNR at 200MSPS)

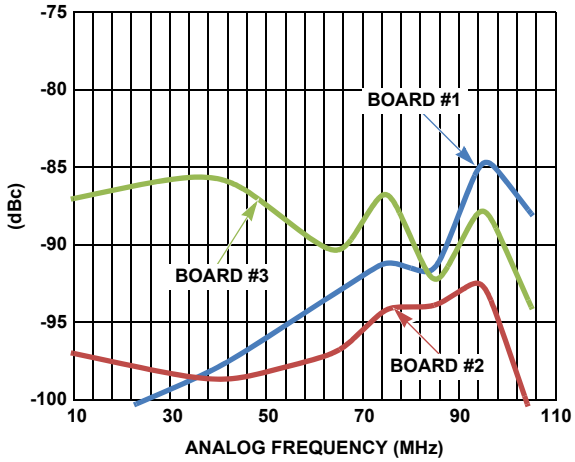

FIGURE 34. HD2 at 250MSPS

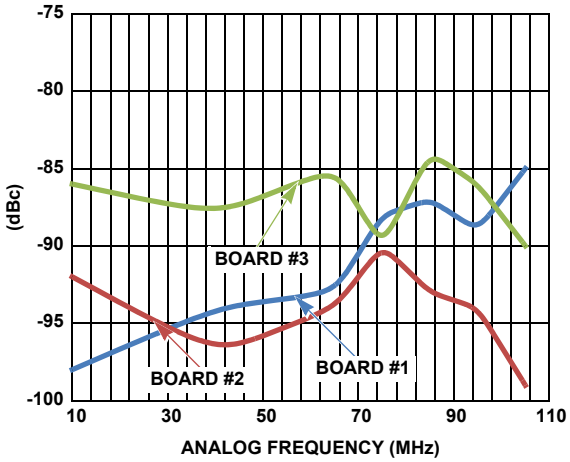

FIGURE 35. HD2 at 200MSPS

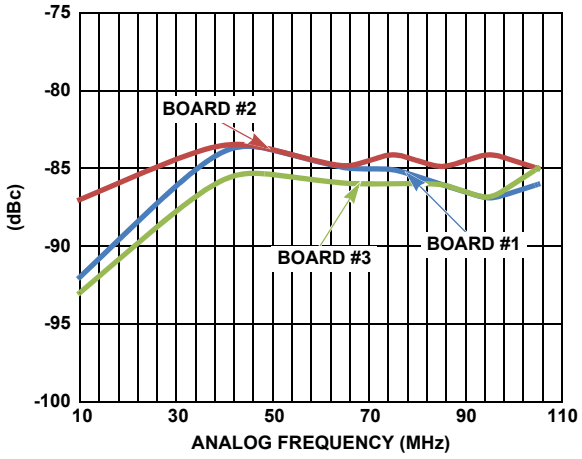

FIGURE 36. HD3 at 250MSPS

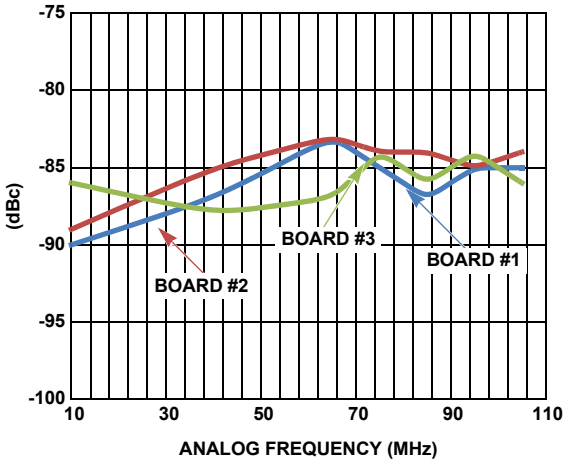

FIGURE 37. HD3 at 200MSPS

Conclusions

This combination amplifier + DAQ/ADC board is essentially delivering a much lower full scale input solution with minimal degradation from ADC only performance. A rough set of specifications might be in the following:

1. 200mV$_{P-P}$ full scale input
2. 100kHz to 100MHz flat response
3. 200MSPS to 500MSPS clock rate
4. <600mW combined power dissipation
5. 65dB SNRFS
6. -80dBc worst case HD2, -80dBc worst case HD3

Considerable flexibility exists on the board to modify the input transformer selections, amplifier gain and interstage filter design to target different frequency ranges for digitization. The ADC itself can also be swapped out for numerous pin-compatible alternatives. These include 8-, 10-, and 12-bit pin-compatible parts in the ISLA1XXP50 family as well as 10-, 12-, and 14-bit pin compatible parts in the KAD55XX family, See Table 1 for a list of ADCs that this PCB supports.

TABLE 1. PCB SUPPORTED ADCs

PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE(Msps)
ISLA112P50	12	500
KAD5512P-50	12	500
ISLA110P50	10	500
KAD5510P-50	10	500
ISLA118P50	8	500
KAD5514P	14	125/170/210/250 grades
KAD5512P	12	125/170/210/250 grades
KAD5512HP	12	125/170/210/250 grades
KAD5510P	10	125/170/210/250 grades

Swapping out the ISLA112P50 for these other options may require a re-design of the interstage filter and Vcm setup circuit values.

In addition, the board will need to be re-programmed to allow for operation with the Konverter ADC software, contact the factory if you need assistance.

In summary, this board offers a good breadboarding platform to get performance measures over a large range of designs before committing to end equipment layout.

Appendix A: RF Generators

Intersil uses the following RF generators as clock and signal sources when characterizing high-speed ADCs:

- Rohde & Schwarz: SMA100A
- Agilent: 8644B (with Low-Noise option)

These generators provide very low jitter to optimize the SNR performance of the ADC under test. Other generators with similar phase noise performance can also be used. Contact Intersil Technical Support for recommendations.

Bill of Materials

DESIGNATOR	COMMENT	DESCRIPTION	SIZE	NUMBER	MANUFACTURER	MAN. PART NUMBER
C1, C6, C7, C31	33µF	Capacitor (Polarized)	C-SIZE	4	Kemet	T491C336K016AT
C2, C3, C1005	0.1µF	Capacitor	0603	3	Murata	GRM188R71E104KA01D
C1007	4.7µF	Capacitor	603	1	TDK	C1608X5R1A475K/0.80
C4, C5, C12, C13, C14, C15, C20, C22, C24, C25, C26, C27, C33, C34, C42, C43, C44, C45, C48, C50, C52, C1014	0.1µF	Capacitor	0402	22	TDK	C1005X7R1C104K
C28, C29, C49, C51	1000pF	Capacitor	0402	4	Panasonic	ECJ-0EB1H102K
C30	10000pF	Capacitor	0402	1	TDK	C1005X7R1C103K
C32	1000pF	Capacitor	0603	1	AVX	06035C102KAT2A
C1010,C1012	4.7µF	Capacitor	402	2	TDK	C1005X5R0J475K
C53	220pF	Capacitor	0603	1	TDK	C1608C0G1H221J
C1001	4.7µF	Capacitor (Polarized)	3528	1	Kemet	T491B475K010AT
C1002	1.0µF	Capacitor	1206	1	TDK	C3216X7R1C105K/1.15
C1004, C1009	0.047µF	Capacitor	0603_X2Y	2	Johanson Dielectrics Inc	160X14W473MV4T
Cdiff	10pF	Capacitor	0603_X2Y	1	Johanson Dielectrics Inc	500X14N100MV4T

Bill of Materials (Continued)

DESIGNATOR	COMMENT	DESCRIPTION	SIZE	NUMBER	MANUFACTURER	MAN. PART NUMBER
INPUT	SMA END LAUNCH	Edge Launch SMA		1	Emerson	142-0701-851
J1	2MM HDR 14P SMT	JTAG		1	Molex	87832-1420
J4	SMA	SMA		2	Amphenol	901-144-8RFX
J6		connector		1	Molex	53475-1879
L3, L4, L13, L14, L15, L16, L17, L18	Bead		0805	8	TDK	MMZ2012R102A
L1001	BEAD		1206	1	Laird signal	HZ1206E601R-10
L1002, L1003	47nH	Inductor	0603	2	Coilcraft	0603CS-47NXGLU
R1016, R1017	28.7Ω	Resistor	0402	2	Panasonic	ERJ-2RKF28R7X
R1, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R30, R35, R36, R38, R40, R41, R42	1k	Resistor	0402	19	Vishay	CRCW04021K00FKED
R2, R29, R31, R37, R39	4.7k	Resistor	0603	5	Yageo	RC0603FR-074K7L
R14, R28	1k	Resistor	0603	2	Yageo	RC0603FR-071KL
R27,	200	Resistor	0402	1	Panasonic	ERJ-2RKF2000X
R1008, R1011	412Ω	Resistor	0402	2	Panasonic	ERJ-2RKF4120X
R32, R33, R1000	0Ω	Resistor	0603	7	Stackpole	RMCF0603ZT0R00
R1013, R1014	29.4Ω	Resistor	0402	2	Panasonic	ERJ-2RKF29R4X
R1019	392Ω	Resistor	0402	1	Panasonic	ERJ-2RKF3920X
R48, R1006, R1007, R1021	100Ω	Resistor	0402	4	Yageo	RC0402FR-07100RL
R1020	118Ω	Resistor	0402	1	Panasonic	ERJ-2RKF1180X
R34	10k	Resistor	0603	1	Yageo	RC0603FR-0710KL
R46	10k	Resistor	0402	1	Stackpole	RMCF0402FT10K0
R49, R50, R51, R52, R53, R54, R55, R56	49.9	Resistor	0402	8	Panasonic	ERJ-2RKF49R9X
R18, R1009, R1010	0Ω	Resistor	0402	3	Panasonic	ERJ-2GE0R00X
R1015, R1018	187Ω	Resistor	0402	2	Panasonic	ERJ-2RKF1870X
Rterm3	50	Resistor	0603	1	Panasonic	ERJ-3EKF49R9V
T1	ADT4-6T	Transformer	CD542	1	Minicircuits	ADT4-6T
T2	ADTL1-4-75+	1:1 Transmission Line Transformer	CD542	1	Minicircuits	ADTL1-4-75+
T3	TC4-1W	Center-Tapped Transformer	AT224	1	Minicircuits	TC4-1W+
U7	74AHC1G04	Inverter	SOT23-5	1	TI	SN74AHC1G04DBVR
U2, U3	24FC128-I/SN	EEPROM	SO8	2	Microchip Tech	24FC128-I/SN
U4	XC2C64A-6VQG44C	CPLD	VQFP44	1	Xilinx	XC2C64A-5VQG44C
U6	ISL55210	Hi Speed Ultra Low Distortion Differential Amplifier	TQFN16	1	Intersil	ISL55210IRTZ
U1	ISLA112P50	500MSPS, 12-bit ADC	QFN 10X10 72	1	Intersil	ISLA112P50IRZ

ISLA112P50/55210EV1Z Schematics

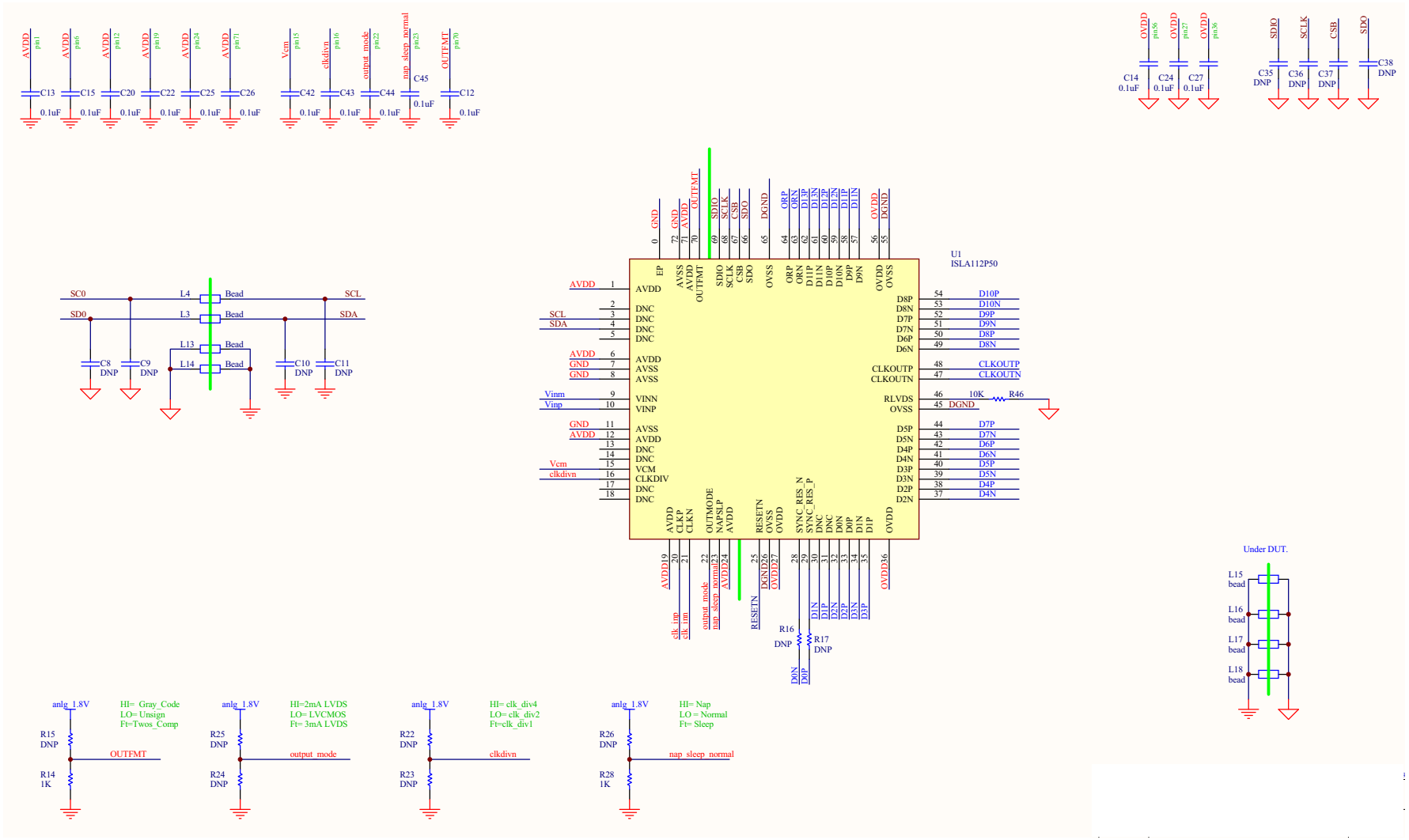

FIGURE 38. ISLA112P50/55210EV1Z (1 OF 3)

ISLA112P50/55210EV1Z Schematics (Continued)

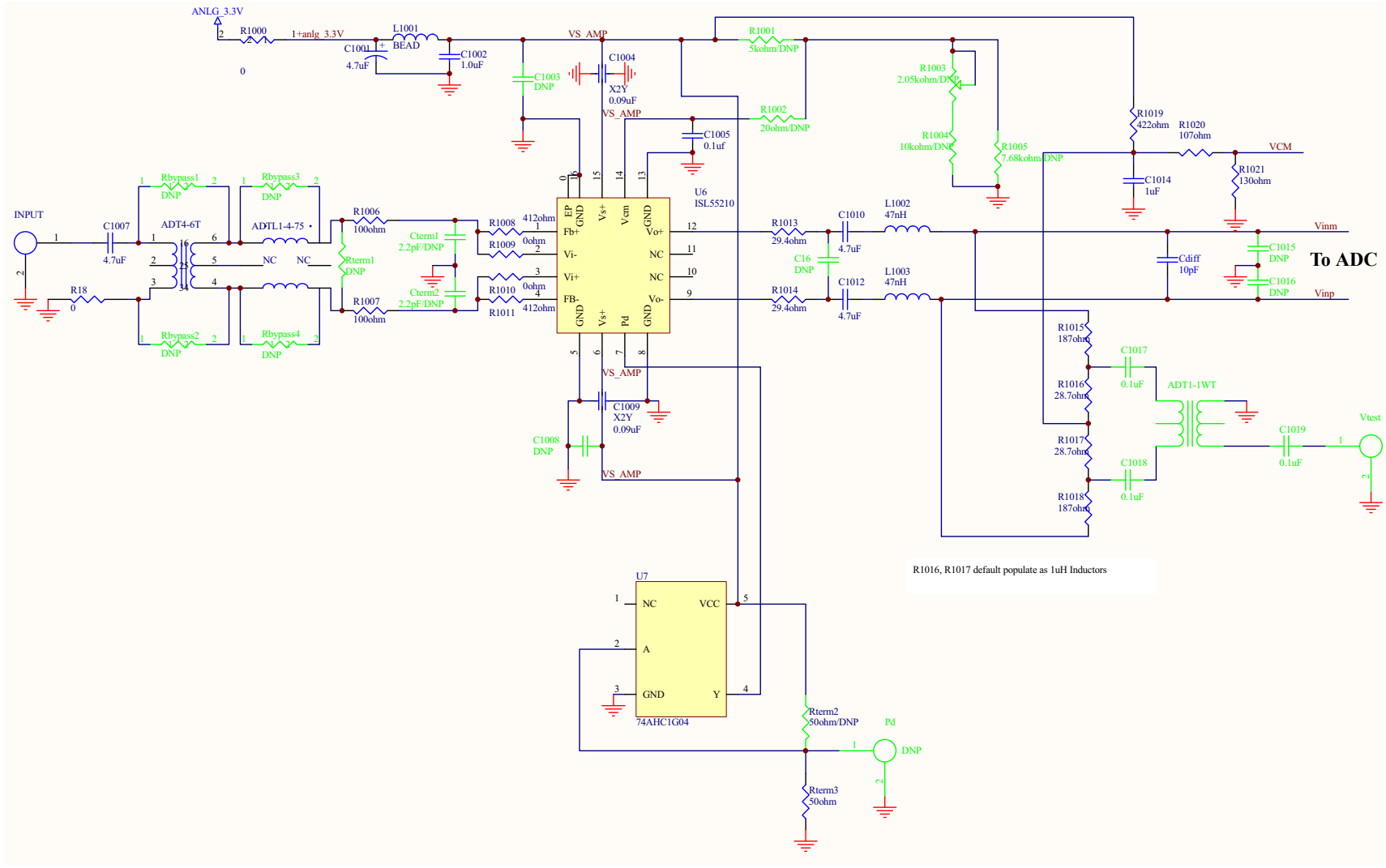

FIGURE 39. ISLA112P50/55210EV1Z (2 OF 3)

ISLA112P50/55210EV1Z Schematics (Continued)

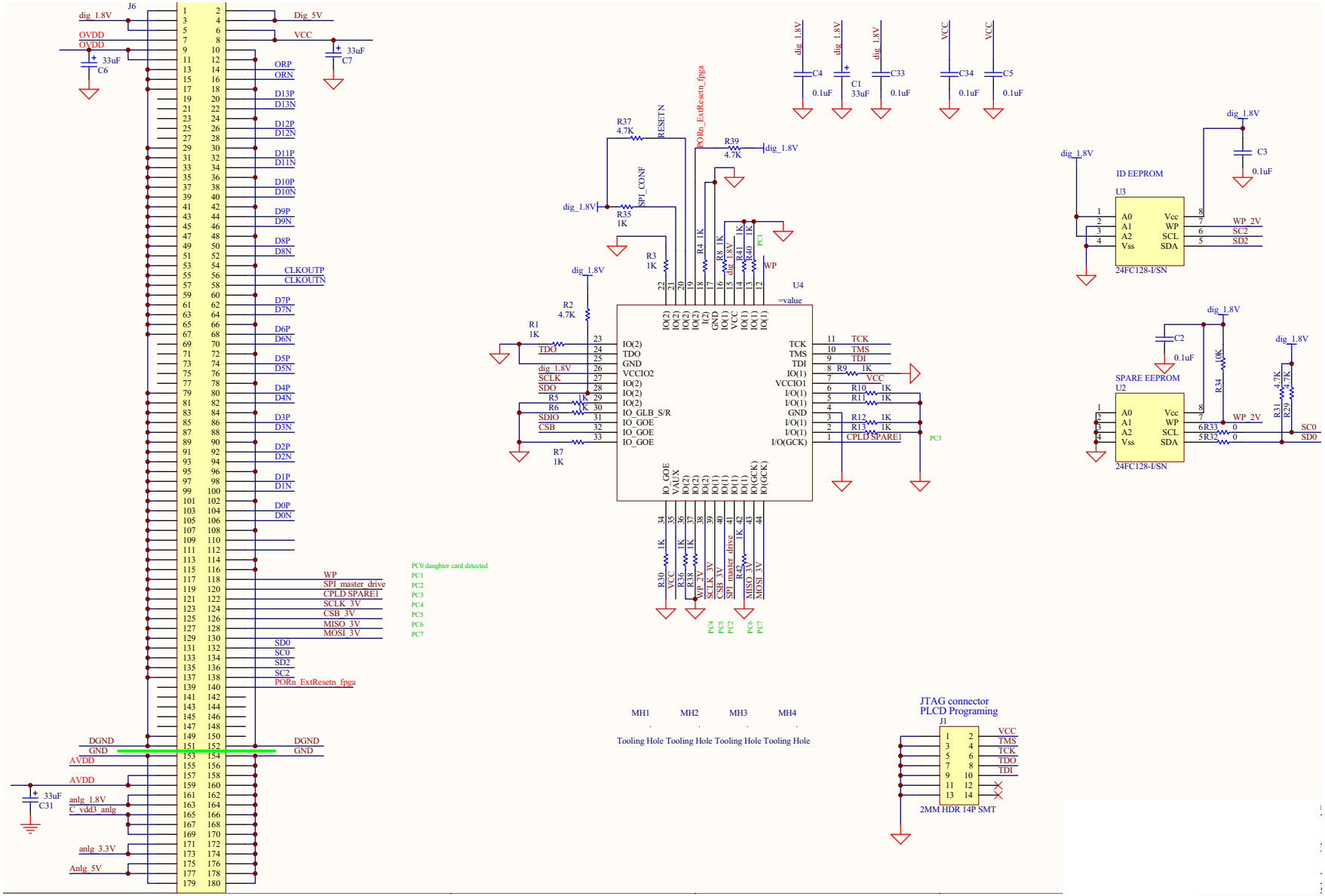

FIGURE 40. ISLA112P50/55210EV1Z (3 OF 3)

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0