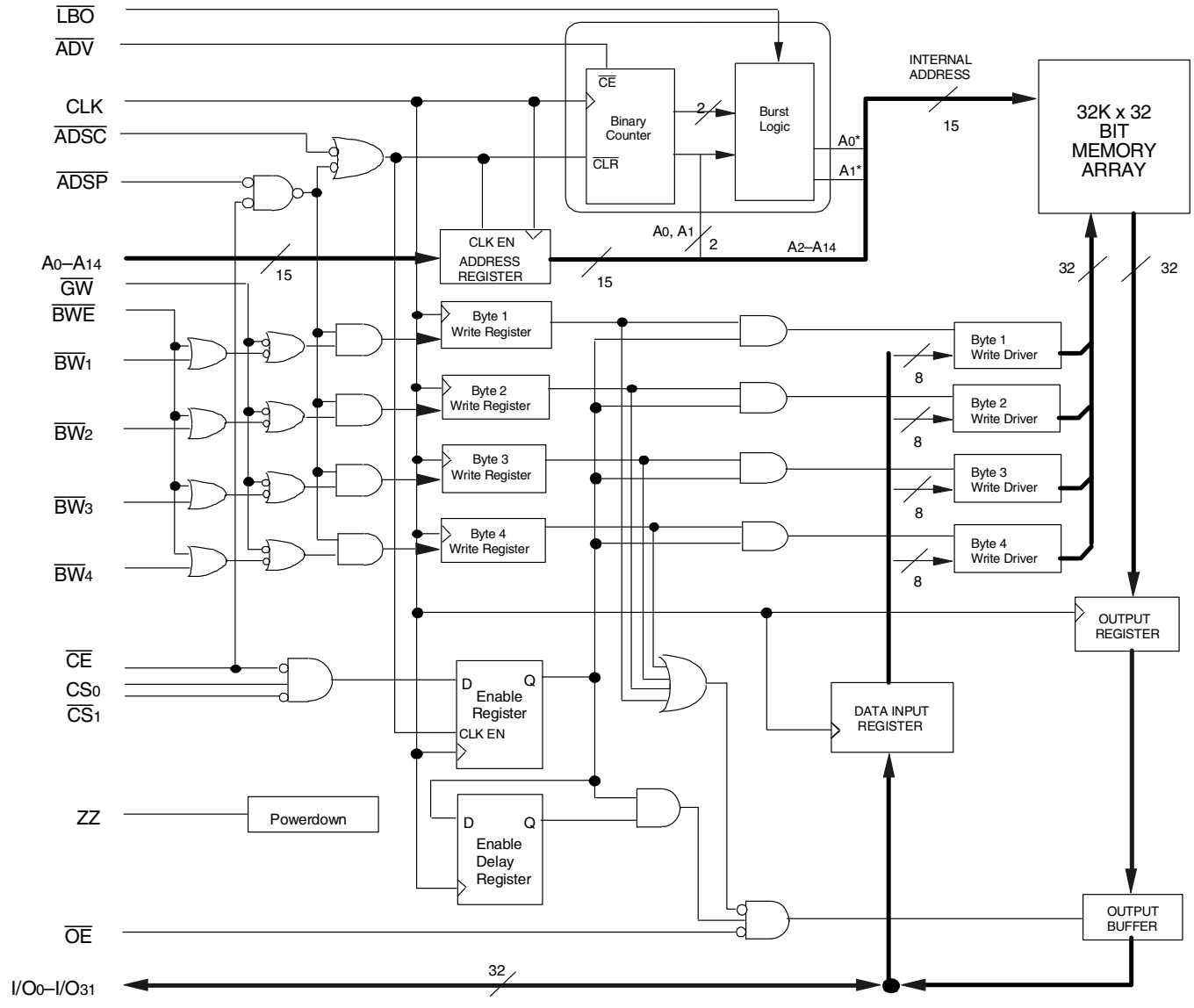
32K x 32 CacheRAM™ 3.3V Synchronous SRAM Burst Counter Single Cycle Deselect

IDT71V432

Features

- **32K x 32 memory configuration**
- **Supports high-performance system speed:**
  Commercial and Industrial:
  - *5ns Clock-to-Data Access (100MHz)*
  - *6ns Clock-to-Data Access (83MHz)*
- **Single-cycle deselect functionality (Compatible with Micron Part # MT58LC32K32D7LG-XX)**
- **$\overline{LBO}$ input selects interleaved or linear burst mode**
- **Self-timed write cycle with global write control ($\overline{GW}$), byte write enable ($\overline{BWE}$), and byte writes ($\overline{BW}$x)**
- **Power down controlled by ZZ input**
- **Operates with a single 3.3V power supply (+10/-5%)**
- **Packaged in a JEDEC Standard 100-pin rectangular plastic thin quad flatpack (TQFP)**
- **Green parts available, see ordering information**

Functional Block Diagram



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OCTOBER 2014

Description

The IDT71V432 is a 3.3V high-speed 1,048,576-bit CacheRAM organized as 32K x 32 with full support of the Pentium™ and PowerPC™ processor interfaces. The pipelined burst architecture provides cost-effective 3-1-1-1 secondary cache performance for processors up to 100 MHz.

The IDT71V432 CacheRAM contains write, data, address, and control registers. Internal logic allows the CacheRAM to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V432 can provide four cycles of data for a single address presented to the CacheRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses will be defined by the internal burst counter and the $\overline{LBO}$ input pin.

The IDT71V432 CacheRAM utilizes high-performance, high-volume 3.3V CMOS process, and is packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) for optimum board density in both desktop and notebook applications.

Pin Description Summary

A_0–A_{14}	Address Inputs	Input	Synchronous
$\overline{CE}$	Chip Enable	Input	Synchronous
CS_0, $\overline{CS_1}$	Chips Selects	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$\overline{GW}$	Global Write Enable	Input	Synchronous
$\overline{BWE}$	Byte Write Enable	Input	Synchronous
$\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADV}$	Burst Address Advance	Input	Synchronous
$\overline{ADSC}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{ADSP}$	Address Status (Processor)	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O_0–I/O_{31}	Data Input/Output	I/O	Synchronous
V_{DD}	3.3V Power	Power	DC
V_{SS}	Ground	Ground	DC

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Pentium processor is a trademark of Intel Corp.
PowerPC is a trademark of International Business Machines, Inc.

Pin Definitions(1)

Symbol	Pin Function	I/O	Active	Description
A_0–A_{14}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{ADSC}$ Low or $\overline{ADSP}$ Low and $\overline{CE}$ Low.
$\overline{ADSC}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{ADSC}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSC}$ is NOT GATED by $\overline{CE}$.
$\overline{ADSP}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{ADSP}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSP}$ is gated by $\overline{CE}$.
$\overline{ADV}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{ADV}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When this input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{BWE}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{BW_1}$–$\overline{BW_4}$. If $\overline{BWE}$ is LOW at the rising edge of CLK then $\overline{BW_X}$ inputs are passed to the next stage in the circuit. A byte write can still be blocked if $\overline{ADSP}$ is LOW at the rising edge of CLK. If $\overline{ADSP}$ is HIGH and $\overline{BW_X}$ is LOW at the rising edge of CLK then data will be written to the SRAM. If $\overline{BWE}$ is HIGH then the byte write inputs are blocked and only $\overline{GW}$ can initiate a write cycle.
$\overline{BW_1}$ - $\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. $\overline{BW_1}$ controls I/O(7:0), $\overline{BW_2}$ controls I/O(15:8), etc. Any active byte write causes all outputs to be disabled. $\overline{ADSP}$ LOW disables all byte writes. $\overline{BW_1}$–$\overline{BW_4}$ must meet specified setup and hold times with respect to CLK.
$\overline{CE}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{CE}$ is used with CS_0 and $\overline{CS_1}$ to enable the IDT71V432. $\overline{CE}$ also gates $\overline{ADSP}$.
CLK	Clock	I	N/A	This is the clock input to the IDT71V432. All timing references for the device are made with respect to this input.
CS_0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS_0 is used with $\overline{CE}$ and $\overline{CS_1}$ to enable the chip.
$\overline{CS_1}$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{CS_1}$ is used with $\overline{CE}$ and CS_0 to enable the chip.
$\overline{GW}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 8-bit data bytes when LOW on the rising edge of CLK. $\overline{GW}$ supercedes individual byte write enables.
I/O_0–I/O_{31}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{LBO}$	Linear Burst Order	I	LOW	Asynchronous burst order selection DC input. When $\overline{LBO}$ is HIGH the Interleaved (Intel) burst sequence is selected. When $\overline{LBO}$ is LOW the Linear (PowerPC) burst sequence is selected. $\overline{LBO}$ is a static DC input and must not change state while the device is operating.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{OE}$ is LOW the data output drivers are enabled on the I/O pins. $\overline{OE}$ is gated internally by a delay circuit driven by $\overline{CE}$, CS_0, and $\overline{CS_1}$. In dual-bank mode, when the user is utilizing two banks of IDT71V432 and toggling back and forth between them using $\overline{CE}$, the internal delay circuit delays the $\overline{OE}$ activation of the data output drivers by one cycle to prevent bus contention between the banks. When used in single bank mode $\overline{CE}$, CS_0, and $\overline{CS_1}$ are all tied active and there is no output enable delay. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedence state.
V_{DD}	Power Supply	N/A	N/A	3.3V power supply inputs.
V_{SS}	Ground	N/A	N/A	Ground pins.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V432 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.

3104 tbl 02

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Absolute Maximum Ratings(1)

Symbol	Rating	Value	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{DD}+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

3104 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} and Input terminals only.
3. I/O terminals.

Capacitance

(T_A = +25°C, f = 1.0MHz, TQFP package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

3104 tbl 06

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	V_{SS}	V_{DD}
Commercial	0°C to +70°C	0V	3.3V+10/-5%
Industrial	–40°C to +85°C	0V	3.3V+10/-5%

3104 tbl 03

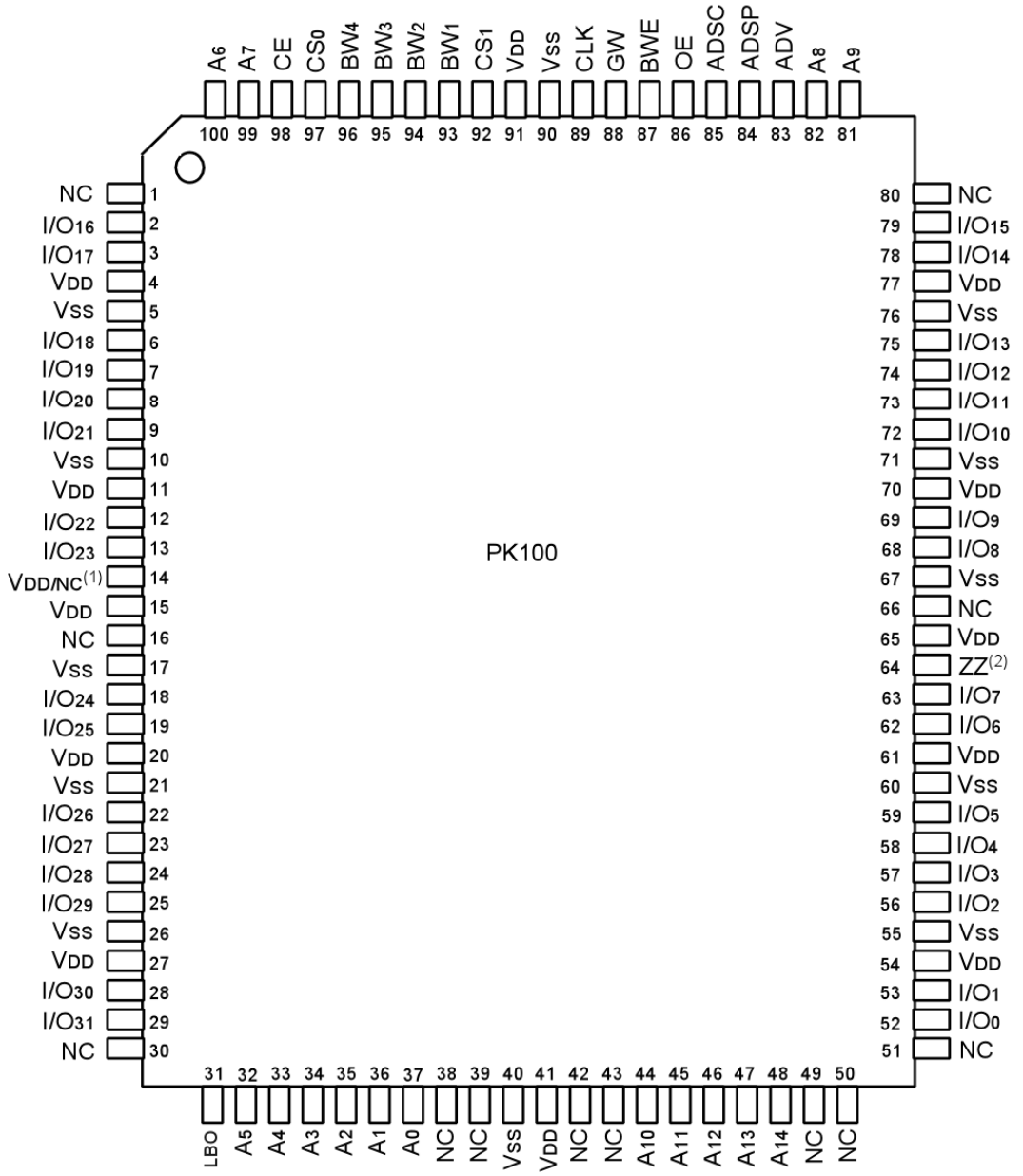
Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.3	3.63	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage — Inputs	2.0	—	4.6(2)	V
V_{IH}	Input High Voltage — I/O	2.0	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

3104 tbl 04

NOTES:
1. V_{IL} (min) = –1.0V for pulse width less than t_{CYC}/2, once per cycle.
2. V_{IH} (max) = 6.0V for pulse width less than t_{CYC}/2, once per cycle.

Pin Configuration



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Top View TQFP

NOTES:
1. Pin 14 can either be directly connected to VDD or not connected.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

Synchronous Truth Table(1,2)

Operation	Address Used	$\overline{CE}$	CS_0	$\overline{CS_1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_X}$	$\overline{OE}$(3)	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	↑	Hi-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	↑	Hi-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	↑	D_{OUT}
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	↑	Hi-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	↑	D_{IN}
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	↑	D_{IN}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	↑	Hi-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	↑	Hi-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	↑	Hi-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	↑	D_{OUT}
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	↑	Hi-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	↑	D_{IN}
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	↑	D_{IN}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	↑	Hi-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	↑	Hi-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	Hi-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	↑	D_{OUT}
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	↑	Hi-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	↑	D_{IN}
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	↑	D_{IN}

3104 tbl 07

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{ZZ}$ = LOW for this table.
3. $\overline{OE}$ is an asynchronous input.

Synchronous Write Function Truth Table(1)

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1(2)	H	L	L	H	H	H
Write Byte 2(2)	H	L	H	L	H	H
Write Byte 3(2)	H	L	H	H	L	H
Write Byte 4(2)	H	L	H	H	H	L

3104 tbl 08

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.

Asynchronous Truth Table(1)

Operation(2)	$\overline{OE}$	ZZ	I/O Status	Power
Read	L	L	Data Out (I/O_0 - I/O_{31})	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z — Data In (I/O_0 - I/O_{31})	Active
Deselected	X	L	High-Z	Standby
Sleep	X	H	High-Z	Sleep

3104 tbl 09

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

Interleaved Burst Sequence Table ($\overline{LBO}$=V_{DD})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

3104 tbl 10

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

Linear Burst Sequence Table ($\overline{LBO}$=V_{SS})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

3104 tbl 11

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V +10/-5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	ZZ and $\overline{LBO}$ Input Leakage Current(1)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$, V_{OUT} = 0V to V_{DD}, V_{DD} = Max.	—	5	µA
V_{OL}	Output Low Voltage (I/O_1–I/O_{31})	I_{OL} = 5mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage (I/O_1–I/O_{31})	I_{OH} = –5mA, V_{DD} = Min.	2.4	—	V

3104 tbl 12

NOTE:
1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1) (V_{DD} = 3.3V +10/-5%, V_{HD} = V_{DD}–0.2V, V_{LD} = 0.2V)

Symbol	Parameter	Test Conditions	IDT71V432S5		IDT71V432S6		Unit
			Com'l.	Ind.	Com'l.	Ind.	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	200	200	180	180	mA
I_{SB}	Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	65	65	60	60	mA
I_{SB1}	Full Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2)	15	15	15	15	mA
I_{ZZ}	Full Sleep Mode Power Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max.	10	10	10	10	mA

3104 tbl 13a

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.

AC Test Loads

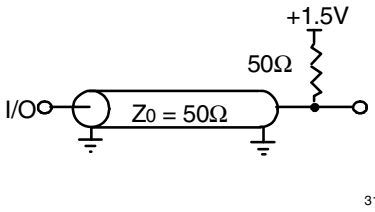

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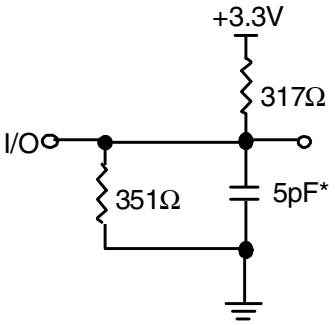
Figure 1. AC Test Load



* Including scope and jig capacitance.

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Figure 2. AC Test Load
(for t_{OHZ}, t_{CHZ}, t_{OLZ}, and t_{DC1})

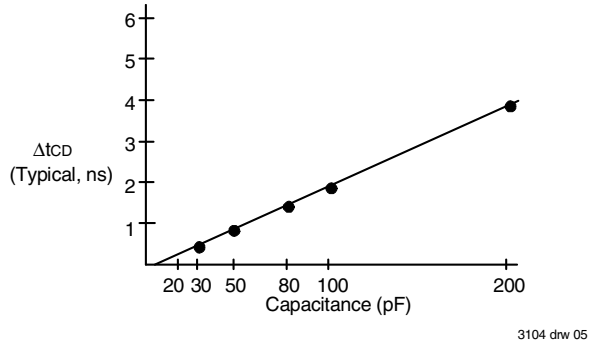

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Figure 3. Lumped Capacitive Load, Typical Derating

AC Test Conditions

Input Pulse Levels	0 to 3.0V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3104 tbl 14

AC Electrical Characteristics

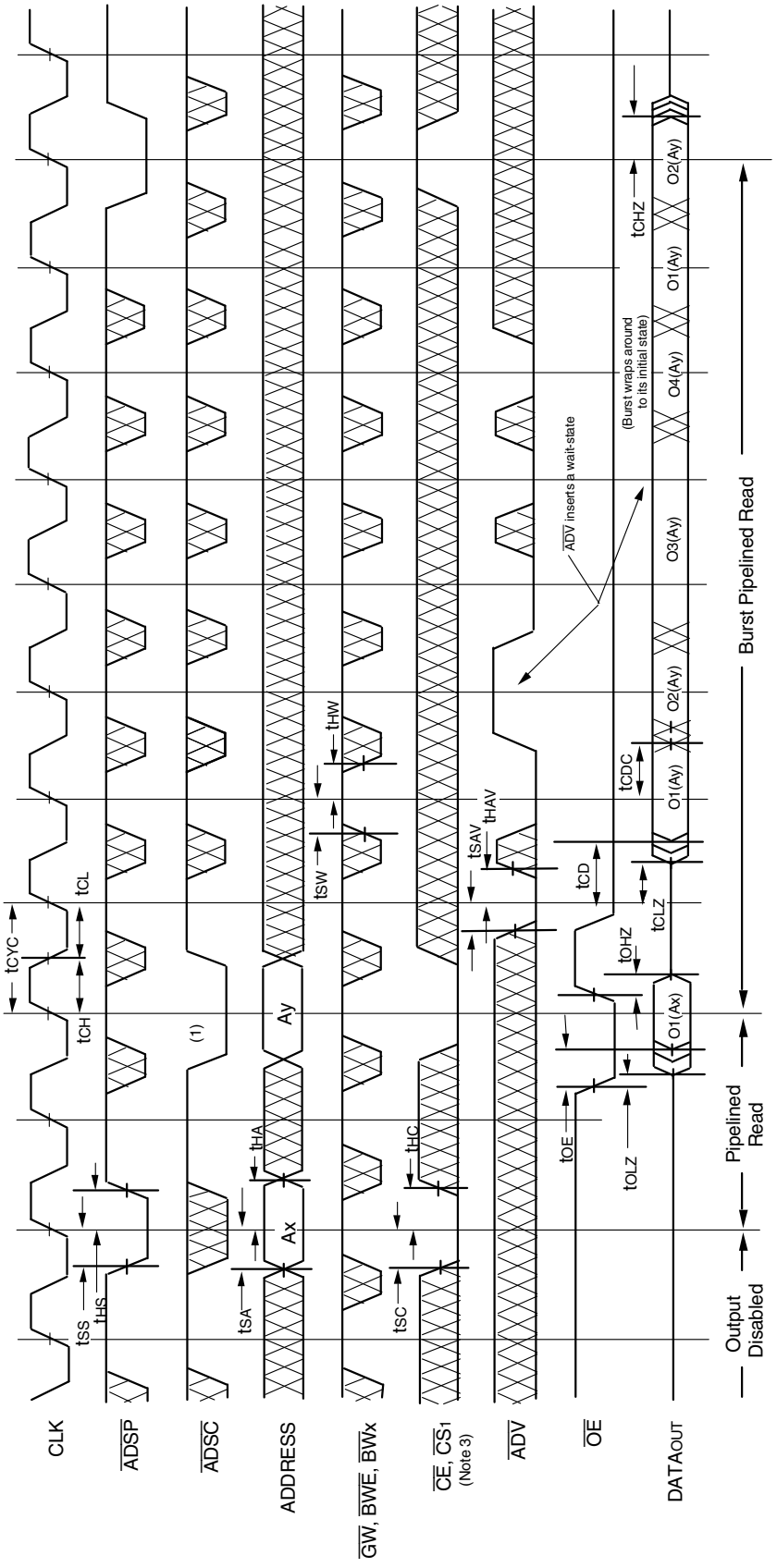
(VDD = 3.3V +10/-5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	71V432S5		71V432S6		Unit
		Min.	Max.	Min.	Max.	
CLOCK PARAMETERS						
t_{CYC}	Clock Cycle Time	10	—	12	—	ns
t_{CH}(1)	Clock High Pulse Width	4	—	4.5	—	ns
t_{CL}(1)	Clock Low Pulse Width	4	—	4.5	—	ns
OUTPUT PARAMETERS						
t_{CD}	Clock High to Valid Data	—	5	—	6	ns
t_{CDC}	Clock High to Data Change	1.5	—	2	—	ns
t_{CLZ}(2)	Clock High to Output Active	0	—	0	—	ns
t_{CHZ}(2)	Clock High to Data High-Z	1.5	5	2	5	ns
t_{OE}	Output Enable Access Time	—	5	—	5	ns
t_{OLZ}(2)	Output Enable Low to Data Active	0	—	0	—	ns
t_{OHZ}(2)	Output Enable High to Data High-Z	—	4	—	5	ns
SETUP TIMES						
t_{SA}	Address Setup Time	2.5	—	2.5	—	ns
t_{SS}	Address Status Setup Time	2.5	—	2.5	—	ns
t_{SD}	Data in Setup Time	2.5	—	2.5	—	ns
t_{SW}	Write Setup Time	2.5	—	2.5	—	ns
t_{SAV}	Address Advance Setup Time	2.5	—	2.5	—	ns
t_{SC}	Chip Enable/Select Setup Time	2.5	—	2.5	—	ns
HOLD TIMES						
t_{HA}	Address Hold Time	0.5	—	0.5	—	ns
t_{HS}	Address Status Hold Time	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	ns
t_{HW}	Write Hold Time	0.5	—	0.5	—	ns
t_{HAV}	Address Advance Hold Time	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	ns
SLEEP MODE AND CONFIGURATION PARAMETERS						
t_{ZZPW}	ZZ Pulse Width	100	—	100	—	ns
t_{ZZR}(3)	ZZ Recovery Time	100	—	100	—	ns
t_{CFG}(4)	Configuration Set-up Time	40	—	50	—	ns

3104 tbl 15a

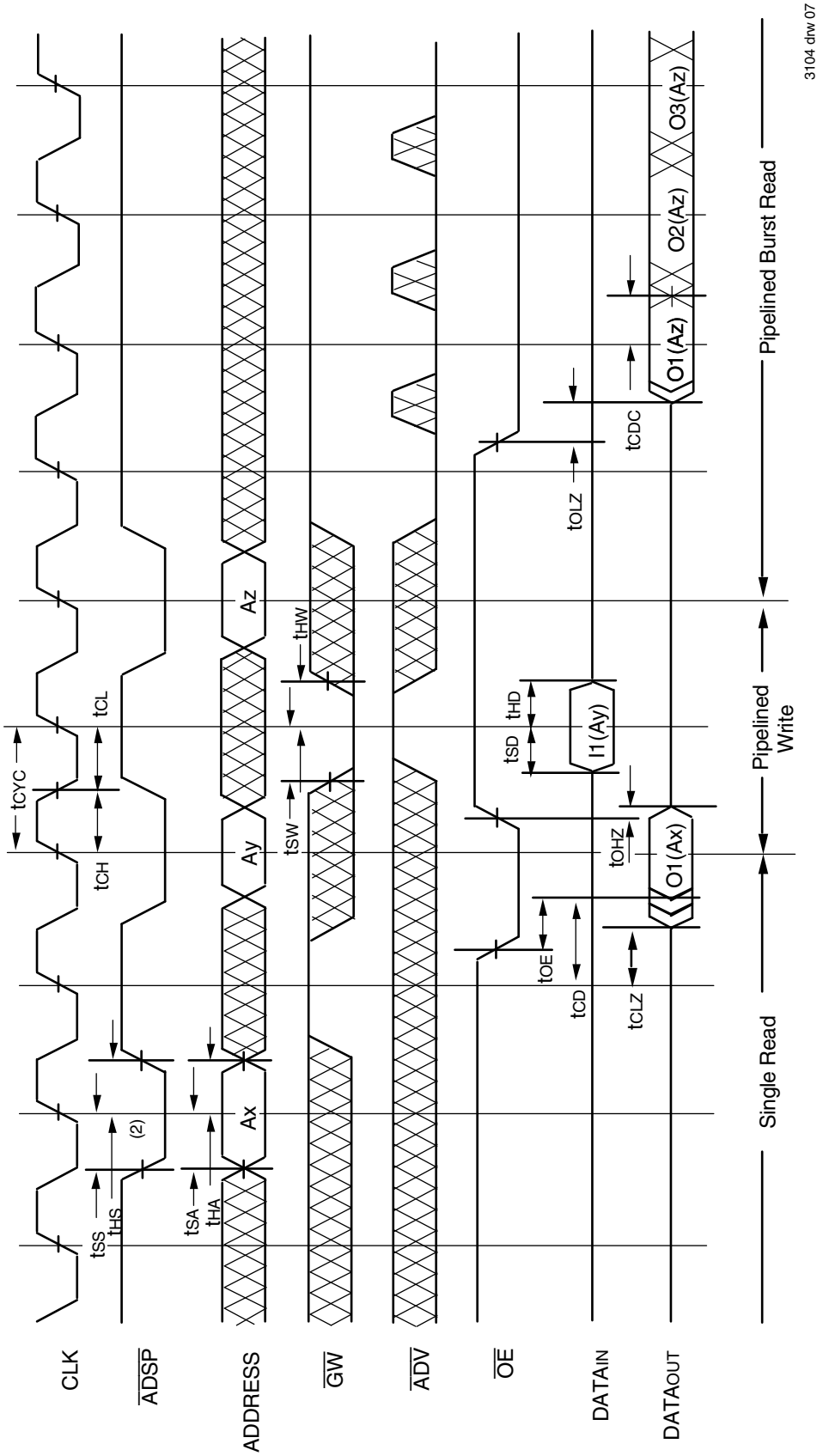
NOTES:
1. Measured as HIGH above 2.0V and LOW below 0.8V.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.

Timing Waveform of Pipelined Read Cycle(1,2)



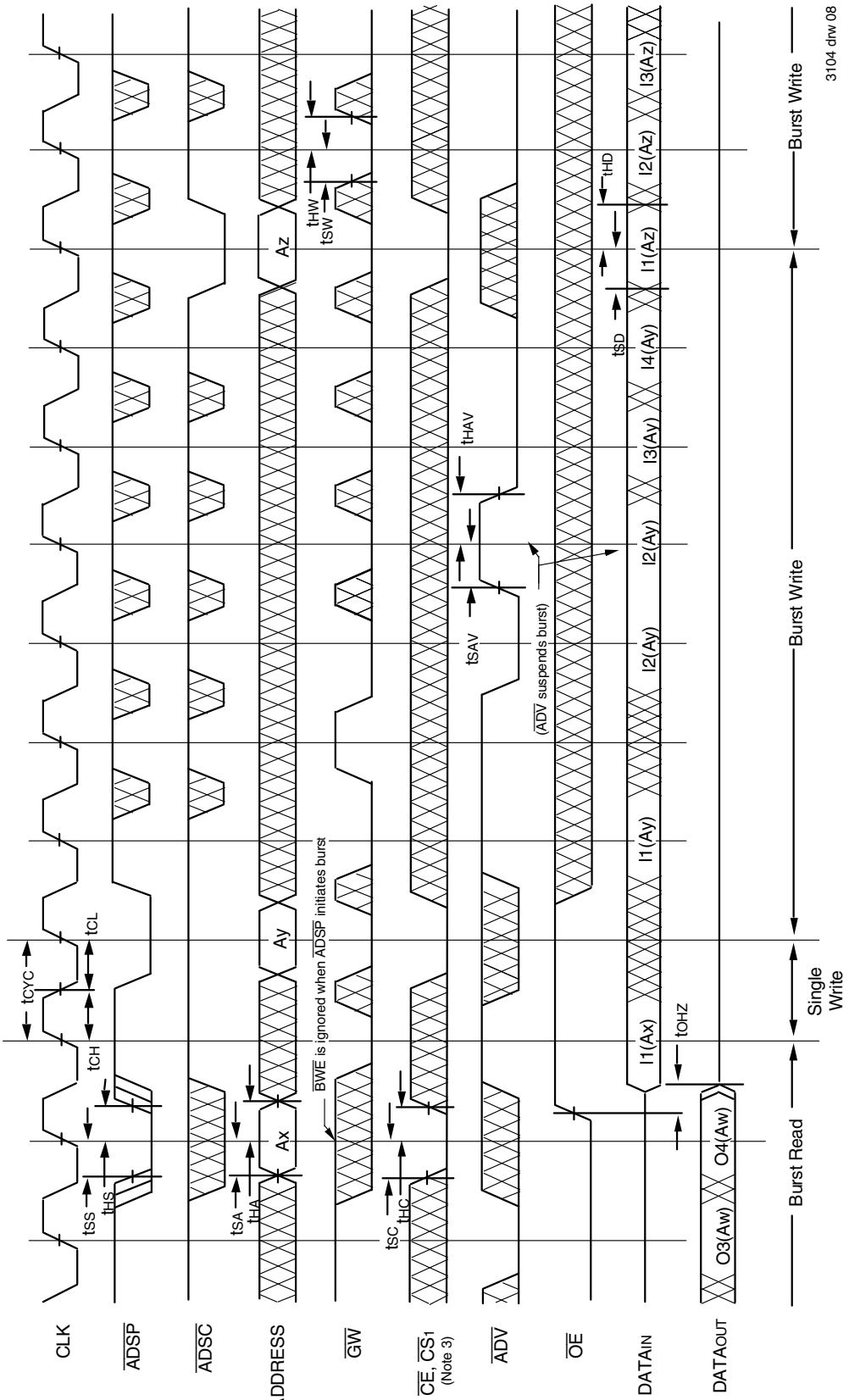
NOTES:
1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, CS_0 is HIGH.

Timing Waveform of Combined Pipelined Read and Write Cycles(1,2,3)



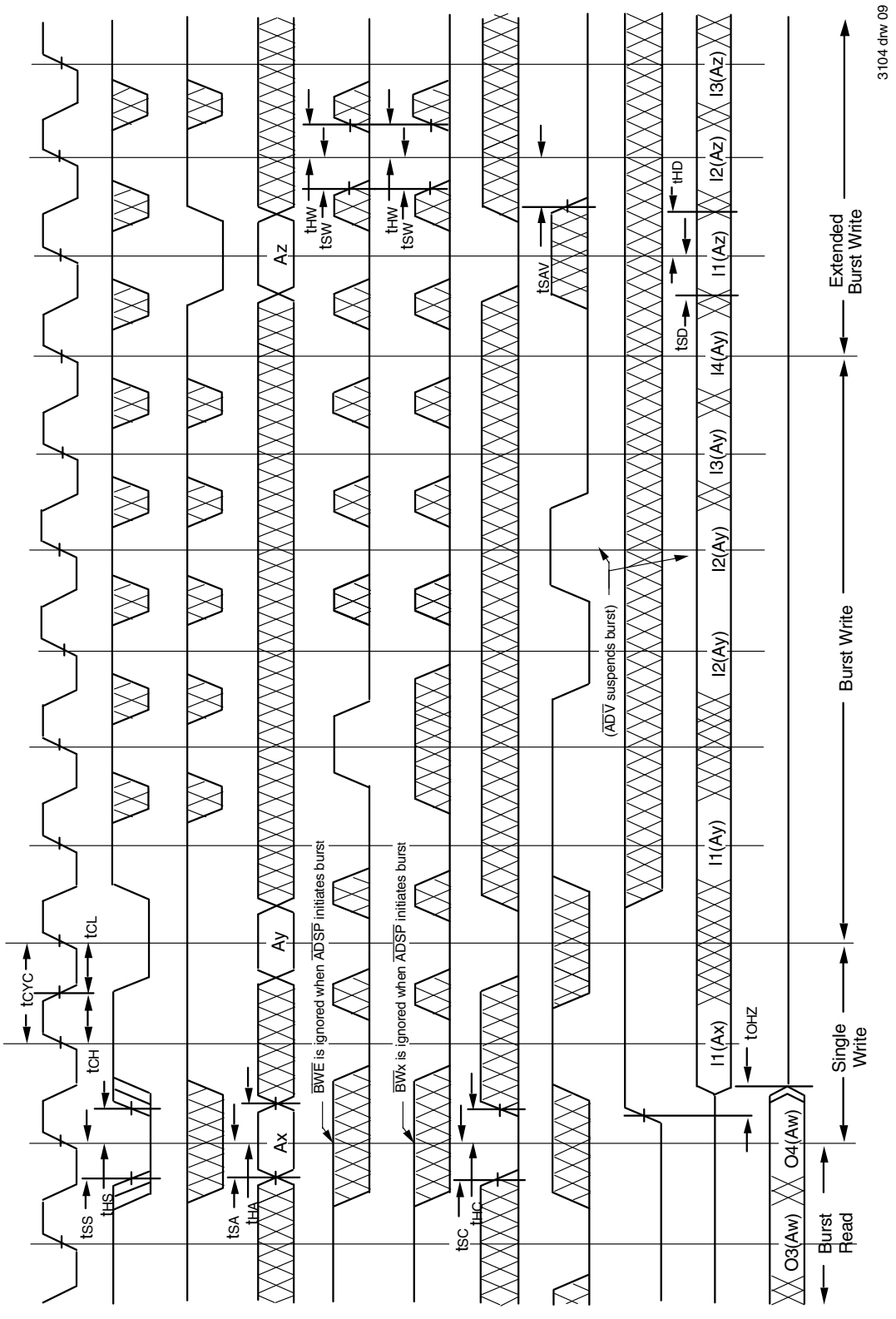
NOTES:
1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS}_1$ are LOW, CS_0 is HIGH.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. O1(Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay. O1(Az) represents the first output from the external addresses Az; O2(Az) represents the next output data in the burst sequence of the base address Az, etc. where A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.

Timing Waveform of Write Cycle No. 1 — $\overline{GW}$ Controlled(1,2,3)



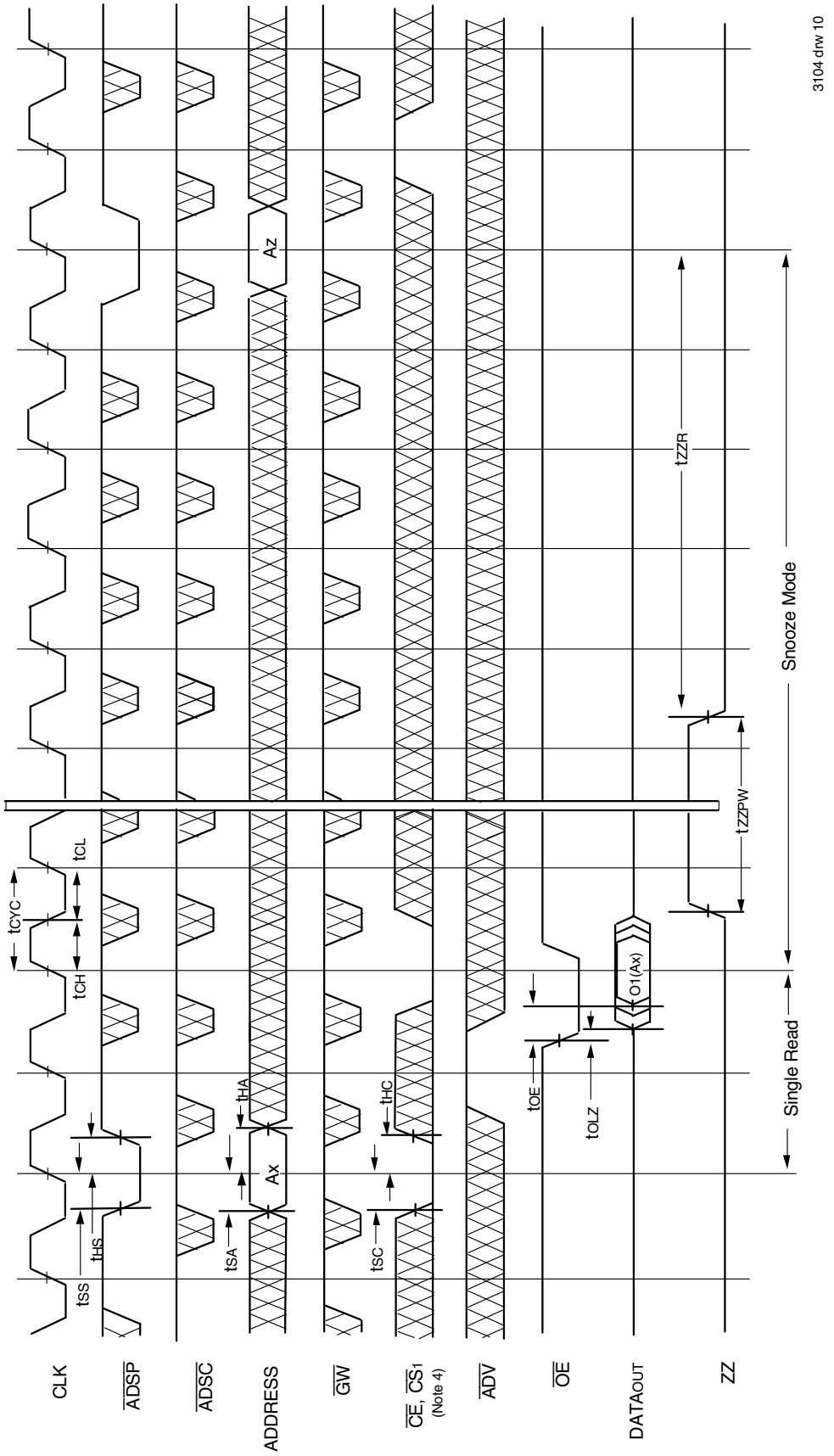
NOTES:
1. ZZ input is LOW, $\overline{BWE}$ is HIGH, and $\overline{LBO}$ is Don't Care for this cycle.
2. O4(Aw) represents the final output data in the burst sequence of the base address Aw. I1(Ax) represents the first input from the external address Ax. I1(Ay) represents the first input from the external address Ay. I2(Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2(Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS_1}$ signals. For example, when $\overline{CE}$ and $\overline{CS_1}$ are LOW on this waveform, CS_0 is HIGH.

Timing Waveform of Write Cycle No. 2 — Byte Controlled(1,2,3)



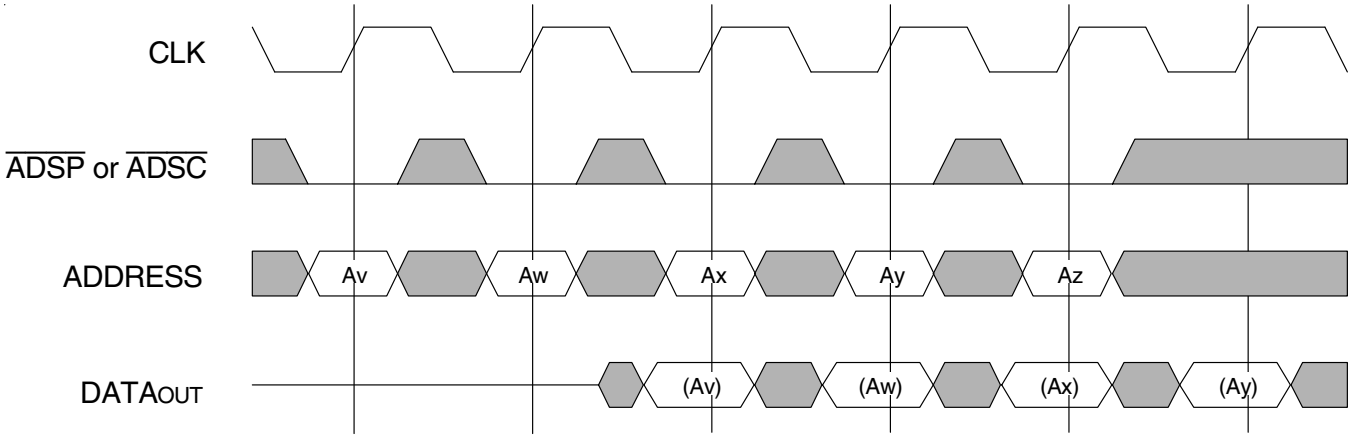
NOTES:
1. $\overline{ZZ}$ input is LOW, $\overline{GW}$ is HIGH, and $\overline{LBO}$ is Don't Care for this cycle.
2. O4(Aw) represents the final output data in the burst sequence of the base address Aw. I1(Ax) represents the first input from the external address Ax. I1(Ay) represents the first input from the external address Ay; I2(Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
   In the case of input I2(Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS_1}$ signals. For example, when $\overline{CE}$ and $\overline{CS_1}$ are LOW on this waveform, CS_0 is HIGH.

Timing Waveform of Sleep (ZZ) and Power-Down Modes(1,2,3)



NOTES:
1. Device must power up in deselected Mode.
2. $\overline{LBO}$ input is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, CS0 is HIGH.

Non-Burst Read Cycle Timing Waveform(1,2,3,4)



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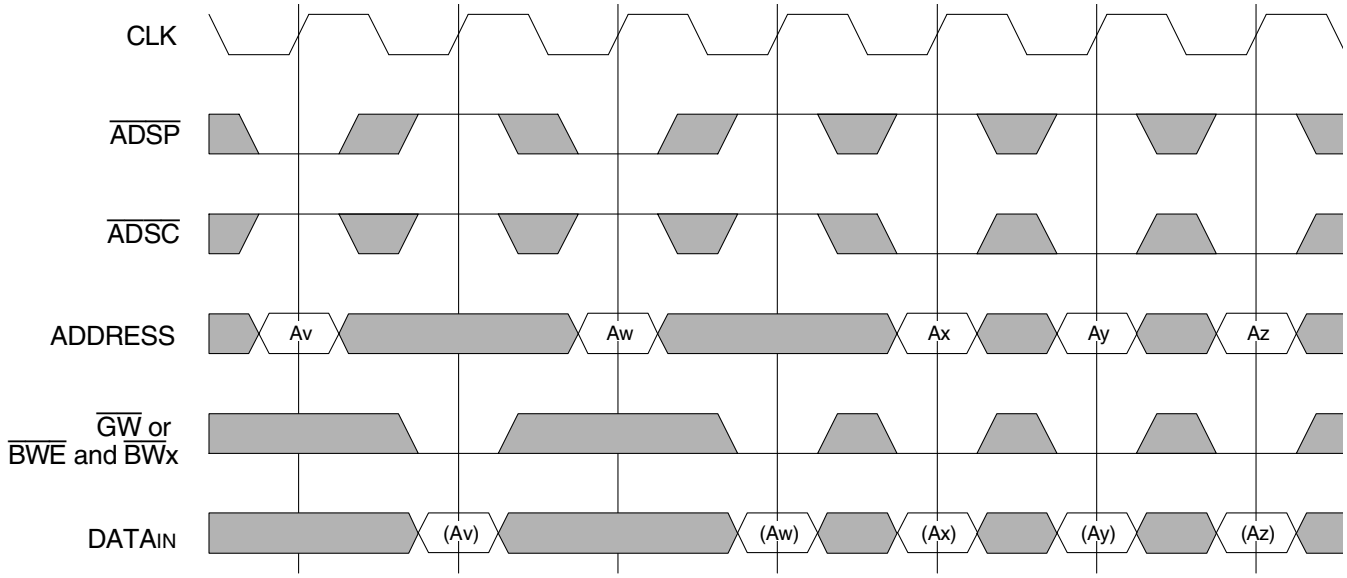
NOTES:
1. ZZ, $\overline{CE}$, $\overline{CS_1}$, and $\overline{OE}$ are LOW for this cycle.
2. $\overline{ADV}$, $\overline{GW}$, $\overline{BWE}$, $\overline{BW}$x, and CS_0 are HIGH for this cycle.
3. (Ax) represents the data for address Ax, etc.
4. For read cycles, $\overline{ADSP}$ and $\overline{ADSC}$ function identically and are therefore interchangeable.

Non-Burst Write Cycle Timing Waveform(1,2,3,4)



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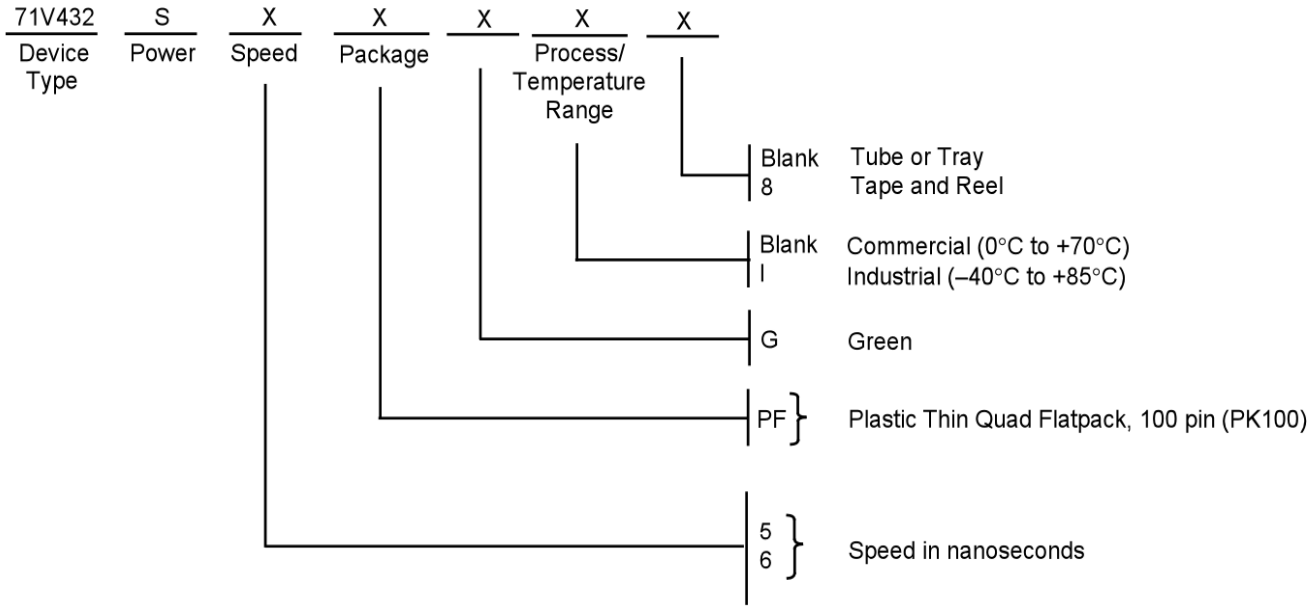
NOTES:
1. ZZ, $\overline{CE}$ and $\overline{CS_1}$ are LOW for this cycle.
2. $\overline{ADV}$, $\overline{OE}$ and CS_0 are HIGH for this cycle.
3. (Ax) represents the data for address Ax, etc.
4. For write cycles, $\overline{ADSP}$ and $\overline{ADSC}$ have different limitations.

Ordering Information



PART NUMBER	SPEED IN MEGAHERTZ	t_{CD} PARAMETER	CLOCK CYCLE TIME
71V432S5PF	100 MHz	5 ns	10 ns
71V432S6PF	83 MHz	6 ns	12 ns

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Datasheet Document History

9/10/99		Updated to new format
	Pg. 3–5	Adjusted page layout, added extra page
	Pg. 5	Added notes to pin configuration
	Pg. 11–14	Revised notes
	Pg. 17	Added Datasheet Document History
03/09/00	Pg. 1, 4, 8, 9, 16	Added Industrial temperature range offerings
04/04/00	Pg. 16	Added 100pin TQFP package Diagram Outline
08/09/00		Added “Not recommended for new designs”
08/17/01		Removed “Not recommended for new designs” from the background on the datasheet
03/31/05	Pg. 17	Added RoHS “Restricted Hazardous Substance Device” to ordering information
08/01/14	Pg. 1-3	Moved the FBD, the pin description and pin definition tables to pages 1 - 3 respectively to align the datasheet reading flow to that of our other established datasheets
	Pg. 17	In the Ordering Information, Tape & Reel added & RoHS designation changed to Green
10/03/14	Pg. 1	Removed *7ns Clock-to-Data Access (66MHz)*. and added green availability in Features
	Pg. 1-2	Moved notes regarding IDT’s use of the CacheRAM, the Pentium processor & the PowerPC terminology
	Pg. 2	Removed the reference to IDT with regards to the CMOS process
	Pg. 5	The package code PK100-1 changed to PK100 to match standard package codes
	Pg. 8	Removed IDT71V432S7 speed grade offering in the DC Chars table
	Pg. 9	Removed 71V432S7 speed grade offering in the AC Chars table
	Pg. 16	Removed TQFP Package Diagram Outline In the Ordering Information, PK100-1 package code changed to PK100 and 7ns speed grade was removed
	Pg. 17	Updated Customer’s SRAM Tech Support phone number and email address

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