

TSL2571

Light-to-Digital Converter

General Description

The TSL2571 family of devices provides ambient light sensing (ALS) that approximates human eye response to light intensity under a variety of lighting conditions and through a variety of attenuation materials. While useful for general purpose light sensing, the device is particularly useful for display management with the purpose of extending battery life and providing optimum viewing in diverse lighting conditions. Display panel and keyboard backlighting can account for up to 30 to 40 percent of total platform power. The ALS features are ideal for use in notebook PCs, LCD monitors, flat-panel televisions, and cell phones.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TSL2571, Light-to-Digital Converter are listed below:

Figure 1:
Added Value Of Using TSL2571

| Benefits | Features |
|--|--|
| <ul style="list-style-type: none"> Enables Operation in IR Light Environments | <ul style="list-style-type: none"> Patented Dual-Diode Architecture |
| <ul style="list-style-type: none"> Enables Dark Room to High Lux Sunlight Operation | <ul style="list-style-type: none"> 1M:1 Dynamic Range |
| <ul style="list-style-type: none"> Digital Interface is Less Susceptible to Noise | <ul style="list-style-type: none"> I²C Digital Interface |
| <ul style="list-style-type: none"> Enables Low Standby Power Consumption | <ul style="list-style-type: none"> 2.5µA Quiescent Current (Sleep Mode) |
| <ul style="list-style-type: none"> Reduces Board Space Requirements while Simplifying Designs | <ul style="list-style-type: none"> Available in 2mm x 2mm Dual Flat No-Lead (FN) Packages |

- Ambient Light Sensing (ALS)
 - Approximates Human Eye Response
 - Programmable Analog Gain
 - Programmable Integration Time
 - Programmable Interrupt Function with Upper and Lower Threshold
 - Resolution Up to 16 Bits
 - Very High Sensitivity — Operates Well Behind Darkened Glass
 - Up to 1,000,000:1 Dynamic Range

- Programmable Wait Timer
 - Programmable from 2.72 ms to > 8 Seconds
 - Wait State — 65µA Typical Current
- I²C Interface Compatible
 - Up to 400 kHz (I²C Fast Mode)
 - Dedicated Interrupt Pin
- Small 2 mm x 2 mm ODFN Package
- Sleep Mode — 2.5µA Typical Current

Applications

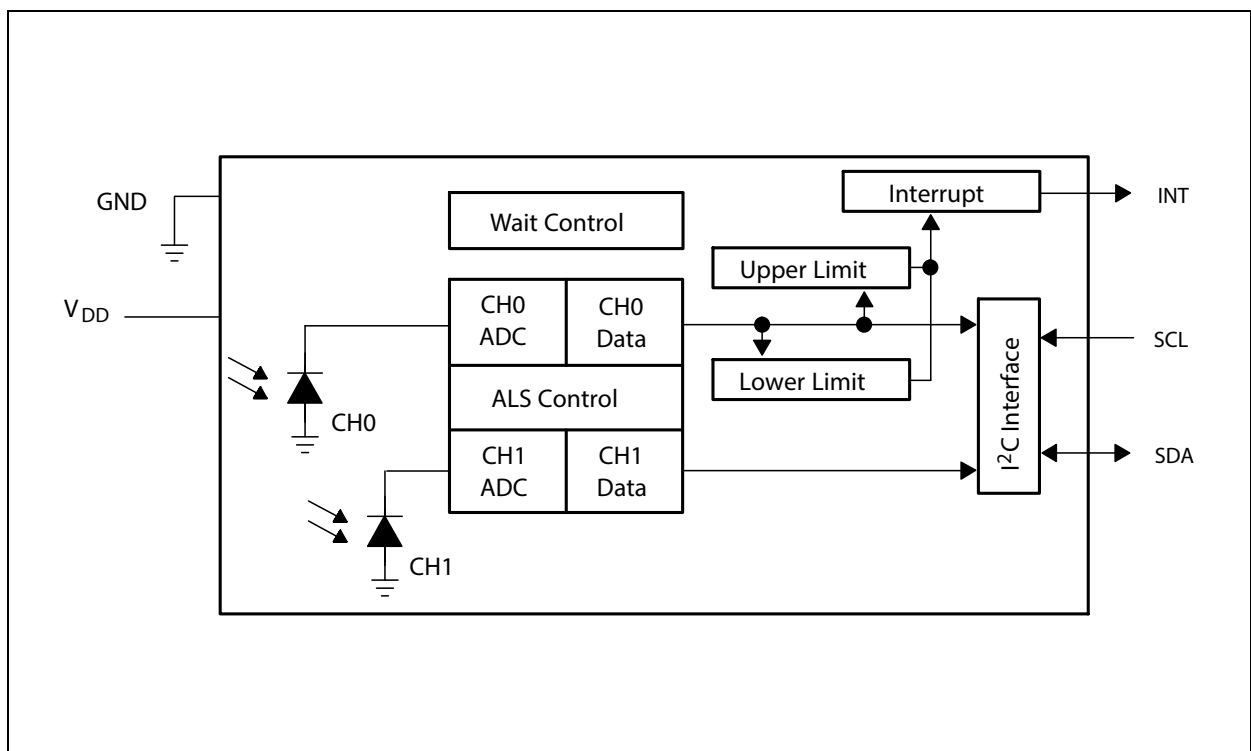
TSL2571, Light-to-Digital Converter is ideal for:

- Display Management
- Backlight Control
- Portable Device Power Optimization
- Cell Phones, PDA, GPS
- Notebooks and Monitors
- LCD TVs

Functional Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TSL2571 Block Diagram



Pin Assignments

Figure 3:
Package FN Dual Flat No-Lead (Top View)

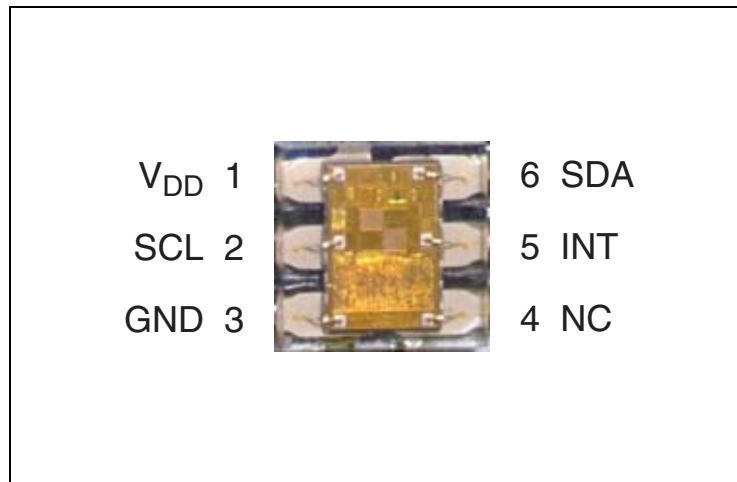


Figure 4:
Terminal Functions

| Terminal | | Type | Description |
|-----------------|----|------|---|
| Name | No | | |
| V _{DD} | 1 | | Supply voltage. |
| SCL | 2 | I | I ² C serial clock input terminal — clock signal for I ² C serial data. |
| GND | 3 | | Power supply ground. All voltages are referenced to GND. |
| NC | 4 | | Do not connect. |
| INT | 5 | O | Interrupt — open drain (active low). |
| SDA | 6 | I/O | I ² C serial data I/O terminal — serial data I/O for I ² C. |

Detailed Description

The TSL2571 light-to-digital device includes on-chip photodiodes, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine, and an I²C interface. The device combines one photodiode (CH0), which is responsive to both visible and infrared light, and one photodiode (CH1), which is responsive primarily to infrared light. Two integrating ADCs simultaneously convert the amplified photodiode currents into a digital value providing up to 16 bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the data registers. This digital output can be read by a microprocessor through which the illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human eye response.

Communication to the device is accomplished through a fast (up to 400 kHz), two-wire I²C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the device is inherently more immune to noise when compared to an analog interface.

The device provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. An interrupt is generated when the value of an ALS conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently.

Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)

| Symbol | Parameter | Min | Max | Units |
|----------------|---------------------------------|-------|-----|-------|
| $V_{DD}^{(1)}$ | Supply voltage | | 3.8 | V |
| V_O | Digital output voltage range | -0.5 | 3.8 | V |
| I_O | Digital Output current | -1 | +20 | mA |
| T_{STRG} | Storage temperature range | -40 | 85 | °C |
| ESD_{HBM} | ESD tolerance, human body model | ±2000 | | V |

Note(s):

1. All voltages are with respect to GND.

Electrical Characteristics

Figure 6:
Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units |
|----------|--------------------------------|-----|-----|-----|-------|
| V_{DD} | Supply voltage | 2.6 | 3 | 3.6 | V |
| T_A | Operating free-air temperature | -30 | | 70 | °C |

Figure 7:
Operating Characteristics; $V_{DD} = 3V$, $T_A = 25^\circ C$ (unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|------------|-------------------------------------|---|--------------|-----|--------------|---------|
| I_{DD} | Supply current | Active | | 175 | 250 | μA |
| | | Wait mode | | 65 | | |
| | | Sleep mode — no I ² C activity | | 2.5 | 4 | |
| V_{OL} | INT SDA output low voltage | 3 mA sink current | 0 | | 0.4 | V |
| | | 6 mA sink current | 0 | | 0.6 | |
| I_{LEAK} | Leakage current, SDA, SCL, INT pins | | -5 | | 5 | μA |
| V_{IH} | SCL SDA input high voltage | TSL25711, TSL25715 | $0.7 V_{DD}$ | | | V |
| | | TSL25713 | 1.25 | | | |
| V_{IL} | SCL SDA input low voltage | TSL25711, TSL25715 | | | $0.3 V_{DD}$ | V |
| | | TSL25713 | | | 0.54 | |

Figure 8:

ALS Characteristics; $V_{DD} = 3V$, $T_A = 25^\circ C$, Gain = 16, AEN = 1 (unless otherwise noted)^{(1) (2) (3)}

| Parameter | Test Conditions | Channel | Min | Typ | Max | Unit |
|---|--|---------|------|------|-------|-----------------------------|
| Dark ADC count value | $E_e = 0$, AGAIN = 120× ATIME = 0xDB (100 ms) | CH0 | 0 | 1 | 5 | counts |
| | | CH1 | 0 | 1 | 5 | |
| ADC integration time step size | ATIME = 0xFF | | 2.58 | 2.72 | 2.9 | ms |
| ADC Number of integration steps | | | 1 | | 256 | steps |
| ADC counts per step | ATIME = 0xFF | | 0 | | 1024 | counts |
| ADC count value | ATIME = 0xC0 | | 0 | | 65535 | counts |
| ADC count value | $\lambda_p = 625$ nm, $E_e = 171.6$ $\mu W/cm^2$ ATIME = 0xF6 (27 ms) ⁽²⁾ | CH0 | 4000 | 5000 | 6000 | counts |
| | | CH1 | | 790 | | |
| | $\lambda_p = 850$ nm, $E_e = 219.7$ $\mu W/cm^2$ ATIME = 0xF6 (27 ms) ⁽³⁾ | CH0 | 4000 | 5000 | 6000 | |
| | | CH1 | | 2800 | | |
| ADC count value ratio: CH1/CH0 | $\lambda_p = 625$ ATIME 0xF6 (27 ms) ⁽²⁾ | | 10.8 | 15.8 | 20.8 | % |
| | $\lambda_p = 850$ ATIME 0xF6 (27 ms) ⁽³⁾ | | 41 | 56 | 68 | |
| R_e Irradiance responsivity | $\lambda_p = 625$ nm, ATIME = 0xF6 (27 ms) ⁽²⁾ | CH0 | | 29.1 | | counts/ ($\mu W/cm^2$) |
| | | CH1 | | 4.6 | | |
| | $\lambda_p = 850$ nm, ATIME = 0xF6 (27 ms) ⁽³⁾ | CH0 | | 22.8 | | |
| | | CH1 | | 12.7 | | |
| Gain scaling, relative to 1× gain setting | 8× | | -10 | | 10 | % |
| | 16× | | -10 | | 10 | |
| | 120× | | -10 | | 10 | |

Note(s):

- Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible 625 nm LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.
- The 625 nm irradiance E_e is supplied by an AlInGaP light-emitting diode with the following typical characteristics: peak wavelength $\lambda_p = 625$ nm and spectral halfwidth $\Delta\lambda_{1/2} = 20$ nm.
- The 850 nm irradiance E_e is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength $\lambda_p = 850$ nm and spectral halfwidth $\Delta\lambda_{1/2} = 42$ nm.

Figure 9:
 Wait Characteristics; $V_{DD} = 3V$, $T_A = 25^\circ C$, $WEN = 1$ (unless otherwise noted)

| Parameter | Test Conditions | Channel | Min | Typ | Max | Unit |
|----------------------------------|-----------------|---------|------|------|-----|-------|
| Wait step size | WTIME = 0xFF | | 2.58 | 2.72 | 2.9 | ms |
| Wait number of integration steps | | | 1 | | 256 | steps |

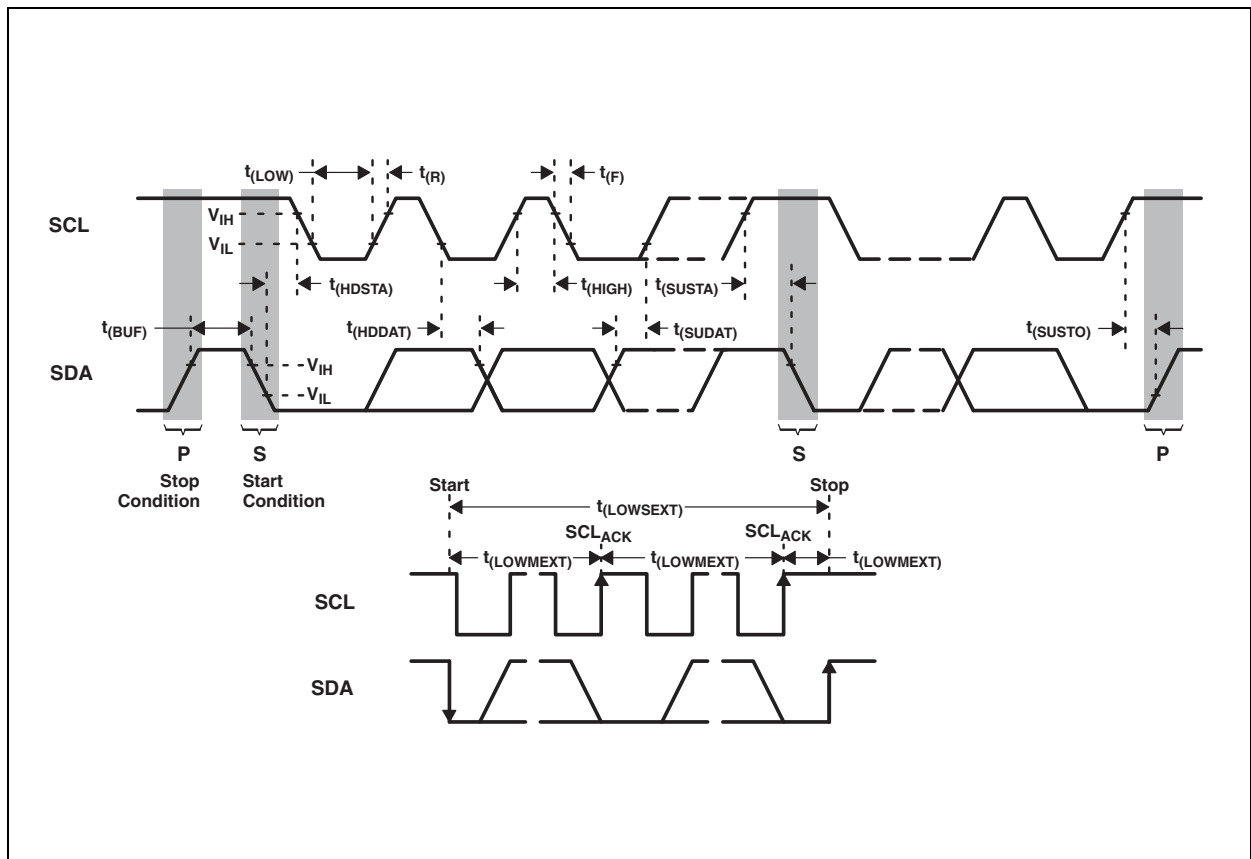
Figure 10:
 AC Electrical Characteristics; $V_{DD} = 3V$, $T_A = 25^\circ C$, (unless otherwise noted)

| Symbol | Parameter ⁽¹⁾ | Test Conditions | Min | Typ | Max | Unit |
|---------------|--|-----------------|-----|-----|-----|---------|
| $f_{(SCL)}$ | Clock frequency (I ² C only) | | 0 | | 400 | kHz |
| $t_{(BUF)}$ | Bus free time between start and stop condition | | 1.3 | | | μs |
| $t_{(HDSTA)}$ | Hold time after (repeated) start condition. After this period, the first clock is generated. | | 0.6 | | | μs |
| $t_{(SUSTA)}$ | Repeated start condition setup time | | 0.6 | | | μs |
| $t_{(SUSTO)}$ | Stop condition setup time | | 0.6 | | | μs |
| $t_{(HDDAT)}$ | Data hold time | | 0 | | | μs |
| $t_{(SUDAT)}$ | Data setup time | | 100 | | | ns |
| $t_{(LOW)}$ | SCL clock low period | | 1.3 | | | μs |
| $t_{(HIGH)}$ | SCL clock high period | | 0.6 | | | μs |
| t_F | Clock/data fall time | | | | 300 | ns |
| t_R | Clock/data rise time | | | | 300 | ns |
| C_i | Input pin capacitance | | | | 10 | pF |

Note(s):

1. Specified by design and characterization; not production tested.

Figure 11:
Timing Diagrams - Parameter Measurement Information



Typical Characteristics

Figure 12:
Spectral Responsivity

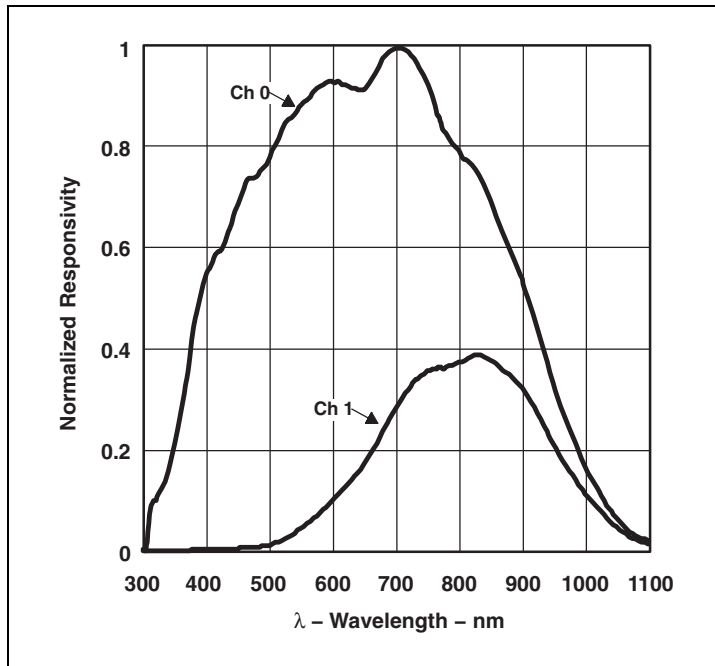


Figure 13:
Normalized I_{DD} vs. V_{DD} and Temperature

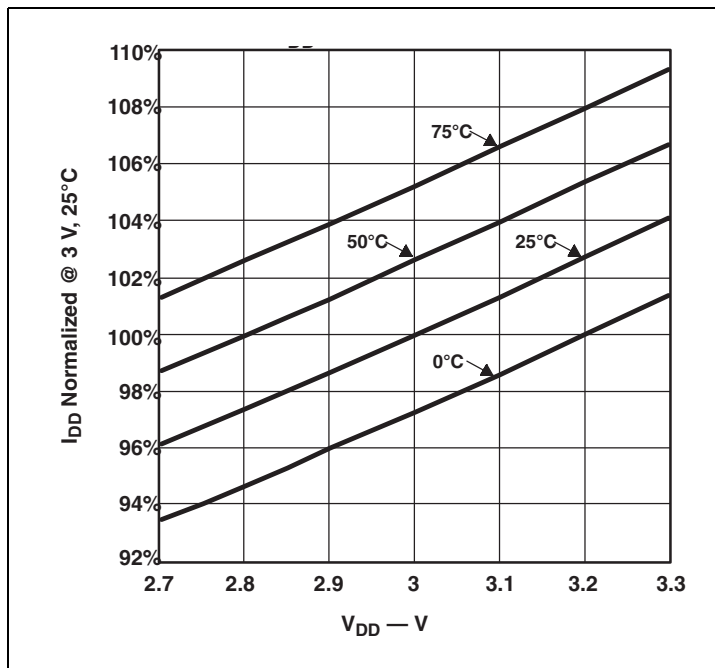
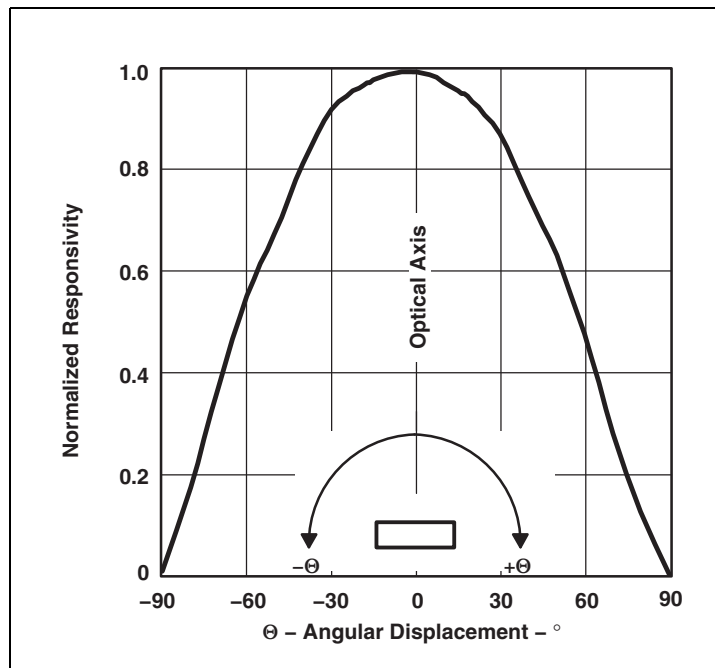


Figure 14:
Normalized Responsivity vs. Angular Displacement

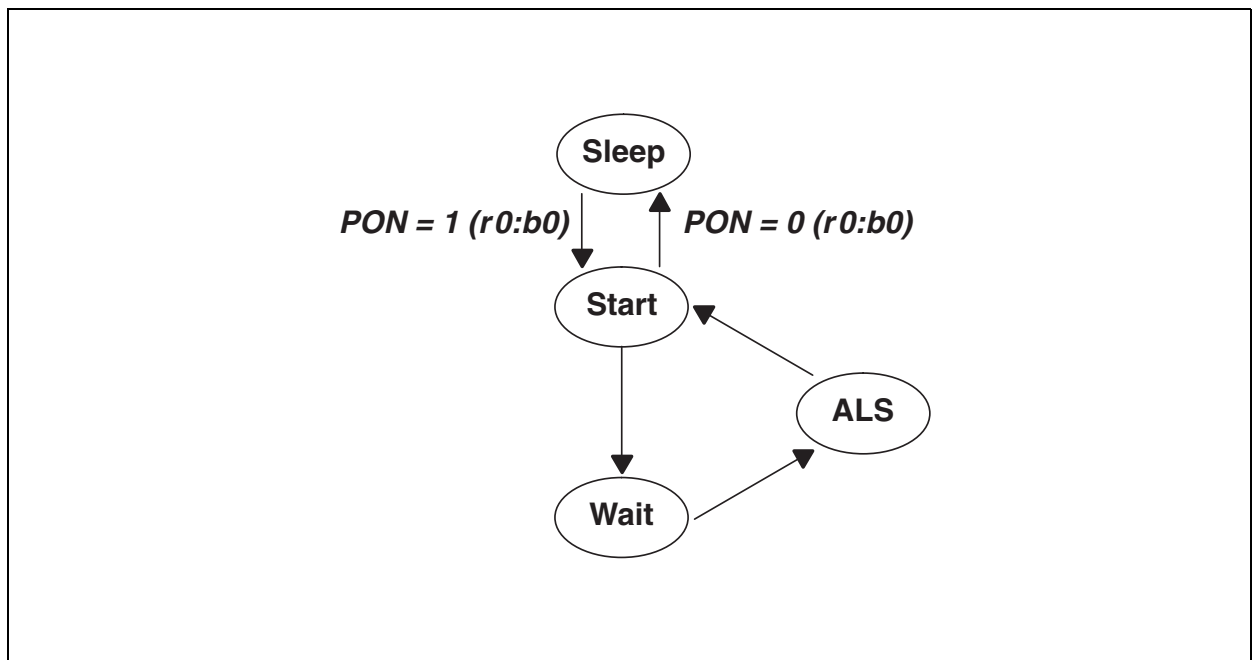


Principles of Operation

System State Machine

The device provides control of ALS and power management functionality through an internal state machine (see Figure 15). After a power-on-reset, the device is in the sleep mode. As soon as the PON bit is set, the device will move to the start state. It will then continue through the Wait and ALS states. If these states are enabled, the device will execute each function. If the PON bit is set to 0, the state machine will continue until all conversions are completed and then go into a low power sleep mode.

Figure 15:
Simplified State Diagram



Note(s): In this document, the nomenclature uses the bit field name in italic followed by the register number and bit number to allow the user to easily identify the register and bit that controls the function. For example, the power on (PON) is in register 0, bit 0. This is represented as *PON (r0:b0)*.

Photodiodes

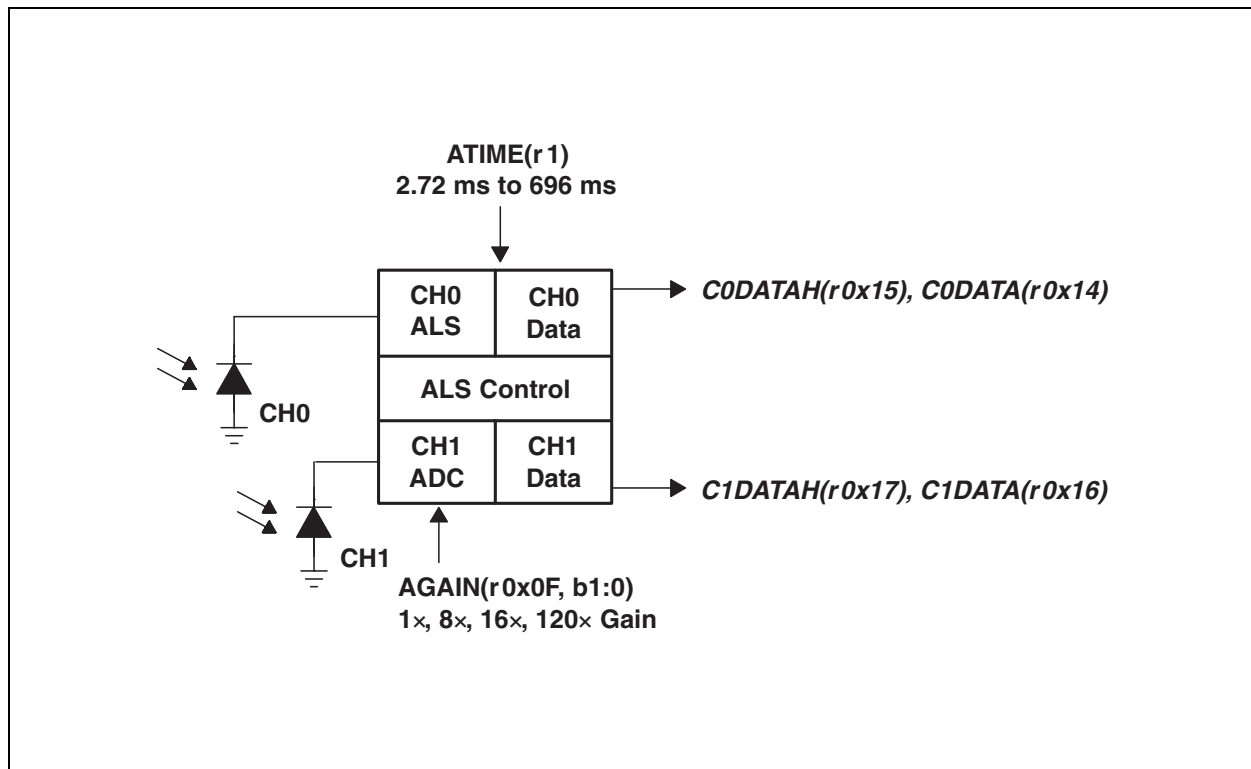
Conventional silicon detectors respond strongly to infrared light, which the human eye does not see. This can lead to significant error when the infrared content of the ambient light is high (such as with incandescent lighting) due to the difference between the silicon detector response and the brightness perceived by the human eye.

This problem is overcome through the use of two photodiodes. The channel 0 photodiode, referred to as the CH0 channel, is sensitive to both visible and infrared light, while the channel 1 photodiode, referred to as CH1, is sensitive primarily to infrared light. Two integrating ADCs convert the photodiode currents to digital outputs. The ADC digital outputs from the two channels are used in a formula to obtain a value that approximates the human eye response in units of lux.

ALS Operation

The ALS engine contains ALS gain control (AGAIN) and two integrating analog-to-digital converters (ADC) for the Channel 0 and Channel 1 photodiodes. The ALS integration time (ATIME) impacts both the resolution and the sensitivity of the ALS reading. Integration of both channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the data registers (C0DATA and C1DATA). This data is also referred to as channel *count*. The transfers are double-buffered to ensure data integrity.

Figure 16:
ALS Operation



The registers for programming the integration and wait times are a 2's complement values. The actual time can be calculated as follows:

$$\text{ATIME} = 256 - \text{Integration Time} / 2.72 \text{ ms}$$

Inversely, the time can be calculated from the register value as follows:

$$\text{Integration Time} = 2.72 \text{ ms} \times (256 - \text{ATIME})$$

In order to reject 50/60-Hz ripple strongly present in fluorescent lighting, the integration time needs to be programmed in multiples of 10 / 8.3 ms or the half cycle time. Both frequencies can be rejected with a programmed value of 50 ms (ATIME = 0xED) or multiples of 50 ms (i.e. 100, 150, 200, 400, 600).

The registers for programming the AGAIN hold a two-bit value representing a gain of 1×, 8×, 16×, or 120×. The gain, in terms of amount of gain, will be represented by the value AGAINx, i.e. AGAINx = 1, 8, 16, or 120.

Lux Equation

The lux calculation is a function of CH0 channel count (C0DATA), CH1 channel count (C1DATA), ALS gain (AGAINx), and ALS integration time in milliseconds (ATIME_ms). If an aperture, glass/plastic, or a light pipe attenuates the light equally across the spectrum (300 nm to 1100 nm), then a scaling factor referred to as glass attenuation (GA) can be used to compensate for attenuation. For a device in open air with no aperture or glass/plastic above the device, GA = 1. If it is not spectrally flat, then a custom lux equation with new coefficients should be generated. (See **ams** application note).

Counts per Lux (CPL) needs to be calculated only when ATIME or AGAIN is changed, otherwise it remains a constant. The first segment of the equation (Lux1) covers fluorescent and incandescent light. The second segment (Lux2) covers dimmed incandescent light. The final lux is the maximum of Lux1, Lux2, or 0.

$$\text{CPL} = (\text{ATIME_ms} \times \text{AGAINx}) / (\text{GA} \times 53)$$

$$\text{Lux1} = (\text{C0DATA} - 2 \times \text{C1DATA}) / \text{CPL}$$

$$\text{Lux2} = (0.6 \times \text{C0DATA} - \text{C1DATA}) / \text{CPL}$$

$$\text{Lux} = \text{MAX}(\text{Lux1}, \text{Lux2}, 0)$$

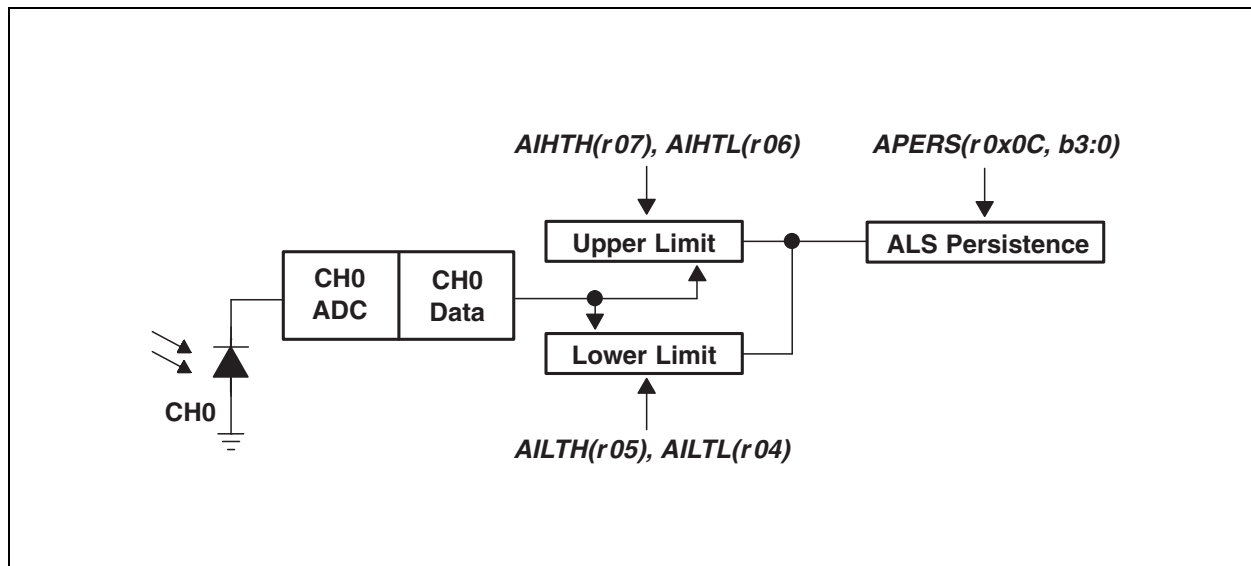
Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity values outside of a user-defined range. While the interrupt function is always enabled and its status is available in the status register (0x13), the output of the interrupt state can be enabled using the ALS interrupt enable (AIEN) field in the enable register (0x00).

Two 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level range. An interrupt can be generated when the ALS CH0 data (CODATA) falls outside of the desired light level range, as determined by the values in the ALS interrupt low threshold registers (AILTx) and ALS interrupt high threshold registers (AIHTx). It is important to note that the low threshold value must be less than the high threshold value for proper operation.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range ALS occurrences before an interrupt is generated. The persistence register (0x0C) allows the user to set the ALS persistence (APERS) value. See the persistence register for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see [Command Register](#)).

Figure 17:
Programmable Interrupt



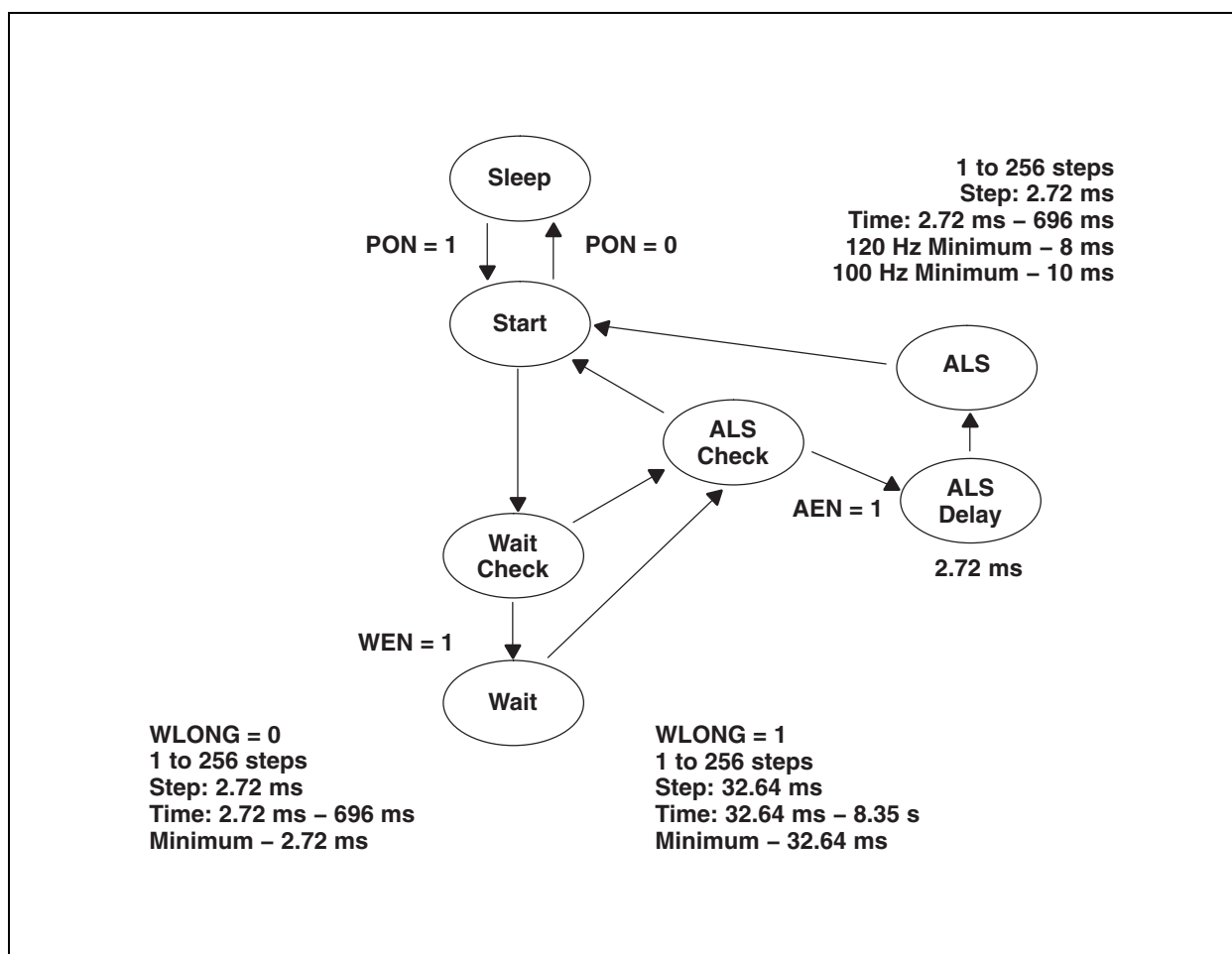
State Diagram

Figure 18 shows a more detailed flow for the state machine. The device starts in the sleep mode. The PON bit is written to enable the device. A 2.72-ms delay will occur before entering the start state.

If the WEN bit is set, the state machine will then cycle through the wait state. If the WLONG bit is set, the wait cycles are extended by 12x over normal operation. When the wait counter terminates, the state machine will step to the ALS state.

The AEN should always be set. In this case, a minimum of 1 integration time step should be programmed. The ALS state machine will continue until it reaches the terminal count at which point the data will be latched in the ALS register and the interrupt set, if enabled.

Figure 18:
Expanded State Diagram



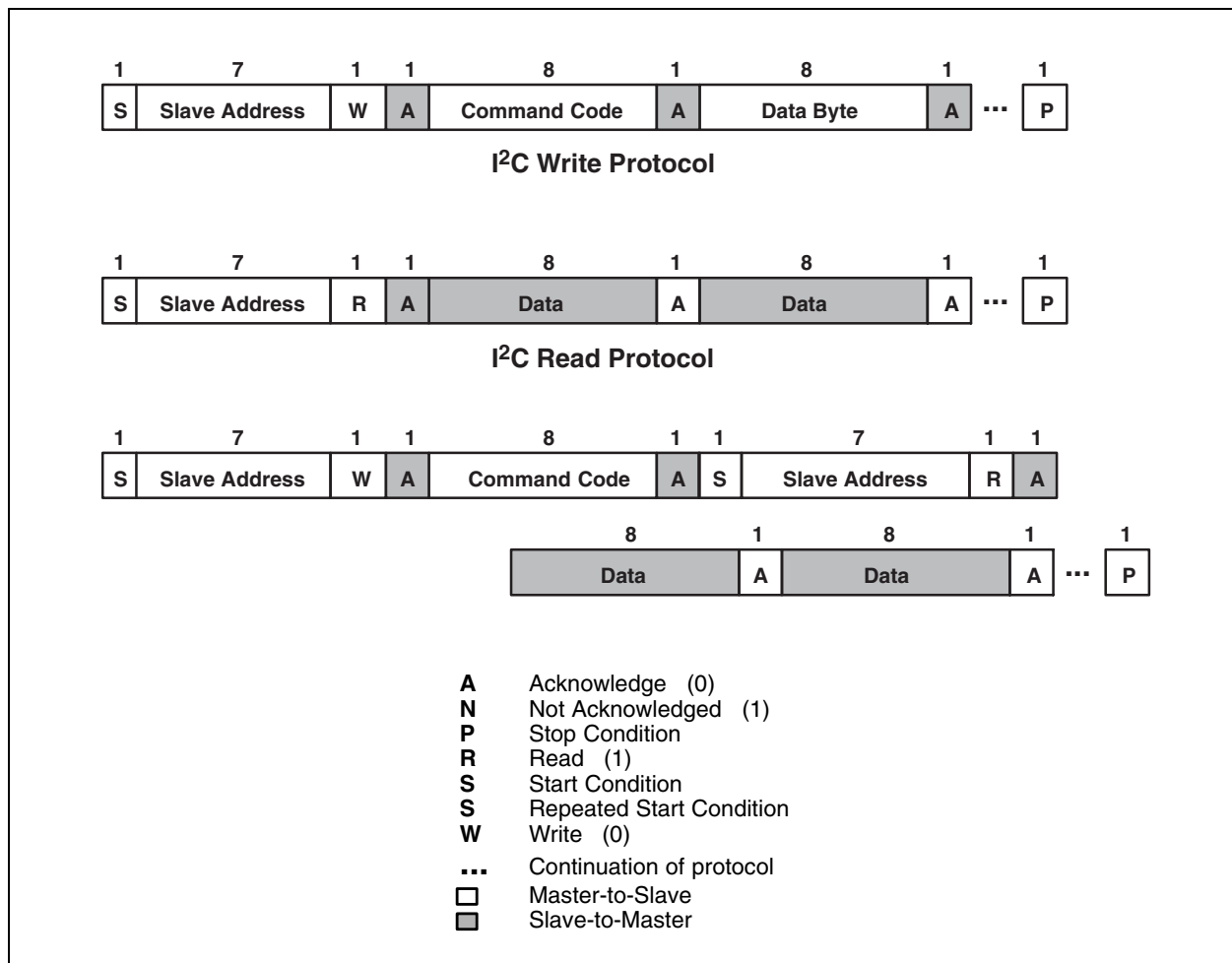
I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (see Figure 34). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at <http://www.i2c-bus.org/references/>.

Figure 19:
I²C Protocols



Register Description

Register Set

The device is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in [Figure 20](#).

Figure 20:
Register Address

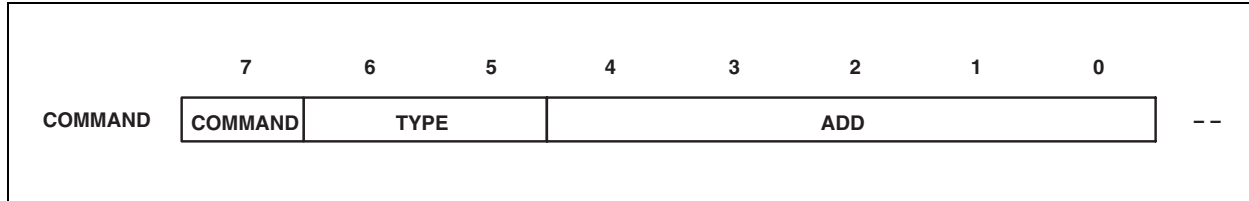
| Address | Register Name | R/W | Register Function | Reset Value |
|---------|---------------|-----|--|-------------|
| --- | COMMAND | W | Specifies register address | 0x00 |
| 0x00 | ENABLE | R/W | Enables states and interrupts | 0x00 |
| 0x01 | ATIME | R/W | ALS ADC time | 0xFF |
| 0x03 | WTIME | R/W | Wait time | 0xFF |
| 0x04 | AILTL | R/W | ALS interrupt low threshold low byte | 0x00 |
| 0x05 | AILTH | R/W | ALS interrupt low threshold high byte | 0x00 |
| 0x06 | AIHTL | R/W | ALS interrupt high threshold low byte | 0x00 |
| 0x07 | AIHTH | R/W | ALS interrupt high threshold high byte | 0x00 |
| 0x0C | PERS | R/W | Interrupt persistence filters | 0x00 |
| 0x0D | CONFIG | R/W | Configuration | 0x00 |
| 0x0F | CONTROL | R/W | Control register | 0x00 |
| 0x12 | ID | R | Device ID | ID |
| 0x13 | STATUS | R | Device status | 0x00 |
| 0x14 | C0DATA | R | CH0 ADC low data register | 0x00 |
| 0x15 | C0DATAH | R | CH0 ADC high data register | 0x00 |
| 0x16 | C1DATA | R | CH1 ADC low data register | 0x00 |
| 0x17 | C1DATAH | R | CH1 ADC high data register | 0x00 |

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I²C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command registers specifies the address of the target register for future write and read operations.

Figure 21:
Command Register

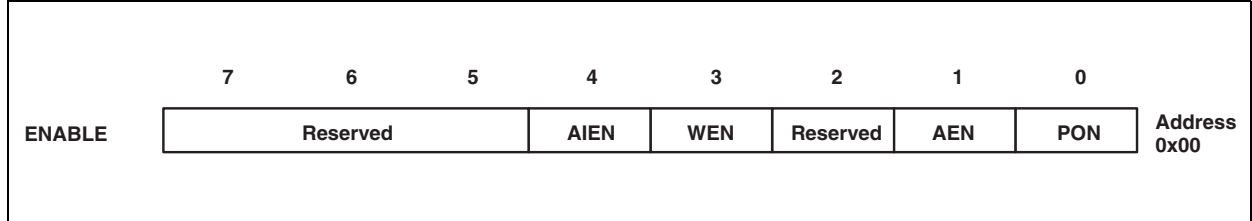


| Field | Bits | Description | | | | | | | | | | |
|--|--|--|-------------------------------------|-------------|-------|------------------------------------|-------|-------------------------------------|-------|-------------------------|----|--|
| COMMAND | 7 | Select Command Register. Must write as 1 when addressing COMMAND register. | | | | | | | | | | |
| TYPE | 6:5 | Selects type of transaction to follow in subsequent data transfers. | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>FIELD VALUE</th> <th>DESCRIPTION</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Repeated byte protocol transaction</td> </tr> <tr> <td>01</td> <td>Auto-increment protocol transaction</td> </tr> <tr> <td>10</td> <td>Reserved — Do not use</td> </tr> <tr> <td>11</td> <td>Special function — See description below</td> </tr> </tbody> </table> | FIELD VALUE | DESCRIPTION | 00 | Repeated byte protocol transaction | 01 | Auto-increment protocol transaction | 10 | Reserved — Do not use | 11 | Special function — See description below |
| | | FIELD VALUE | DESCRIPTION | | | | | | | | | |
| | | 00 | Repeated byte protocol transaction | | | | | | | | | |
| | | 01 | Auto-increment protocol transaction | | | | | | | | | |
| | | 10 | Reserved — Do not use | | | | | | | | | |
| 11 | Special function — See description below | | | | | | | | | | | |
| Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes. | | | | | | | | | | | | |
| ADD | 4:0 | Address register/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write and read transactions. The field values listed below apply only to special function commands: | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>FIELD VALUE</th> <th>DESCRIPTION</th> </tr> </thead> <tbody> <tr> <td>00000</td> <td>Normal — no action</td> </tr> <tr> <td>00110</td> <td>ALS interrupt clear</td> </tr> <tr> <td>other</td> <td>Reserved — do not write</td> </tr> </tbody> </table> | FIELD VALUE | DESCRIPTION | 00000 | Normal — no action | 00110 | ALS interrupt clear | other | Reserved — do not write | | |
| | | FIELD VALUE | DESCRIPTION | | | | | | | | | |
| | | 00000 | Normal — no action | | | | | | | | | |
| | | 00110 | ALS interrupt clear | | | | | | | | | |
| other | Reserved — do not write | | | | | | | | | | | |
| ALS interrupt clear — clears any pending ALS interrupt. This special function is self clearing. | | | | | | | | | | | | |

Enable Register (0x00)

The ENABLE register is used to power the device ON/OFF, enable functions, and interrupts.

Figure 22:
Enable Register



| Field | Bits | Description |
|--------------------|------|---|
| Reserved | 7:5 | Reserved. Write as 0. |
| AIEN | 4 | ALS interrupt mask. When asserted, permits ALS interrupts to be generated. |
| WEN | 3 | Wait enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer. |
| Reserved | 2 | Reserved. Write as 0. |
| AEN | 1 | ALS Enable. Writing a 1 activates the ALS. Writing a 0 disables the ALS. |
| PON ⁽¹⁾ | 0 | Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator. |

Note(s):

1. A minimum interval of 2.72 ms must pass after PON is asserted before ALS can be initiated. This required time is enforced by the hardware in cases where the firmware does not provide it.

ALS Timing Register (0x01)

The ALS timing register controls the internal integration time of the ALS ADCs in 2.72-ms increments.

Figure 23:
ALS Timing Register

| Field | Bits | Description | | | |
|-------|------|-------------|--------------|---------|-----------|
| | | VALUE | INTEG_CYCLES | TIME | MAX COUNT |
| ATIME | 7:0 | 0xFF | 1 | 2.72 ms | 1024 |
| | | 0xF6 | 10 | 27.2 ms | 10240 |
| | | 0xDB | 37 | 101 ms | 37888 |
| | | 0xC0 | 64 | 174 ms | 65535 |
| | | 0x00 | 256 | 696 ms | 65535 |
| | | | | | |

Wait Time Register (0x03)

Wait time is set 2.72 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number.

Figure 24:
Wait Time Register

| Field | Bits | Description | | | |
|-------|------|----------------|-----------|------------------|------------------|
| | | REGISTER VALUE | WAIT TIME | TIME (WLONG = 0) | TIME (WLONG = 1) |
| WTIME | 7:0 | 0xFF | 1 | 2.72 ms | 0.032 s |
| | | 0xB6 | 74 | 201 ms | 2.4 s |
| | | 0x00 | 256 | 696 ms | 8.3 s |
| | | | | | |

Note(s):

1. The Wait Time Register should be configured before AEN is asserted.

ALS Interrupt Threshold Registers (0x04 - 0x07)

The ALS interrupt threshold registers provides the values to be used as the high and low trigger points for the comparison function for interrupt generation. If CODATA crosses below the low threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

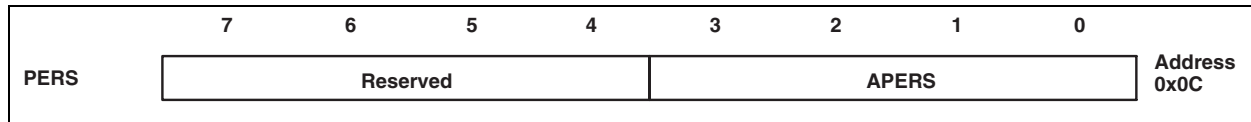
Figure 25:
ALS Interrupt Threshold Registers

| Register | Address | Bits | Description |
|----------|---------|------|-------------------------------|
| AILTL | 0x04 | 7:0 | ALS low threshold lower byte |
| AILTH | 0x05 | 7:0 | ALS low threshold upper byte |
| AIHTL | 0x06 | 7:0 | ALS high threshold lower byte |
| AIHTH | 0x07 | 7:0 | ALS high threshold upper byte |

Persistence Register (0x0C)

The persistence register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by threshold register for some specified amount of time. ALS interrupts are generated using CODATA.

Figure 26:
Persistence Register

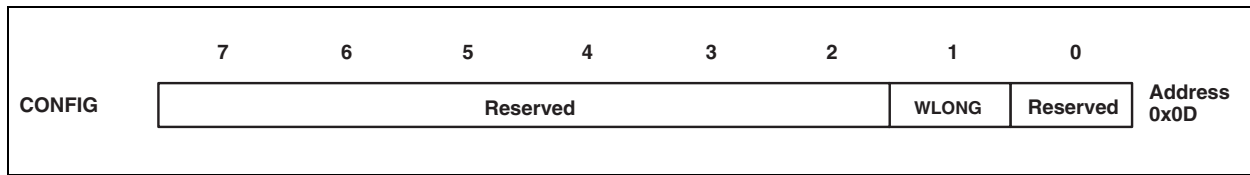


| Field | Bits | Description | | |
|----------|------|--|---------|--|
| Reserved | 7:4 | Reserved | | |
| APERS | 3:0 | Interrupt persistence. Controls rate of interrupt to the host processor. | | |
| | | FIELD VALUE | MEANING | INTERRUPT PERSISTENCE FUNCTION |
| | | 0000 | Every | Every ALS cycle generates an interrupt |
| | | 0001 | 1 | 1 value outside of threshold range |
| | | 0010 | 2 | 2 consecutive values out of range |
| | | 0011 | 3 | 3 consecutive values out of range |
| | | 0100 | 5 | 5 consecutive values out of range |
| | | 0101 | 10 | 10 consecutive values out of range |
| | | 0110 | 15 | 15 consecutive values out of range |
| | | 0111 | 20 | 20 consecutive values out of range |
| | | 1000 | 25 | 25 consecutive values out of range |
| | | 1001 | 30 | 30 consecutive values out of range |
| | | 1010 | 35 | 35 consecutive values out of range |
| | | 1011 | 40 | 40 consecutive values out of range |
| | | 1100 | 45 | 45 consecutive values out of range |
| | | 1101 | 50 | 50 consecutive values out of range |
| | | 1110 | 55 | 55 consecutive values out of range |
| 1111 | 60 | 60 consecutive values out of range | | |

Configuration Register (0x0D)

The configuration register sets the wait long time.

Figure 27:
Configuration Register

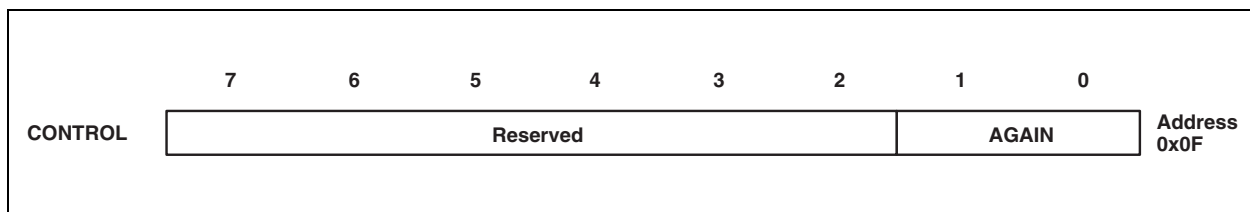


| Field | Bits | Description |
|----------|------|---|
| Reserved | 7:2 | Reserved. Write as 0. |
| WLONG | 1 | Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register. |
| Reserved | 0 | Reserved. Write as 0. |

Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

Figure 28:
Control Register

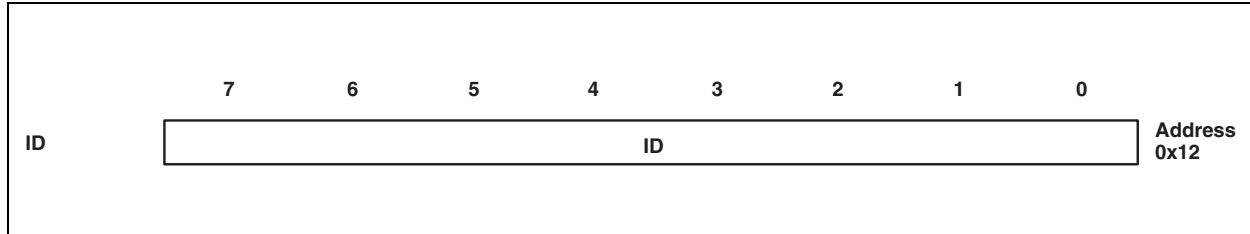


| Field | Bits | Description | |
|----------|------|---------------------------|-----------------------|
| Reserved | 7:2 | Reserved. Write bits as 0 | |
| AGAIN | 1:0 | ALS Gain Control. | |
| | | FIELD VALUE | ALS GAIN VALUE |
| | | 00 | 1× gain |
| | | 01 | 8× gain |
| | | 10 | 16× gain |
| | | 11 | 120× gain |

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

Figure 29:
ID Register

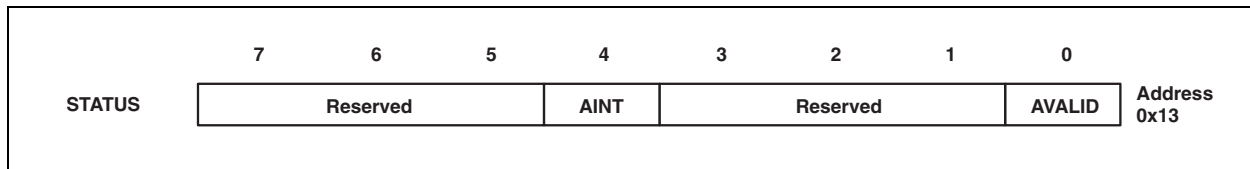


| Field | Bits | Description | |
|-------|------|----------------------------|------------------------------|
| ID | 7:0 | Part number identification | 0x04 = TSL25711 and TSL25715 |
| | | | 0x0D = TSL25713 |

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Figure 30:
Status Register



| Field | Bit | Description |
|----------|-----|---|
| Reserved | 7:5 | Reserved. Write as 0. |
| AINT | 4 | ALS Interrupt. Indicates that the device is asserting an ALS interrupt. |
| Reserved | 3:1 | Reserved. |
| AVALID | 0 | ALS Valid. Indicates that the ALS CH0 / CH1 channels have completed an integration cycle. |

ADC Channel Data Registers (0x14 - 0x17)

ALS data is stored as two 16-bit values. To ensure the data is read correctly, a two-byte read I²C transaction should be used with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored in a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Figure 31:
ADC Channel Data Registers

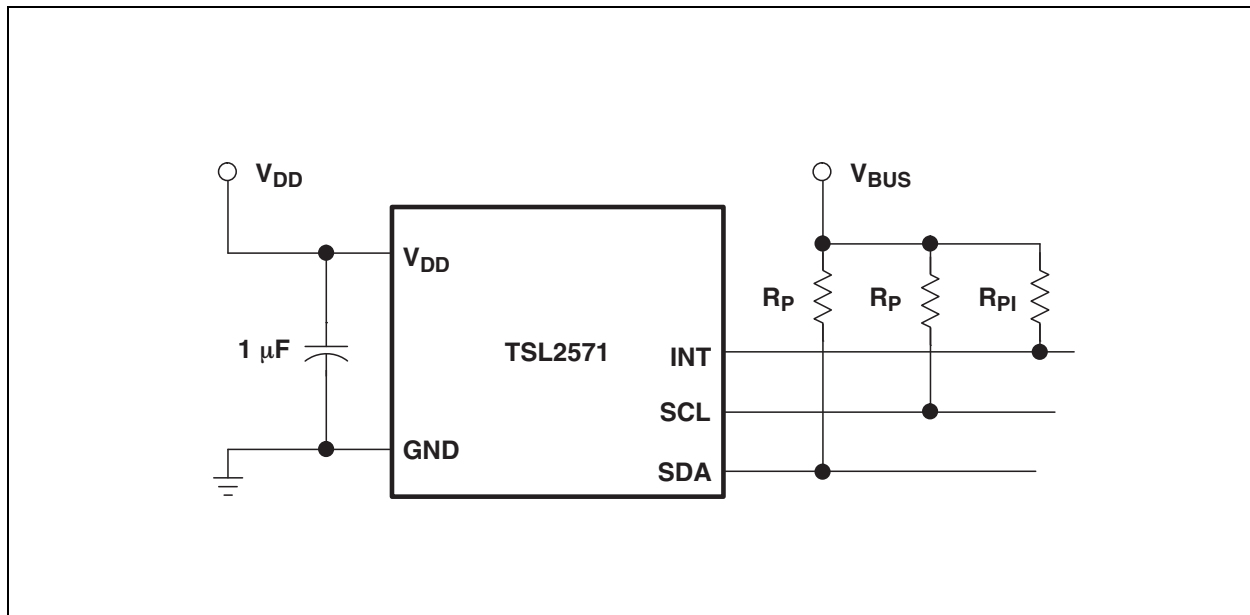
| Register | Address | Bits | Description |
|----------|---------|------|------------------------|
| C0DATA | 0x14 | 7:0 | ALS CH0 data low byte |
| C0DATAH | 0x15 | 7:0 | ALS CH0 data high byte |
| C1DATA | 0x16 | 7:0 | ALS CH1 data low byte |
| C1DATAH | 0x17 | 7:0 | ALS CH1 data high byte |

Application Information Hardware

Typical Hardware Application

A typical hardware application circuit is shown in [Figure 32](#). A 1- μF low-ESR decoupling capacitor should be placed as close as possible to the VDD pin.

Figure 32:
Typical Application Hardware Circuit



V_{BUS} in [Figure 32](#) refers to the I²C bus voltage, which is either V_{DD} or 1.8 V. Be sure to apply the specified I²C bus voltage shown in the Available Options table for the specific device being used.

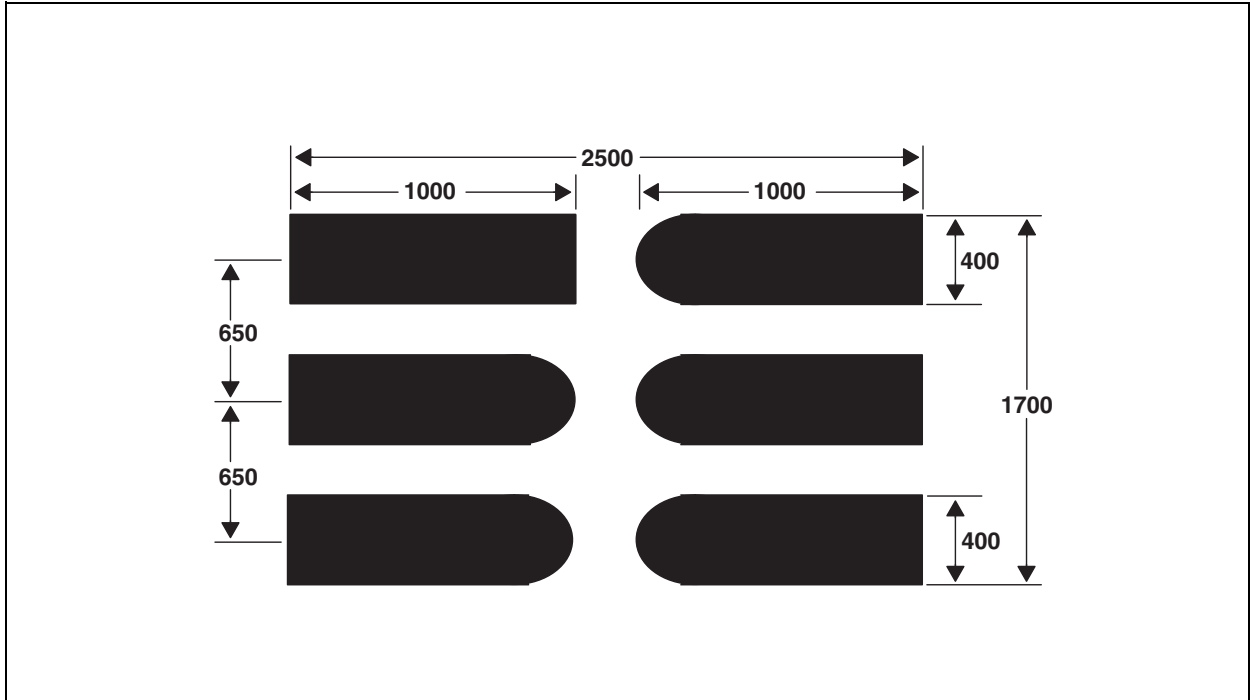
The I²C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (R_{p}) value is a function of the I²C bus speed, the I²C bus voltage, and the capacitive load. The **ams** EVM running at 400 kbps, uses 1.5-k Ω resistors. A 10-k Ω pull-up resistor (R_{PI}) can be used for the interrupt line.

PCB Pad Layout

Suggested PCB pad layout guidelines for the Dual Flat No-Lead (FN) surface mount package are shown in [Figure 33](#).

Note(s): Pads can be extended further if hand soldering is needed.

Figure 33:
Suggested FN Package PCB Layout

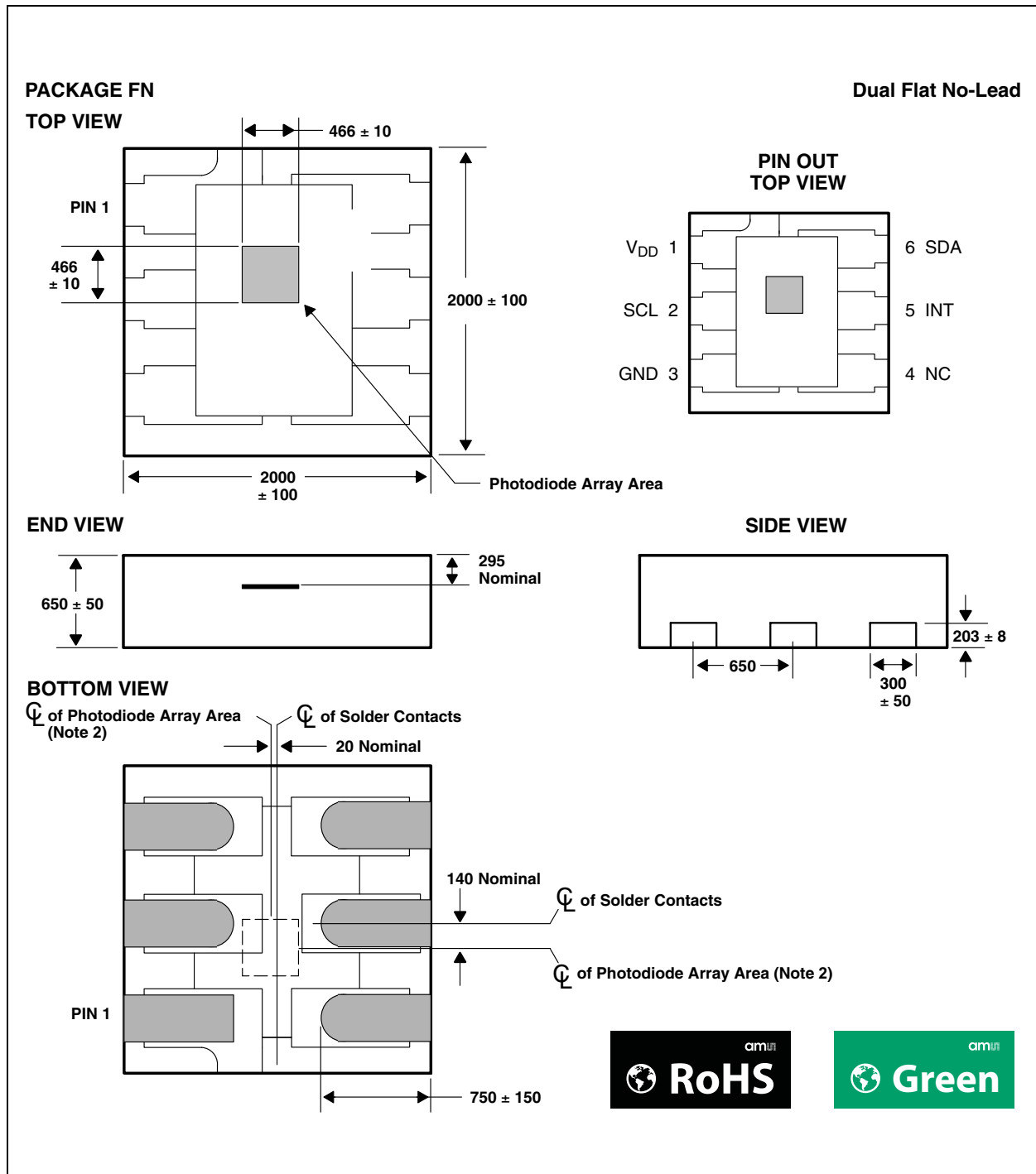


Note(s):

1. All linear dimensions are in micrometers.
2. This drawing is subject to change without notice.

Mechanical Data

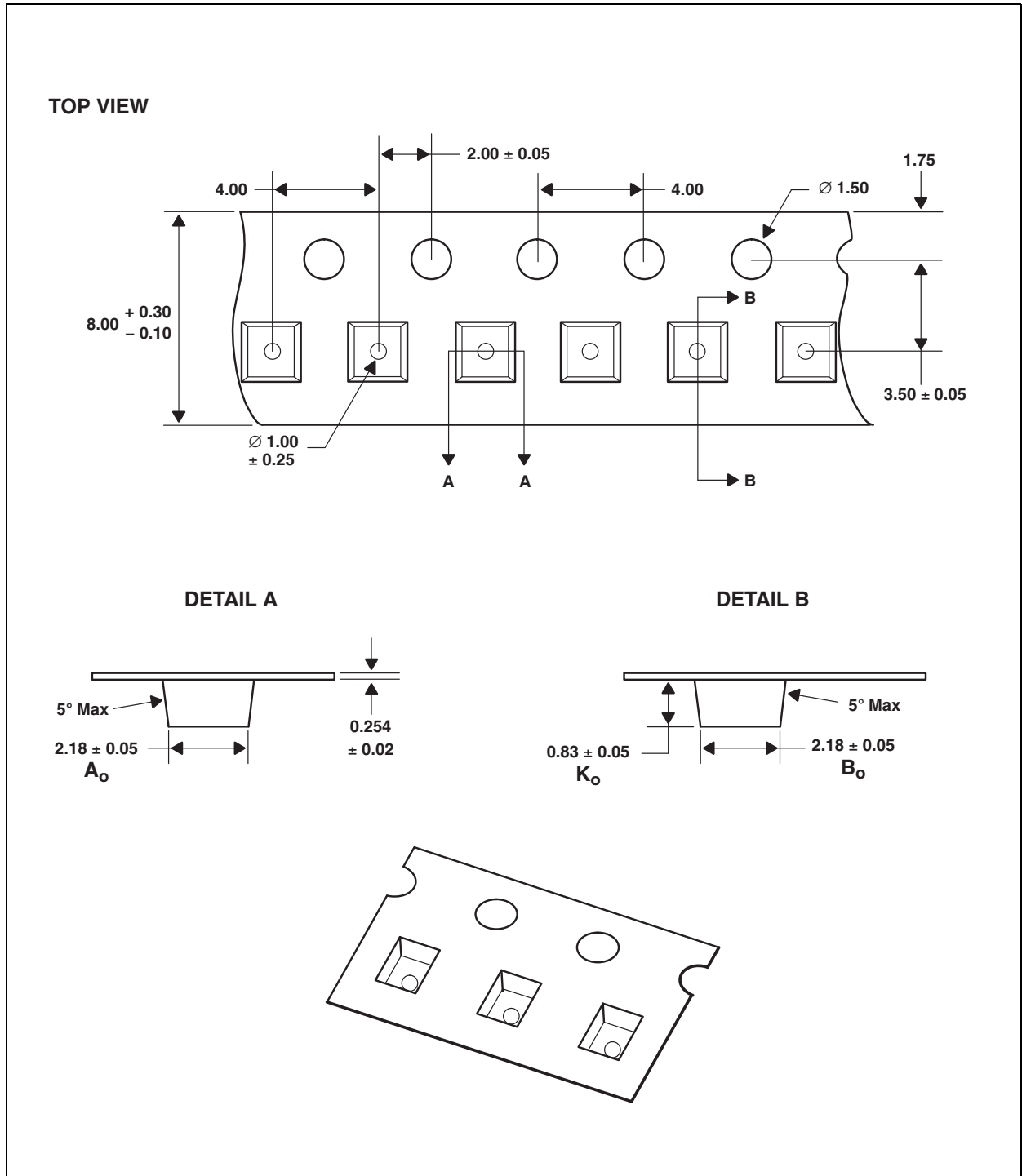
Figure 34:
Package FN — Dual Flat No-Lead Packaging Configuration



Note(s):

1. All linear dimensions are in micrometers. Dimension tolerance is $\pm 20\mu\text{m}$ unless otherwise noted.
2. The die is centered within the package within a tolerance of ± 3 mils.
3. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

Figure 35:
Package FN Carrier Tape



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_o , B_o , and K_o are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains 3500 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Manufacturing Information

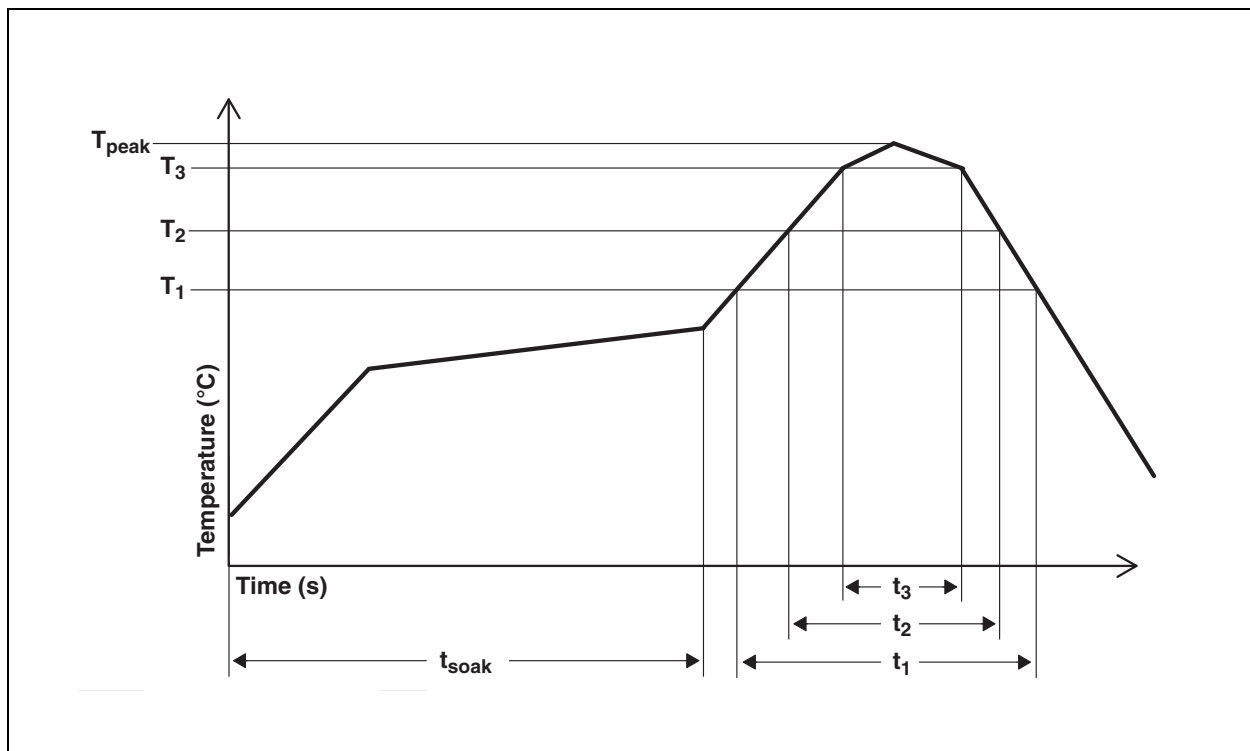
The FN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 36:
Solder Reflow Profile

| Parameter | Reference | Device |
|--|------------|--------------------------|
| Average temperature gradient in preheating | | 2.5°C/s |
| Soak time | t_{soak} | 2 to 3 minutes |
| Time above 217°C (T_1) | t_1 | Max 60 s |
| Time above 230°C (T_2) | t_2 | Max 50 s |
| Time above $T_{peak} - 10^\circ\text{C}$ (T_3) | t_3 | Max 10 s |
| Peak temperature in reflow | T_{peak} | 260°C |
| Temperature gradient in cooling | | Max -5°C/s |

Figure 37:
Solder Reflow Profile Graph



Note(s):

1. Not to scale - for reference only.

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping.

Devices are packed in a sealed aluminized envelope called a moisture barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The FN package has been assigned a moisture sensitivity level of MSL 3 and the devices should be stored under the following conditions:

- Temperature Range: 5°C to 50°C
- Relative Humidity: 60% maximum
- Total Time: 12 months from the date code on the aluminized envelope—if unopened
- Opened Time: 168 hours or fewer

Rebaking will be required if the devices have been stored unopened for more than 12 months or if the aluminized envelope has been open for more than 168 hours. If rebaking is required, it should be done at 50°C for 12 hours.

Ordering & Contact Information

Figure 38:
Ordering Information

| Ordering Code | Device | Address | Package - Leads | Interface Description |
|---------------|----------|---------|-----------------|---|
| TSL25711FN | TSL25711 | 0x39 | FN-6 | I ² C Vbus = V _{DD} Interface |
| TSL25713FN | TSL25713 | 0x39 | FN-6 | I ² C Vbus = 1.8 V Interface |
| TSL25715FN | TSL25715 | 0x29 | FN-6 | I ² C Vbus = V _{DD} Interface |

Buy our products or get free samples online at:

www.ams.com/ICdirect

Technical Support is available at:

www.ams.com/Technical-Support

Provide feedback about this document at:

www.ams.com/Document-Feedback

For further information and requests, e-mail us at:

ams_sales@ams.com

For sales offices, distributors and representatives, please visit:

www.ams.com/contact

Headquarters

ams AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe

Tel: +43 (0) 3136 500 0

Website: www.ams.com

RoHS Compliant & ams Green Statement

RoHS: The term RoHS compliant means that ams AG products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ams Green (RoHS compliant and no Sb/Br): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

Important Information: The information provided in this statement represents ams AG knowledge and belief as of the date that it is provided. ams AG bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. ams AG has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams AG and ams AG suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

Copyrights & Disclaimer

Copyright ams AG, Tobelbader Strasse 30, 8141 Premstaetten, Austria-Europe. Trademarks Registered. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

Devices sold by ams AG are covered by the warranty and patent indemnification provisions appearing in its General Terms of Trade. ams AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein. ams AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with ams AG for current information. This product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by ams AG for each application. This product is provided by ams AG "AS IS" and any express or implied warranties, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose are disclaimed.

ams AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of ams AG rendering of technical or other services.

Document Status

| Document Status | Product Status | Definition |
|--------------------------|-----------------|--|
| Product Preview | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice |
| Preliminary Datasheet | Pre-Production | Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice |
| Datasheet | Production | Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade |
| Datasheet (discontinued) | Discontinued | Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs |

Revision Information

| Changes from 1-00 (2016-May-26) to current revision 1-01 (2018-Mar-27) | Page |
|--|------|
| Updated Figure 7 | 6 |
| Updated Figure 29 | 25 |
| Updated Figure 38 | 33 |

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide

| | |
|-----------|---|
| 1 | General Description |
| 1 | Key Benefits & Features |
| 2 | Applications |
| 2 | Functional Block Diagram |
| 3 | Pin Assignments |
| 4 | Detailed Description |
| 5 | Absolute Maximum Ratings |
| 6 | Electrical Characteristics |
| 10 | Typical Characteristics |
| 12 | Principles of Operation |
| 12 | System State Machine |
| 13 | Photodiodes |
| 13 | ALS Operation |
| 14 | Lux Equation |
| 15 | Interrupts |
| 16 | State Diagram |
| 17 | I ² C Protocol |
| 18 | Register Description |
| 18 | Register Set |
| 19 | Command Register |
| 20 | Enable Register (0x00) |
| 21 | ALS Timing Register (0x01) |
| 21 | Wait Time Register (0x03) |
| 22 | ALS Interrupt Threshold Registers (0x04 - 0x07) |
| 23 | Persistence Register (0x0C) |
| 24 | Configuration Register (0x0D) |
| 24 | Control Register (0x0F) |
| 25 | ID Register (0x12) |
| 25 | Status Register (0x13) |
| 26 | ADC Channel Data Registers (0x14 - 0x17) |
| 27 | Application Information Hardware |
| 27 | Typical Hardware Application |
| 28 | PCB Pad Layout |
| 29 | Mechanical Data |
| 31 | Manufacturing Information |
| 32 | Moisture Sensitivity |
| 33 | Ordering & Contact Information |
| 34 | RoHS Compliant & ams Green Statement |
| 35 | Copyrights & Disclaimer |
| 36 | Document Status |
| 37 | Revision Information |

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ams:](#)

[TSL25715FN](#)