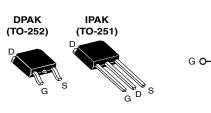
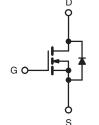


**Vishay Siliconix** 

## **Power MOSFET**

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	60					
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V 0.20					
Q <sub>g</sub> (Max.) (nC)	11					
Q <sub>gs</sub> (nC)	3.1					
Q <sub>gd</sub> (nC)	5.8					
Configuration	Single					





N-Channel MOSFET

#### **FEATURES**

- Dynamic dV/dt Rating
- Surface Mount (IRFR014, SiHFR014)
- Straight Lead (IRFU014, SiHFU014)
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



- And Reel HALOGEN
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

### DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION							
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)			
Lead (Pb)-free and Halogen-free	SiHFR014-GE3	SiHFR014TRL-GE3	SiHFR014TR-GE3	SIHFU014-GE3			
Lood (Db) free	IRFR014PbF	IRFR014TRLPbF <sup>a</sup>	IRFR014TRPbFa	IRFU014PbF			
Lead (Pb)-free	SiHFR014-E3	SiHFR014TL-E3 <sup>a</sup>	SiHFR014T-E3a	SiHFU014-E3			

#### Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub>	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V <sub>DS</sub>	60	N/	
Gate-Source Voltage			V <sub>GS</sub>	± 20	V	
Continuous Drain Current	1	7.7				
Continuous Drain Current	– I <sub>D</sub>	4.9	А			
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	31				
Linear Derating Factor			0.20	W/°C		
Linear Derating Factor (PCB Mount) <sup>e</sup>				0.020	W/ C	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	27.4	mJ	
Maximum Power Dissipation	D	25	W			
Maximum Power Dissipation (PCB Mount) <sup>e</sup>	P <sub>D</sub>	2.5	vv			
Peak Diode Recovery dV/dtc	dV/dt	4.5	V/ns			
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C			
Soldering Recommendations (Peak Temperature) <sup>d</sup>		260	-0			

#### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

- b.  $V_{DD}$  = 25 V, starting T<sub>J</sub> = 25 °C, L = 924 µH, R<sub>g</sub> = 25  $\Omega$ , I<sub>AS</sub> = 7.7 A (see fig. 12).
- c.  $I_{SD} \le 10$  A, dl/dt  $\le 90$  A/µs,  $V_{DD} \le V_{DS}$ ,  $T_J \le 150$  °C.

d. 1.6 mm from case.

e. When mounted on 1" square PCB (FR-4 or G-10 material).



Vishay Siliconix

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	-	110			
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	R <sub>thJA</sub>	-	-	50	°C/W		
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	-	5.0			

#### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static		·					•
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> =	= 0 V, I <sub>D</sub> = 250 μA	60	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_J$	Referenc	e to 25 °C, I <sub>D</sub> = 1 mA	-	0.068	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	- V <sub>GS</sub> , I <sub>D</sub> = 250 μΑ	2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	,	$V_{GS} = \pm 20 V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>		= 60 V, V <sub>GS</sub> = 0 V	-	-	25	μA
	200		V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	250	ſ
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 V$			-	0.20	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> :	= 25 V, I <sub>D</sub> = 4.6 A	2.4	-	-	S
Dynamic		_				-	
Input Capacitance	Ciss		$V_{GS} = 0 V$ ,	-	300	-	
Output Capacitance	C <sub>oss</sub>	]	$V_{DS} = 25 V$ ,	-	160	-	pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1.	0 MHz, see fig. 5	-	29	-	
Total Gate Charge	Qg			-	-	11	
Gate-Source Charge	Q <sub>gs</sub>	$V_{GS} = 10 V$	$I_D = 10 \text{ A}, V_{DS} = 48 \text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	-	3.1	nC
Gate-Drain Charge	Q <sub>gd</sub>	1		-	-	5.8	
Turn-On Delay Time	t <sub>d(on)</sub>			-	10	-	
Rise Time	t <sub>r</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 10 A,		-	50	-	]
Turn-Off Delay Time	t <sub>d(off)</sub>	$R_g = 24 \Omega$ ,	$R_D = 2.7 \Omega$ , see fig. $10^{b}$	-	13	-	ns
Fall Time	t <sub>f</sub>	1		-	19	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead 6 mm (0.25") 1	from	-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>	package and die contact <sup>c</sup>	center of	-	7.5	-	
Drain-Source Body Diode Characteristic	S						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET sym showing the	bol	-	-	7.7	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>	integral revers p - n junction	÷ ===/	-	-	31	
Body Diode Voltage	$V_{SD}$	T <sub>J</sub> = 25 °C	, $I_{\rm S}$ = 7.7 A, $V_{\rm GS}$ = 0 V <sup>b</sup>	-	-	1.6	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T _ 05 °O L	- 10 A dl/dt 100 A/a-b	-	70	140	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	$I_{\rm J} = 25  {}^{-}{\rm C},  I_{\rm F}$	= 10 A, dl/dt = 100 A/µs <sup>b</sup>	-	0.20	0.40	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic tu	rn-on time is negligible (turn	-on is dor	ninated b	v Ls and	Ln)

#### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width  $\leq 300~\mu s;$  duty cycle  $\leq 2~\%.$ 



Vishay Siliconix

### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

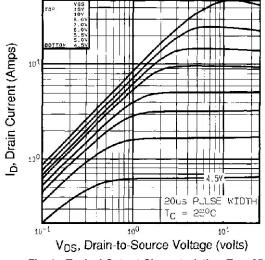


Fig. 1 - Typical Output Characteristics,  $T_C = 25 \ ^{\circ}C$ 

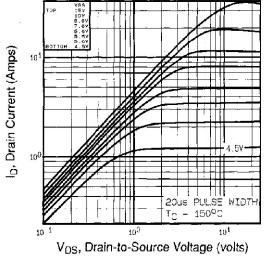


Fig. 2 - Typical Output Characteristics, T<sub>C</sub> = 150 °C

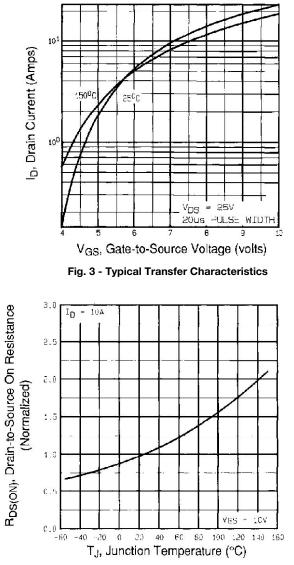


Fig. 4 - Normalized On-Resistance vs. Temperature

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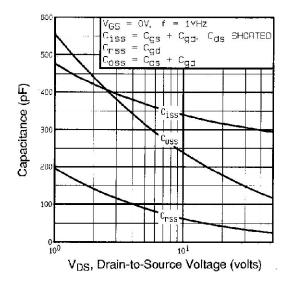
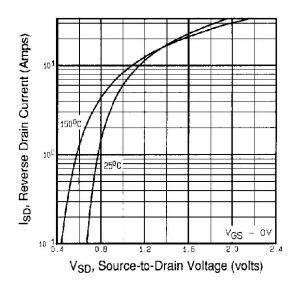
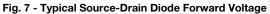


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage





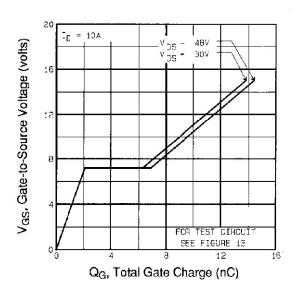


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

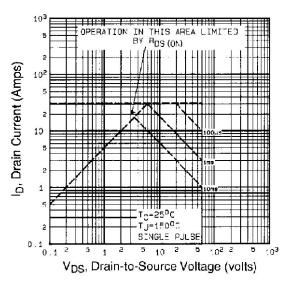
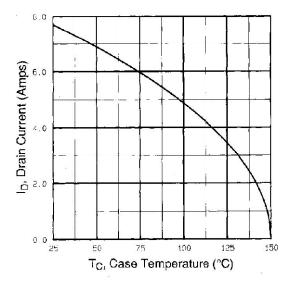


Fig. 8 - Maximum Safe Operating Area



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#### Fig. 9 - Maximum Drain Current vs. Case Temperature

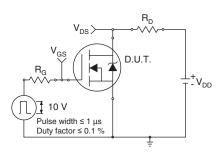


Fig. 10a - Switching Time Test Circuit

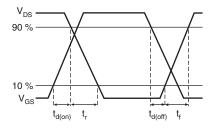


Fig. 10b - Switching Time Waveforms

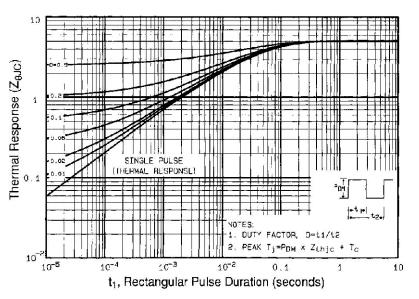


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



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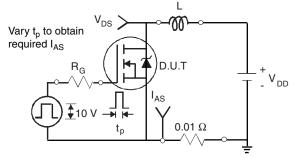


Fig. 12a - Unclamped Inductive Test Circuit

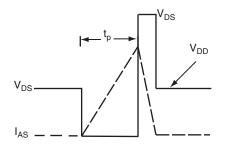


Fig. 12b - Unclamped Inductive Waveforms

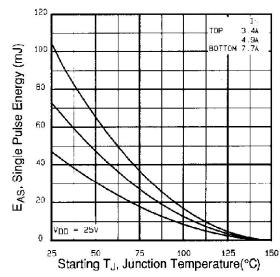


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

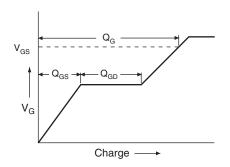
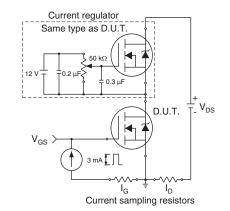


Fig. 13a - Basic Gate Charge Waveform



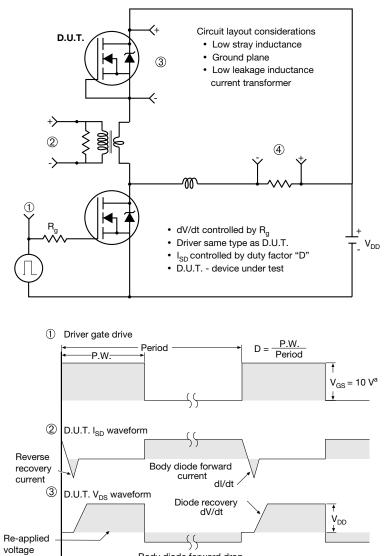


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#### Peak Diode Recovery dV/dt Test Circuit



Inductor current

Note

4

a.  $V_{GS} = 5$  V for logic level devices

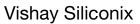
Fig. 14 - For N-Channel

 $I_{SD}$ 

Body diode forward drop

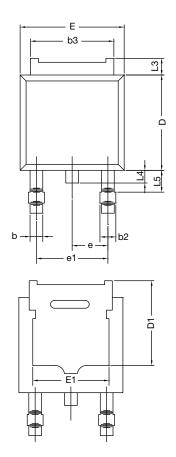
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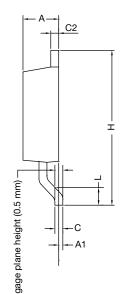
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**TO-252AA Case Outline** 





	MILLIN	IETERS	INCHES			
DIM.	MIN.	MAX.	MIN.	MAX.		
А	2.18	2.38	0.086	0.094		
A1	-	0.127	-	0.005		
b	0.64	0.88	0.025	0.035		
b2	0.76	1.14	0.030	0.045		
b3	4.95	5.46	0.195	0.215		
С	0.46	0.61	0.018	0.024		
C2	0.46	0.89	0.018	0.035		
D	5.97	6.22	0.235	0.245		
D1	4.10	-	0.161	-		
Е	6.35	6.73	0.250	0.265		
E1	4.32	-	0.170	-		
Н	9.40	10.41	0.370	0.410		
е	2.28	BSC	0.090	BSC		
e1	4.56	BSC	0.180 BSC			
L	1.40	1.78	0.055	0.070		
L3	0.89	1.27	0.035	0.050		
L4	-	1.02	-	0.040		
L5	1.01	1.52	0.040	0.060		
ECN: T16- DWG: 534	0236-Rev. P, <sup>•</sup> 7	16-May-16				

Notes

• Dimension L3 is for reference only.



**Vishay Siliconix** 

### **TO-251AA (HIGH VOLTAGE)**



	MILLI	METERS	INC	HES		MILLI	METERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.	DIM.	MIN.	MAX.	MIN.	MA
А	2.18	2.39	0.086	0.094	D1	5.21	-	0.205	-
A1	0.89	1.14	0.035	0.045	E	6.35	6.73	0.250	0.2
b	0.64	0.89	0.025	0.035	E1	4.32	-	0.170	-
b1	0.65	0.79	0.026	0.031	е	2.29	BSC	2.29	BSC
b2	0.76	1.14	0.030	0.045	L	8.89	9.65	0.350	0.3
b3	0.76	1.04	0.030	0.041	L1	1.91	2.29	0.075	0.0
b4	4.95	5.46	0.195	0.215	L2	0.89	1.27	0.035	0.0
с	0.46	0.61	0.018	0.024	L3	1.14	1.52	0.045	0.0
c1	0.41	0.56	0.016	0.022	θ1	0'	15'	0'	15
c2	0.46	0.86	0.018	0.034	θ2	25'	35'	25'	35
D	5.97	6.22	0.235	0.245		•	•	•	

#### Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimension are shown in inches and millimeters.
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
- 4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
- 5. Lead dimension uncontrolled in L3.
- 6. Dimension b1, b3 and c1 apply to base metal only.
- 7. Outline conforms to JEDEC outline TO-251AA.



Vishay Siliconix

### **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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