

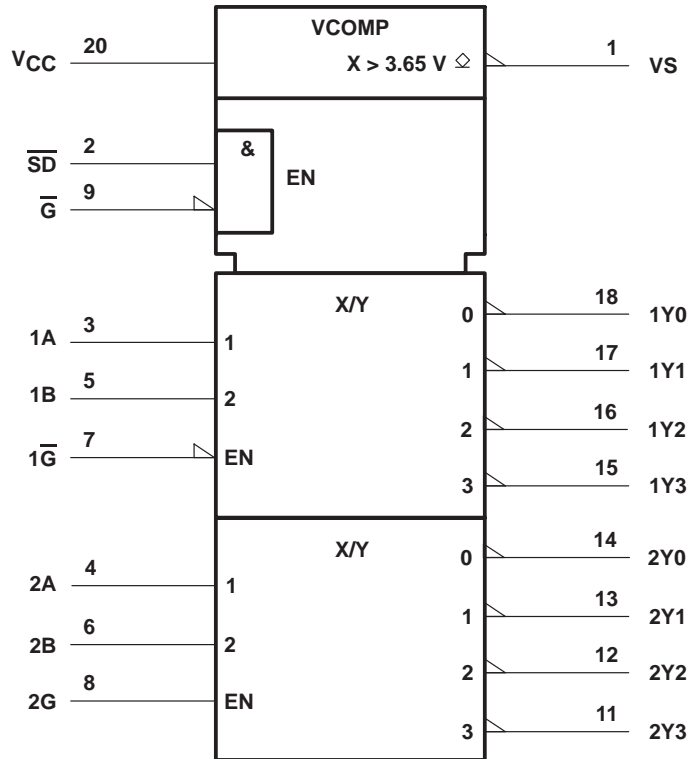
SN74BCT2414

MEMORY DECODER

WITH ON-CHIP SUPPLY VOLTAGE MONITOR

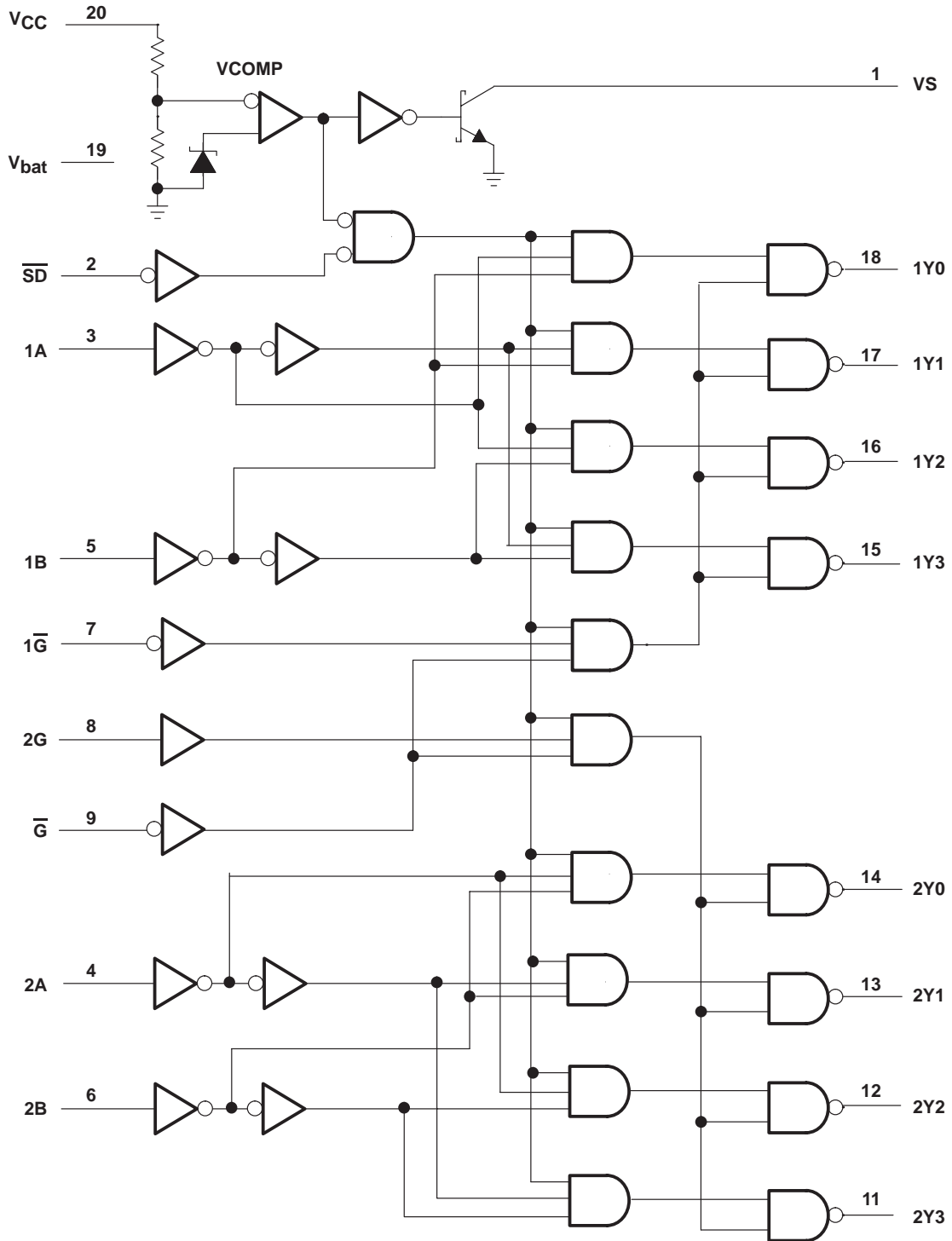
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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FUNCTION TABLES

INPUTS					OUTPUTS			
CONTROL			SELECT					
\overline{G}	$1\overline{G}$	\overline{SD}	1B	1A	1Y0	1Y1	1Y2	1Y3
H	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	L	X	X	H	H	H	H
L	L	H	L	L	L	H	H	H
L	L	H	L	H	H	L	H	H
L	L	H	H	L	H	H	L	H
L	L	H	H	H	H	H	H	L

INPUTS					OUTPUTS			
CONTROL			SELECT					
\overline{G}	2G	\overline{SD}	2B	2A	2Y0	2Y1	2Y2	2Y3
H	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	L	X	X	H	H	H	H
L	H	H	L	L	L	H	H	H
L	H	H	L	H	H	L	H	H
L	H	H	H	L	H	H	L	H
L	H	H	H	H	H	H	H	L

NOTE: For a 3-line to 8-line decoder, the following pins must be shorted: $1\overline{G}$ to 2G, 1A to 2A and 1B to 2B.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{bat}	-0.5 V to 7 V
Supply voltage range, V_{CC}	-0.5 V to 7 V
Supply voltage V_{CC} with respect to V_{bat}	-1.5 V
Input voltage range, V_I	-0.5 V to $V_{CC} + 0.5$ V
Off-state output voltage range at V_S	-0.5 V to 7 V
Voltage range applied to any Y output in the power-off state	-0.5 V to 7 V
Voltage applied to any Y output in the power-off state with respect to V_{bat}	0.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{bat}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	μ A
I_{OL}	Low-level output current	Y outputs		8	mA
		VS outputs		20	
t_t	Input transition time	0		10	ns/V
T_A	Operating free-air temperature	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.2	V	
V_{OH}		$V_{bat} = V_{CC} = 4.5$ V	$I_{OH} = -20$ μ A	4.4			V	
			$I_{OH} = -400$ μ A	3.5				
		$V_{bat} = 2$ V, $V_{CC} = 0$,	$I_{OH} = -50$ μ A	1.8				
V_{OL}	All except VS	$V_{bat} = V_{CC} = 4.5$ V	$I_{OL} = 4$ mA			0.4	V	
			$I_{OL} = 8$ mA			0.5		
	VS	$V_{bat} = V_{CC} = 4.5$ V,	$I_{OL} = 20$ mA			1		
V_T^{\ddagger}					3.65		V	
I_I		$V_{bat} = V_{CC} = 5.5$ V,	$V_I = 5.5$ V			100	μ A	
I_{IH}		$V_{bat} = V_{CC} = 5.5$ V,	$V_I = 2.7$ V			± 20	μ A	
I_{IL}		$V_{bat} = V_{CC} = 5.5$ V,	$V_I = 0.5$ V			± 20	μ A	
I_{OH}	VS	$V_{bat} = 4.5$ V,	$V_{CC} = 0$			1	μ A	
I_O^{\S}		$V_{bat} = V_{CC} = 5.5$ V,	$V_O = 2.25$ V	-30		-200	mA	
I_{CC}		$V_{bat} = V_{CC} = 5.5$ V	Outputs high			3	mA	
			Outputs low			3		
I_{bat}		$V_{bat} = 2.5$ V,	$V_{CC} = 0$		1	10	μ A	
							20	
	$V_{bat} = V_{CC} = 5.5$ V	Outputs high					3	mA
		Outputs low						
C_i		$V_{bat} = V_{CC} = 5$ V,	$V_I = 0$ or 3 V			4	pF	
C_o	Any Y	$V_{bat} = V_{CC} = 0$				6.5	pF	
	VS					5		

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^{\circ}$ C.

‡ This value represents the V_{CC} monitor threshold voltage. Typical range is from 3.5 V to 3.8 V.

§ This output condition has been chosen to produce a current that closely approximates one half of the short-circuit output current, I_{OS} . Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	A or B	Any Y	1	5	10	1	12	ns
t _{PHL}			2	5.8	10	2	12	
t _{PLH}	Any \overline{G}	Any Y	1	4.5	9	1	10	ns
t _{PHL}			2	5.5	9	2	11	
t _{PLH}	\overline{SD}	Any Y	2	6.5	11	2	12	ns
t _{PHL}			2	6.5	11	2	12	

switching characteristics (see Note 1)

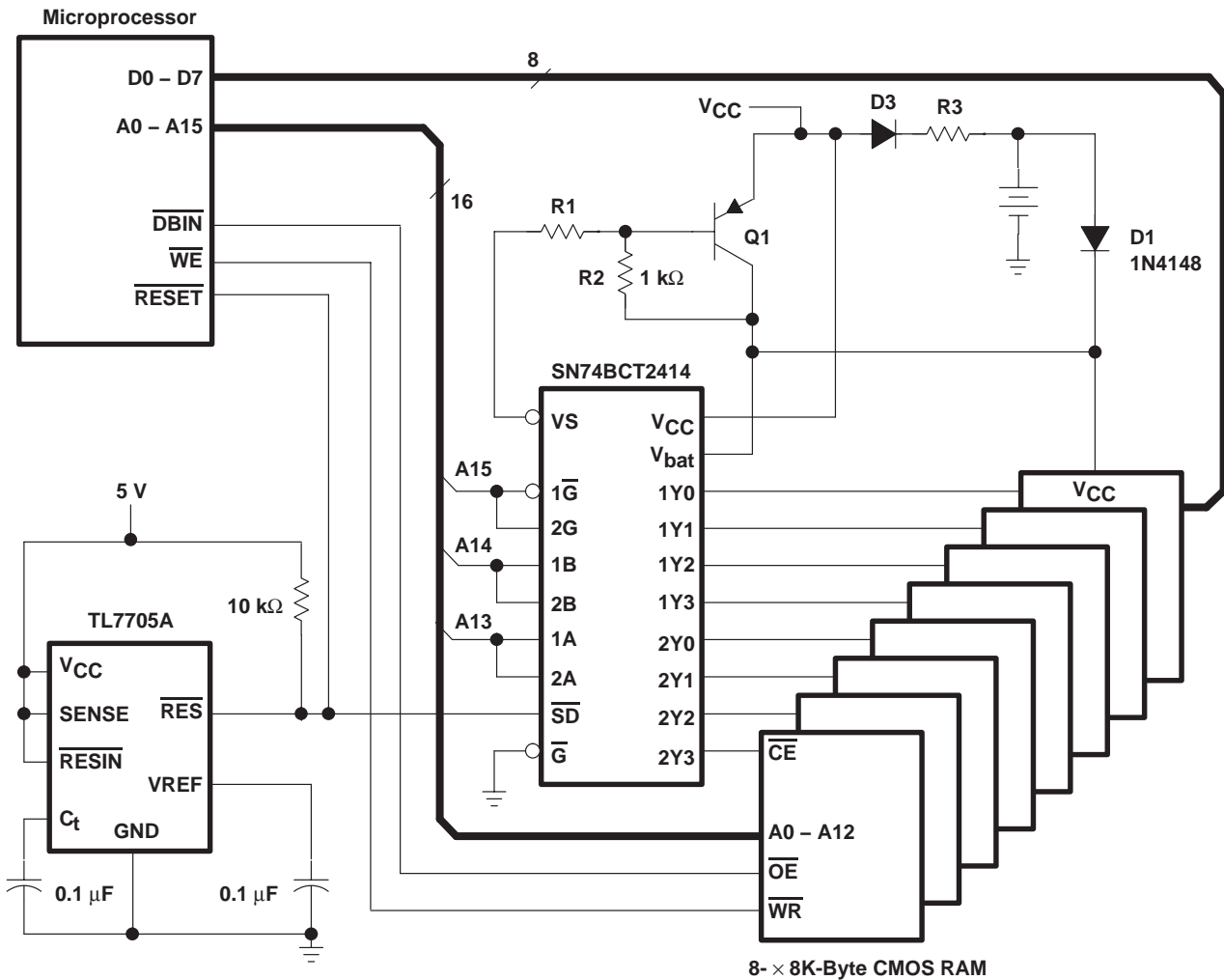
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	V _{CC}	Any Y	10	25	50	10	250	ns
t _{PHL}			15	45	100	15	250	
t _{PLH}	V _{CC}	VS	10	28	50	10	250	ns
t _{PHL}			20	50	100	20	250	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

APPLICATION INFORMATION

A typical application circuit for a battery-buffered memory in a microcomputer system is shown in Figure 1 which uses the SN74BCT2414. When power fails, the supply-voltage supervisor (TL7705) resets the microcomputer and disables the memory by switching the shutdown input \overline{SD} of the memory decoder to a logic zero. All memory decoder outputs are forced to a logic one. Abnormal write commands from the microprocessor, which may be issued during further voltage breakdown, no longer affect the contents of the memory. When the system supply voltage becomes lower than approximately 3.65 V, the voltage monitor inside the SN74BCT2414 memory decoder disconnects the input buffers of this circuit from the decoding logic internally and keeps all outputs at a logic one. The VS output is also switched off, disconnecting the system supply voltage from the memory circuits. During this low-voltage condition, the memory decoder and the memory circuits are supplied by the battery.



For further information on this device, please contact factory.

Figure 1. Memory System With Battery Backup

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74BCT2414DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT2414	Samples
SN74BCT2414N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	SN74BCT2414N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



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NOTES:

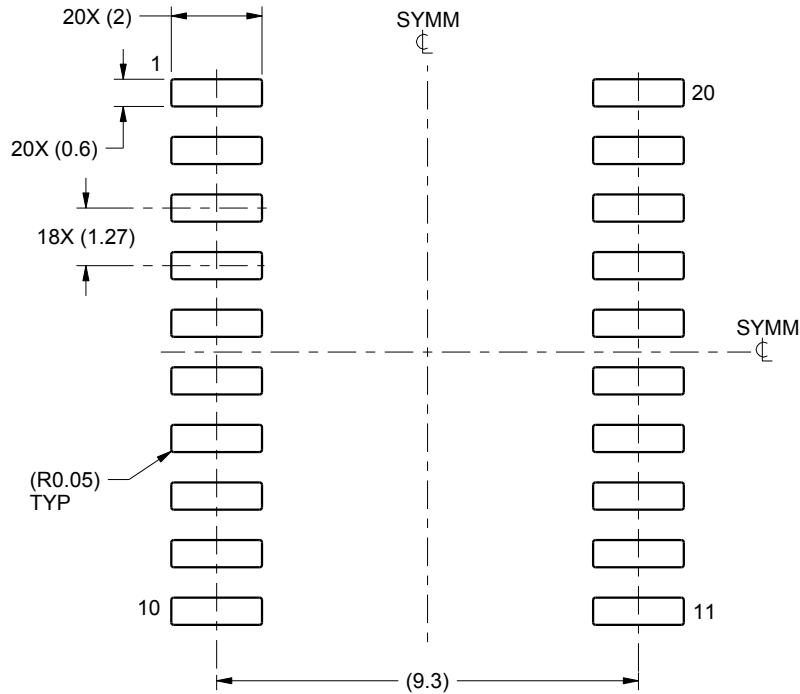
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

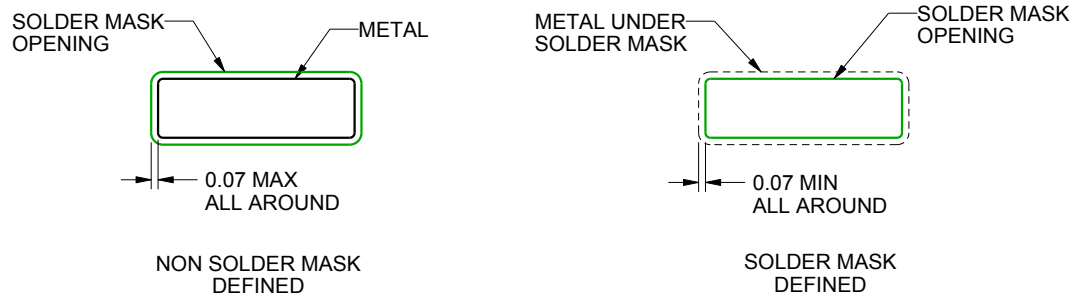
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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