



## Dual N-Channel 30 V (D-S) MOSFETs

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
Channel-1	30	0.0240 at V <sub>GS</sub> = 10 V	11	3.5 nC
		0.0320 at V <sub>GS</sub> = 4.5 V	11	
Channel-2	30	0.0110 at V <sub>GS</sub> = 10 V	28	6.8 nC
		0.0165 at V <sub>GS</sub> = 4.5 V	28	

### FEATURES

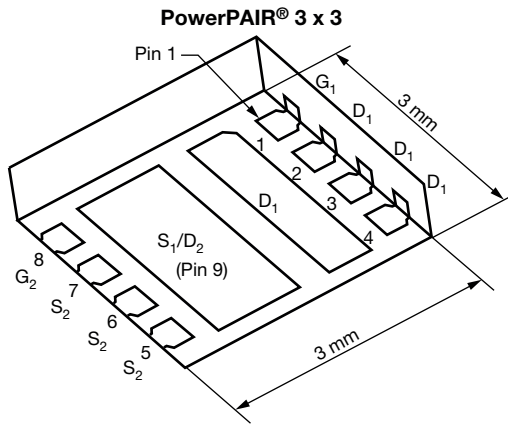
- PowerPAIR Optimizes High-Side and Low-Side MOSFETs for Synchronous Buck Converters
- TrenchFET<sup>®</sup> Power Mosfets
- 100 % R<sub>g</sub> and UIS Tested
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



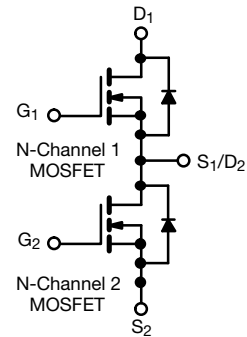
RoHS  
COMPLIANT  
HALOGEN  
FREE

### APPLICATIONS

- Computing System Power
- POL
- Synchronous Buck Converter



**Ordering Information:**  
SiZ300DT-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
Parameter	Symbol	Channel-1	Channel-2	Unit	
Drain-Source Voltage	V <sub>DS</sub>	30		V	
Gate-Source Voltage	V <sub>GS</sub>	± 20			
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	11 <sup>a</sup>	28 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	11 <sup>a</sup>	28 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	9.8 <sup>b, c</sup>	14.9 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	7.8 <sup>b, c</sup>	11.9 <sup>b, c</sup>	
Pulsed Drain Current (t = 300 μs)	I <sub>DM</sub>	30	40		
Continuous Source Drain Diode Current	I <sub>S</sub>	T <sub>A</sub> = 25 °C	11 <sup>a</sup>	26	
		T <sub>A</sub> = 25 °C	3.2 <sup>b, c</sup>	3.8 <sup>b, c</sup>	
Avalanche Current	I <sub>AS</sub>	12	15		
Single Pulse Avalanche Energy	E <sub>AS</sub>	7	11	mJ	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	16.7	31	W
		T <sub>C</sub> = 70 °C	10.7	20	
		T <sub>A</sub> = 25 °C	3.7 <sup>b, c</sup>	4.2 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	2.4 <sup>b, c</sup>	2.7 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260			

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Channel-1		Channel-2		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>a, b</sup>	$t \leq 10$ s	$R_{thJA}$	27	34	24	30	°C/W
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	6	7.5	3.2	4	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under steady state conditions is 69 °C/W for channel-1 and 64 °C/W for channel-2.

SPECIFICATIONS ( $T_J = 25$ °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250 \mu A$	Ch-1	30			V
		$V_{GS} = 0 V, I_D = 250 \mu A$	Ch-2	30			
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu A$	Ch-1		24		mV/°C
		$I_D = 250 \mu A$	Ch-2		30		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu A$	Ch-1		- 4.1		
		$I_D = 250 \mu A$	Ch-2		- 5		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	Ch-1	1		2.4	V
		$V_{DS} = V_{GS}, I_D = 250 \mu A$	Ch-2	1		2.2	
Gate Source Leakage	$I_{GSS}$	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	Ch-1			$\pm 100$	nA
			Ch-2			$\pm 100$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30 V, V_{GS} = 0 V$	Ch-1			1	$\mu A$
		$V_{DS} = 30 V, V_{GS} = 0 V$	Ch-2			1	
		$V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55$ °C	Ch-1			5	
		$V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55$ °C	Ch-2			5	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5 V, V_{GS} = 10 V$	Ch-1	10			A
		$V_{DS} \geq 5 V, V_{GS} = 10 V$	Ch-2	10			
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10 V, I_D = 9.8 A$	Ch-1		0.0200	0.0240	$\Omega$
		$V_{GS} = 10 V, I_D = 15 A$	Ch-2		0.0090	0.0110	
		$V_{GS} = 4.5 V, I_D = 8.5 A$	Ch-1		0.0265	0.0320	
		$V_{GS} = 4.5 V, I_D = 12 A$	Ch-2		0.0135	0.0165	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15 V, I_D = 9.8 A$	Ch-1		30		S
		$V_{DS} = 15 V, I_D = 15 A$	Ch-2		30		
<b>Dynamic<sup>a</sup></b>							
Input Capacitance	$C_{iss}$	Channel-1 $V_{DS} = 15 V, V_{GS} = 0 V, f = 1$ MHz	Ch-1		400		pF
			Ch-2		730		
Output Capacitance	$C_{oss}$	Channel-2 $V_{DS} = 15 V, V_{GS} = 0 V, f = 1$ MHz	Ch-1		125		
			Ch-2		155		
Reverse Transfer Capacitance	$C_{rss}$		Ch-1		25		
			Ch-2		65		
Total Gate Charge	$Q_g$	$V_{DS} = 15 V, V_{GS} = 10 V, I_D = 9.8 A$	Ch-1		7.4	12	nC
		$V_{DS} = 15 V, V_{GS} = 10 V, I_D = 15 A$	Ch-2		14.2	22	
		Channel-1 $V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 9.8 A$	Ch-1		3.5	5.3	
			Ch-2		6.8	11	
Gate-Source Charge	$Q_{gs}$	Channel-2 $V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 15 A$	Ch-1		1.5		
			Ch-2		2.2		
Gate-Drain Charge	$Q_{gd}$		Ch-1		1.1		
			Ch-2		2.3		
Gate Resistance	$R_g$	$f = 1$ MHz	Ch-1	0.5	2.6	5.2	$\Omega$
			Ch-2	0.5	2.6	5.2	

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width  $\leq 300 \mu s$ , duty cycle  $\leq 2\%$ .



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
<b>Dynamic<sup>a</sup></b>								
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.9\ \Omega$ $I_D \cong 8\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		25	50	ns	
			Ch-2		25	50		
Rise Time	$t_r$		Ch-1		45	90		
			Ch-2		80	160		
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		10	20		
			Ch-2		20	40		
Fall Time	$t_f$		Ch-1		10	20		
			Ch-2		40	80		
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.9\ \Omega$ $I_D \cong 8\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		5	10		
			Ch-2		5	10		
Rise Time	$t_r$		Ch-1		10	20		
			Ch-2		20	40		
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		10	20		
			Ch-2		15	30		
Fall Time	$t_f$		Ch-1		7	15		
			Ch-2		10	20		
<b>Drain-Source Body Diode Characteristics</b>								
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			11	A	
			Ch-2					26
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		Ch-1			30		
			Ch-2					40
Body Diode Voltage	$V_{SD}$	$I_S = 8\text{ A}$ , $V_{GS} = 0\text{ V}$	Ch-1		0.84	1.2	V	
		$I_S = 10\text{ A}$ , $V_{GS} = 0\text{ V}$	Ch-2		0.82	1.2		
Body Diode Reverse Recovery Time	$t_{rr}$	Channel-1 $I_F = 8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		17	35	ns	
			Ch-2		20	40		
Body Diode Reverse Recovery Charge	$Q_{rr}$			Ch-1		9	20	nC
				Ch-2		14	30	
Reverse Recovery Fall Time	$t_a$	Channel-2 $I_F = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		9.5		ns	
			Ch-2		12.5			
Reverse Recovery Rise Time	$t_b$			Ch-1		7.5		
				Ch-2		7.5		

## Notes:

- a. Guaranteed by design, not subject to production testing.  
 b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

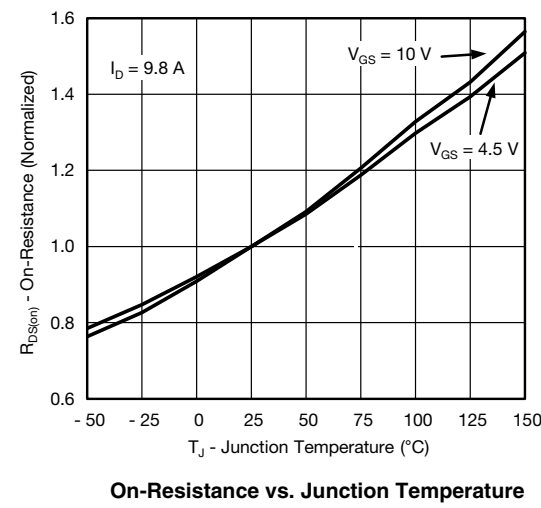
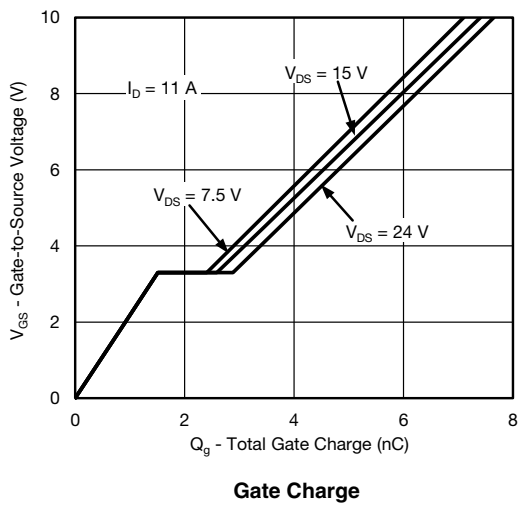
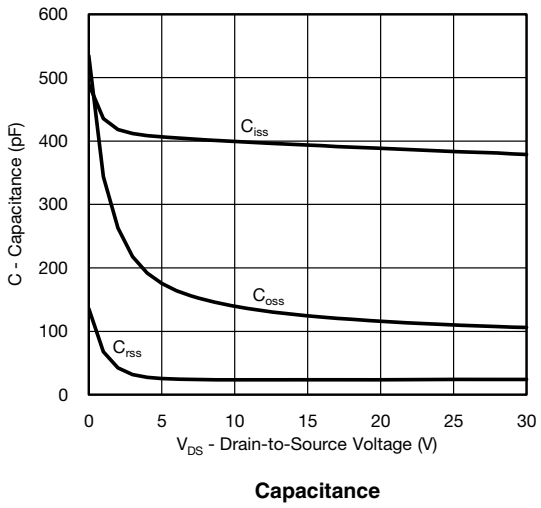
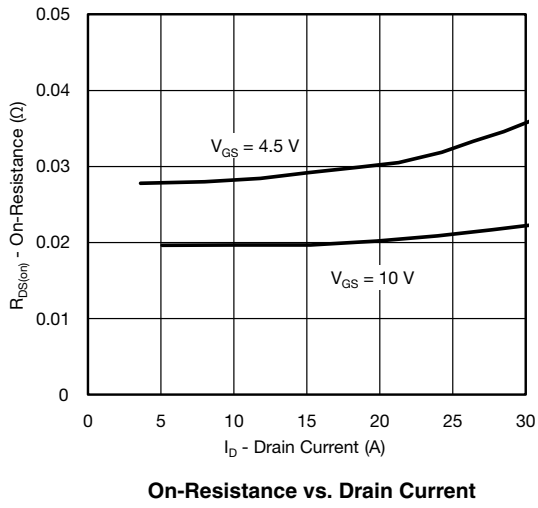
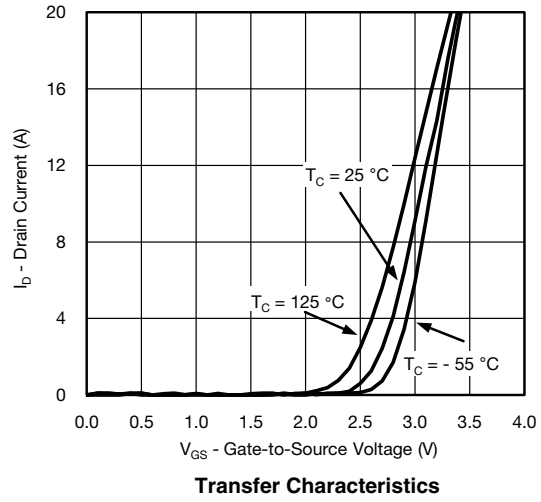
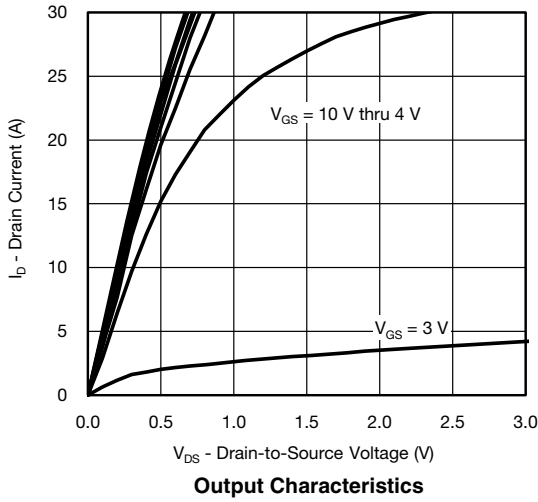
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# SiZ300DT

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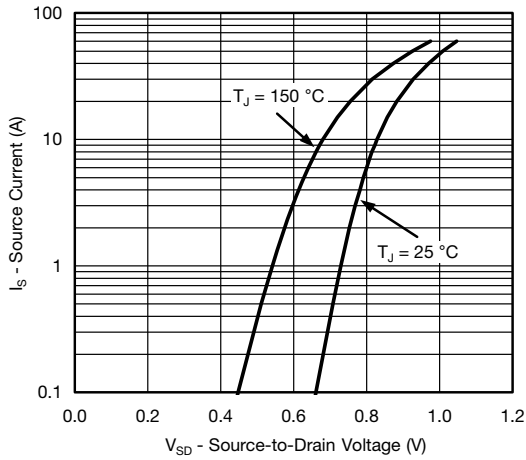


## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

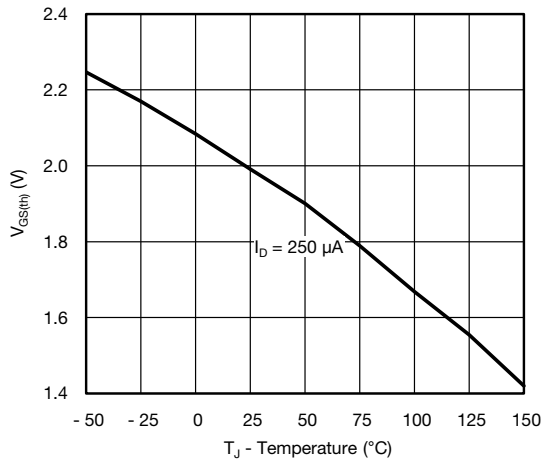




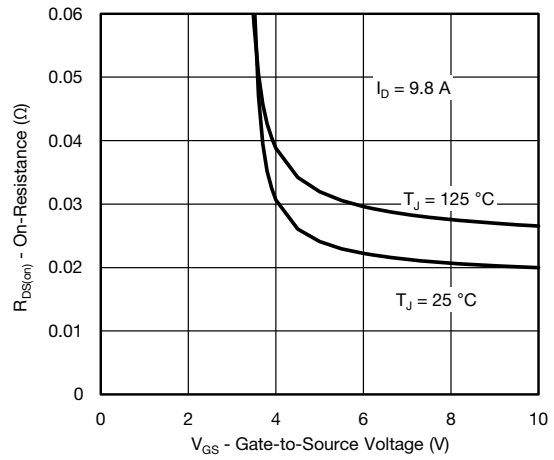
**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



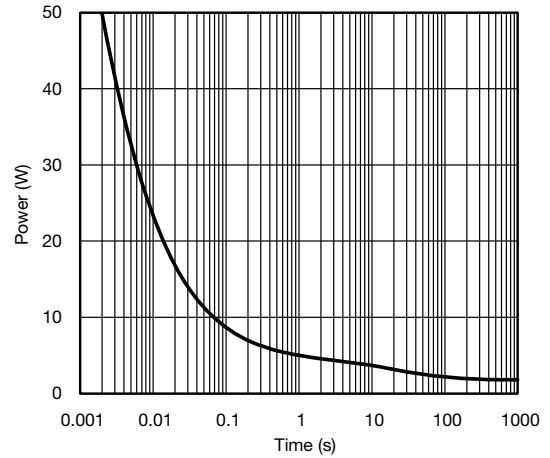
**Source-Drain Diode Forward Voltage**



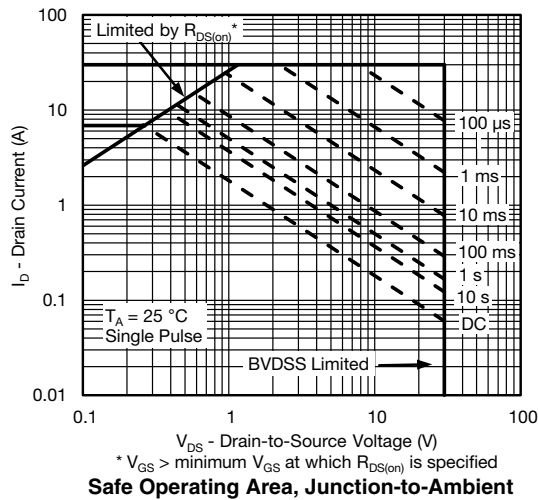
**Threshold Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



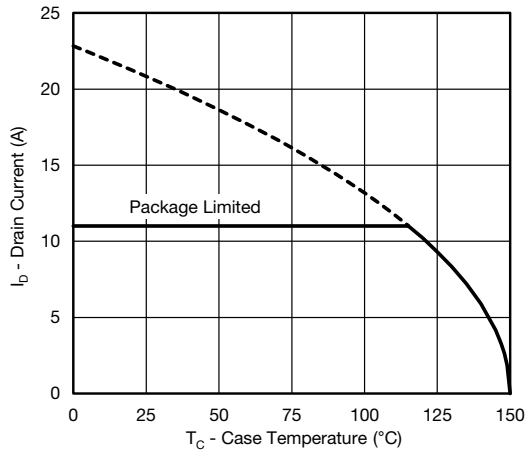
**Single Pulse Power**



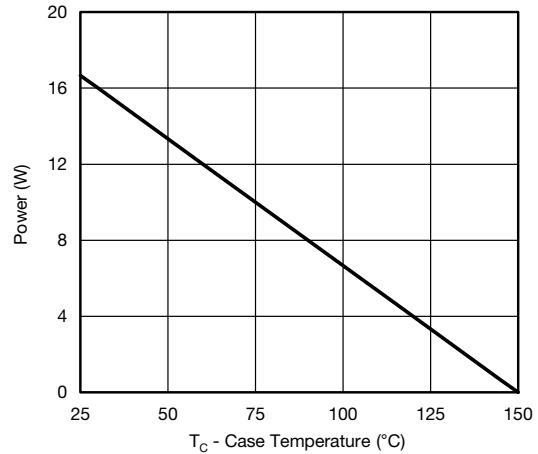
**Safe Operating Area, Junction-to-Ambient**



**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating\***

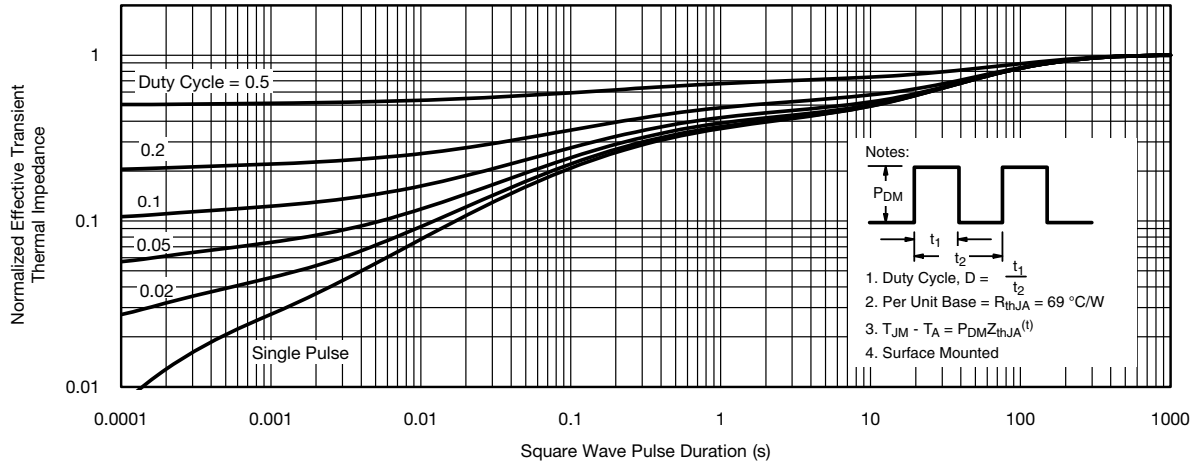


**Power, Junction-to-Case**

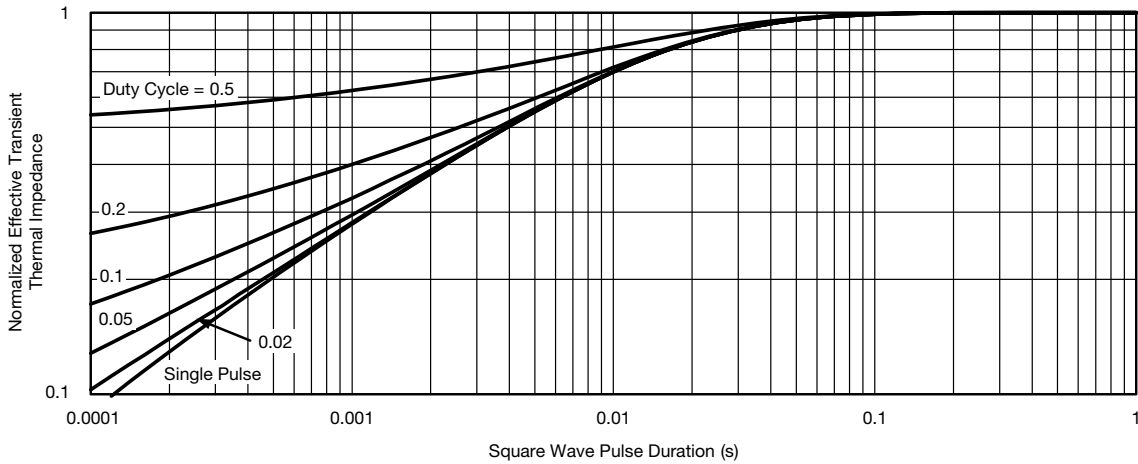
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

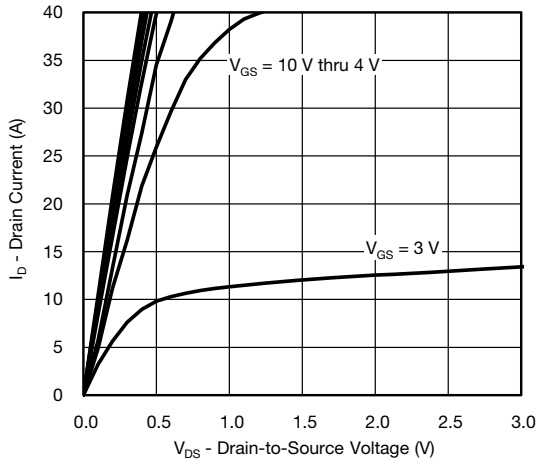


**Normalized Thermal Transient Impedance, Junction-to-Ambient**

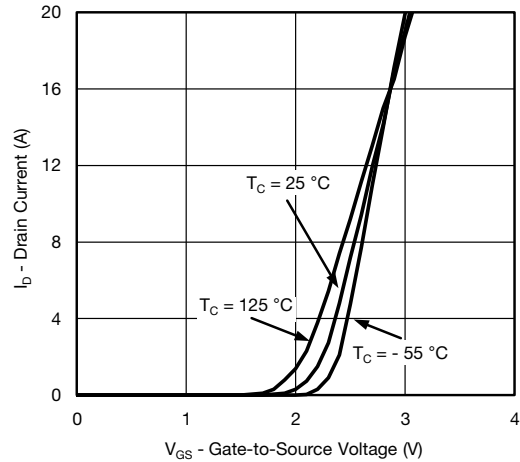


**Normalized Thermal Transient Impedance, Junction-to-Case**

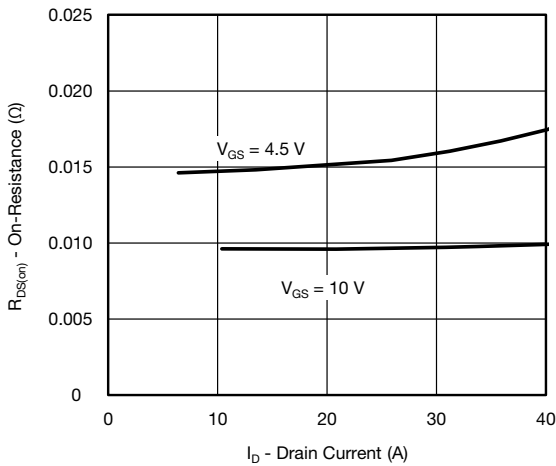
**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



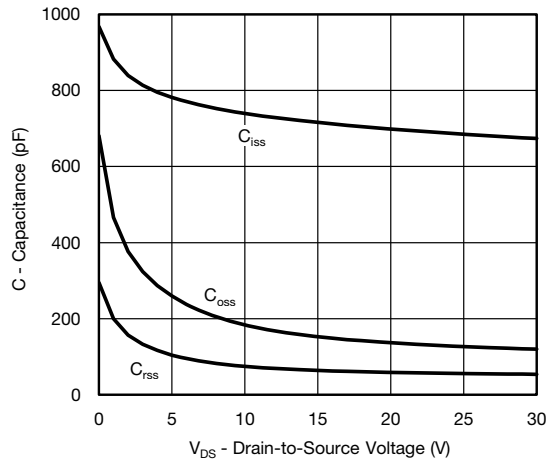
**Output Characteristics**



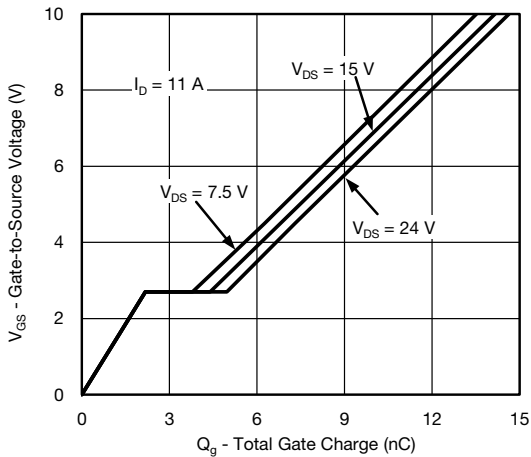
**Transfer Characteristics**



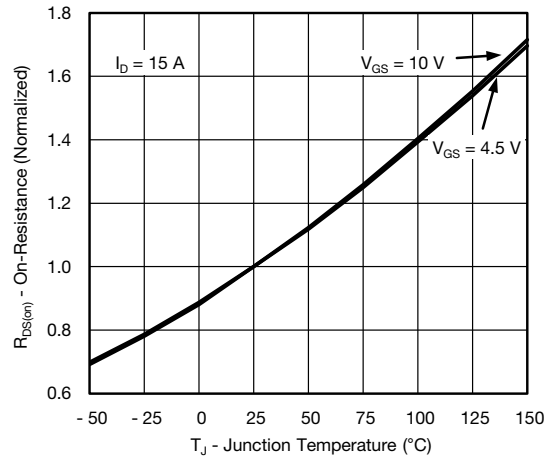
**On-Resistance vs. Drain Current**



**Capacitance**



**Gate Charge**

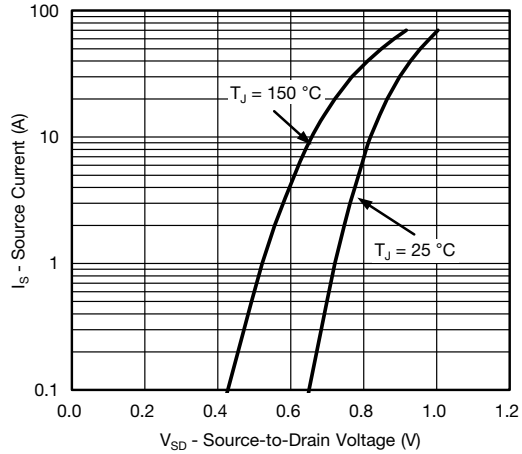


**On-Resistance vs. Junction Temperature**

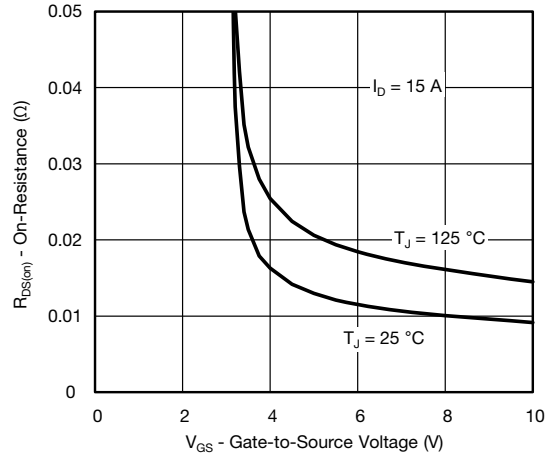




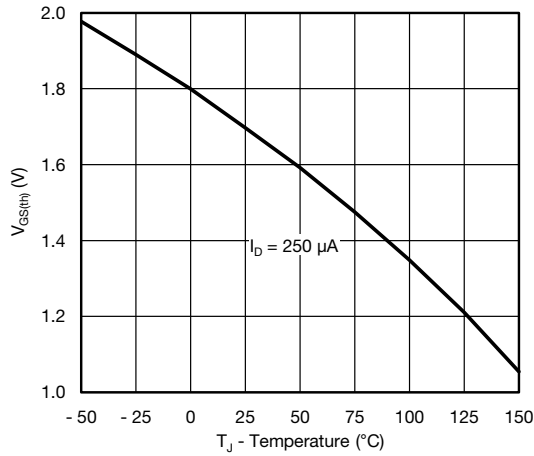
**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



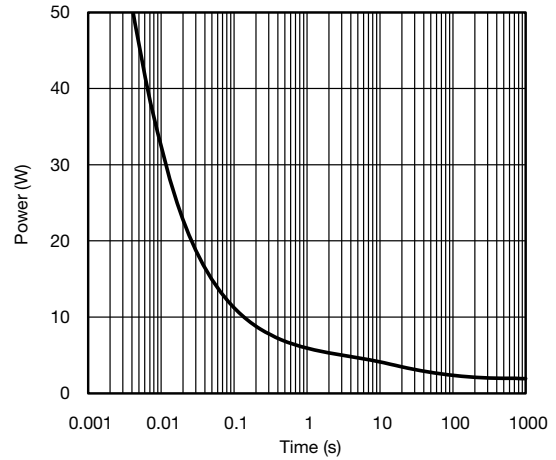
**Source-Drain Diode Forward Voltage**



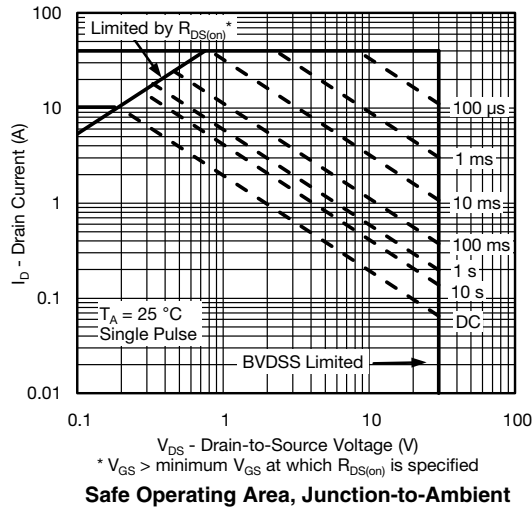
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power**



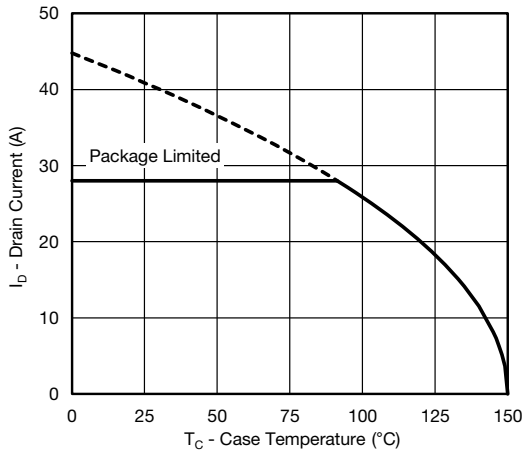
**Safe Operating Area, Junction-to-Ambient**

# SiZ300DT

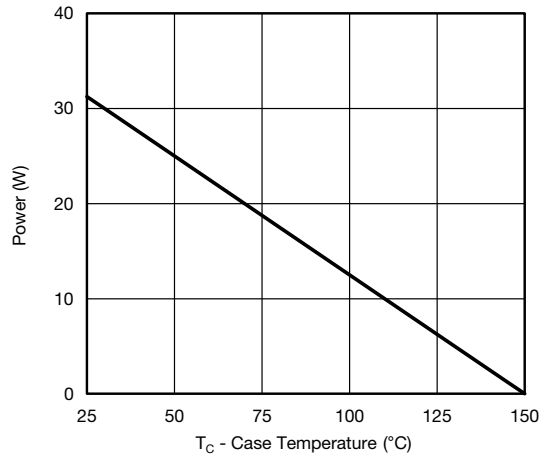
Vishay Siliconix



## CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating\*

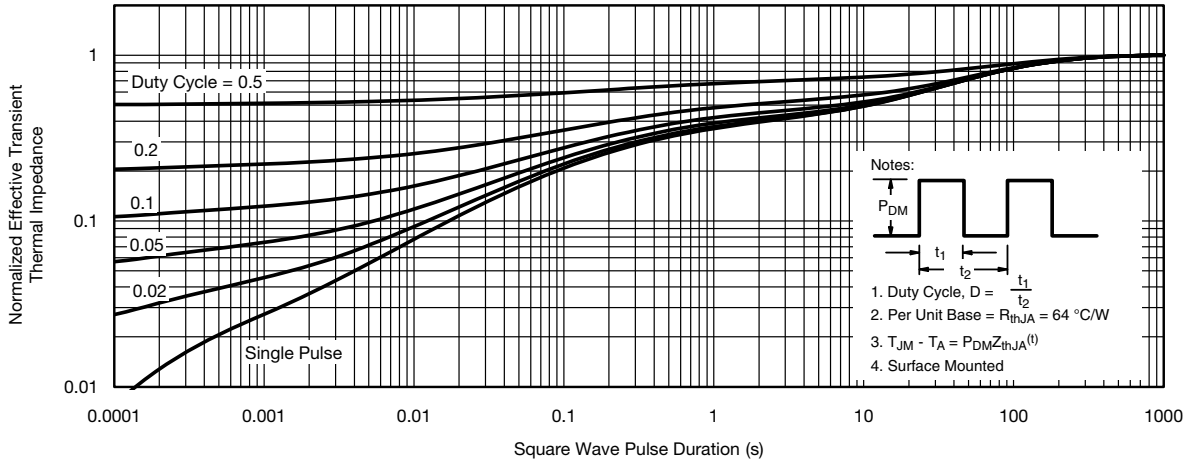


Power, Junction-to-Case

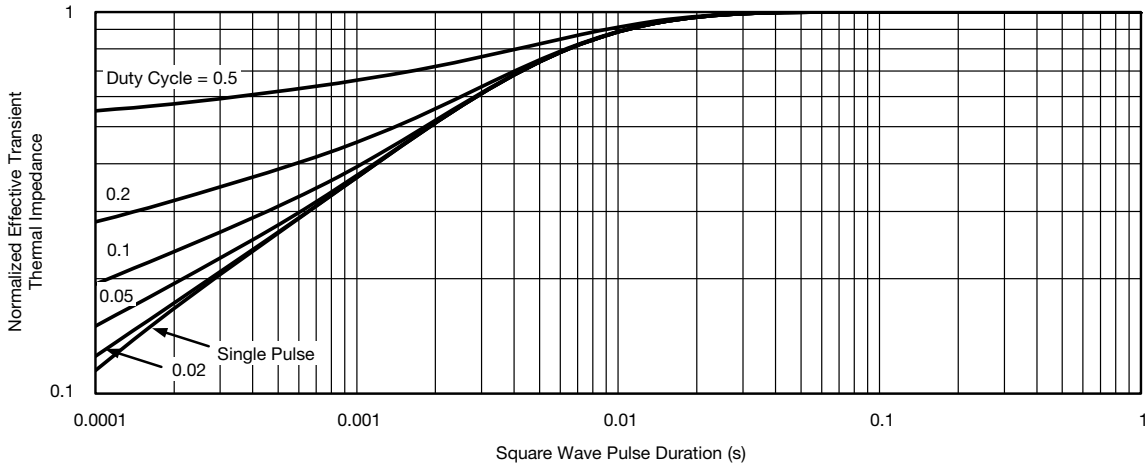
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?267715](http://www.vishay.com/ppg?267715).



PowerPAIR® 3 x 3 Case Outline



Note  
\* Indicates pin #1 orientation (optional)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.35	2.40	2.45	0.093	0.094	0.096
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	0.94	0.99	1.04	0.037	0.039	0.041
E2	0.47	0.52	0.57	0.019	0.020	0.022
e	0.65 BSC			0.026 BSC		
K	0.25 typ.			0.010 typ.		
K1	0.35 typ.			0.014 typ.		
K2	0.30 typ.			0.012 typ.		
L	0.27	0.32	0.37	0.011	0.013	0.015
ECN: T12-0347-Rev. C, 18-Jun-12						
DWG: 5998						

## RECOMMENDED MINIMUM PAD FOR PowerPAIR® 3 x 3



Recommended PAD for PowerPAIR 3 x 3

Dimensions in millimeters (inches)

Keep-Out 3.5 mm x 3.5 mm for non terminating traces



## **Disclaimer**

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