



STF16N65M5, STI16N65M5 STP16N65M5, STU16N65M5, STW16N65M5

N-channel 650 V, 0.230 Ω , 12 A MDmesh™ V Power MOSFET
in TO-220FP, I²PAK, TO-220, IPAK, TO-247

Features

Type	V _{DSS} @ T _{Jmax}	R _{DS(on)} max	I _D
STF16N65M5 STI16N65M5 STP16N65M5 STU16N65M5 STW16N65M5	710 V	< 0.279 Ω	12 A

- Worldwide best R_{DS(on)}
- Higher V_{DSS} rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

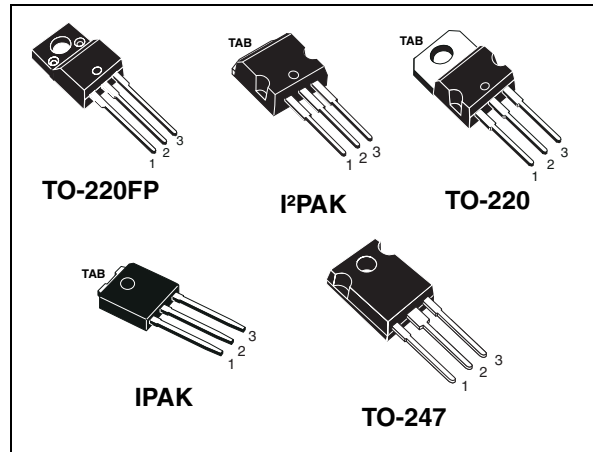


Figure 1. Internal schematic diagram

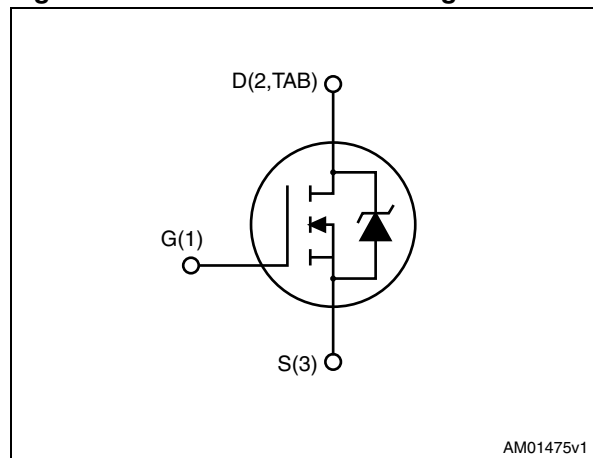


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF16N65M5 STI16N65M5 STP16N65M5 STU16N65M5 STW16N65M5	16N65M5	TO-220FP I ² PAK TO-220 IPAK TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	TO-220, I ² PAK, IPAK, TO-247	
V _{DS}	Drain-source voltage (V _{GS} = 0)	650		V
V _{GS}	Gate-source voltage	± 25		V
I _D	Drain current (continuous) at T _C = 25 °C	12 ⁽¹⁾	12	A
I _D	Drain current (continuous) at T _C = 100 °C	7.3 ⁽¹⁾	7.3	A
I _{DM} ⁽²⁾	Drain current (pulsed)	48 ⁽¹⁾	48	A
P _{TOT}	Total dissipation at T _C = 25 °C	90	25	W
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j max)	4		A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	200		mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2500		V
T _{stg}	Storage temperature	- 55 to 150		°C
T _j	Max. operating junction temperature	150		°C

- Limited by maximum junction temperature
- Pulse width limited by safe operating area
- I_{SD} ≤ 12 A, di/dt ≤ 400 A/μs, V_{DD} = 400 V, V_{Peak} < V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value					Unit	
		TO-220FP	I ² PAK	TO-220	IPAK	TO-247		
R _{thj-case}	Thermal resistance junction-case max	5	1.38				°C/W	
R _{thj-amb}	Thermal resistance junction-ambient max	62.5		100	50		°C/W	
T _l	Maximum lead temperature for soldering purpose	300						°C

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$		0.230	0.279	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	1250	-	pF
C_{oss}	Output capacitance			30		pF
C_{rss}	Reverse transfer capacitance			3		pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}, V_{GS} = 0$	-	100	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			30		pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	2	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 10\text{ V}$ (see Figure 20)	-	31	-	nC
Q_{gs}	Gate-source charge			8		nC
Q_{gd}	Gate-drain charge			12		nC

- $C_{oss\text{ eq.}}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
- $C_{oss\text{ eq.}}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t_d (v)	Voltage delay time	$V_{DD} = 400$ V, $I_D = 8$ A,		25		ns
t_r (v)	Voltage rise time	$R_G = 4.7$ Ω , $V_{GS} = 10$ V		7		ns
t_f (i)	Current fall time	(see Figure 21)	-	6	-	ns
t_c (off)	Crossing time	(see Figure 24)		8		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12$ A, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 12$ A, $di/dt = 100$ A/ μ s		300		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100$ V (see Figure 24)	-	3.5		μ C
I_{RRM}	Reverse recovery current			23		A
t_{rr}	Reverse recovery time	$I_{SD} = 12$ A, $di/dt = 100$ A/ μ s		350		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100$ V, $T_j = 150$ °C	-	4		μ C
I_{RRM}	Reverse recovery current	(see Figure 24)		24		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

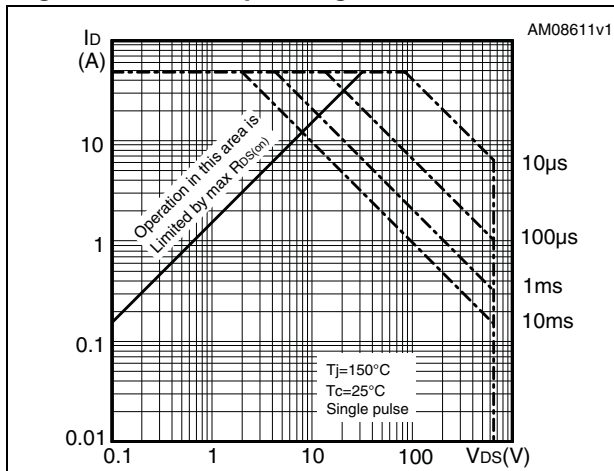


Figure 3. Thermal impedance for TO-220FP

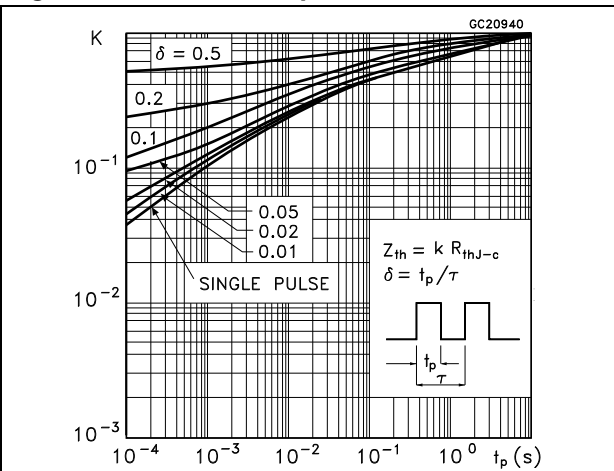


Figure 4. Safe operating area for TO-220, I²PAK, TO-247

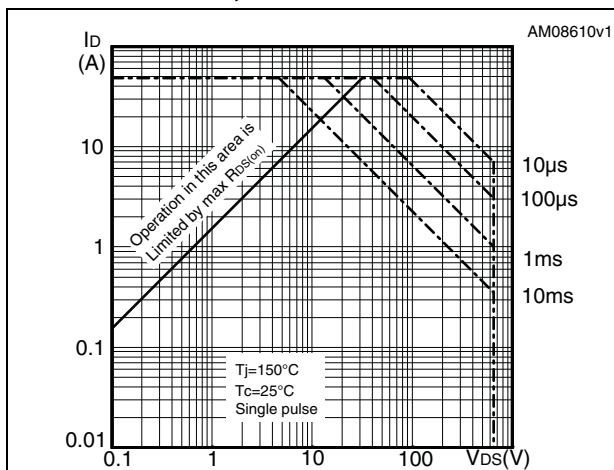


Figure 5. Thermal impedance for TO-220, I²PAK, TO-247

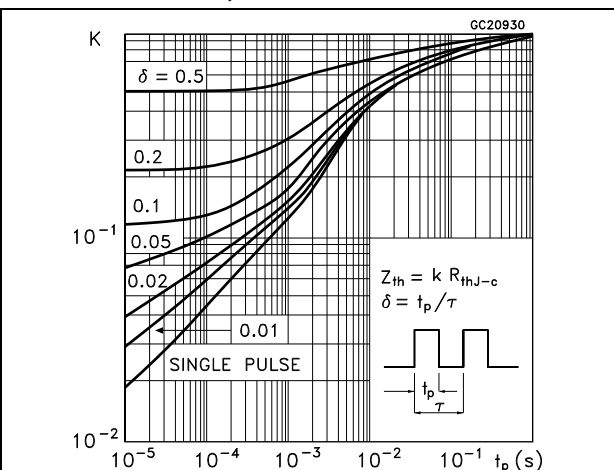


Figure 6. Safe operating area for IPAK

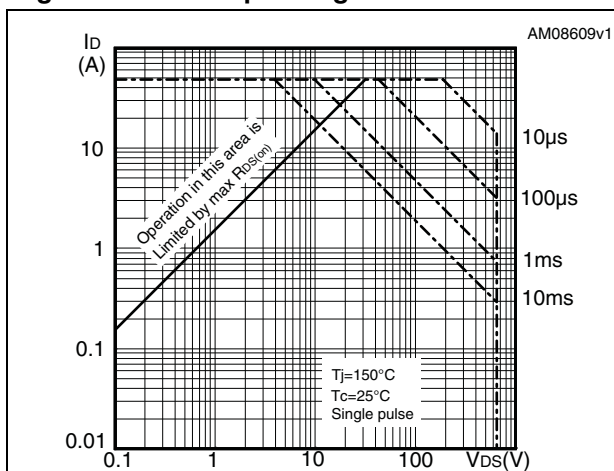


Figure 7. Thermal impedance for IPAK

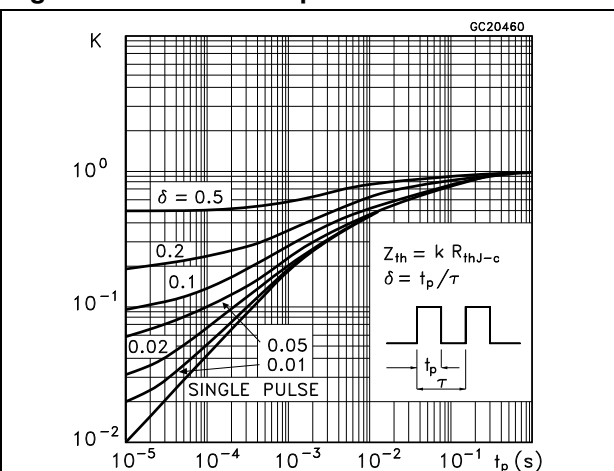


Figure 8. Output characteristics

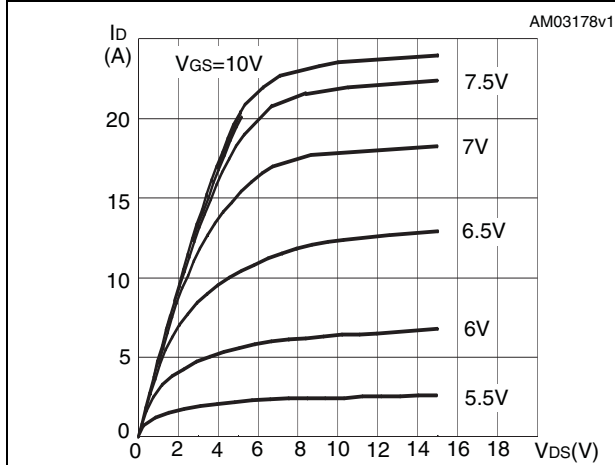


Figure 9. Transfer characteristics

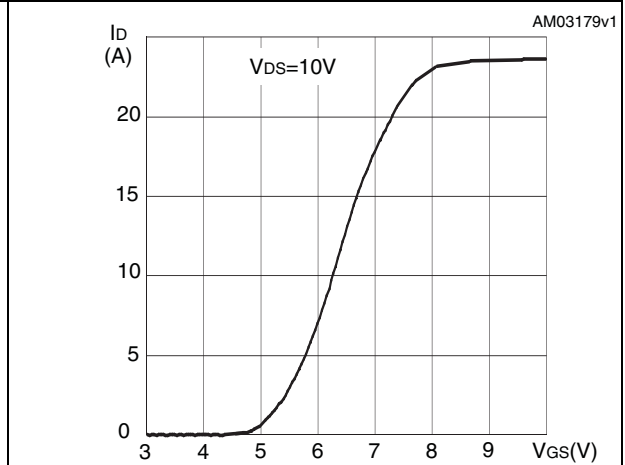


Figure 10. Normalized B_{VDSS} vs temperature

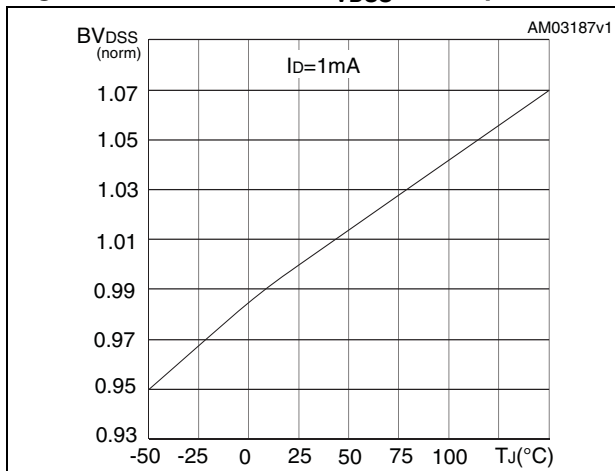


Figure 11. Static drain-source on resistance

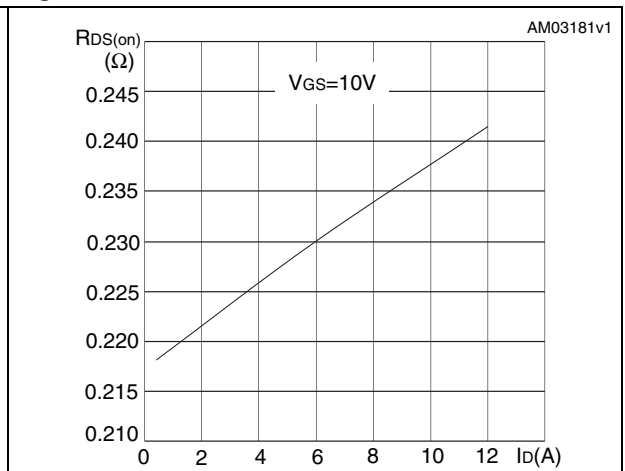


Figure 12. Output capacitance stored energy

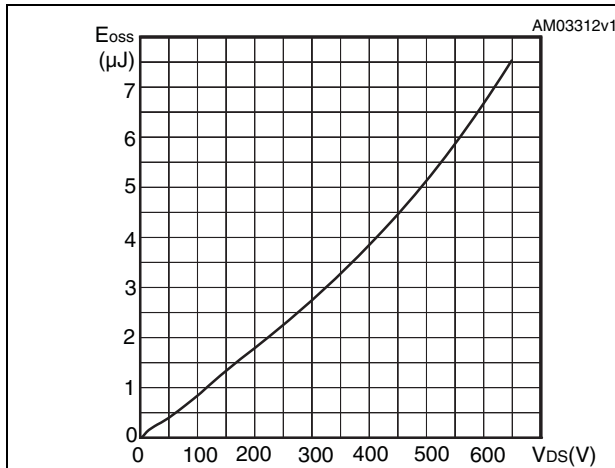


Figure 13. Capacitance variations

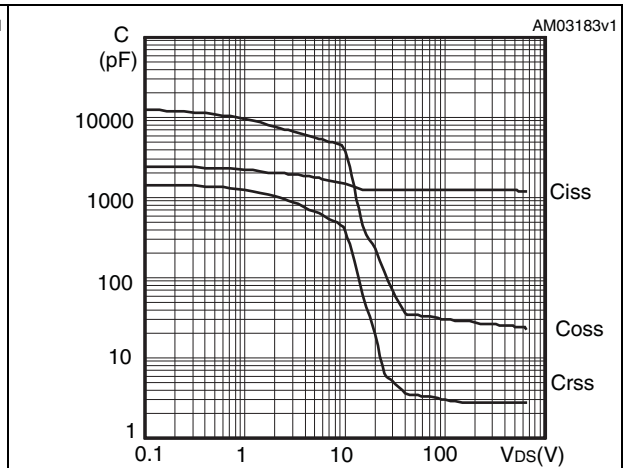


Figure 14. Gate charge vs gate-source voltage Figure 15. Normalized on resistance vs temperature

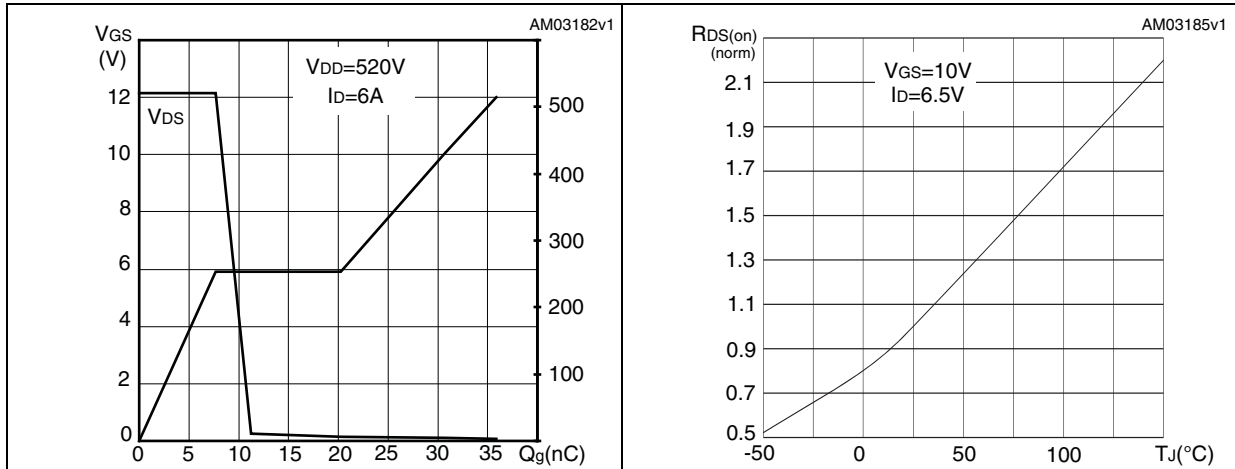


Figure 16. Normalized gate threshold voltage vs temperature Figure 17. Source-drain diode forward characteristics

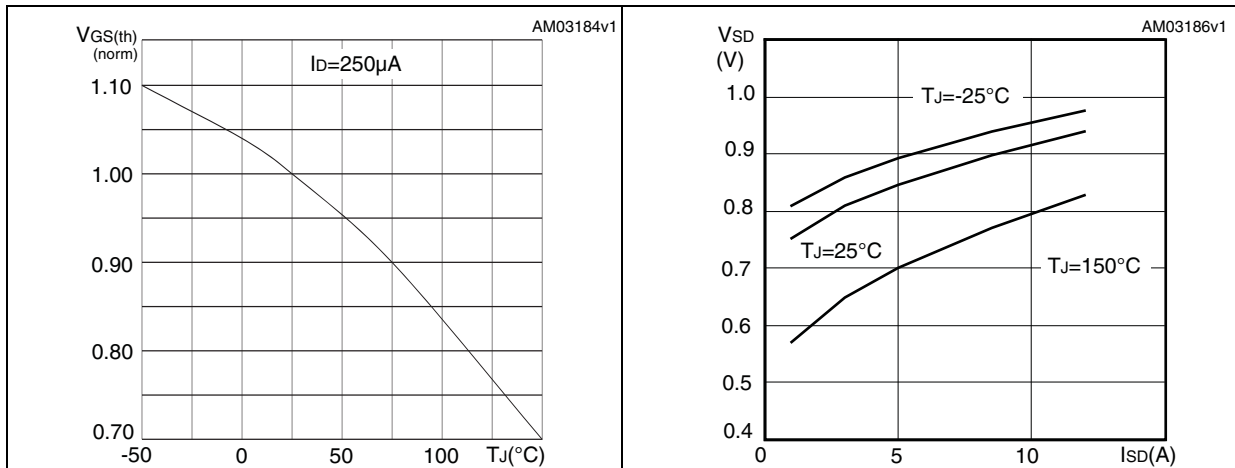
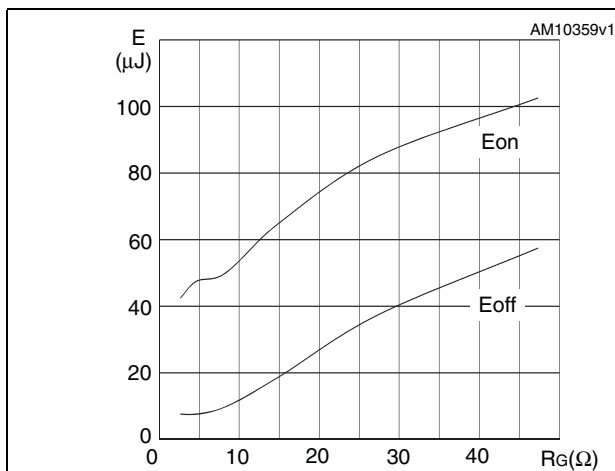


Figure 18. Switching losses vs gate resistance (1)



1. E_{on} including reverse recovery of a SiC diode

3 Test circuits

Figure 19. Switching times test circuit for resistive load

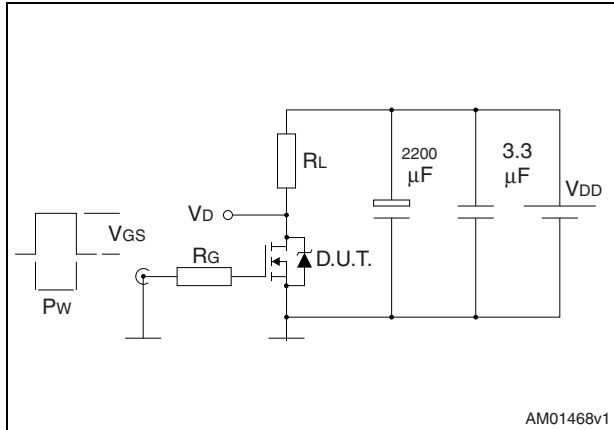


Figure 20. Gate charge test circuit

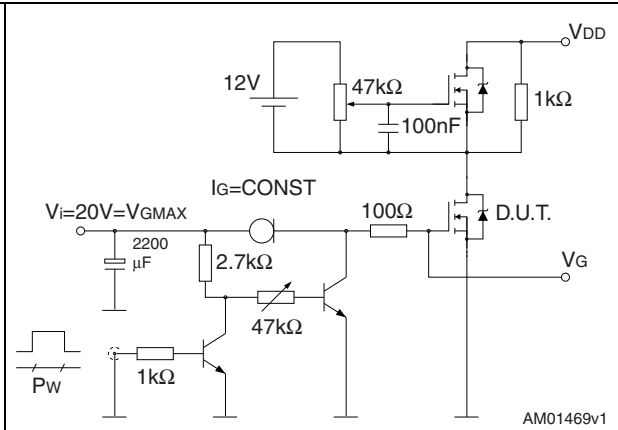


Figure 21. Test circuit for inductive load switching and diode recovery times

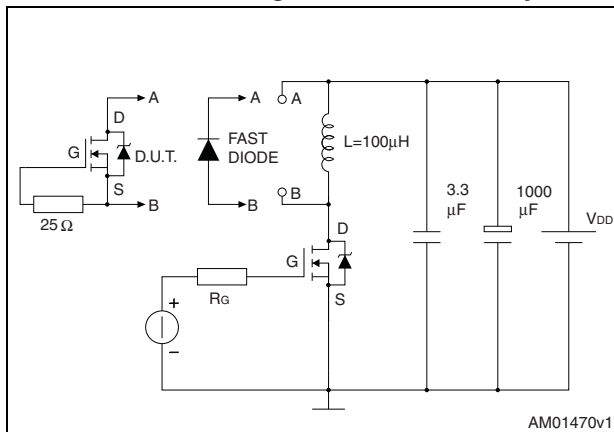


Figure 22. Unclamped inductive load test circuit

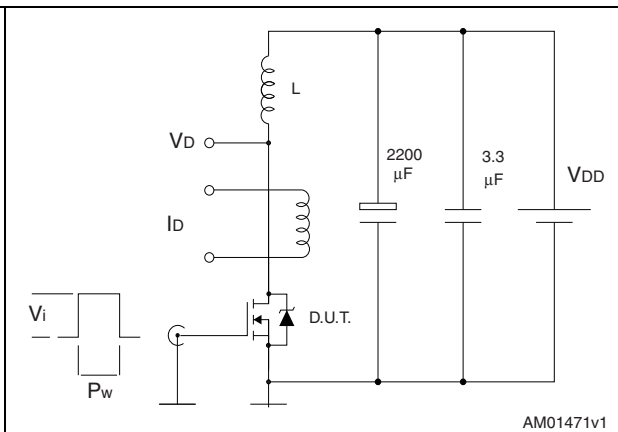


Figure 23. Unclamped inductive waveform

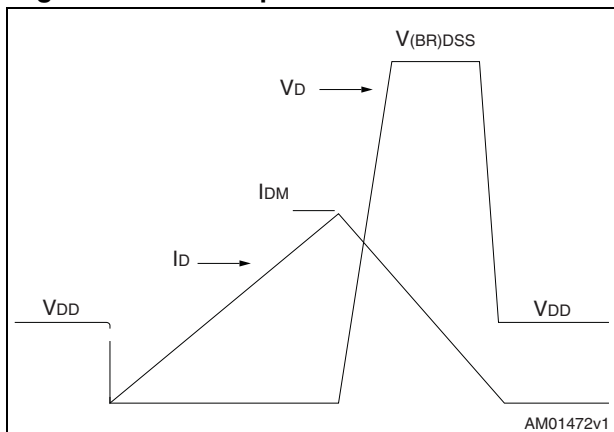
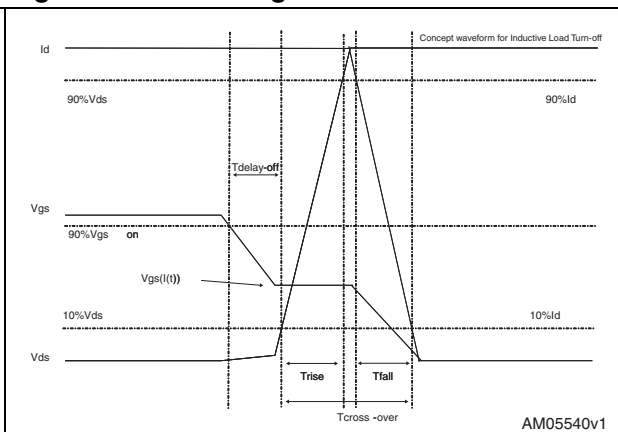


Figure 24. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 25. TO-220FP drawing

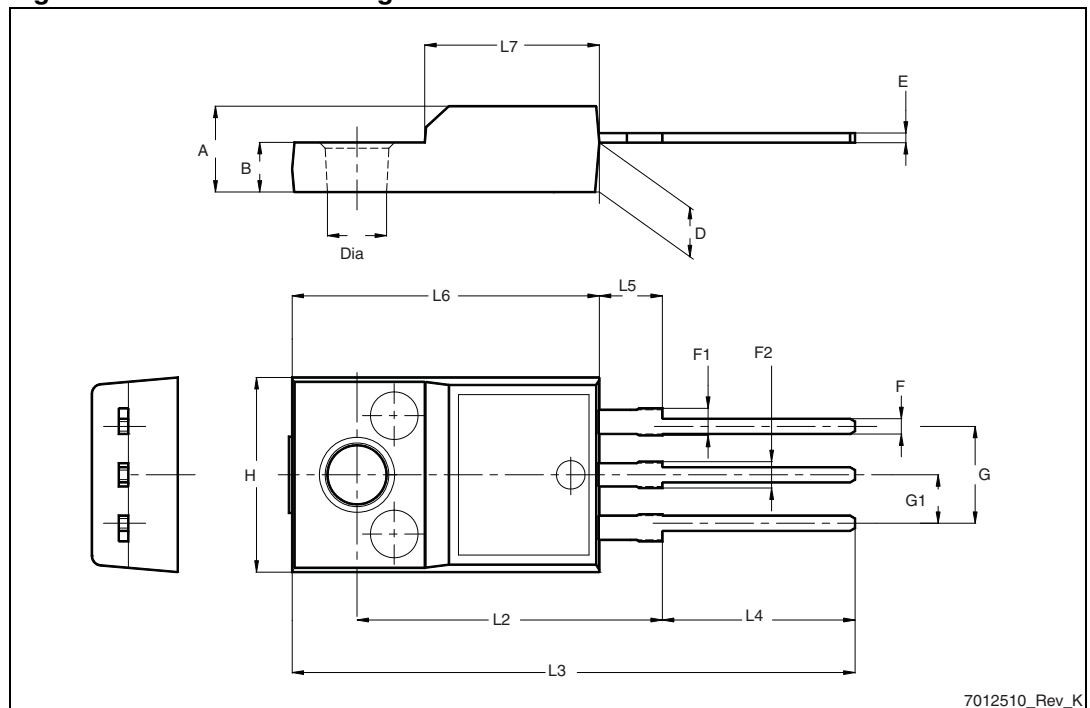
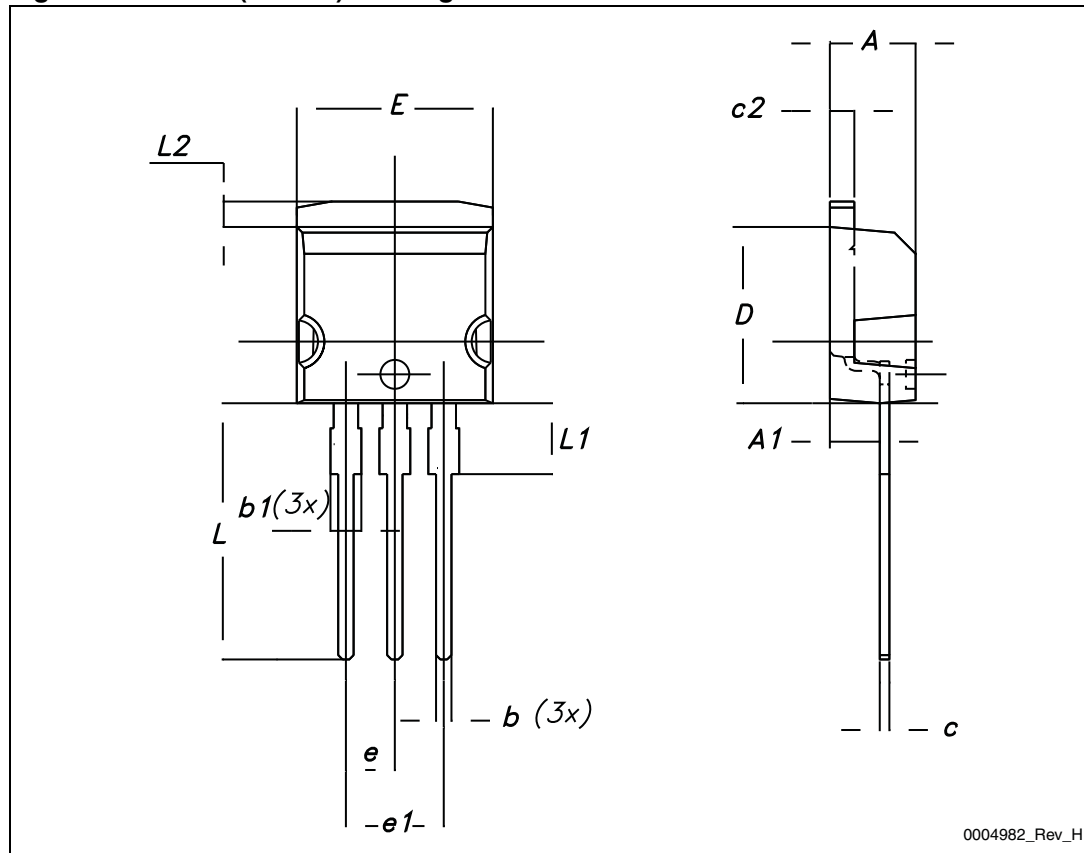


Table 9. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 26. I²PAK (TO-262) drawing



0004982_Rev_H

Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing

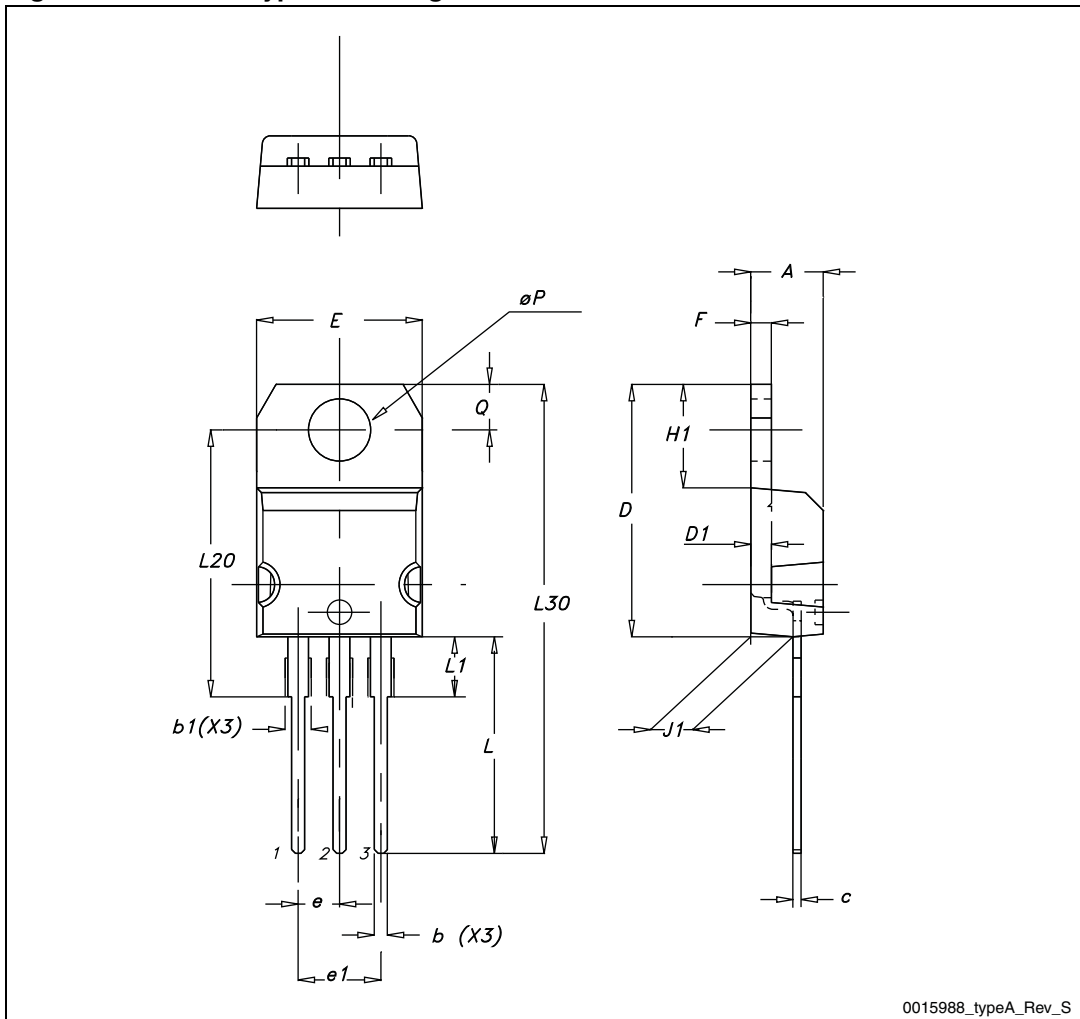


Table 11. IPAK (TO-251) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.3	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10 °	

Figure 28. IPAK (TO-251) drawing

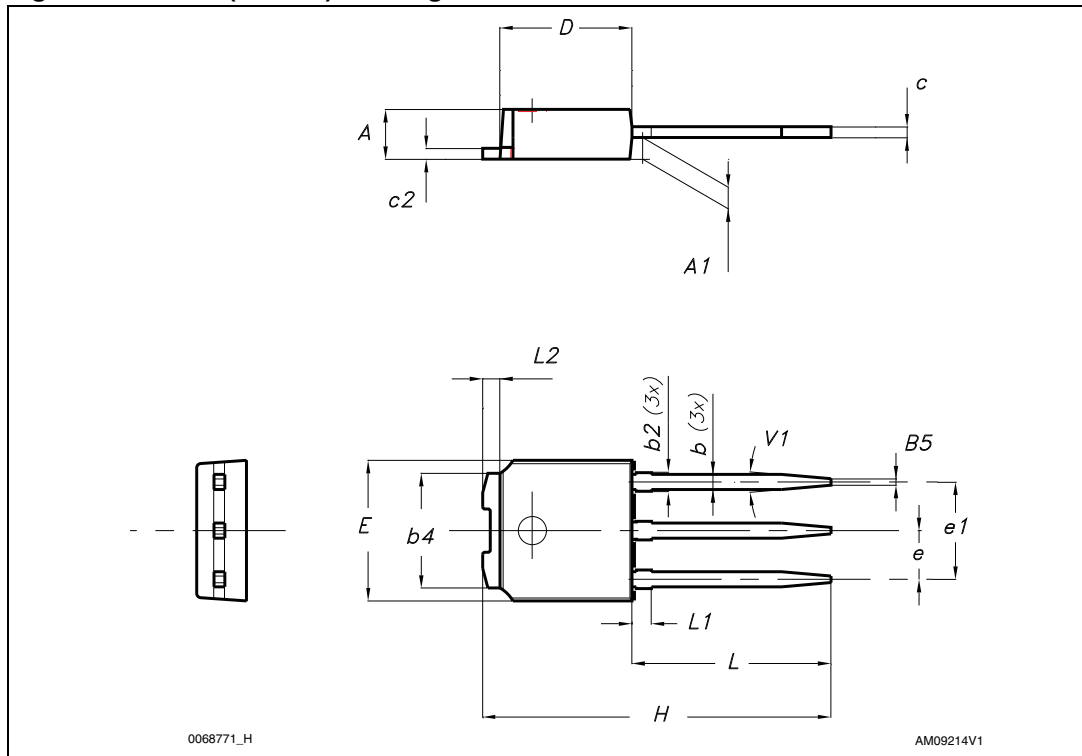


Table 12. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	

Figure 29. TO-247 drawing



0075325_F

5 Revision history

Table 13. Document revision history

Date	Revision	Changes
12-Feb-2009	1	First release.
21-Oct-2010	2	<ul style="list-style-type: none"> – Document status promoted from preliminary data to datasheet. – Added new package, mechanical data: I²PAK. – Removed DPAK, D²PAK packages and mechanical data.
10-Feb-2011	3	Modified R _{DS(on)} value (see Table 4 and Figure 11).
13-Oct-2011	4	Modified Section 2.1: Electrical characteristics (curves) : <ul style="list-style-type: none"> – Figure 8, Figure 9, Figure 10, Figure 11, Figure 15 and Figure 16 – Added Figure 18 Updated R _{DS(on)} value in Table 4 Updated values in Table 6 Minor text changes.

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