Lead-free Green

AP7361

1A LOW DROPOUT ADJUSTABLE AND FIXED-MODE REGULATOR WITH ENABLE

Description

The AP7361 is a 1A, adjustable and fixed output voltage, ultra-low dropout linear regulator with enable. The device includes pass element, error amplifier, band-gap reference, current limit and thermal shutdown circuitry. The device is turned on when the EN pin is set to logic high level.

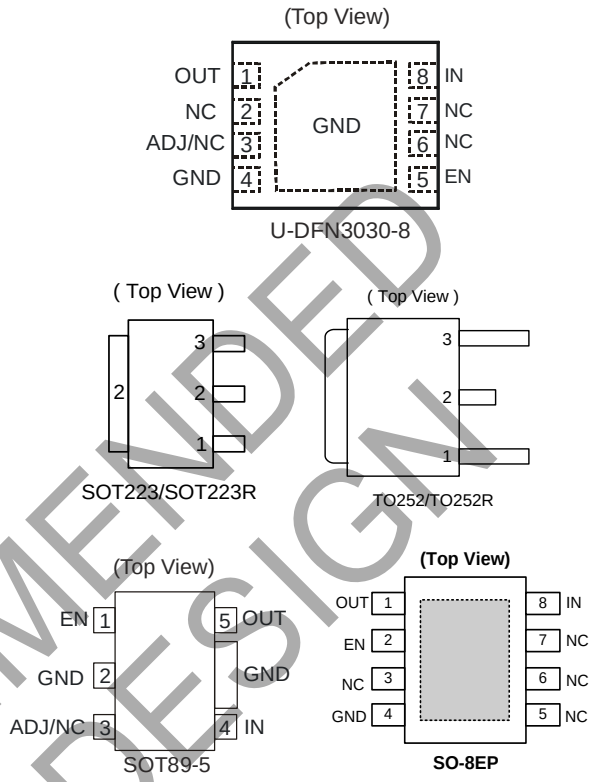
The characteristics of the low dropout voltage and low quiescent current make it suitable for low to medium power applications, for example, laptop computers, audio and video applications, and battery powered devices. The typical quiescent current is approximately 70μA. Built-in current-limit and thermal-shutdown functions prevent IC from damage in fault conditions.

The AP7361 is available in U-DFN3030-8, SOT89-5, SOT223, TO252 and SO-8EP package.

Features

- Wide input voltage range: 2.2V - 6V
- 150mV Very Low Dropout at 300mA Load
- 500mV Very Low Dropout at 1A Load
- Low Quiescent Current (I_Q): 70μA Typical
- Adjustable Output Voltage Range: 1V to 5.0V
- Fixed Output Options: 1V to 3.3V
- Very-Fast Transient Response
- High PSRR
- Accurate Voltage Regulation
- Current Limiting and Short Circuit Protection
- Thermal Shutdown Protection
- Stable with Ceramic Output Capacitor ≥ 2.2μF
- Ambient Temperature Range -40°C to +85°C
- U-DFN3030-8, SOT89-5, SOT223/SOT223R, TO252/TO252R and SO-8EP
- Available in "Green" Molding Compound (No Br, Sb)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Pin Assignments

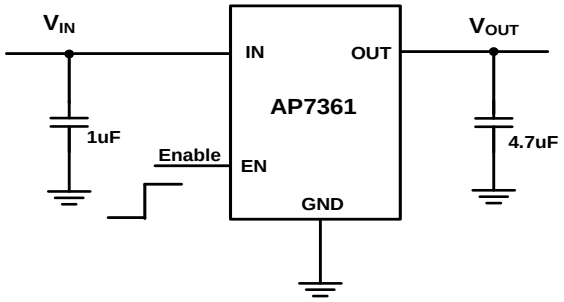


Applications

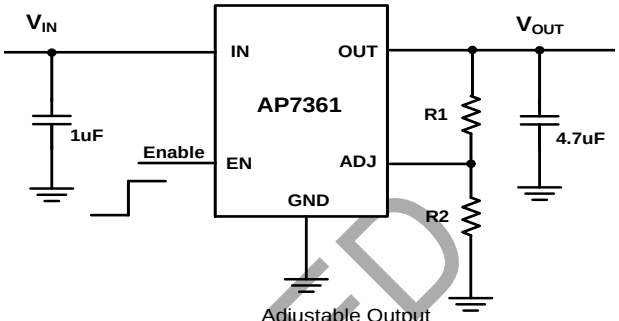
- Servers and Laptops
- FPGA and DSP Core or I/O Power
- TV, and Home Electrical Appliances
- Battery-Powered Devices

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

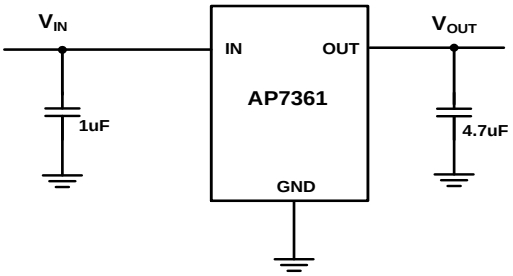
Typical Applications Circuit



Fixed Version
U-DFN3030-8, SOT89-5 and SO-8EP



Adjustable Output
U-DFN3030-8 and SOT89-5

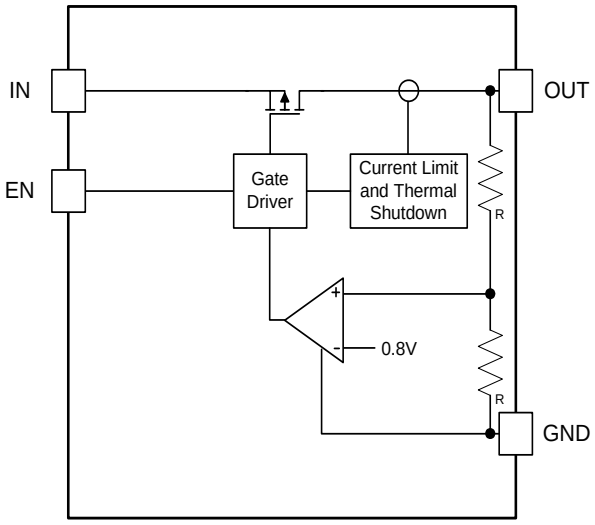


Fixed Version
TO252, SOT223

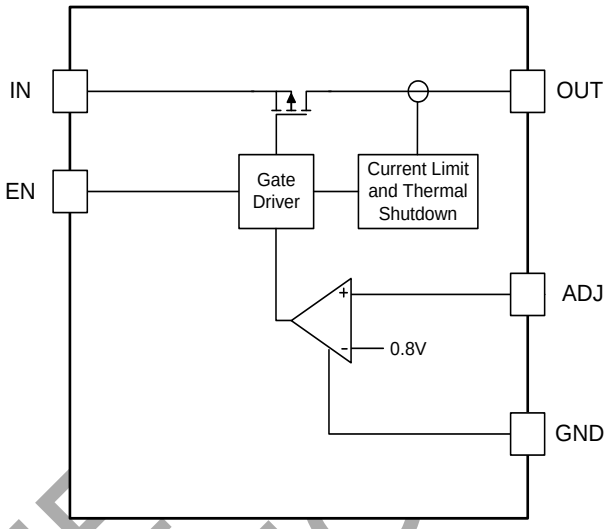
Pin Descriptions

Pin Name	Pin Number							Function
	U-DFN3030-8	SOT89-5	TO252	TO252R	SOT223	SOT223R	SO-8EP	
IN	8	4	1	3	1	3	8	The input of the regulator. Bypass to ground through at least 1μF ceramic capacitor.
OUT	1	5	3	2	3	2	1	The output of the regulator. Bypass to ground through at least 2.2μF ceramic capacitor. For improved ac load response a larger capacitor is recommended.
GND	4	2	2	1	2	1	4	Ground
ADJ	3	3	NA	NA	NA	NA	NA	Adjustable voltage version only – a resistor divider from this pin to the OUT pin and ground sets the output voltage.
EN	5	1	NA	NA	NA	NA	2	Enable input, active high
NC	2, 6, 7	NA	NA	NA	NA	NA	3, 5, 6, 7	No connection

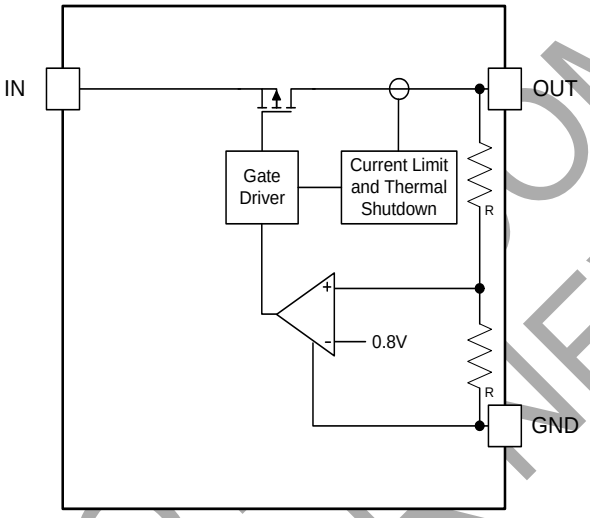
Functional Block Diagram



Fixed Version U-DFN3030-8, SOT89-5 and SO-8EP



Adjustable Version U-DFN3030-8 and SOT89-5



Fixed Version
TO252, SOT223

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter		Ratings	Unit
ESD HBM	Human Body Model ESD Protection		> 2	KV
ESD MM	Machine Model ESD Protection (Note 5)		> 200	V
V_{IN}	Input Voltage		6.5	V
	OUT, ADJ, EN Voltage		V_{IN} +0.3	V
T_J	Operating Junction Temperature Range		-40 to +150	°C
T_{ST}	Storage Temperature Range		-65 to +150	°C
P_D	Power Dissipation (Note 4)		Internally limited by maximum junction temperature of +150°C	
P_D	Power Dissipation (Note 4)	U-DFN3030-8	1,700	mW
		TO252	1,250	
		SOT223	1,100	
		SOT89-5	800	
		SO-8EP	1,190	

Notes: 4. Ratings apply to ambient temperature at +25°C.
5. ESD MM rating at 150V for EN pin.

Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	2.2	6.0	V
I_{OUT}	Output Current (Note 6)	0	1.0	A
T_A	Operating Ambient Temperature	-40	+85	°C

Note: 6. The device maintains a stable, regulated output voltage without a load current. When the output current is large, attention should be given to the limitation of the package power dissipation.

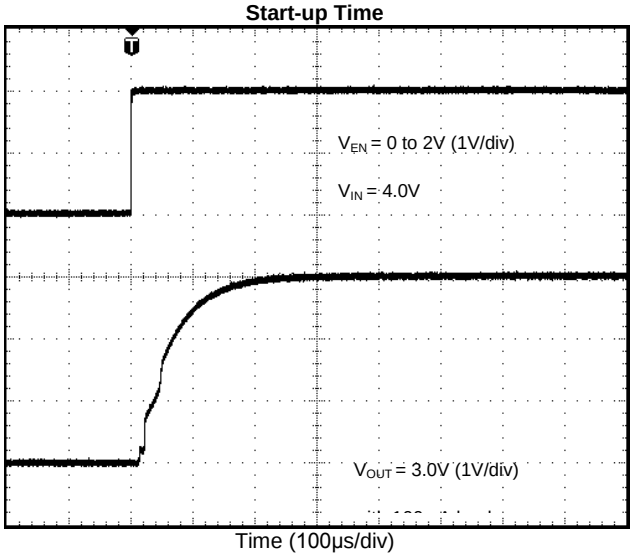
Electrical Characteristics (@T_A = +25°C, V_{IN} = V_{OUT} +1V, C_{IN} = 1µF, C_{OUT} = 4.7µF, V_{EN} = V_{IN} unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{REF}	FB Reference Voltage	I_{OUT} = 10mA, T_A = +25°C		0.8		V
I_{ADJ}	ADJ Pin Leakage			0.1	0.5	µA
I_Q	Input Quiescent Current	Enabled, I_{OUT} = 0A		70	90	µA
I_{SHDN}	Input Shutdown Current	V_{EN} = 0V, I_{OUT} = 0A	-1	0.05	1	µA
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 100mA, T_A = +25°C	-1		1	%
		I_{OUT} = 100mA, -40°C ≤ T_A ≤ +85°C	-2		2	
		Over V_{IN}, I_{OUT}, and T_A	-3	±0.5	3	
$\frac{\Delta VOUT}{\Delta VIN \times V_{OUT}}$	Line Regulation	V_{IN} = V_{OUT} +1V to 6V, I_{OUT} = 100mA; T_A = +25°C		0.01	0.1	%/V
		-40°C ≤T_A ≤ +85°C			0.2	
$\Delta V_{OUT} / V_{OUT}$	Load Regulation	I_{OUT} from 1mA to 300mA	-1.0	0.5	1.0	%
		I_{OUT} from 1mA to 1A	-1.0	0.5	1.0	%
$V_{DROPOUT}$	Dropout Voltage (Note 7)	I_{OUT} = 300mA		150	200	mV
		I_{OUT} = 500mA		250	350	
		I_{OUT} = 1A		500	700	
V_{IL}	EN Input Logic Low Voltage		0		0.3	V
V_{IH}	EN Input Logic High Voltage		1.0		V_{IN}	V
I_{EN}	EN Input Leakage	V_{IN} = 6V, V_{EN} = 0V or 6V	-0.1	0.01	0.1	µA
I_{LIMIT}	Current Limit	V_{IN} = V_{OUT} +1V	1.1	1.5		A
I_{SHORT}	Short-Circuit Current	V_{IN} = V_{OUT} +1V, Output Voltage < 15% V_{OUT}		200		mA
PSRR	Power Supply Rejection Ratio (Note 8)	f = 1KHz, I_{OUT} = 100mA	60	65		dB
		f = 10KHz, I_{OUT} = 100mA		45		
t_{ST}	Start-Up Time	V_{OUT} = 3V, C_{OUT} = 1µF, R_L = 30Ω		200		µs
$\frac{\Delta VOUT}{\Delta T_A \times VOUT}$	Output Voltage Temperature Coefficient	I_{OUT} = 100mA, -40°C ≤ T_A ≤ +85°C		±130		ppm/°C
T_{SHDN}	Thermal Shutdown Threshold			150		°C
T_{HYS}	Thermal Shutdown Hysteresis			20		°C
θ_{JA}	Thermal Resistance Junction-to-Ambient	U-DFN3030-8 (Note 9)		70		°C/W
		TO252 (Note 9)		95		
		SOT223 (Note 9)		110		
		SOT89-5 (Note 9)		150		
		SO-8EP (Note 9)		100		

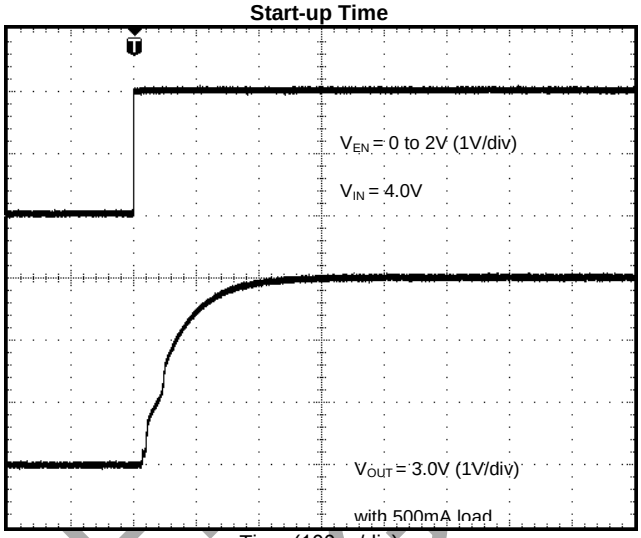
Notes:
7. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value. This parameter only applies to output voltages above 1.5V since minimum V_{IN} = 2.2V.
8. For V_{IN} ≥ 2.5V and V_{IN} = V_{OUT} +1V. For V_{IN} < 2.5V, the PSRR performance may be reduced.
9. Test condition: DFN3030E-8, SO-8EP device mounted on 2"x2", FR-4 substrate PCB, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane. TO252 device mounted on 2"x2" FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout. SOT223 the device is mounted on FR-4 substrate PC board, with minimum recommended pad layout. SOT89-5L device mounted on 1"x1" FR-4 substrate PC board, with minimum recommended pad layout.

Typical Performance Characteristics

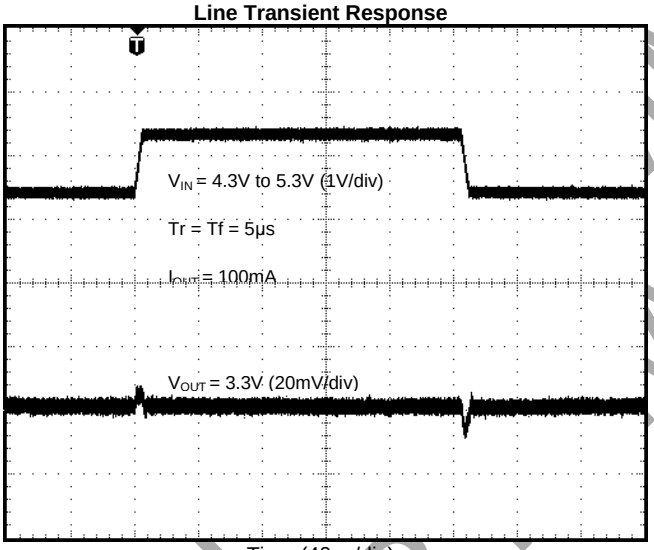
Start-up Time



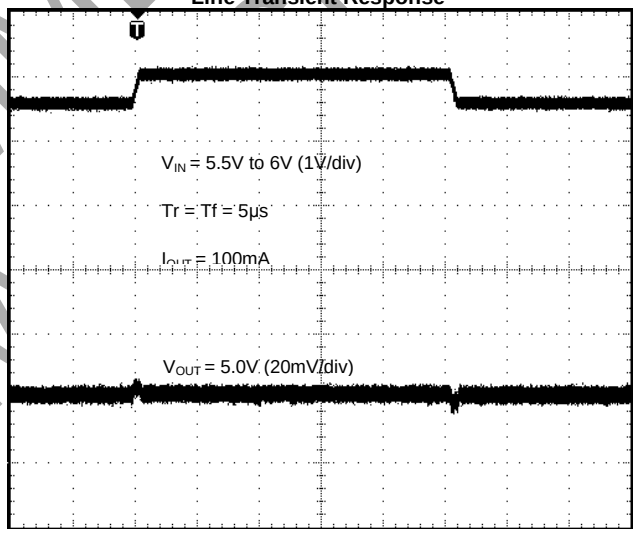
Start-up Time



Line Transient Response

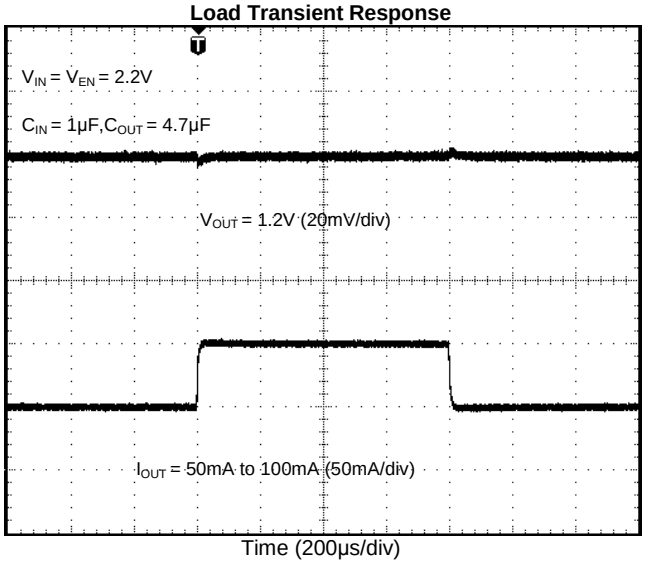


Line Transient Response

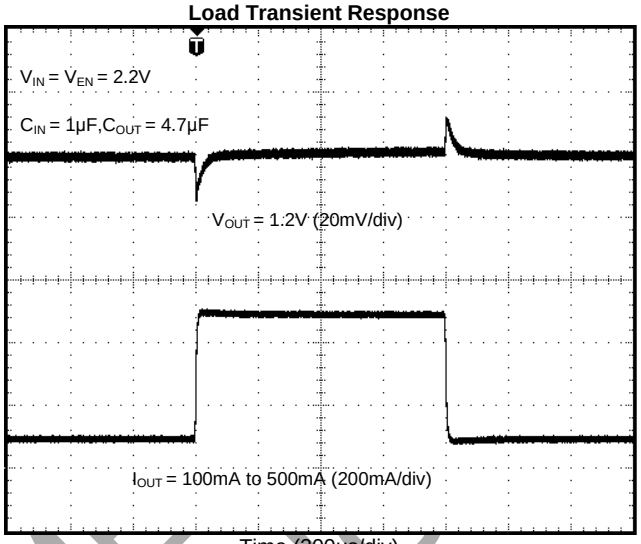


Typical Performance Characteristics (cont.)

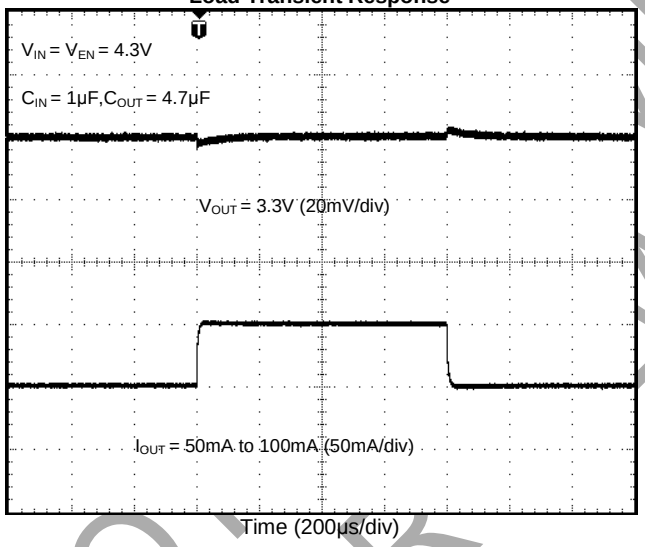
Load Transient Response



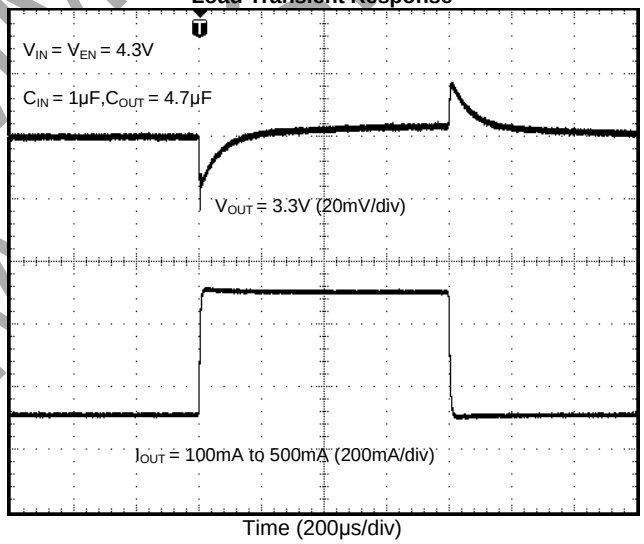
Load Transient Response



Load Transient Response

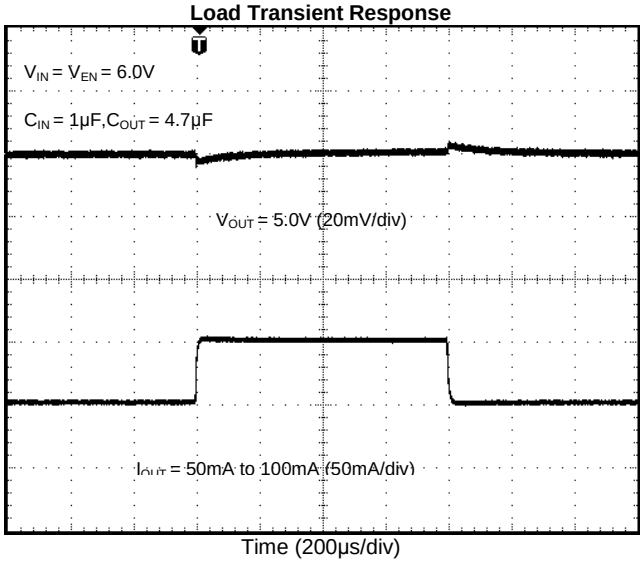


Load Transient Response

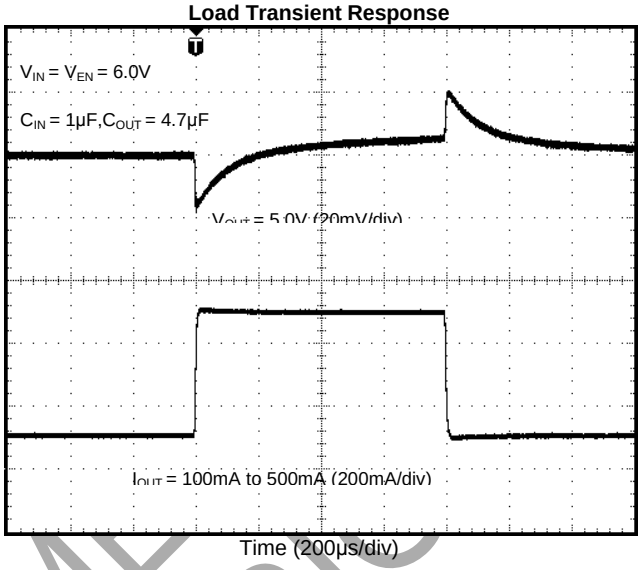


Typical Performance Characteristics (cont.)

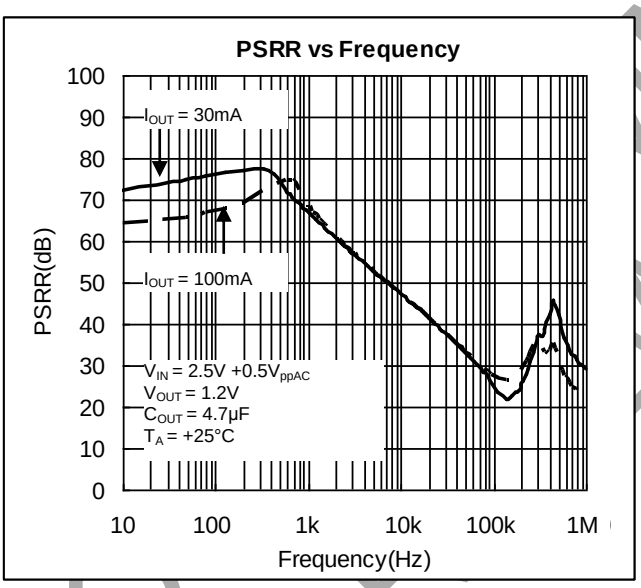
Load Transient Response



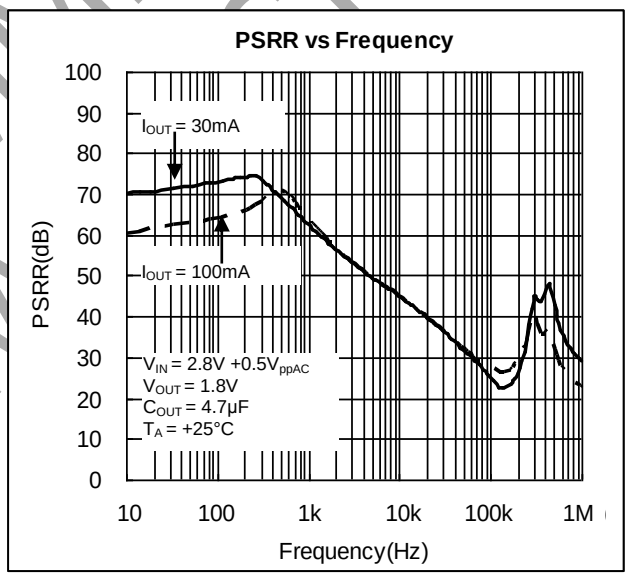
Load Transient Response



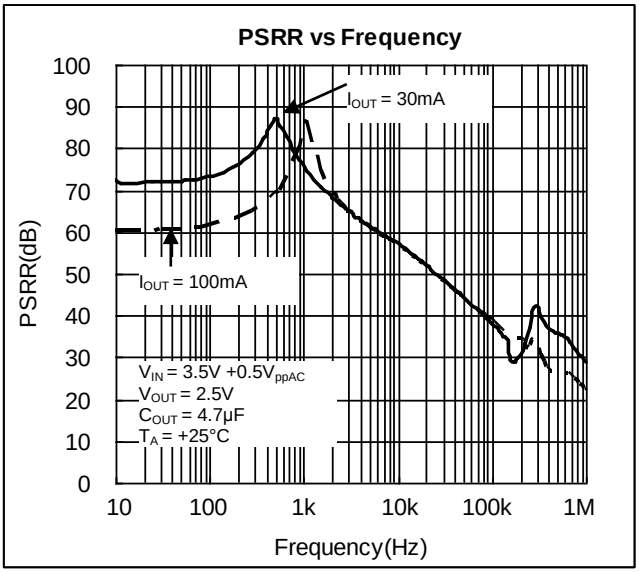
PSRR vs Frequency

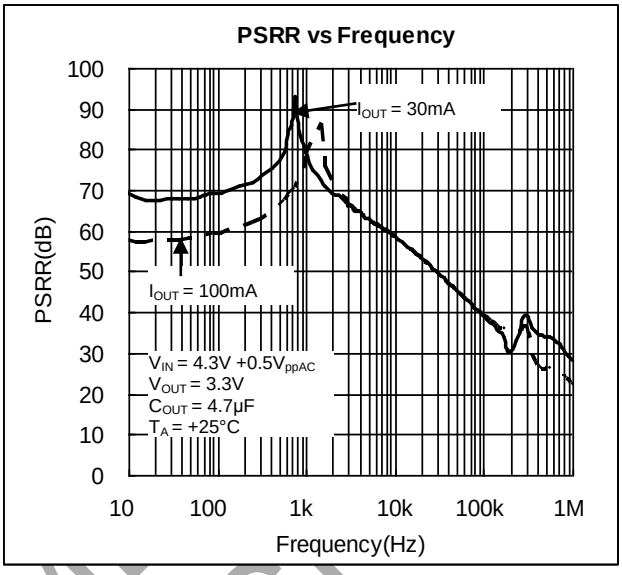


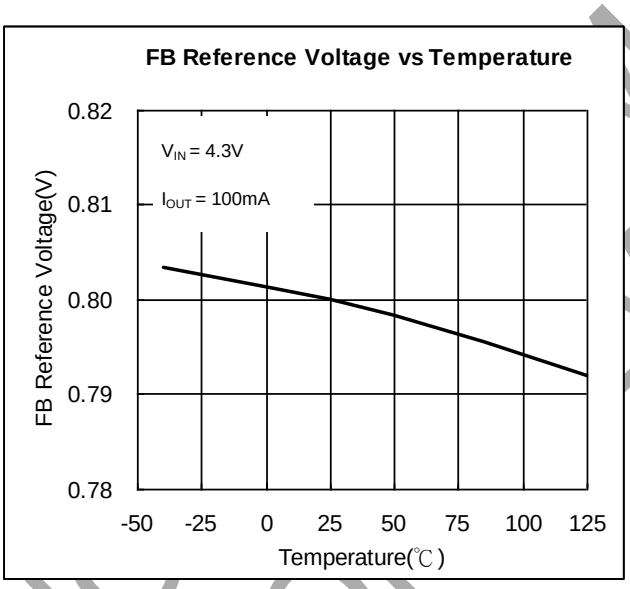
PSRR vs Frequency

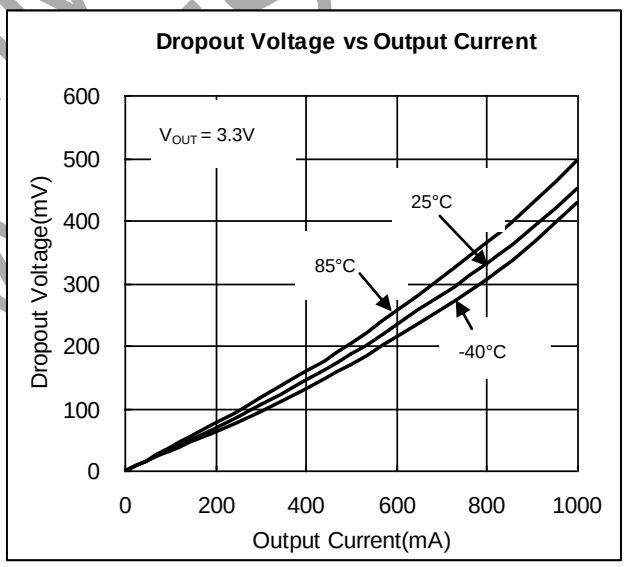


Typical Performance Characteristics (cont.)

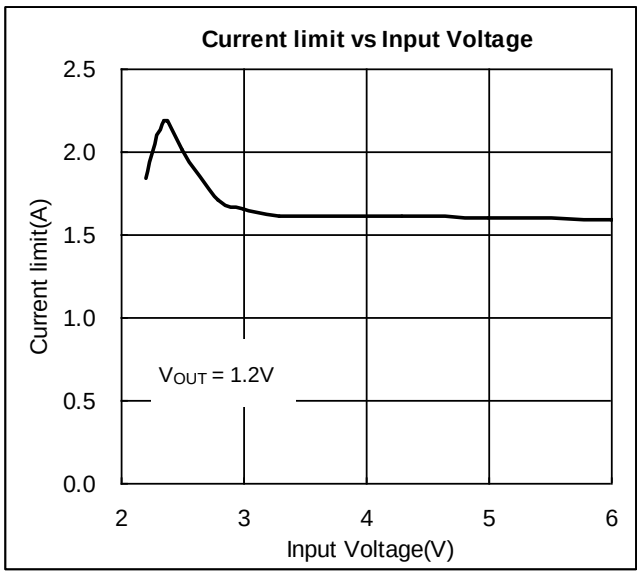


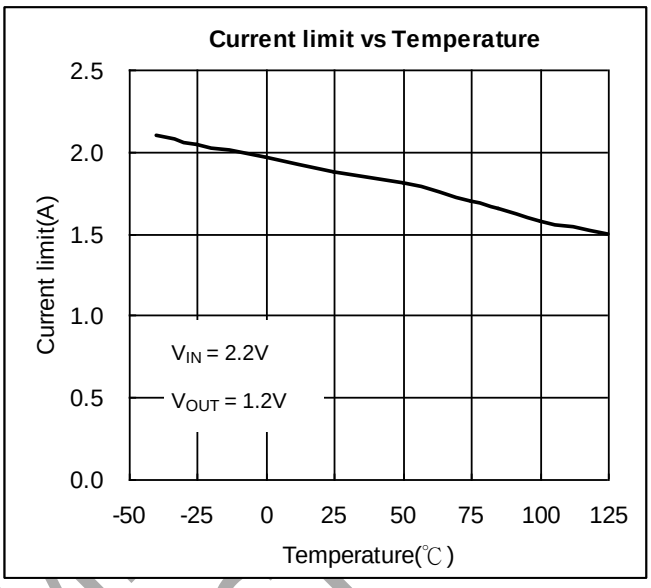


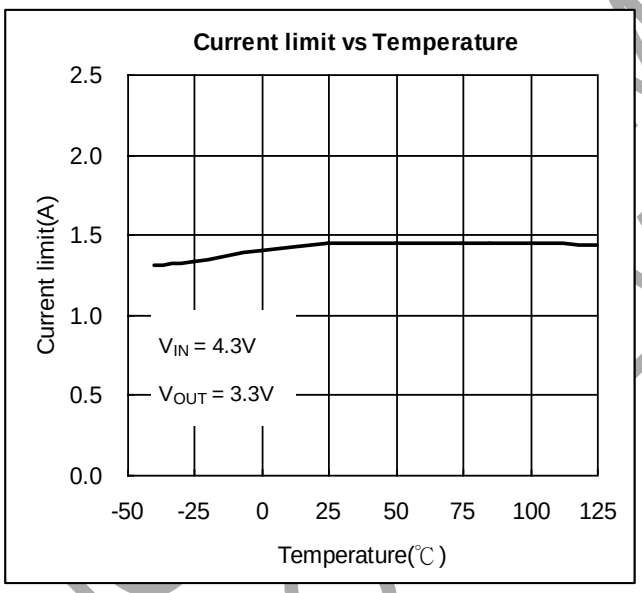


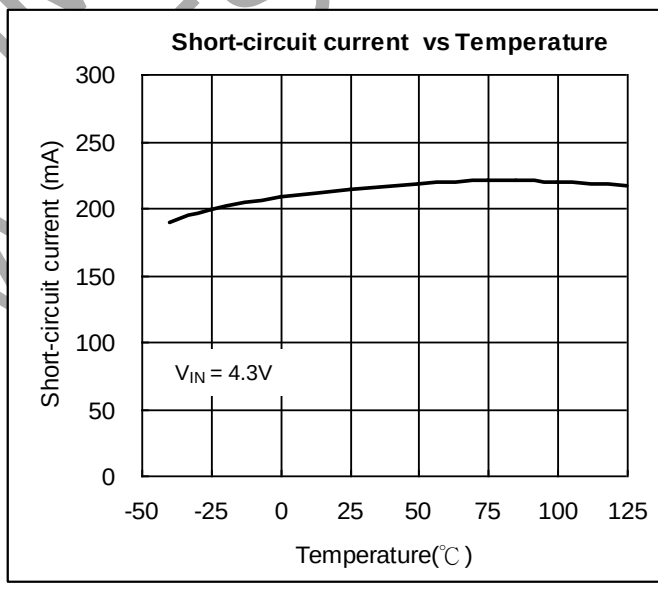


Typical Performance Characteristics (cont.)

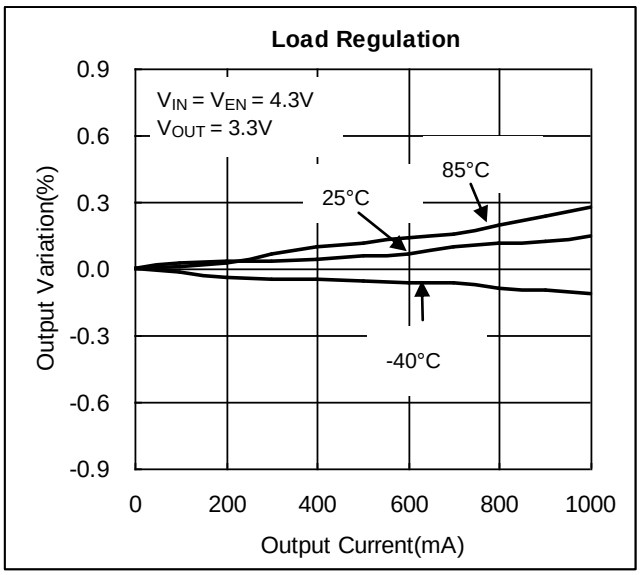


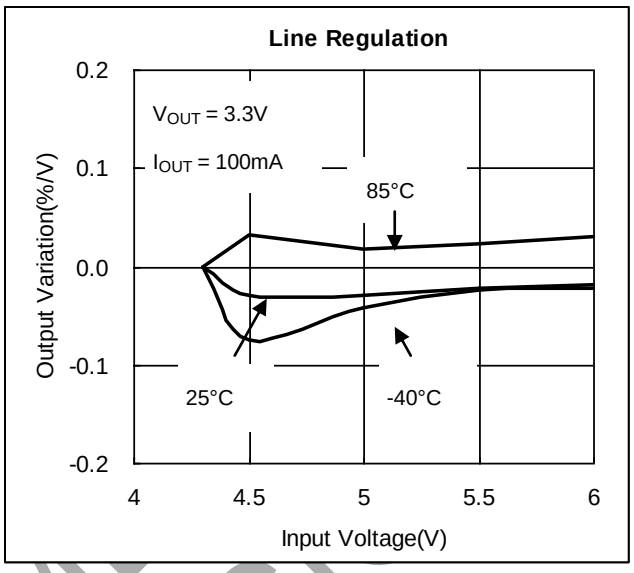


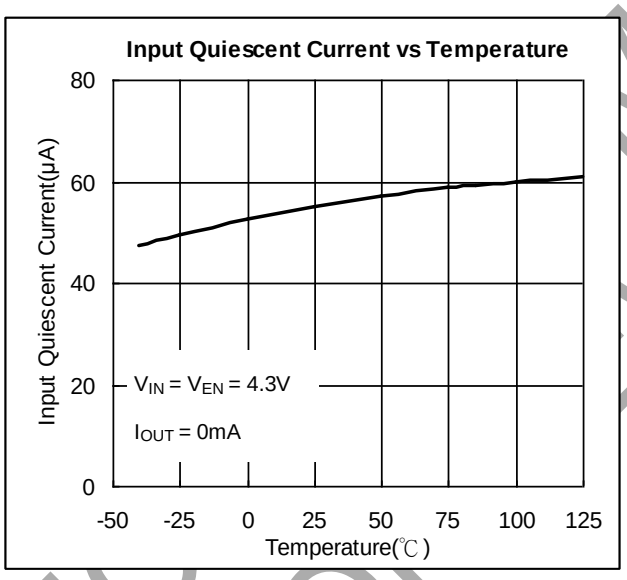


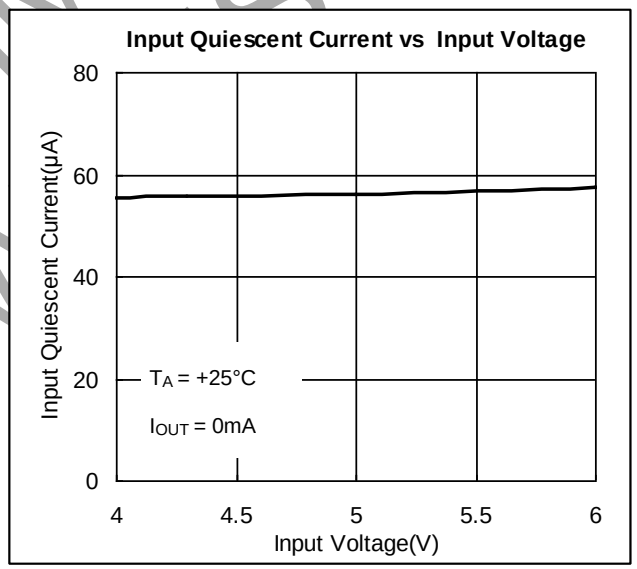


Typical Performance Characteristics (cont.)









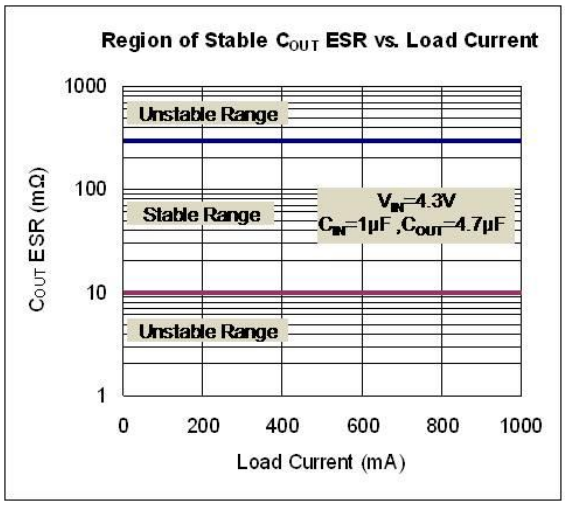
Application Information

Input Capacitor

A 1μF ceramic capacitor is recommended between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both IN and GND pins. A lower ESR capacitor type allows the use of less capacitance, while a higher ESR type requires more capacitance.

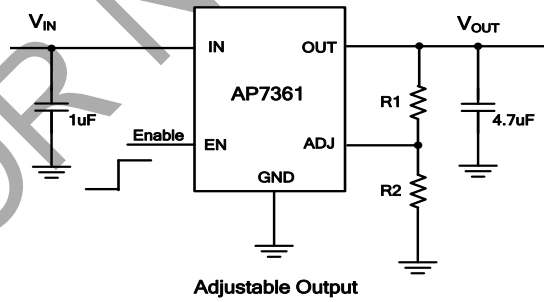
Output Capacitor

The output capacitor is required to stabilize and improve the transient response of the LDO. The AP7361 is stable with very small ceramic output capacitors. Using a ceramic capacitor value that is at least 2.2μF with 10mΩ ≦ ESR ≦ 300mΩ on the output ensures stability. Higher capacitance values help to improve line and load transient response. The output capacitance may be increased to keep low undershoot and overshoot. Output capacitor must be placed as close as possible to OUT and GND pins.



Adjustable Operation

Adjustable operation is not available in the SOT223 TO252 and SO-8EP package. The AP7361 provides output voltage from 0.8V to 5.0V through external resistor divider as shown below.



Adjustable Output

The output voltage is calculated by:

$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_2}\right)$$

Where V_{REF} = 0.8V (the internal reference voltage)

Rearranging the equation will give the following that is used for adjusting the output to a particular voltage:

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}}-1\right)$$

To maintain the stability of the internal reference voltage, R_2 need to be kept smaller than 80kΩ.

Application Information

No Load Stability

Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

ON/OFF Input Operation

The ON/OFF feature is not available in the SOT223 and TO252 package.

The AP7361 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

Current Limit Protection

When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to prevent overcurrent and to protect the regulator from damage due to overheating.

Short-Circuit Protection

When OUT pin is short-circuit to GND, short circuit protection will be triggered and clamp the output current to approximately 200mA. Full current is restored when the output voltage exceeds 15% of Vout. This feature protects the regulator from overcurrent and damage due to overheating.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +150°C, allowing the device to cool down. When the junction temperature reduces to approximately +130°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Ultra Fast Start-up

After enabled, the AP7361 is able to provide full power in as little as tens of microseconds, typically 200µs, without sacrificing low ground current. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

Low Quiescent Current

The AP7361, consuming only around 70µA for all input range, provides great power saving in portable and low power applications.

Power Dissipation

The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The maximum power dissipation, handled by the device, depends on the maximum junction to ambient thermal resistance, maximum ambient temperature, and maximum device junction temperature, which can be calculated by the equation in the following:

$$P_D(max@T_A) = \frac{(+150°C - T_A)}{R_{\theta JA}}$$

Ordering Information

AP7361 - XX XXX - X

Output	Package	Packing
Blank : ADJ 10 : 1.0V 12 : 1.2V 15 : 1.5V 18 : 1.8V 25 : 2.5V 28 : 2.8V 33 : 3.3V	FGE : U-DFN3030-8	7 : Tape & Reel

AP7361 - XX X - XX

Output	Package	Packing
Blank : adj * 10 : 1.0V 12 : 1.2V 15 : 1.5V 18 : 1.8V 25 : 2.5V 28 : 2.8V 33 : 3.3V	DR : TO252R ER : SOT223R	13 : Tape & Reel

AP7361 - XX X - XX

Output	Package	Packing
Blank : ADJ * 10 : 1.0V 12 : 1.2V 15 : 1.5V 18 : 1.8V 25 : 2.5V 28 : 2.8V 33 : 3.3V	Y : SOT89-5 D : TO252 E : SOT223 SP : SO-8EP	13 : Tape & Reel

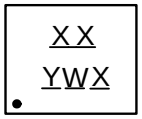
* adjustable only in SOT89-5

Part Number	Package Code	Packaging	7"/13" Tape and Reel	
			Quantity	Part Number Suffix
AP7361-XXFGE-7	FGE	U-DFN3030-8	3,000/Tape & Reel	-7
AP7361-XXY-13	Y	SOT89-5	2,500/Tape & Reel	-13
AP7361-XXD-13	D	TO252	2,500/Tape & Reel	-13
AP7361-XXDR-13	DR	TO252R	2,500/Tape & Real	-13
AP7361-XXE-13	E	SOT223	2,500/Tape & Reel	-13
AP7361-XXER-13	ER	SOT223R	2,500/Tape & Reel	-13
AP7361-XXSP-13	SP	SO-8EP	2,500/Tape & Reel	-13

Marking Information

(1) U-DFN3030-8

(Top View)

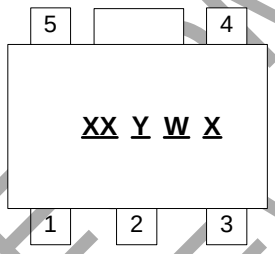


XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : A~Z : Internal code

Device	Package	Identification Code
AP7361ADJ	U-DFN3030-8	PA
AP7361-10	U-DFN3030-8	PB
AP7361-12	U-DFN3030-8	PC
AP7361-15	U-DFN3030-8	PD
AP7361-18	U-DFN3030-8	PE
AP7361-25	U-DFN3030-8	PF
AP7361-28	U-DFN3030-8	PG
AP7361-33	U-DFN3030-8	PH

(2) SOT89-5

(Top View)



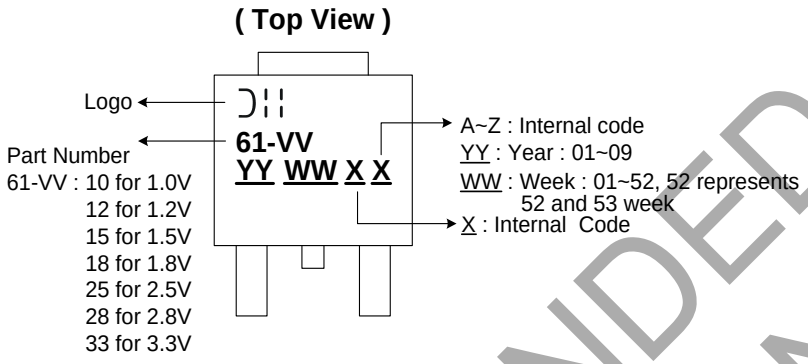
XX : Identification code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week;
z represents 52 and 53 week
X : A~Z : Internal code

Device	Package	Identification Code
AP7361ADJ	SOT89-5	PA
AP7361-10	SOT89-5	PB
AP7361-12	SOT89-5	PC
AP7361-15	SOT89-5	PD
AP7361-18	SOT89-5	PE
AP7361-25	SOT89-5	PF
AP7361-28	SOT89-5	PG
AP7361-33	SOT89-5	PH

Marking Information (cont.)

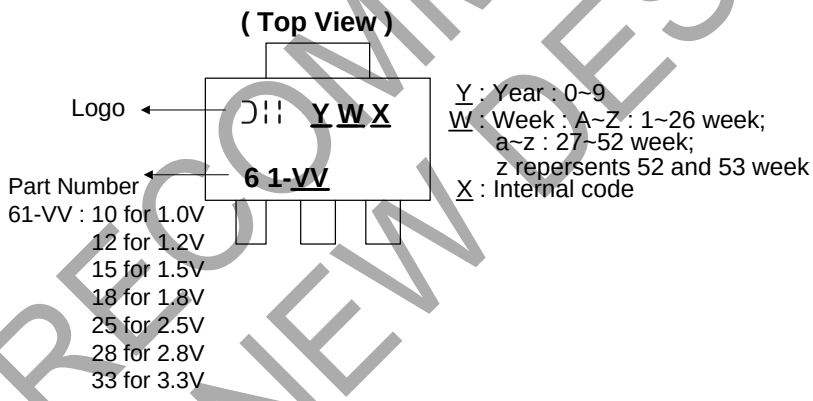
(3) TO252

Pin 1: V_{IN}, Pin 2: GND, Pin 3: V_{OUT}



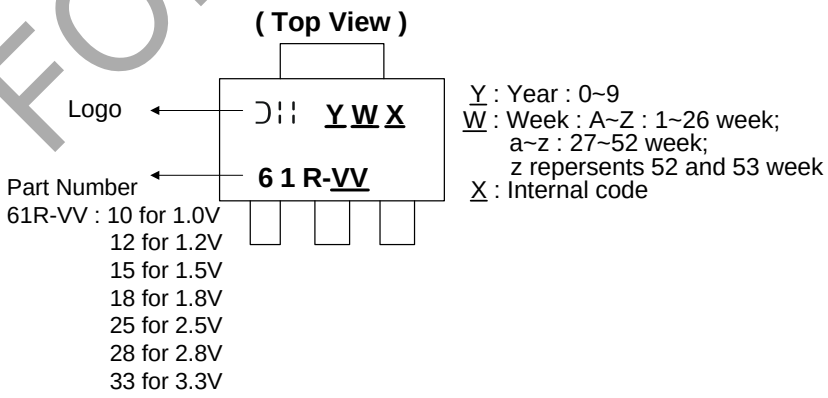
(4) SOT223

Pin 1: V_{IN}, Pin 2: GND, Pin 3: V_{OUT}



(5) SOT223R

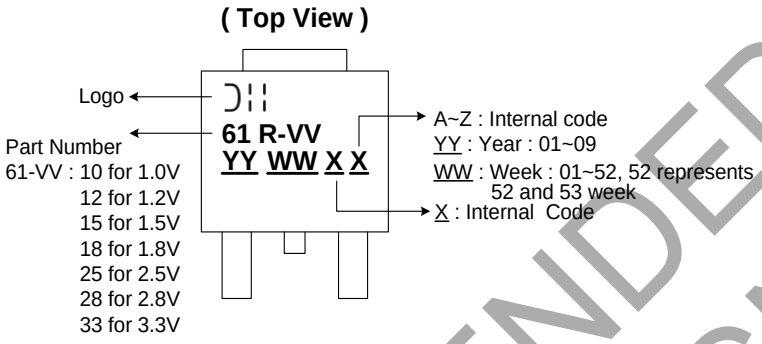
Pin 1: GND, Pin 2: V_{OUT}, Pin 3: V_{IN}



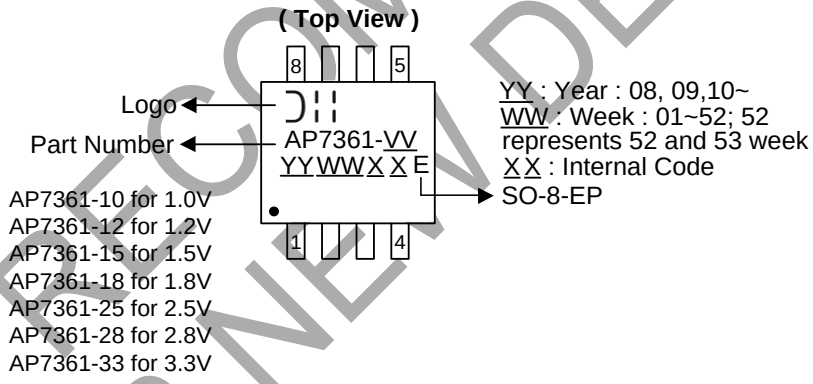
Marking Information (cont.)

(6) TO252-R

Pin 1: GND, Pin 2: V_{OUT}, Pin 3: V_{IN}



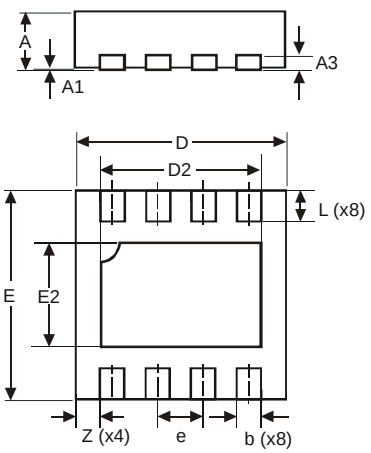
(7) SO-8EP



Package Outline Dimensions (All dimensions in mm.)

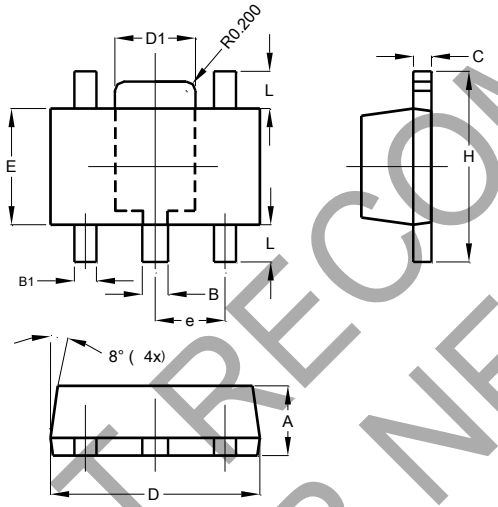
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1): U-DFN3030-8



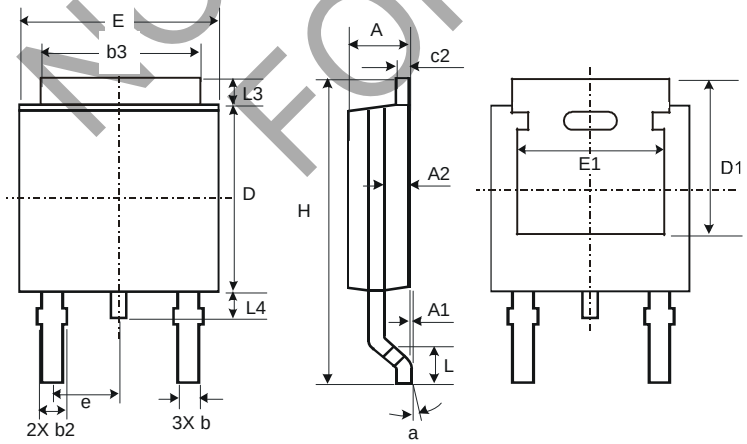
U-DFN3030-8 Type E			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	–	–	0.15
b	0.20	0.30	0.25
D	2.95	3.05	3.00
D2	2.15	2.35	2.25
E	2.95	3.05	3.00
e	–	–	0.65
E2	1.40	1.60	1.50
L	0.30	0.60	0.45
Z	–	–	0.40
All Dimensions in mm			

(2): SOT89-5



SOT89-5			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.60	1.50
B	0.50	0.62	0.56
B1	0.44	0.54	0.48
C	0.35	0.43	0.38
D	4.40	4.60	4.50
D1	1.62	1.83	1.733
E	2.40	2.60	2.50
e	-	-	1.50
H	3.95	4.25	4.10
L	0.65	0.95	0.80
All Dimensions in mm			

(3): TO252

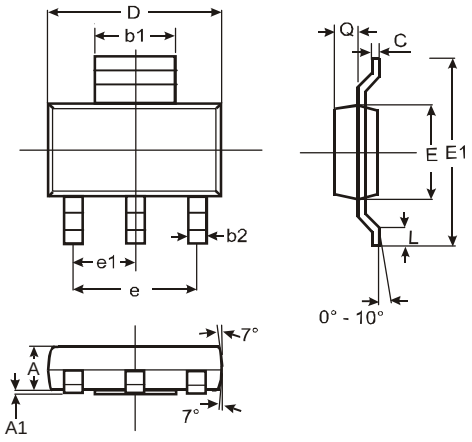


TO252			
Dim	**Min**	**Max**	**Typ**
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c2	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	–	–
e	–	–	2.286
E	6.45	6.70	6.58
E1	4.32	–	–
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	–
All Dimensions in mm			

Package Outline Dimensions (cont.) (All dimensions in mm.)

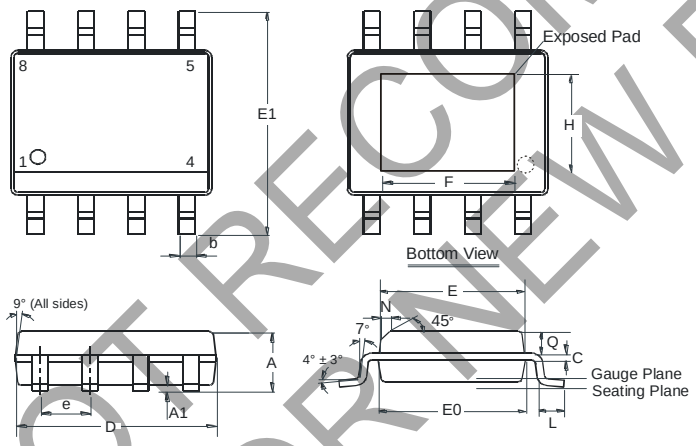
Please see http://www.diodes.com/package-outlines.html for the latest version.

(4): SOT223 and SOT223R



SOT223			
Dim	**Min**	**Max**	**Typ**
A	1.55	1.65	1.60
A1	0.010	0.15	0.05
b1	2.90	3.10	3.00
b2	0.60	0.80	0.70
C	0.20	0.30	0.25
D	6.45	6.55	6.50
E	3.45	3.55	3.50
E1	6.90	7.10	7.00
e	—	—	4.60
e1	—	—	2.30
L	0.85	1.05	0.95
Q	0.84	0.94	0.89
All Dimensions in mm			

(5): SO-8EP

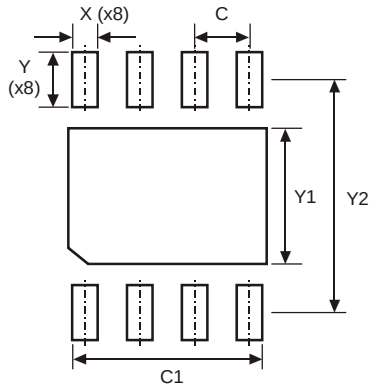


SO-8EP (SOP-8L-EP)			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

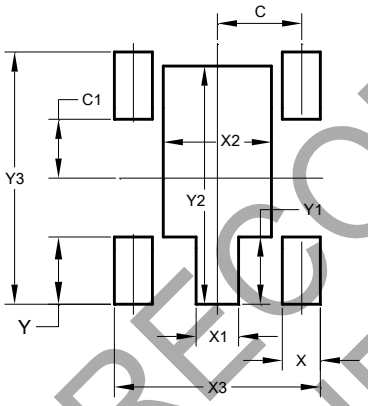
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1): U-DFN3030-8



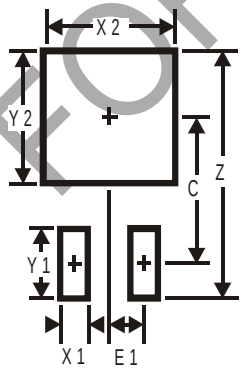
Dimensions	Value (in mm)
C	0.65
C1	2.35
X	0.30
Y	0.65
Y1	1.60
Y2	2.75

(2): SOT89-5



Dimensions	Value (in mm)
C	1.500
C1	1.050
X	0.680
X1	0.760
X2	1.930
X3	3.680
Y	1.200
Y1	1.200
Y2	4.250
Y3	4.500

(3): TO252

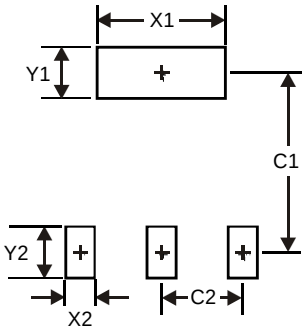


Dimensions	Value (in mm)
Z	11.6
X1	1.5
X2	7.0
Y1	2.5
Y2	7.0
C	6.9
E1	2.3

Suggested Pad Layout (cont.)

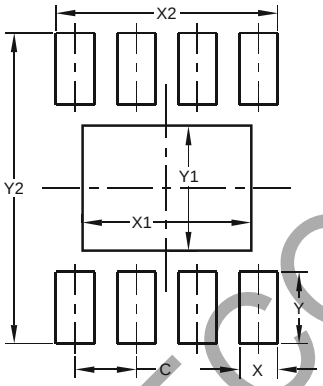
Please see http://www.diodes.com/package-outlines.html for the latest version.

(4): SOT223 and SOT223R



Dimensions	Value (in mm)
X1	3.3
X2	1.2
Y1	1.6
Y2	1.6
C1	6.4
C2	2.3

(5): SO-8EP



Dimensions	Value(in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

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