LMH6570 2:1 High Speed Video Multiplexer

1 Features

- 500 MHz, 500 mV_{PP}, −3 dB Bandwidth, A_V=2
- 400 MHz, 2V_{PP}, −3 dB Bandwidth, A_V=2
- 8 ns Channel Switching Time
- 70 dB Channel to Channel Isolation @ 10 MHz
- 0.02%, 0.05° Diff. Gain, Diff. Phase
- 0.1 dB Gain Flatness to 150 MHz
- 2200 V/µs Slew Rate
- Wide Supply Voltage Range: 6 V (±3 V) to 12 V (±6 V)
- −68 dB HD2 @ 5 MHz
- −84 dB HD3 @ 5 MHz

2 Applications

- Video Router
- Multi Input Video Monitor
- Instrumentation / Test Equipment
- Receiver IF Diversity Switch
- Multi Channel A/D Driver
- Picture in Picture Video Switch

3 Description

The LMH6570 is a high performance analog multiplexer optimized for professional grade video and other high fidelity, high bandwidth analog applications. The output amplifier selects one of two buffered input signals based on the state of the SEL pin. The LMH6570 provides a 400 MHz bandwidth at 2-V_{PP} output signal levels. Multimedia and high definition television (HDTV) applications can benefit from the 0.1-dB bandwidth of 150 MHz and the 2200-V/µs slew rate of LMH6570.

The LMH6570 supports composite video applications with its 0.02% and 0.05° differential gain and phase errors for NTSC and PAL video signals while driving a single, back terminated 75-Ω load. An 80-mA linear output current is available for driving multiple video load applications.

The LMH6570 gain is set by external feedback and gain set resistors for maximum flexibility.

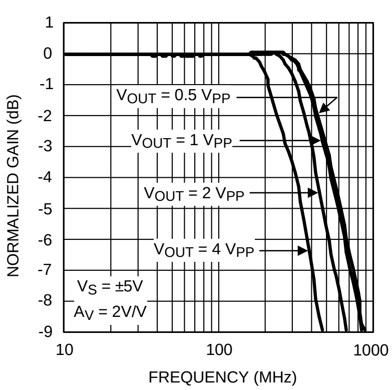
The LMH6570 is available in the 8-pin SOIC package.

Device Information(1)

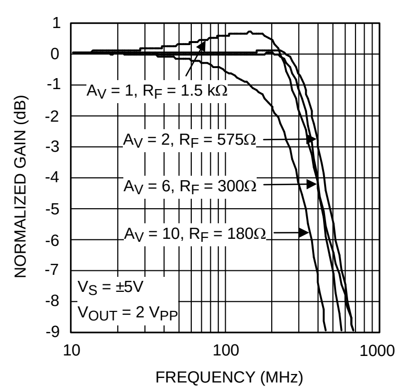
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6570	SOIC (8)	4.9 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Frequency Response vs. V_{OUT}



Frequency Response vs. Gain



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2013) to Revision D — **Page**

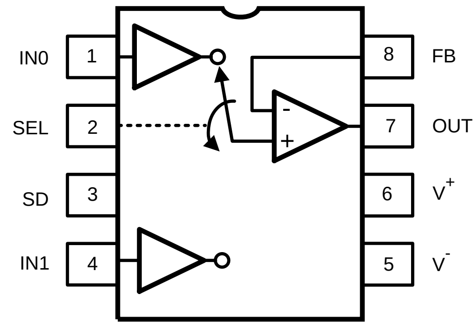
- Added the following sections: Device Information Table; *Power Supply Recommendations*; *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* 1
- Revised text in *Application and Implementation* section, formerly titled "Application Notes" 12
- Revised text in *Multiplexer Expansion* section. Added Figure 27, Figure 28, and Figure 29 14

Changes from Revision B (April 2013) to Revision C — **Page**

- Changed layout of National Data Sheet to TI format 18

5 Pin Configuration and Functions

8-Pin SOIC
D Package
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN0	I	Input Channel 0
2	SEL	I	Select Pin
3	SD	I	Shutdown
4	IN1	I	Input Channel 1
5	V^-	I	V^- Supply
6	V^+	I	V^+ Supply
7	OUT	O	Output
8	FB	I	Feedback

Truth Table

SEL	SD	OUTPUT
1	0	IN1 * (1+RF/RG)
0	0	IN0 * (1+RF/RG)
X	1	Shutdown

6 Specifications

6.1 Absolute Maximum Ratings[(1)(2)]

		MIN	MAX	UNIT
Supply Voltage ($V^+ - V^-$)			13.2	V
I_{OUT}[(3)]			130	mA
Signal & Logic Input Pin Voltage			±(V_S + 0.6)	V
Signal & Logic Input Pin Current			±20	mA
Maximum Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Soldering Information	Infrared or Convection (20 sec)		235	°C
	Wave Soldering (10 sec)		260	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See *Power Dissipation* for more details. A short circuit condition should be limited to 5 seconds or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Machine model (MM)[(2)]	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance. Human body model, 1.5kΩ in series with 100 pF.
(2) Machine model, 0 Ω In series with 200 pF

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating Temperature	−40		85	°C
Supply Voltage	6		12	V

6.4 Thermal Information

THERMAL METRIC[(1)]		D	UNIT
		8 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	150	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	50	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics ±5V

V_S = ±5 V, R_L = 100 Ω, R_F = 576 Ω, A_V = 2 V/V, T_J = 25 °C, unless otherwise specified.

PARAMETER		TEST CONDITIONS[1]		MIN[2]	TYP[3]	MAX[2]	UNIT
FREQUENCY DOMAIN PERFORMANCE							
SSBW	−3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}			500		MHz
LSBW	–3 dB Bandwidth	V_{OUT} = 2 V_{PP}[4]			400		MHz
.1 dBBW	0.1 dB Bandwidth	V_{OUT} = 0.25 V_{PP}			150		MHz
DG	Differential gain	R_L = 150 Ω, f = 4.43 MHz			0.02%		
DP	Differential phase	R_L = 150 Ω, f = 4.43 MHz			0.05		deg
XTLK	Channel to channel crosstalk	All Hostile, f = 5 MHz			−70		dBc
TIME DOMAIN RESPONSE							
T_{RS}	Channel to channel switching time	Logic transition to 90% output			8		ns
	Enable and disable times	Logic transition to 90% or 10% output.			10		ns
T_{RL}	Rise and fall time	4 V Step			2.4		ns
T_{SS}	Settling time to 0.05%	2 V Step			17		ns
OS	Overshoot	2 V Step			5%		
SR	Slew rate	4 V Step[4][5]			2200		V/µs
DISTORTION							
HD2	2^{nd} Harmonic distortion	2 V_{PP} , 5 MHz			−68		dBc
HD3	3^{rd} Harmonic distortion	2 V_{PP} , 5 MHz			−84		dBc
IMD	3^{rd} Order intermodulation products	10 MHz, Two tones 2 Vpp at output			−80		dBc
EQUIVALENT INPUT NOISE							
VN	Voltage	>1 MHz, Input Referred			5		nV√HZ
ICN	Current	>1 MHz, Input Referred			5		pA/√Hz
STATIC, DC PERFORMANCE							
CHGM	Channel to channel gain difference	DC, Difference in gain between channels			±0.005%	±0.034%	
			-40°C ≤ T_J ≤ 85°C			±0.036%	
V_{IO}	Input offset voltage	V_{IN} = 0 V			1	±15	mV
			-40°C ≤ T_J ≤ 85°C			±21	
DVIO	Offset voltage drift[6]				30		µV/°C
IBN	Input bias current[7]	V_{IN} = 0 V			−3	±8	µA
			-40°C ≤ T_J ≤ 85°C			±10	
DIBN	Bias current drift[6]				11		nA/°C

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A. See Thermal Information for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical numbers are the most likely parametric norm.
(4) Parameter ensured by design.
(5) Slew Rate is the average of the rising and falling edges.
(6) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(7) Positive Value is current into device.

Electrical Characteristics ±5V (continued)

V_S = ±5 V, R_L = 100 Ω, R_F = 576 Ω, A_V = 2 V/V, T_J = 25 °C, unless otherwise specified.

PARAMETER		TEST CONDITIONS (1)		MIN (2)	TYP (3)	MAX (2)	UNIT
I_{BI}	Inverting input bias current (7)	Pin 8, Feedback point, V_{IN} = 0 V			−3	±18	uA
			-40°C ≤ T_J ≤ 85°C			±22	
PSRR	Power supply rejection ratio	DC, Input referred		48	50		dB
			-40°C ≤ T_J ≤ 85°C	46			
ICC	Supply current	No Load, Shutdown Pin (SD) > 0.8 V			13.8	15	mA
			-40°C ≤ T_J ≤ 85°C			16	
	Supply current shutdown	Shutdown Pin (SD) > 2 V			1.1	1.3	mA
			-40°C ≤ T_J ≤ 85°C			1.4	
V_{IH}	Logic high threshold	Select Pin & Shutdown pin (SEL, SD)		2.0			V
V_{IL}	Logic low threshold	Select Pin & Shutdown pin (SEL, SD)				0.8	V
I_{iL}	Logic pin input current low (7)	Logic Input = 0 V Select Pin & Shutdown Pin (SEL, SD)		−8	−1		µA
			-40°C ≤ T_J ≤ 85°C	-10			
I_{iH}	Logic pin input current high (7)	Logic Input = 5.0 V, Select Pin & Shutdown Pin (SEL, SD)			57	68	µA
			-40°C ≤ T_J ≤ 85°C			75	
MISCELLANEOUS PERFORMANCE							
RIN+	Input resistance				5		kΩ
CIN	Input capacitance				0.8		pF
R_{OUT}	Output resistance	Output Active, (SD < 0.8 V)			0.04		Ω
R_{OUT}	Output resistance	Output Disabled, (SD > 2 V)			3000		Ω
C_{OUT}	Output capacitance	Output Disabled, (SD > 2 V)			3.1		pF
V_O	Output voltage range	No Load		±3.51	±3.7		V
			-40°C ≤ T_J ≤ 85°C	±3.50			
V_{OL}		R_L = 100 Ω		±3.16	±3.5		V
			-40°C ≤ T_J ≤ 85°C	±3.15			
CMIR	Input voltage range			±2.5	±2.6		V
I_O	Linear output current (7)	V_{IN} = 0 V		+60	±80		mA
				-70			
			-40°C ≤ T_J ≤ 85°C	±55			
I_{SC}	Short circuit current (8)	V_{IN} = ±2 V, Output shorted to ground			±230		mA

(8) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See *Power Dissipation* for more details. A short circuit condition should be limited to 5 seconds or less.

6.6 Electrical Characteristics ±3.3V

V_S = ±3.3 V, R_L = 100 Ω, R_F = 576 Ω, A_V = 2 V/V, unless otherwise specified.

PARAMETER		TEST CONDITIONS(1)	MIN(2)	TYP(3)	MAX(2)	UNIT
FREQUENCY DOMAIN PERFORMANCE						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		475		MHz
LSBW	−3 dB Bandwidth	V_{OUT} = 2.0 V_{PP}		375		MHz
0.1 dBBW	0.1 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		100		MHz
GFP	Peaking	DC to 200 MHz		0.4		dB
XTLK	Channel to channel crosstalk	All Hostile, f = 5 MHz		−70		dBc
TIME DOMAIN RESPONSE						
T_{RL}	Rise and Fall time	2 V Step		2		ns
T_{SS}	Settling time to 0.05%	2 V Step		20		ns
OS	Overshoot	2 V Step		5%		
SR	Slew rate	2 V Step		1400		V/µs
DISTORTION						
HD2	2nd Harmonic distortion	2 V_{PP}, 10 MHz		−67		dBc
HD3	3rd Harmonic distortion	2 V_{PP}, 10 MHz		−87		dBc
STATIC, DC PERFORMANCE						
V_{IO}	Input offset voltage	V_{IN} = 0 V		1		mV
IBN	Input bias current(4)	V_{IN} = 0 V		-3		µA
PSRR	Power supply rejection ratio	DC, Input Referred		49		dB
ICC	Supply current	No Load		12.5		mA
V_{IH}	Logic high threshold	Select Pin & Shutdown pin (SEL, SD), $V_{IH} \cong V^+ * 0.4$		1.3		V
V_{IL}	Logic low threshold	Select Pin & Shutdown pin (SEL, SD), $V_{IL} \cong V^+ * 0.12$		0.4		V
MISCELLANEOUS PERFORMANCE						
R_{IN+}	Input resistance			5		kΩ
C_{IN}	Input capacitance			0.8		pF
R_{OUT}	Output resistance			0.06		Ω
V_O	Output voltage range	No Load		±2		V
V_{OL}		R_L = 100 Ω		±1.8		V
CMIR	Input voltage range			±1.2		V
I_O	Linear output current(5)	V_{IN} = 0 V		±60		mA
I_{SC}	Short circuit current(5)	V_{IN} = ±1 V, Output shorted to ground		±150		mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Thermal Information for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical numbers are the most likely parametric norm.
(4) Positive Value is current into device.
(5) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See *Power Dissipation* for more details. A short circuit condition should be limited to 5 seconds or less.

6.7 Typical Performance Characteristics

V_s = ±5 V, R_L = 100 Ω, A_V = 2, R_F = R_G = 576 Ω, unless otherwise specified.

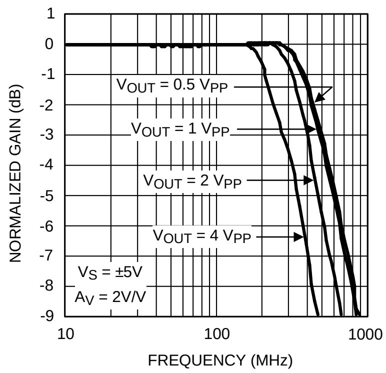


Figure 1. Frequency Response vs. V_{OUT}

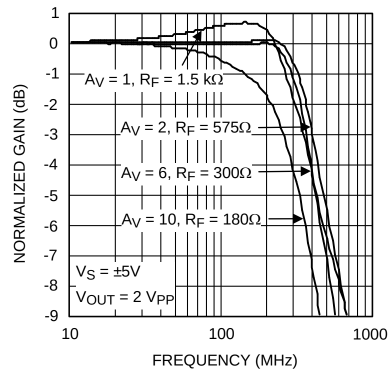


Figure 2. Frequency Response vs. Gain

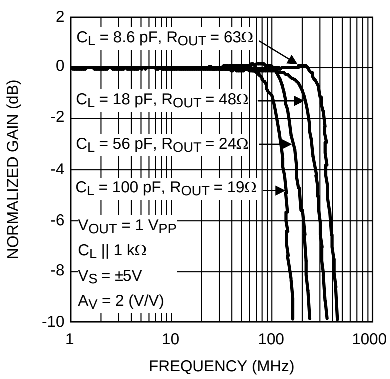


Figure 3. Frequency Response vs. Capacitive Load

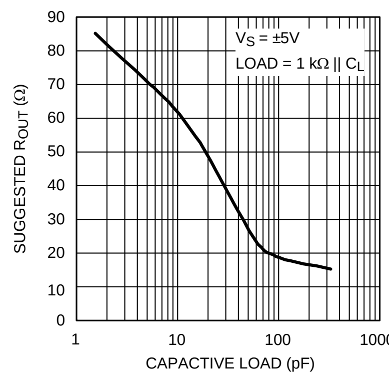


Figure 4. Suggested R_{OUT} vs. Capacitive Load

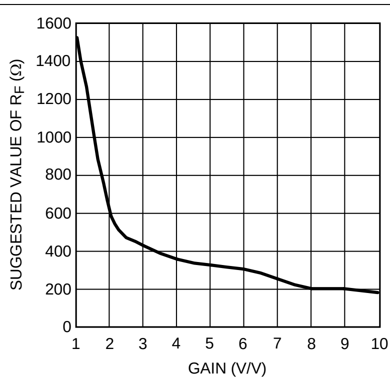


Figure 5. Suggested Value of R_F vs. Gain

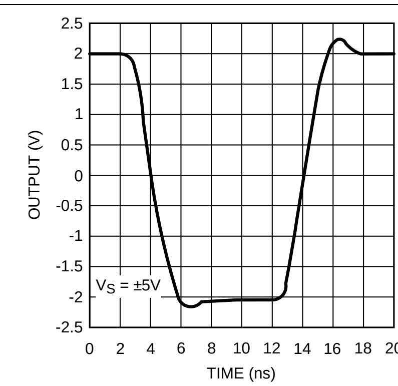


Figure 6. Pulse Response $4V_{PP}$

Typical Performance Characteristics (continued)

V_s = ±5 V, R_L = 100 Ω, A_V = 2, R_F = R_G = 576 Ω, unless otherwise specified.

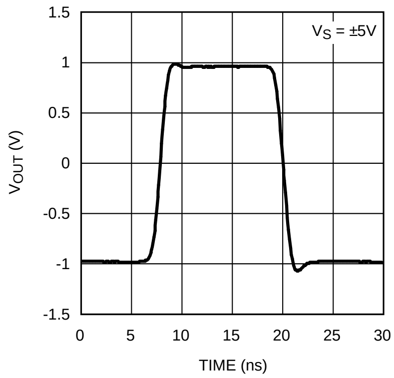


Figure 7. Pulse Response 2V_{PP}

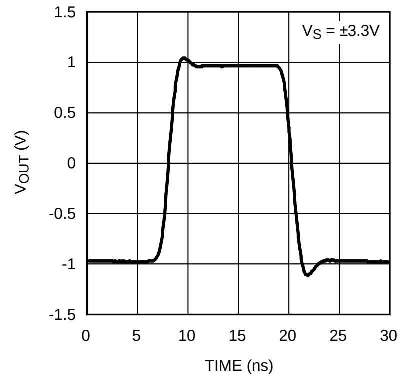


Figure 8. Pulse Response 2V_{PP}

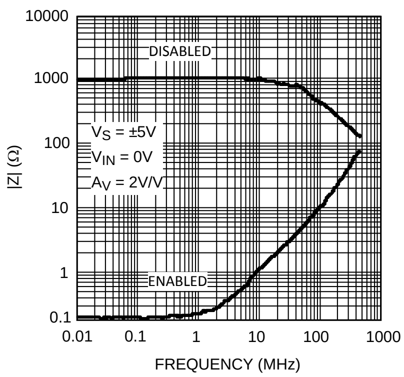


Figure 9. Closed Loop Output Impedance

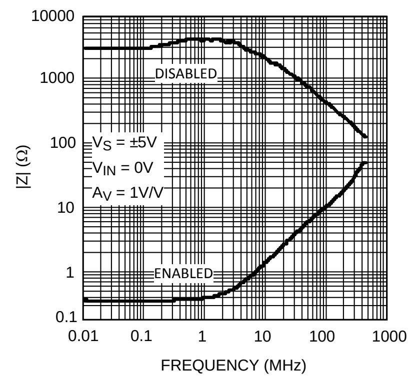


Figure 10. Closed Loop Output Impedance

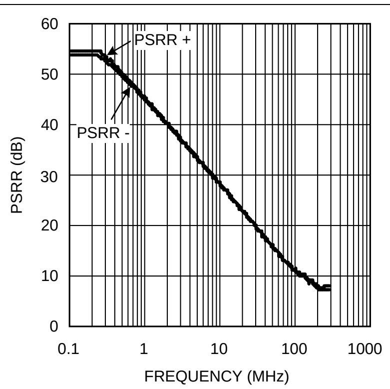


Figure 11. PSRR vs. Frequency

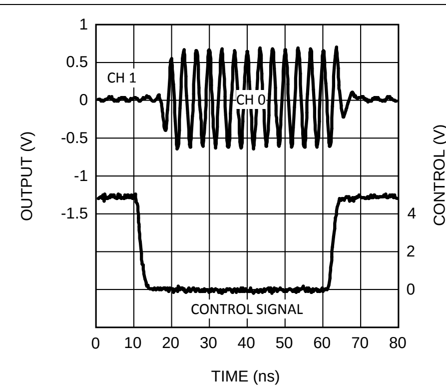


Figure 12. Channel Switching

Typical Performance Characteristics (continued)

V_s = ±5 V, R_L = 100 Ω, A_V = 2, R_F = R_G = 576 Ω, unless otherwise specified.

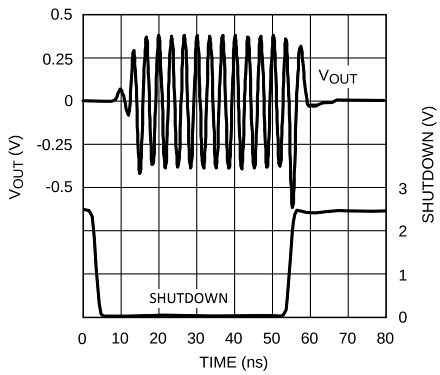


Figure 13. SHUTDOWN Switching

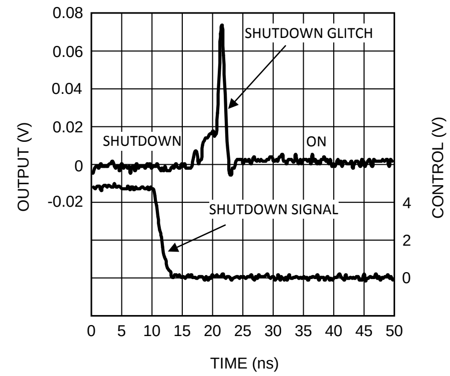


Figure 14. Shutdown Glitch

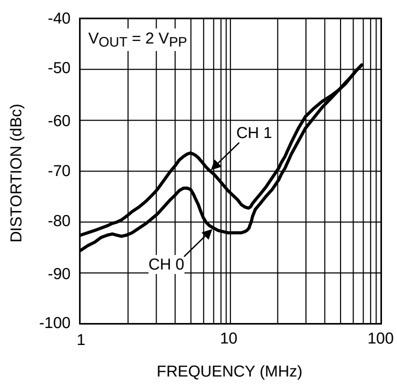


Figure 15. HD2 vs. Frequency

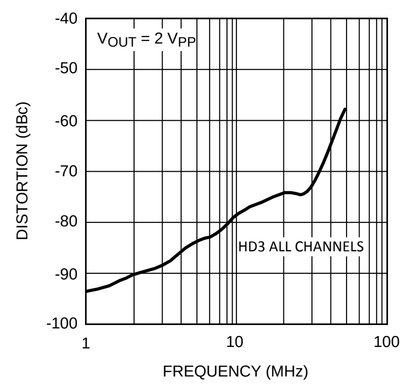


Figure 16. HD3 vs. Frequency

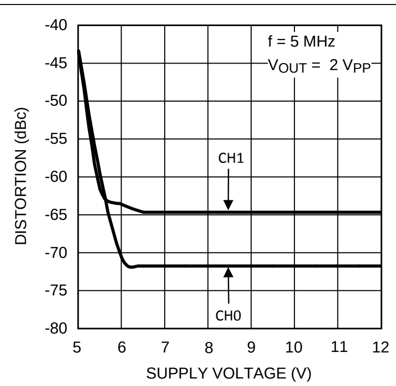


Figure 17. HD2 vs. V_S

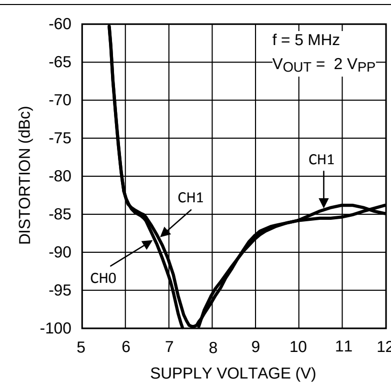


Figure 18. HD3 vs. V_S

Typical Performance Characteristics (continued)

V_S = ±5 V, R_L = 100 Ω, A_V = 2, R_F = R_G = 576 Ω, unless otherwise specified.

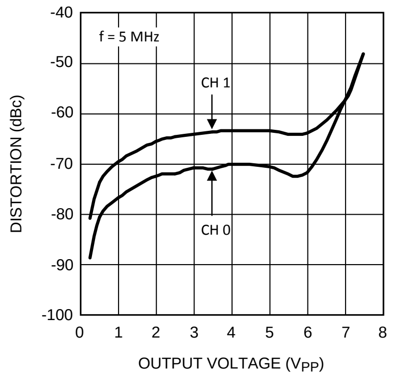


Figure 19. HD2 vs. V_{OUT}

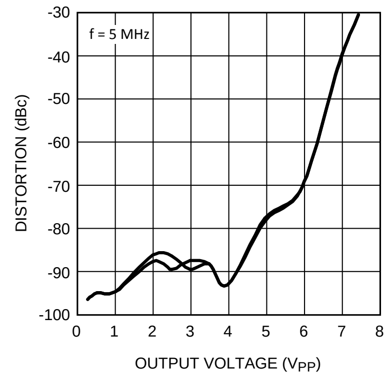
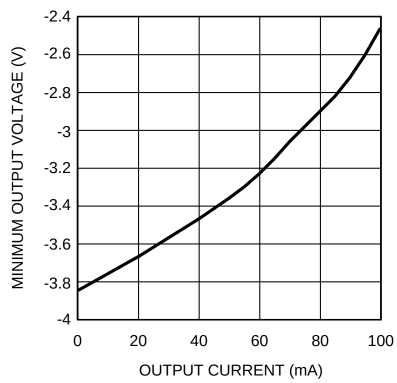
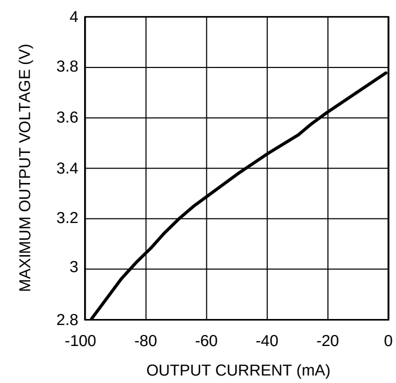


Figure 20. HD3 vs. V_{OUT}



Positive value is current into device

Figure 21. Minimum V_{OUT} vs. I_{OUT}



Positive value is current into device

Figure 22. Maximum V_{OUT} vs. I_{OUT}

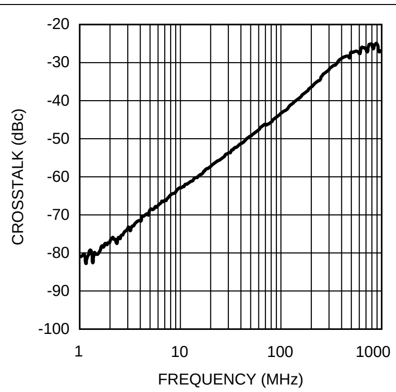


Figure 23. Crosstalk vs. Frequency

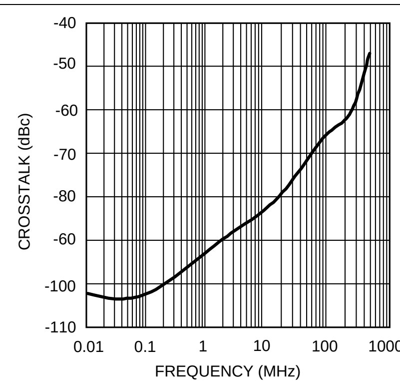


Figure 24. Off Isolation

7 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The LMH6570 is a high-speed 2:1 analog multiplexer, optimized for very high speed and low distortion. With selectable gain and excellent AC performance, the LMH6570 is ideally suited for switching high resolution, presentation grade video signals. The LMH6570 has no internal ground reference. Single or split supply configurations are both possible, however, all logic functions are referenced to the mid supply point. The LMH6570 features very high speed channel switching and disable times. When disabled the LMH6570 output is high impedance making MUX expansion possible by combining multiple devices. See *Multiplexer Expansion*. The LMH6570 SEL defaults to logic low (IN0 active). The default state for the SD pin is also logic low (device enabled). Both pins can be left floating if the default state is desired.

7.2 Typical Application

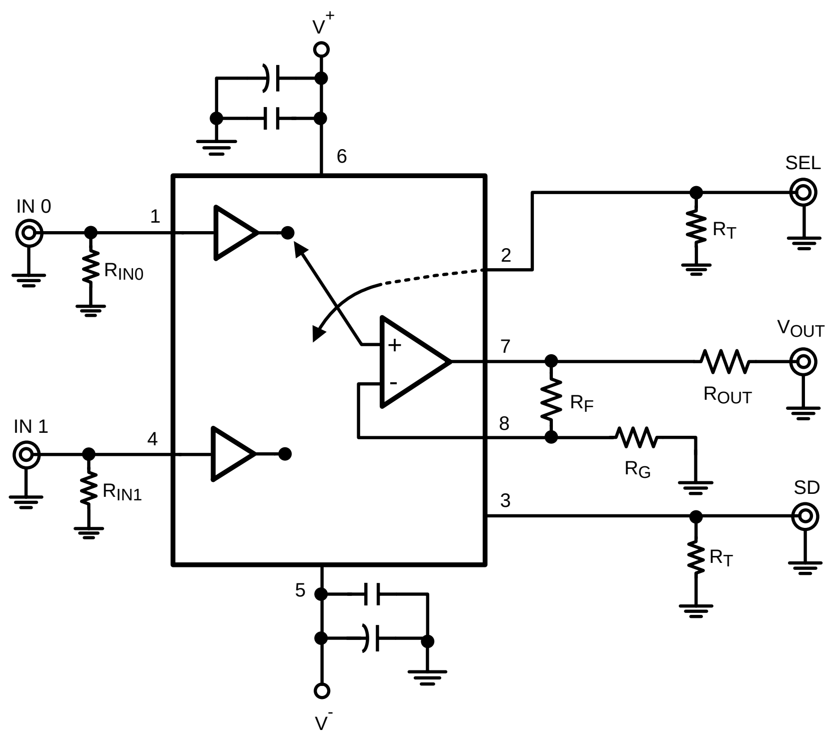


Figure 25. Typical Application

7.2.1 Video Performance

The LMH6570 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 25 shows a typical configuration for driving a 75-Ω cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.

Typical Application (continued)

7.2.2 Feedback Resistor Selection

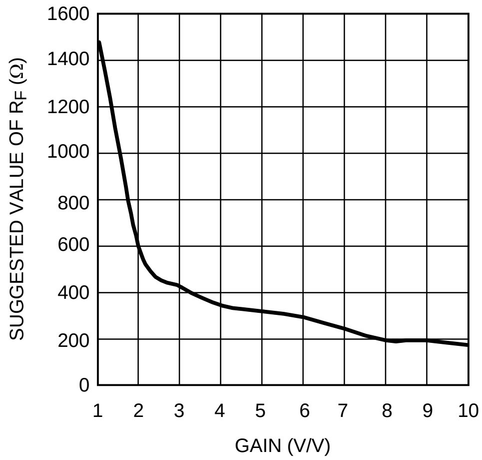


Figure 26. Suggested R_F vs. Gain

The LMH6570 has a current feedback output buffer with gain determined by external feedback (R_F) and gain set (R_G) resistors. With current feedback amplifiers, the closed loop frequency response is a function of R_F. For a gain of 2 V/V, the recommended value of R_F is 576 Ω. For other gains, see Figure 26. Generally, lowering R_F from the recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below the recommended value will cause overshoot, ringing and, eventually, oscillation.

Since all applications are slightly different, it is worth some experimentation to find the optimal R_F for a given circuit. For more information see *Current Feedback Loop Gain Analysis and Performance Enhancement*, Application Note OA-13 (SNOA366), which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The impedance looking into pin 8 is approximately 20 Ω. This allows for good bandwidth at gains up to 10 V/V. When used with gains over 10 V/V, the LMH6570 will exhibit a “gain bandwidth product” similar to a typical voltage feedback amplifier. For gains of over 10 V/V consider selecting a high performance video amplifier like the LMH6720 to provide additional gain.

Typical Application (continued)

7.2.3 Multiplexer Expansion

It is possible to use multiple LMH6570 devices to expand the number of inputs that can be selected for output. Figure 27 shows a 4:1 MUX using two LMH6570 devices.

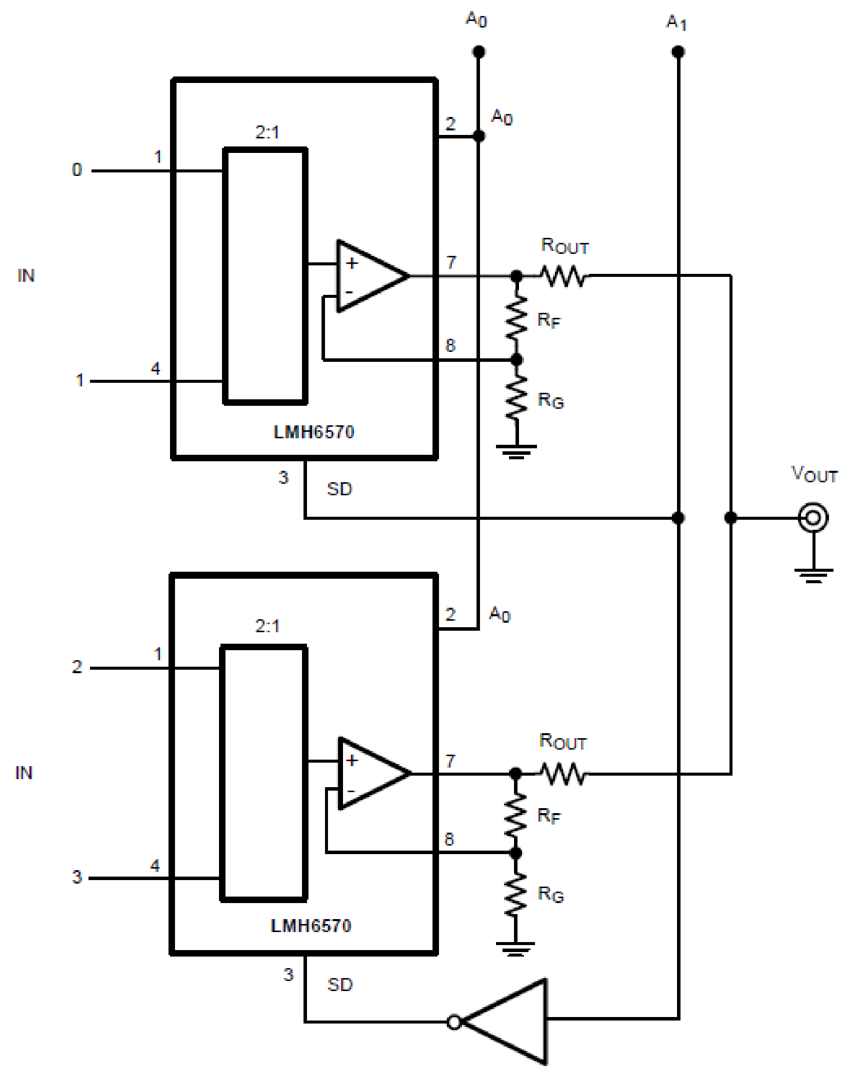


Figure 27. 4:1 MUX Using Two LMH6570 Devices

In such an application, the output settling may be longer than the LMH6570 switching specifications (~20 ns), while switching between two separate LMH6570 devices. The switching time limiting factor occurs when one LMH6570 is turned off and another one is turned on, using the SD (shutdown) pin. The output settling time consists of the time needed for the first LMH6570 to enter high impedance state plus the time required for the second LMH6570 output to dissipate left-over output charge of the first device (limited by the output current capability of the second device) and the time needed to settle to the final voltage value.

Typical Application (continued)

While Figure 27 MUX expansion benefits from more isolation, originating from the parasitic loading of the un-selected channels on the selected channel, afforded by individual R_{OUT} on each multiplexer output, this configuration does not produce the fastest transition between individual LMH6570 devices. For fastest transition between LMH6570 devices, the configuration of Figure 28 can be used where the LMH6570 output pins are all shorted together.

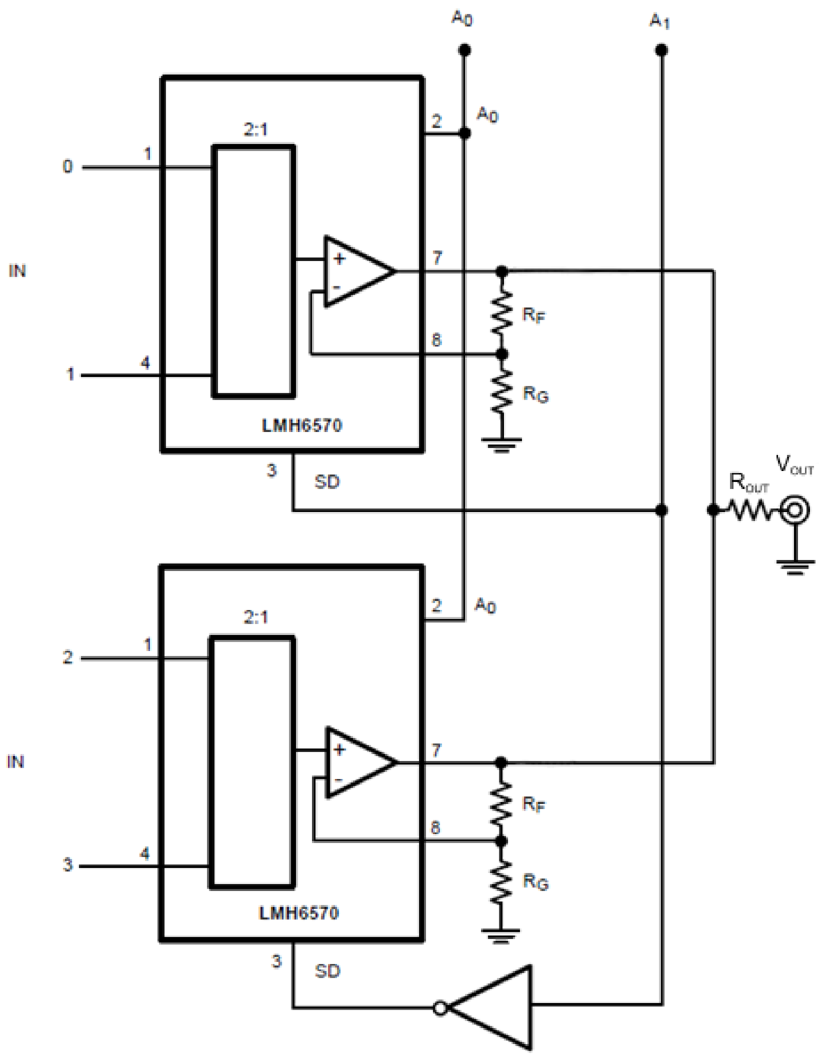


Figure 28. Alternate 4:1 MUX Expansion Schematic (for Faster SD Switching)

Typical Application (continued)

Figure 29 shows typical transition waveforms and shows that SD pin switching settles in less than 145 ns.

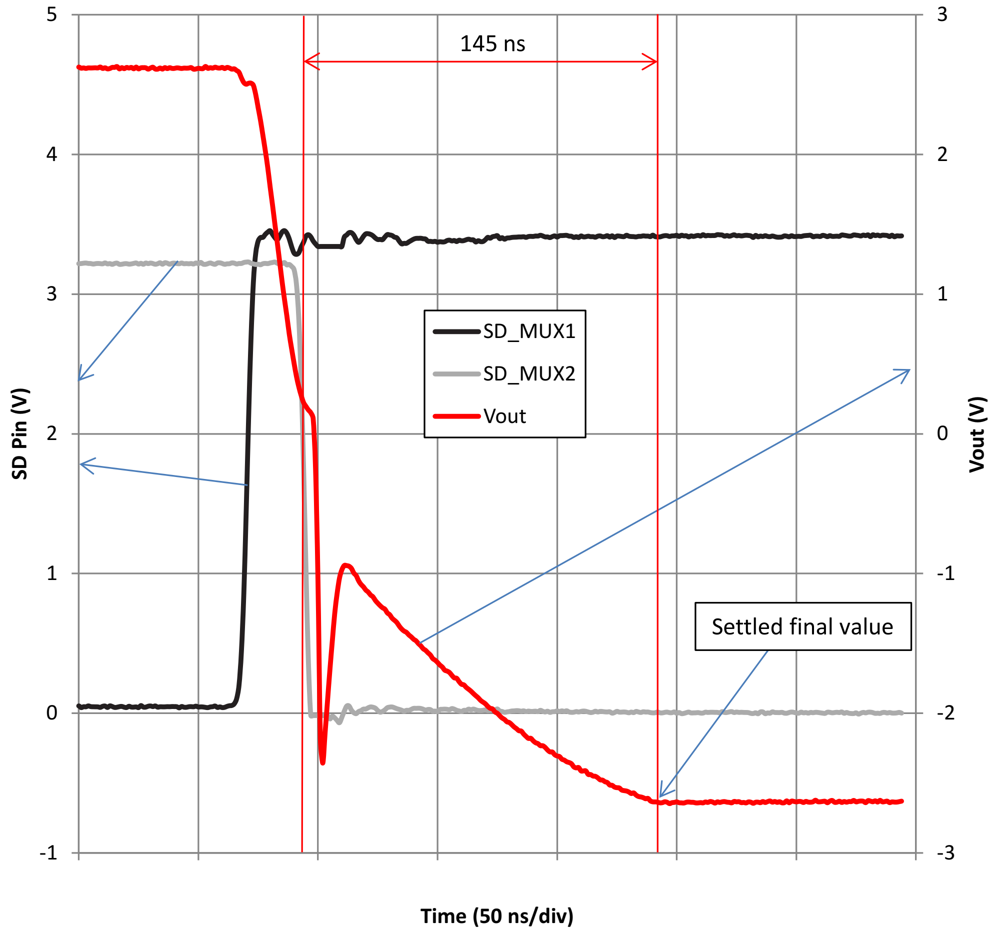


Figure 29. SD pin Switching Waveform and Output Settling

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added, to drive the SHUTDOWN pin of each device. Figure 30 shows one possible approach to this delay circuit. The delay circuit shown will delay H to L transitions of SHUTDOWN (R1 and C1 decay) but will not delay its L to H transition. R2 should be kept small compared to R1 in order to not reduce the SHUTDOWN voltage and to produce little or no delay to SHUTDOWN.

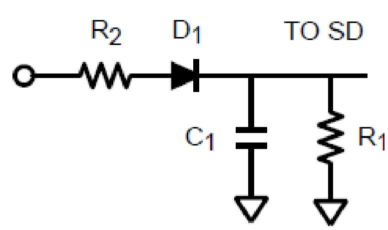


Figure 30. Delay Circuit Implementation

Typical Application (continued)

With the SHUTDOWN pin putting the output stage into a high impedance state, several LMH6570 devices can be tied together to form a larger input MUX. However, there is a loading effect on the active output caused by the unselected devices. The circuit in Figure 31 shows how to compensate for this effect. For the 8:1 MUX function shown in Figure 31, the gain error would be about 0.7% or −0.06dB. In the circuit in Figure 31, resistor ratios have been adjusted to compensate for this gain error. By adjusting the gain of each multiplexer circuit the error can be reduced to the tolerance of the resistors used (1% in this example).

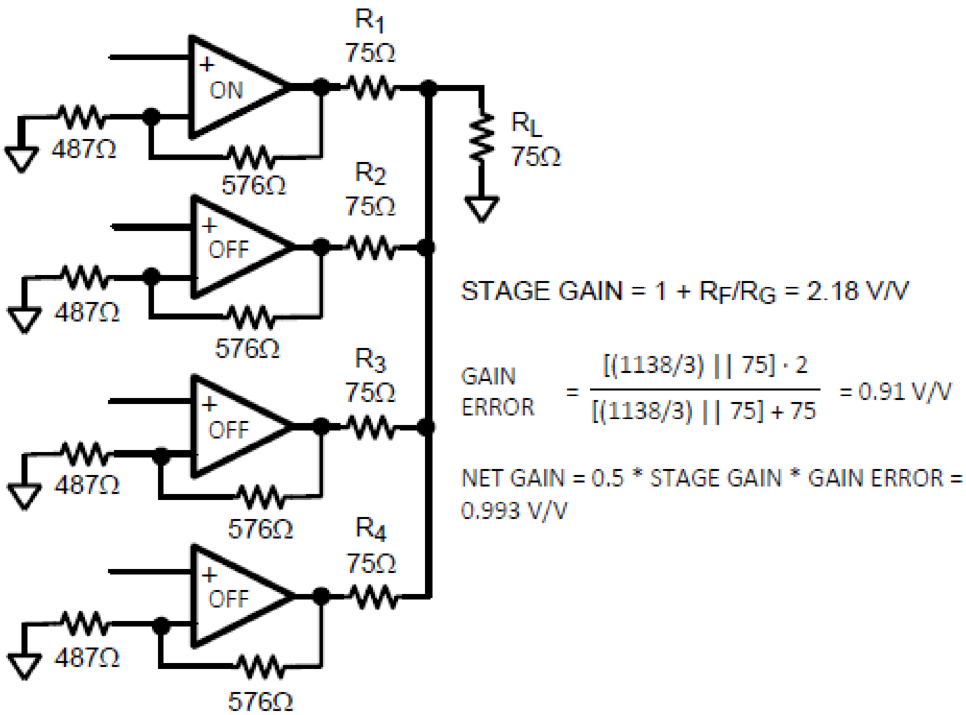


Figure 31. Multiplexer Gain Compensation

NOTE

Disabling of the LMH6570 using the EN pin is not recommended for use when doing multiplexer expansion. While disabled, If the voltage between the selected input and the chip output exceeds approximately 2 V the device will begin to enter a soft breakdown state. This will show up as reduced input to output isolation. The signal on the non-inverting input of the output driver amplifier will leak through to the inverting input, and then to the output through the feedback resistor. The worst case is a gain of 1 configuration where the non-inverting input follows the active input buffer and (through the feedback resistor) the inverting input follows the voltage driving the output stage. The solution for this is to use shutdown mode for multiplexer expansion.

7.2.4 Other Applications

The LMH6570 could support a dual antenna receiver with two physically separate antennas. Monitoring the signal strength of the active antenna and switching to the other antenna when a fade is detected is a simple way to achieve spacial diversity. This method gives about a 3 dB boost in average signal strength and is the least expensive method for combining signals.

Typical Application (continued)

7.2.5 Driving Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. Figure 32 shows the use of a series output resistor, R_{OUT}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 33 gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

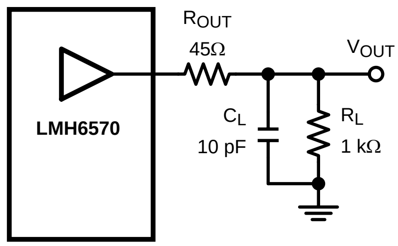


Figure 32. Decoupling Capacitive Loads

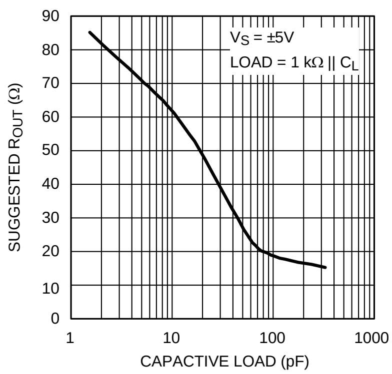


Figure 33. Suggested R_{OUT} vs. Capacitive Load

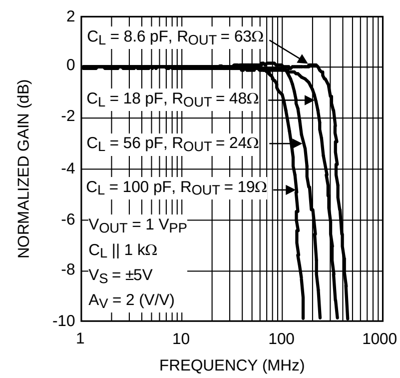


Figure 34. Frequency Response vs. Capacitive Load

7.2.6 ESD Protection

The LMH6570 is protected against electrostatic discharge (ESD) on all pins. The LMH6570 will survive 2000-V Human Body model and 200-V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. However, there are occasions when the ESD diodes will be evident. If the LMH6570 is driven by a large signal while the device is powered down, the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device. Therefore, it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

8 Power Supply Recommendations

8.1 Power Dissipation

The LMH6570 is optimized for maximum speed and performance in the small form factor of the standard SOIC package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the maximum power dissipation for the LMH6570:

1. Calculate the quiescent (no-load) power:

   $P_{AMP} = I_{CC} * (V_S)$,

   where

   - $V_S = V^+ - V^-$ (1)

2. Calculate the RMS power dissipated in the output stage:

   $P_D \text{ (rms)} = \text{rms} ((V_S - V_{OUT}) * I_{OUT})$

   where

   - V_{OUT} and I_{OUT} are the voltage across
   - The current through the external load and V_S is the total supply voltage (2)

3. Calculate the total RMS power:

   $P_T = P_{AMP} + P_D$ (3)

The maximum power that t-he LMH6570 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° – T_{AMB})/ R_{θJA}$

where

- T_{AMB} = Ambient temperature (°C)
- $R_{θJA}$ = Thermal resistance, from junction to ambient, for a given package (°C/W)
- For the SOIC package $R_{θJA}$ is 150 °C/W (4)

9 Layout

9.1 Layout Guidelines

To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, whereas the smaller ceramic capacitors should be placed as close to the device as possible. In Figure 25, the capacitor between V^+ and V^- is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01 μF and 0.1 μF ceramic capacitors for each supply bypass.

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- *Current Feedback Loop Gain Analysis and Performance Enhancement*, Application Note OA-13 (SNOA366)
- *IC Package Thermal Metrics* Application Report (SPRA953)

10.2 Trademarks

All trademarks are the property of their respective owners.

10.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6570MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 70MA	Samples
LMH6570MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 70MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

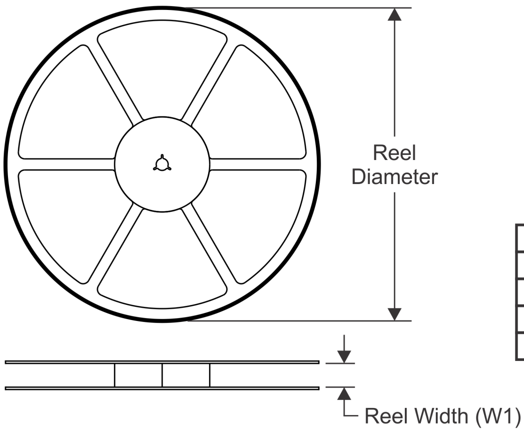
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

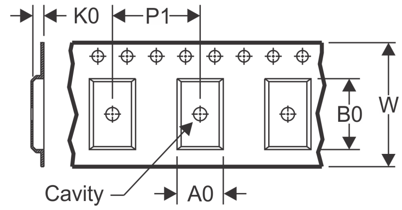
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

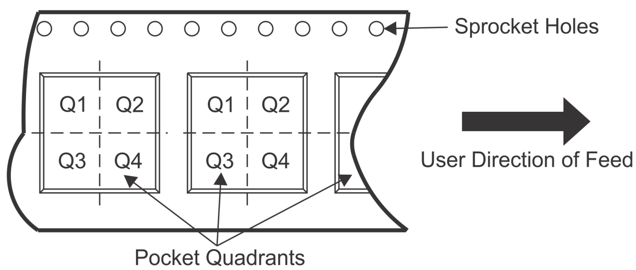


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

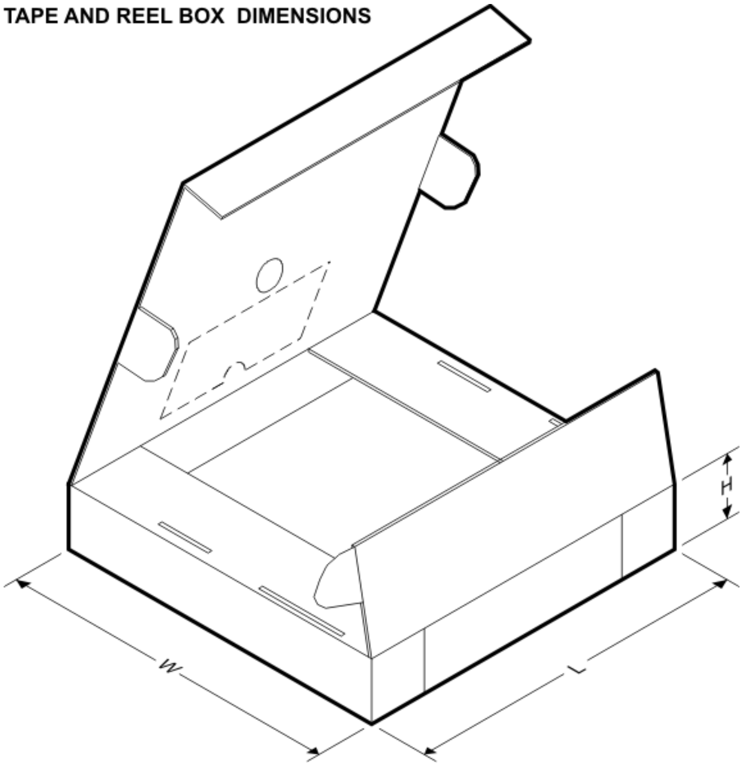
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

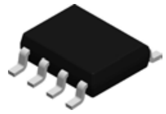
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6570MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6570MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

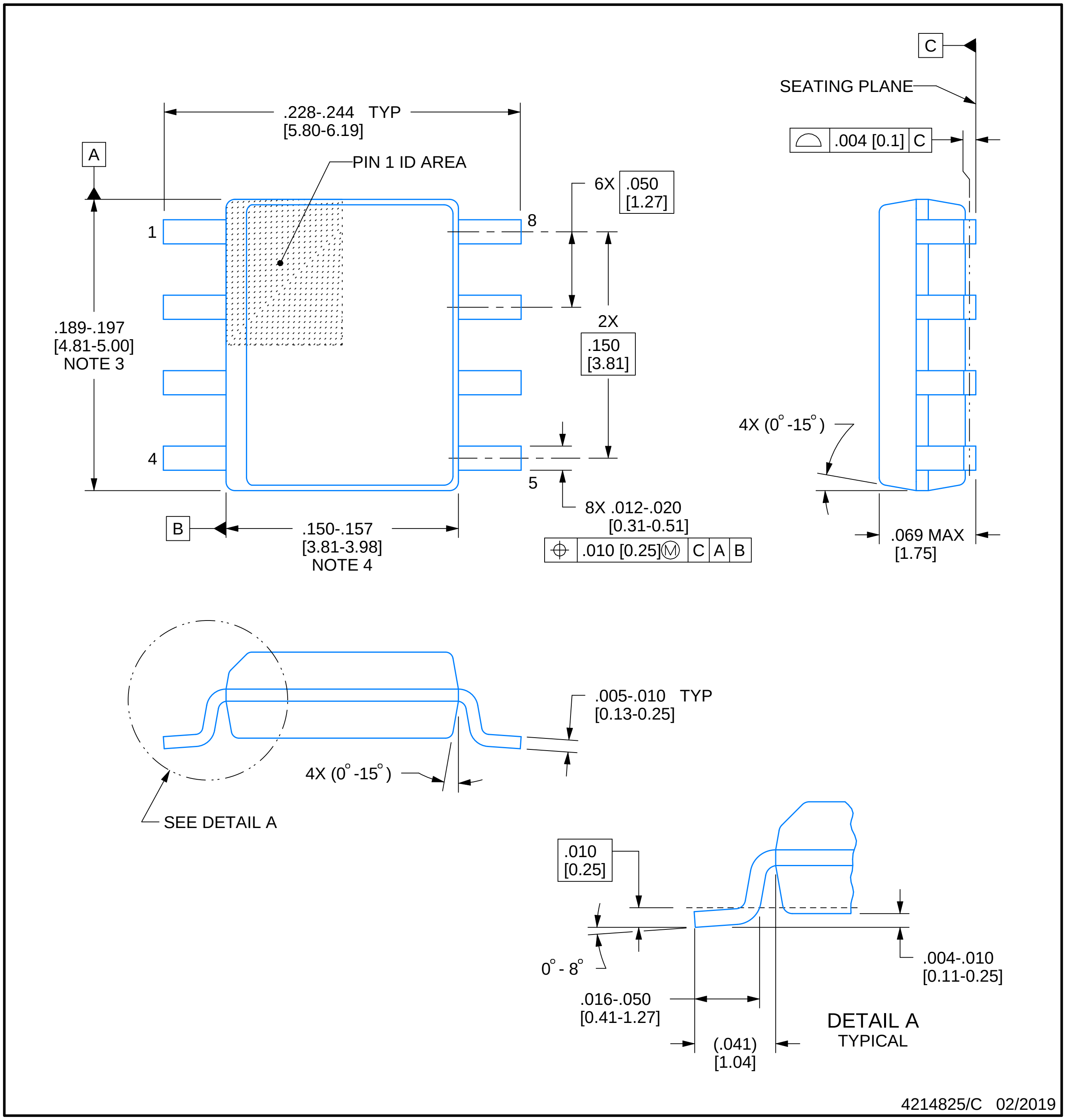


PACKAGE OUTLINE

D0008A

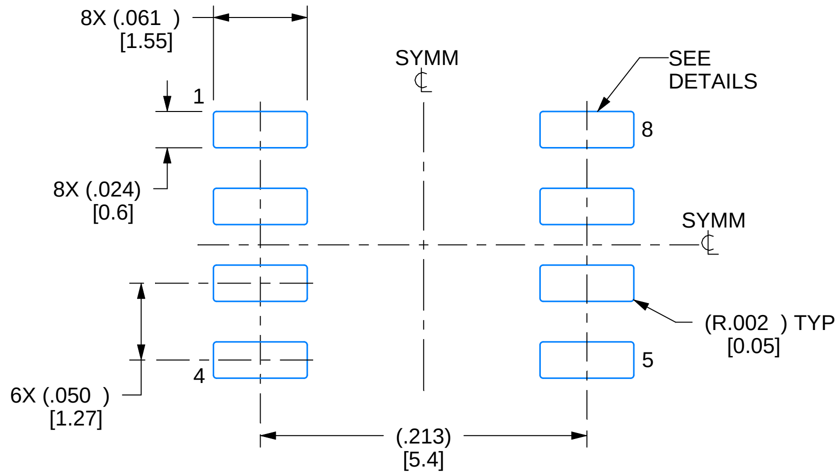
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

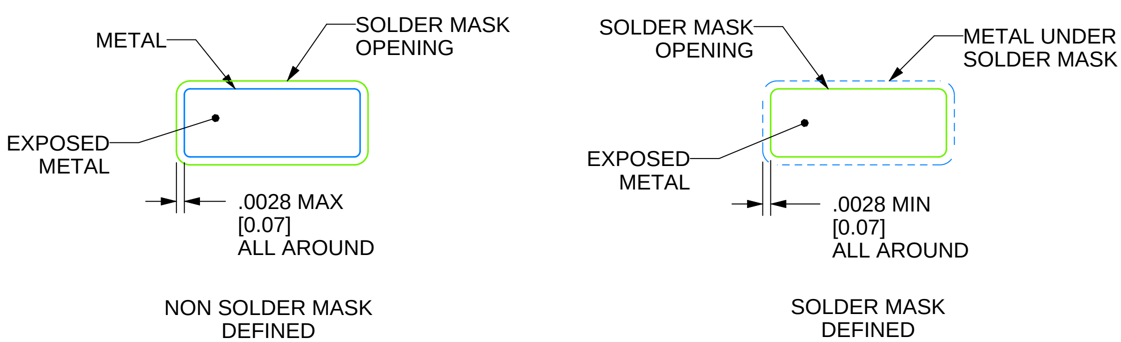


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

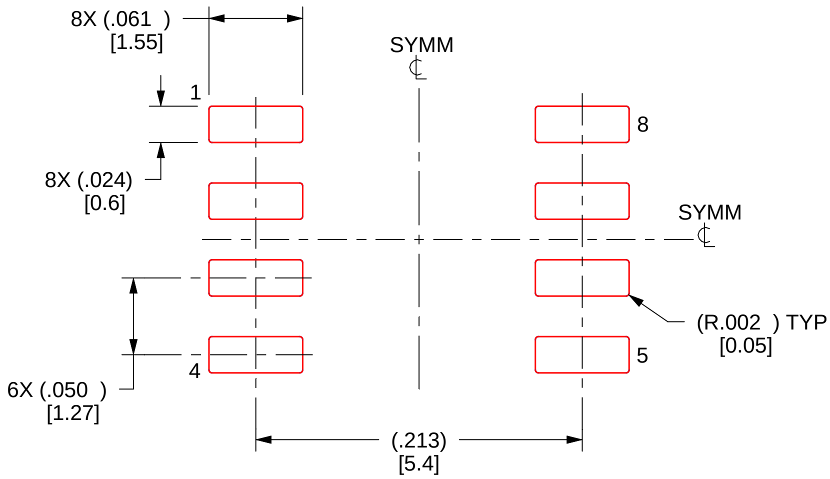


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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