

0.9-Ω SPDT ANALOG SWITCH 5-V/3.3-V SINGLE-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

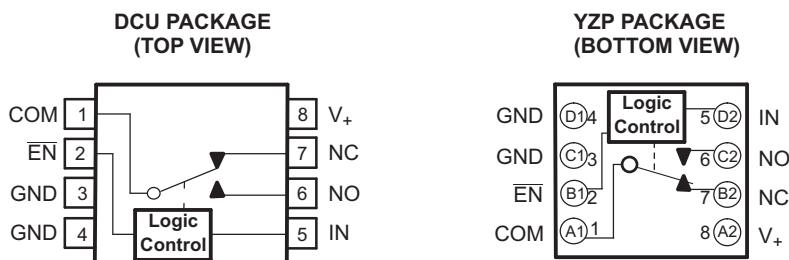
Check for Samples: [TS5A3154](#)

FEATURES

- Specified Make-Before-Break Switching
- Low ON-State Resistance (0.9 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals



DESCRIPTION/ORDERING INFORMATION

The TS5A3154 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent channel-to-channel ON-state resistance matching. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Table 1. ORDERING INFORMATION

| T _A | PACKAGE ^{(1) (2)} | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽³⁾ |
|----------------|---|--------------|-----------------------|---------------------------------|
| –40°C to 85°C | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Reel of 3000 | TS5A3154YZPR | __ _JX_ |
| | SSOP – DCU | Reel of 3000 | TS5A3154DCUR | JCF_ |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(3) DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

Table 2. FUNCTION TABLE

| $\overline{\text{EN}}$ | IN | NC TO COM, COM TO NC | NO TO COM, COM TO NO |
|------------------------|----|-------------------------|-------------------------|
| L | L | ON | OFF |
| L | H | OFF | ON |
| H | X | OFF | OFF |

Table 3. Summary of Characteristics⁽¹⁾

| Configuration | Single-Pole, Double-Throw 2:1 Multiplexer/Demultiplexer (SPDT) |
|--|---|
| Number of channels | 1 |
| ON-state resistance (r_{on}) | 0.9 Ω |
| ON-state resistance match (Δr_{on}) | 0.1 Ω |
| ON-state resistance flatness ($r_{\text{on(flat)}}$) | 0.15 Ω |
| Turn-on/turn-off time ($t_{\text{ON}}/t_{\text{OFF}}$) | 8 ns/12.5 ns |
| Make-before-break time (t_{MBB}) | 12 ns |
| Charge injection (Q_{C}) | 10 pC |
| Bandwidth (BW) | 100 MHz |
| OFF isolation (O_{ISO}) | -64 dB at 1 MHz |
| Crosstalk (X_{TALK}) | -64 dB at 1 MHz |
| Total harmonic distortion (THD) | 0.004% |
| Leakage current ($I_{\text{COM(OFF)}}$ / $I_{\text{NC(OFF)}}$) | ± 20 nA |
| Power-supply current (I_{+}) | 0.1 μA |
| Package option | 8-pin SSOP or DSBGA |

(1) $V_{+} = 5$ V, $T_{\text{A}} = 25^{\circ}\text{C}$

Absolute Minimum and Maximum Ratings^{(1) (2)}

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------------------------------|--|--|-------------|------|
| V_+ | Supply voltage range ⁽³⁾ | -0.5 | 6.5 | V |
| V_{NC} , V_{NO} , V_{COM} | Analog voltage range ^{(3) (4) (5)} | -0.5 | $V_+ + 0.5$ | V |
| I_K | Analog port diode current | $V_{NC}, V_{NO}, V_{COM} < 0$ or $V_{NO}, V_{NC}, V_{COM} > V_+$ | | mA |
| I_{NC} , I_{COM} , I_{NO} | On-state switch current | -200 | 200 | mA |
| | On-state peak switch current ⁽⁶⁾ | -400 | 400 | |
| V_I | Digital input voltage range ^{(3) (4)} | -0.5 | 6.5 | V |
| I_{IK} | Digital input clamp current | $V_I < 0$ | | mA |
| I_+ | Continuous current through V_+ | | 100 | mA |
| I_{GND} | Continuous current through GND | -100 | 100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁷⁾ | DCU package | | 227 |
| | | YZP package | | 102 |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply⁽¹⁾

$V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT | |
|---|----------------------------------|--|--|-------|-------|-------|-------|----------|---------------|
| Analog Switch | | | | | | | | | |
| Analog signal range | V_{COM}, V_{NO}, V_{NC} | | | | 0 | | V_+ | V | |
| Peak ON resistance | r_{peak} | $0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -100 \text{ mA}$, | Switch ON, See Figure 13 | 25°C | 4.5 V | 0.9 | 1.1 | Ω | |
| | | | | Full | | | | | 1.3 |
| ON-state resistance | r_{on} | $V_{NO} \text{ or } V_{NC} = 2.5 \text{ V}$, $I_{COM} = -100 \text{ mA}$, | Switch ON, See Figure 13 | 25°C | 4.5 V | 0.8 | 0.9 | Ω | |
| | | | | Full | | | | | 1.1 |
| ON-state resistance matching between channels | Δr_{on} | $V_{NO} \text{ or } V_{NC} = 2.5 \text{ V}$, $I_{COM} = -100 \text{ mA}$, | Switch ON, See Figure 13 | 25°C | 4.5 V | 0.05 | 0.1 | Ω | |
| | | | | Full | | | | | 0.1 |
| ON-state resistance flatness | $r_{on(flat)}$ | $0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -100 \text{ mA}$, | Switch ON, See Figure 13 | 25°C | 4.5 V | 0.15 | | Ω | |
| | | | | Full | | | | | |
| | | | | 25°C | | 4.5 V | 0.09 | | 0.15 |
| Full | 0.15 | | | | | | | | |
| NC, NO OFF leakage current | $I_{NC(OFF)}, I_{NO(OFF)}$ | $V_{NC} \text{ or } V_{NO} = 1 \text{ V}$, $V_{COM} = 4.5 \text{ V}$, or $V_{NC} \text{ or } V_{NO} = 4.5 \text{ V}$, $V_{COM} = 1 \text{ V}$, | Switch OFF, See Figure 14 | 25°C | 5.5 V | -20 | 2 | 20 | nA |
| | | | | Full | | -150 | 150 | | |
| | $I_{NC(PWROFF)}, I_{NO(PWROFF)}$ | $V_{NC} \text{ or } V_{NO} = 0 \text{ to } 5.5 \text{ V}$, $V_{COM} = 5.5 \text{ V to } 0$, | Switch OFF, See Figure 14 | 25°C | 0 V | -5 | 0.7 | 5 | μA |
| | | | | Full | | -25 | 25 | | |
| NC, NO ON leakage current | $I_{NC(ON)}, I_{NO(ON)}$ | $V_{NC} \text{ or } V_{NO} = 1 \text{ V}$, $V_{COM} = \text{Open}$, or $V_{NC} \text{ or } V_{NO} = 4.5 \text{ V}$, $V_{COM} = \text{Open}$, | Switch ON, See Figure 15 | 25°C | 5.5 V | -20 | 2 | 20 | nA |
| | | | | Full | | -150 | 150 | | |
| COM OFF leakage current | $I_{COM(OFF)}$ | $V_{COM} = 1 \text{ V}$, $V_{NC} \text{ or } V_{NO} = 4.5 \text{ V}$, or $V_{COM} = 4.5 \text{ V}$, $V_{NC} \text{ or } V_{NO} = 1 \text{ V}$, | Switch OFF, See Figure 14 | 25°C | 5.5 V | -20 | 2 | 20 | nA |
| | | | | Full | | -150 | 150 | | |
| | $I_{COM(PWROFF)}$ | $V_{NC} \text{ or } V_{NO} = 0 \text{ to } 5.5 \text{ V}$, $V_{COM} = 5.5 \text{ V to } 0$, | Switch OFF, See Figure 14 | 25°C | 0 V | -5 | 0.7 | 5 | μA |
| | | | | Full | | -25 | 25 | | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{COM} = 1 \text{ V}$, $V_{NC} \text{ or } V_{NO} = \text{Open}$, or $V_{COM} = 4.5 \text{ V}$, $V_{NC} \text{ or } V_{NO} = \text{Open}$, | Switch ON, See Figure 15 | 25°C | 5.5 V | -20 | 2 | 20 | nA |
| Full | -150 | 150 | | | | | | | |
| Digital Control Inputs (I_N, \overline{EN})⁽²⁾ | | | | | | | | | |
| Input logic high | V_{IH} | | | Full | | 2.4 | 5.5 | V | |
| Input logic low | V_{IL} | | | Full | | 0 | 0.8 | V | |
| Input leakage current | I_{IH}, I_{IL} | $V_I = 5.5 \text{ V or } 0 \text{ V}$ | | 25°C | 5.5 V | -100 | 25 | 100 | nA |
| | | | | Full | | -100 | 100 | | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 5-V Supply⁽¹⁾ (continued)
 $V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT | |
|--------------------------------------|----------------------------------|---|--|-------|----------------|-----|-------|------|---------------|
| Dynamic | | | | | | | | | |
| Turn-on time, IN or \overline{OE} | t_{ON} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 5 V | 1 | 5.2 | 8 | ns |
| | | | | Full | 4.5 V to 5.5 V | 1 | | 9 | |
| Turn-off time, IN or \overline{OE} | t_{OFF} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 5 V | 5 | 9.5 | 12.5 | ns |
| | | | | Full | 4.5 V to 5.5 V | 4 | | 13.5 | |
| Make-before-break time | t_{MBB} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 18 | 25°C | 5 V | 4 | 6.3 | 12 | ns |
| | | | | Full | 4.5 V to 5.5 V | 4 | | 13 | |
| Charge injection | Q_C | $V_{GEN} = 0$, $R_{GEN} = 0$, | $C_L = 1\text{ nF}$, See Figure 22 | 25°C | 5 V | | 10 | pC | |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch OFF, See Figure 16 | 25°C | 5 V | | 19 | pF | |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 5 V | | 57 | pF | |
| COM OFF capacitance | $C_{COM(OFF)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 5 V | | 36 | pF | |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 5 V | | 57 | pF | |
| Digital input capacitance | C_I | $V_I = V_+$ or GND, | See Figure 16 | 25°C | 5 V | | 2 | pF | |
| Bandwidth | BW | $R_L = 50\ \Omega$, | Switch ON, See Figure 19 | 25°C | 5 V | | 100 | MHz | |
| OFF isolation | O_{ISO} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch OFF, See Figure 20 | 25°C | 5 V | | -64 | dB | |
| Crosstalk | X_{TALK} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch ON, See Figure 21 | 25°C | 5 V | | -64 | dB | |
| Total harmonic distortion | THD | $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, | $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 23 | 25°C | 5 V | | 0.004 | % | |
| Supply | | | | | | | | | |
| Positive supply current | I_+ | $V_I = V_+$ or GND, | Switch ON or OFF | 25°C | 5.5 V | | 0.02 | 0.1 | μA |
| | | | | Full | | | | 0.5 | |

Electrical Characteristics for 3.3-V Supply⁽¹⁾

$V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT | |
|---|----------------------------|--|------------------------------|-------|-----|------|----------------------|----------|---------------|
| Analog Switch | | | | | | | | | |
| Analog signal range | V_{COM}, V_{NO}, V_{NC} | | | | 0 | | V_+ | V | |
| Peak ON resistance | r_{peak} | $0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -100\text{ mA}$, Switch ON, See Figure 13 | 25°C Full | 3 V | | 1.3 | 1.6 1.9 | Ω | |
| ON-state resistance | r_{on} | $V_{NO} \text{ or } V_{NC} = 2\text{ V}$, $I_{COM} = -100\text{ mA}$, Switch ON, See Figure 13 | 25°C Full | 3 V | | 1.2 | 1.5 1.7 | Ω | |
| ON-state resistance match between channels | Δr_{on} | $V_{NO} \text{ or } V_{NC} = 2\text{ V}, 0.8\text{ V}$ $I_{COM} = -100\text{ mA}$, Switch ON, See Figure 13 | 25°C Full | 3 V | | 0.08 | 0.15 0.15 | Ω | |
| ON-state resistance flatness | $r_{on(flat)}$ | $0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -100\text{ mA}$, $V_{NO} \text{ or } V_{NC} = 2\text{ V}, 0.8\text{ V}$, $I_{COM} = -100\text{ mA}$, Switch ON, See Figure 13 | 25°C Full 25°C Full | 3 V | | 0.3 | 0.09 0.15 0.15 | Ω | |
| NC, NO OFF leakage current | $I_{NC(OFF)}, I_{NO(OFF)}$ | $V_{NC} \text{ or } V_{NO} = 1\text{ V}, V_{COM} = 3\text{ V}$, or $V_{NC} \text{ or } V_{NO} = 3\text{ V}, V_{COM} = 1\text{ V}$, Switch OFF, See Figure 14 | 25°C | 3.6 V | | -20 | 2 | 20 | nA |
| | | | Full | | | | | | |
| NC, NO ON leakage current | $I_{NC(ON)}, I_{NO(ON)}$ | $V_{NC} \text{ or } V_{NO} = 0 \text{ to } 3.6\text{ V}$, $V_{COM} = 3.6\text{ V to } 0\text{ V}$, Switch OFF, See Figure 14 | 25°C | 0 V | | -1 | 0.2 | 1 | μA |
| | | | Full | | | | | | |
| COM OFF leakage current | $I_{COM(OFF)}$ | $V_{COM} = 1\text{ V}, V_{NC} \text{ or } V_{NO} = 3\text{ V}$, or $V_{COM} = 3\text{ V}, V_{NC} \text{ or } V_{NO} = 1\text{ V}$, Switch OFF, See Figure 14 | 25°C | 3.6 V | | -20 | 2 | 20 | nA |
| | | | Full | | | | | | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{COM} = 1\text{ V}, V_{NC} \text{ or } V_{NO} = \text{Open}$, or $V_{COM} = 3\text{ V}, V_{NC} \text{ or } V_{NO} = \text{Open}$ Switch ON, See Figure 15 | 25°C | 3.6 V | | -20 | 2 | 20 | nA |
| | | | Full | | | | | | |
| Digital Control Inputs (I_N, \overline{EN})⁽²⁾ | | | | | | | | | |
| Input logic high | V_{IH} | | Full | | | 2 | | 5.5 | V |
| Input logic low | V_{IL} | | Full | | | 0 | | 0.8 | V |
| Input leakage current | I_{IH}, I_{IL} | $V_I = 5.5\text{ V or } 0$ | 25°C | 3.6 V | | -100 | 25 | 100 | nA |
| | | | Full | | | | | | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3.3-V Supply⁽¹⁾ (continued)
 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT | |
|--|--|--|--|-------|-----------------|------|-----------|---------------|----|
| Dynamic | | | | | | | | | |
| Turn-on time, IN or $\overline{\text{OE}}$ | t_{ON} | $V_{\text{COM}} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\ \text{pF}$, See Figure 17 | 25°C | 3.3 V | 3 | 6 | 10 | ns |
| | | | | Full | 3 V to 3.6 V | 2 | | 10.5 | |
| Turn-off time, IN or $\overline{\text{OE}}$ | t_{OFF} | $V_{\text{COM}} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\ \text{pF}$, See Figure 17 | 25°C | 3.3 V | 5 | 10 | 15 | ns |
| | | | | Full | 3 V to 3.6 V | 4 | | 17 | |
| Make-before- break time | t_{MBB} | $V_{\text{COM}} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\ \text{pF}$, See Figure 18 | 25°C | 3.3 V | 4 | 5.7 | 12 | ns |
| | | | | Full | 3 V to 3.6 V | 4 | | 13 | |
| Charge injection | Q_C | $V_{\text{GEN}} = 0$, $R_{\text{GEN}} = 0$, | $C_L = 1\ \text{nF}$, See Figure 22 | 25°C | 3.3 V | | 9 | pC | |
| NC, NO OFF capacitance | $C_{\text{NC(OFF)}}$, $C_{\text{NO(OFF)}}$ | V_{NC} or $V_{\text{NO}} = V_+$ or GND, | Switch OFF, See Figure 16 | 25°C | 3.3 V | | 19 | pF | |
| NC, NO ON capacitance | $C_{\text{NC(ON)}}$, $C_{\text{NO(ON)}}$ | V_{NC} or $V_{\text{NO}} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 3.3 V | | 57 | pF | |
| COM OFF capacitance | $C_{\text{COM(OFF)}}$ | $V_{\text{COM}} = V_+$ or GND, | Switch ON, See | 25°C | 3.3 V | | 36 | pF | |
| COM ON capacitance | $C_{\text{COM(ON)}}$ | $V_{\text{COM}} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 3.3 V | | 57 | pF | |
| Digital input capacitance | C_I | $V_I = V_+$ or GND, | See Figure 16 | 25°C | 3.3 V | | 2 | pF | |
| Bandwidth | BW | $R_L = 50\ \Omega$, | Switch ON, See Figure 19 | 25°C | 3.3 V | | 100 | MHz | |
| OFF isolation | O_{ISO} | $R_L = 50\ \Omega$, $f = 1\ \text{MHz}$, | Switch OFF, See Figure 20 | 25°C | 3.3 V | | -64 | dB | |
| Crosstalk | X_{TALK} | $R_L = 50\ \Omega$, $f = 1\ \text{MHz}$, | Switch ON, See Figure 21 | 25°C | 3.3 V | | -64 | dB | |
| Total harmonic distortion | THD | $R_L = 600\ \Omega$, $C_L = 50\ \text{pF}$, | $f = 20\ \text{Hz to }20\ \text{kHz}$, See Figure 23 | 25°C | 3.3 V | | 0.01 0 | % | |
| Supply | | | | | | | | | |
| Positive supply current | I_+ | $V_I = V_+$ or GND, | Switch ON or OFF | 25°C | 3.6 V | 0.01 | 0.1 | μA | |
| | | | | Full | | | 0.25 | | |

Electrical Characteristics for 2.5-V Supply⁽¹⁾

$V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT | |
|---|----------------------------------|--|--|-------|-------|------|-------|----------|---------------|
| Analog Switch | | | | | | | | | |
| Analog signal range | V_{COM}, V_{NO}, V_{NC} | | | | 0 | | V_+ | V | |
| Peak ON resistance | r_{peak} | $0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -8\text{ mA}$, | Switch ON, See Figure 13 | 25°C | 2.3 V | 1.9 | 2.5 | Ω | |
| | | | | Full | | | | | |
| ON-state resistance | r_{on} | $V_{NO} \text{ or } V_{NC} = 1.8\text{ V}$, $I_{COM} = -8\text{ mA}$, | Switch ON, See Figure 13 | 25°C | 2.3 V | 1.6 | 2.1 | Ω | |
| | | | | Full | | | | | |
| ON-state resistance matching between channels | Δr_{on} | $V_{NO} \text{ or } V_{NC} = 1.8\text{ V}$, $I_{COM} = -8\text{ mA}$, | Switch ON, See Figure 13 | 25°C | 2.3 V | 0.12 | 0.2 | Ω | |
| | | | | Full | | | | | |
| ON-state resistance flatness | $r_{on(flat)}$ | $0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -8\text{ mA}$, | Switch ON, See Figure 13 | 25°C | 2.3 V | 0.65 | | Ω | |
| | | | | Full | | | | | |
| | | | | 25°C | | 0.5 | | | |
| | | | | Full | | 1 | | | |
| NC, NO OFF leakage current | $I_{NC(OFF)}, I_{NO(OFF)}$ | $V_{NC} \text{ or } V_{NO} = 0.5\text{ V}$, $V_{COM} = 2.3\text{ V}$, or $V_{NC} \text{ or } V_{NO} = 2.3\text{ V}$, $V_{COM} = 0.5\text{ V}$, | Switch OFF, See Figure 14 | 25°C | 2.7 V | -20 | 2 | 20 | nA |
| | | | | Full | | -50 | | 50 | |
| | $I_{NC(PWROFF)}, I_{NO(PWROFF)}$ | $V_{NC} \text{ or } V_{NO} = 0 \text{ to } 2.7\text{ V}$, $V_{COM} = 2.7\text{ V to } 0$, | Switch OFF, See Figure 14 | 25°C | 0 V | -1 | | 1 | μA |
| | | | | Full | | -10 | | 10 | |
| NC, NO ON leakage current | $I_{NC(ON)}, I_{NO(ON)}$ | $V_{NC} \text{ or } V_{NO} = 0.5\text{ V}$, $V_{COM} = \text{Open}$, or $V_{NC} \text{ or } V_{NO} = 2.3\text{ V}$, $V_{COM} = \text{Open}$, | Switch ON, See Figure 15 | 25°C | 2.7 V | -20 | | 20 | nA |
| | | | | Full | | -50 | | 50 | |
| COM OFF leakage current | $I_{COM(OFF)}$ | $V_{COM} = 0.5\text{ V}$, $V_{NC} \text{ or } V_{NO} = 2.3\text{ V}$, or $V_{COM} = 2.3\text{ V}$, $V_{NC} \text{ or } V_{NO} = 0.5\text{ V}$, | Switch OFF, See Figure 14 | 25°C | 2.7 V | -20 | | 20 | nA |
| | | | | Full | | -50 | | 50 | |
| | $I_{COM(PWROFF)}$ | $V_{NC} \text{ or } V_{NO} = 0 \text{ to } 2.7\text{ V}$, $V_{COM} = 2.7\text{ V to } 0$, | Switch OFF, See Figure 14 | 25°C | 0 V | -1 | | 1 | μA |
| | | | | Full | | -10 | | 10 | |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{COM} = 0.5\text{ V}$, $V_{NC} \text{ or } V_{NO} = \text{Open}$, or $V_{COM} = 2.3\text{ V}$, $V_{NC} \text{ or } V_{NO} = \text{Open}$, | Switch ON, See Figure 15 | 25°C | 2.7 V | -20 | | 20 | nA |
| | | | | Full | | -50 | | 50 | |
| Digital Control Inputs (IN, $\overline{\text{EN}}$)⁽²⁾ | | | | | | | | | |
| Input logic high | V_{IH} | | Full | | 1.8 | | 5.5 | V | |
| Input logic low | V_{IL} | | Full | | 0 | | 0.6 | V | |
| Input leakage current | I_{IH}, I_{IL} | $V_I = 5.5\text{ V or } 0$ | 25°C | 2.7 V | -100 | 25 | 100 | nA | |
| | | | Full | | -100 | | 100 | | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 2.5-V Supply⁽¹⁾ (continued)
 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT | |
|--------------------------------------|----------------------------------|---|--|-------|----------------|-------|-------|---------------|----|
| Dynamic | | | | | | | | | |
| Turn-on time, IN or \overline{OE} | t_{ON} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 2.5 V | 4 | 7.0 | 11.5 | ns |
| | | | | Full | 2.3 V to 2.7 V | 3.5 | | 12 | |
| Turn-off time, IN or \overline{OE} | t_{OFF} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 2.5 V | 5 | 11.5 | 18.5 | ns |
| | | | | Full | 2.3 V to 2.7 V | 4 | | 21 | |
| Make-before-break time | t_{MKB} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 18 | 25°C | 2.5 V | 4 | 6.3 | 15 | ns |
| | | | | Full | 2.3 V to 2.7 V | 4 | | 16 | |
| Charge injection | Q_C | $V_{GEN} = 0$, $R_{GEN} = 0$, | $C_L = 1\text{ nF}$, See Figure 22 | 25°C | 2.5 V | | 7 | pC | |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch OFF, See Figure 16 | 25°C | 2.5 V | | 19 | pF | |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 2.5 V | | 57 | pF | |
| COM OFF capacitance | $C_{COM(OFF)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 2.5 V | | 36 | pF | |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 2.5 V | | 57 | pF | |
| Digital input capacitance | C_I | $V_I = V_+$ or GND, | See Figure 16 | 25°C | 2.5 V | | 2 | pF | |
| Bandwidth | BW | $R_L = 50\ \Omega$, | Switch ON, See Figure 19 | 25°C | 2.5 V | | 100 | MHz | |
| OFF isolation | O_{ISO} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch OFF, See Figure 20 | 25°C | 2.5 V | | -64 | dB | |
| Crosstalk | X_{TALK} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch ON, See Figure 21 | 25°C | 2.5 V | | -64 | dB | |
| Total harmonic distortion | THD | $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, | $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 23 | 25°C | 2.5 V | | 0.020 | % | |
| Supply | | | | | | | | | |
| Positive supply current | I_+ | $V_I = V_+$ or GND, | Switch ON or OFF | 25°C | 2.7 V | 0.001 | 0.05 | μA | |
| | | | | Full | | | 0.15 | | |

Electrical Characteristics for 1.8-V Supply⁽¹⁾

$V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT |
|---|----------------------------------|---|------------------------------|--------------|--------|------|---------------|--------------------|
| Analog Switch | | | | | | | | |
| Analog signal range | V_{COM}, V_{NO}, V_{NC} | | | | 0 | | V_+ | V |
| Peak ON resistance | r_{peak} | $0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -2\text{ mA}$, | Switch ON, See Figure 13 | 25°C Full | 1.65 V | 5.5 | 25 30 | Ω |
| ON-state resistance | r_{on} | $V_{NO} \text{ or } V_{NC} = 1.5\text{ V}$, $I_{COM} = -2\text{ mA}$, | Switch ON, See Figure 13 | 25°C Full | 1.65 V | 2 | 2.7 3.1 | Ω |
| ON-state resistance matching between channels | Δr_{on} | $V_{NO} \text{ or } V_{NC} = 1.5\text{ V}$, $I_{COM} = -2\text{ mA}$, | Switch ON, See Figure 13 | 25°C Full | 1.65 V | 0.16 | 0.3 0.3 | Ω |
| ON-state resistance flatness | $r_{on(flat)}$ | $0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -2\text{ mA}$, $V_{NO} \text{ or } V_{NC} = 0.6\text{ V}, 1.5\text{ V}$, $I_{COM} = -2\text{ mA}$, | Switch ON, See Figure 13 | 25°C Full | 1.65 V | 3 | 3 20 25 | Ω |
| NC, NO OFF leakage current | $I_{NC(OFF)}, I_{NO(OFF)}$ | $V_{NC} \text{ or } V_{NO} = 0.3\text{ V}$, $V_{COM} = 1.65\text{ V}$, or $V_{NC} \text{ or } V_{NO} = 1.65\text{ V}$, $V_{COM} = 0.3\text{ V}$, | Switch OFF, See Figure 14 | 25°C Full | 1.95 V | -20 | 1.5 50 | 20 nA |
| | $I_{NC(PWROFF)}, I_{NO(PWROFF)}$ | $V_{NC} \text{ or } V_{NO} = 0 \text{ to } 1.95\text{ V}$, $V_{COM} = 1.95\text{ V to } 0$, | Switch OFF, See Figure 14 | 25°C Full | 0 V | -1 | 0.1 10 | 1 μA |
| NC, NO ON leakage current | $I_{NC(ON)}, I_{NO(ON)}$ | $V_{NC} \text{ or } V_{NO} = 0.3\text{ V}$, $V_{COM} = \text{Open}$, or $V_{NC} \text{ or } V_{NO} = 1.65\text{ V}$, $V_{COM} = \text{Open}$, | Switch ON, See Figure 15 | 25°C Full | 1.95 V | -20 | 1.5 50 | 20 nA |
| COM OFF leakage current | $I_{COM(OFF)}$ | $V_{NC} \text{ or } V_{NO} = 1.65\text{ V}$, $V_{COM} = 0.3\text{ V}$, or $V_{NC} \text{ or } V_{NO} = 0.3\text{ V}$, $V_{COM} = 1.65\text{ V}$, | Switch OFF, See Figure 14 | 25°C Full | 1.95 V | -20 | 1.5 50 | 20 nA |
| | $I_{COM(PWROFF)}$ | $V_{NC} \text{ or } V_{NO} = 1.95\text{ V to } 0$, $V_{COM} = 0 \text{ to } 1.95\text{ V}$, | Switch OFF, See Figure 14 | 25°C Full | 0 V | -1 | 0.06 10 | 1 μA |
| COM ON leakage current | $I_{COM(ON)}$ | $V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0.3\text{ V}$, or $V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 1.65\text{ V}$, | Switch ON, See Figure 15 | 25°C Full | 1.95 V | -20 | 1.5 50 | 20 nA |
| Digital Control Inputs (I_N, \overline{EN})⁽²⁾ | | | | | | | | |
| Input logic high | V_{IH} | | | Full | | 1.5 | 5.6 | V |
| Input logic low | V_{IL} | | | Full | | 0 | 0.6 | V |
| Input leakage current | I_{IH}, I_{IL} | $V_I = 5.5\text{ V or } 0$ | | 25°C | 1.95 V | -100 | 25 | 100 |
| | | | | Full | | -100 | | 100 |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 1.8-V Supply⁽¹⁾ (continued)
 $V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | T_A | V_+ | MIN | TYP | MAX | UNIT | |
|--------------------------------------|----------------------------------|---|--|-------|------------------|-------|------|---------------|----|
| Dynamic | | | | | | | | | |
| Turn-on time, IN or \overline{OE} | t_{ON} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 5 V | 5 | 20.5 | ns | |
| | | | | Full | 1.65 V to 1.95 V | 4.5 | 21 | | |
| Turn-off time, IN or \overline{OE} | t_{OFF} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 17 | 25°C | 5 V | 7 | 16.5 | 27.5 | ns |
| | | | | Full | 1.65 V to 1.95 V | 5 | 30 | | |
| Make-before-break time | t_{MKB} | $V_{COM} = V_+$, $R_L = 50\ \Omega$, | $C_L = 35\text{ pF}$, See Figure 18 | 25°C | 5 V | 4 | 8.3 | 15 | ns |
| | | | | Full | 1.65 V to 1.95 V | 4 | 16 | | |
| Charge injection | Q_C | $V_{GEN} = 0$, $R_{GEN} = 0$, | $C_L = 1\text{ nF}$, See Figure 22 | 25°C | 1.8 V | 5 | | pC | |
| NC, NO OFF capacitance | $C_{NC(OFF)}$, $C_{NO(OFF)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch OFF, See Figure 16 | 25°C | 1.8 V | 19 | | pF | |
| NC, NO ON capacitance | $C_{NC(ON)}$, $C_{NO(ON)}$ | V_{NC} or $V_{NO} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 1.8 V | 57 | | pF | |
| COM OFF capacitance | $C_{COM(OFF)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 1.8 V | 36 | | pF | |
| COM ON capacitance | $C_{COM(ON)}$ | $V_{COM} = V_+$ or GND, | Switch ON, See Figure 16 | 25°C | 1.8 V | 57 | | pF | |
| Digital input capacitance | C_I | $V_I = V_+$ or GND, | See Figure 16 | 25°C | 1.8 V | 2.0 | | pF | |
| Bandwidth | BW | $R_L = 50\ \Omega$, | Switch ON, See Figure 19 | 25°C | 1.8 V | 100 | | MHz | |
| OFF isolation | O_{ISO} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch OFF, See Figure 20 | 25°C | 1.8 V | -64 | | dB | |
| Crosstalk | X_{TALK} | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, | Switch ON, See Figure 21 | 25°C | 1.8 V | -64 | | dB | |
| Total harmonic distortion | THD | $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, | $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 23 | 25°C | 1.8 V | 0.060 | | % | |
| Supply | | | | | | | | | |
| Positive supply current | I_+ | $V_I = V_+$ or GND, | Switch ON or OFF | 25°C | 1.95 V | 0.001 | 0.05 | μA | |
| | | | | Full | | 0.1 | | | |

TYPICAL PERFORMANCE

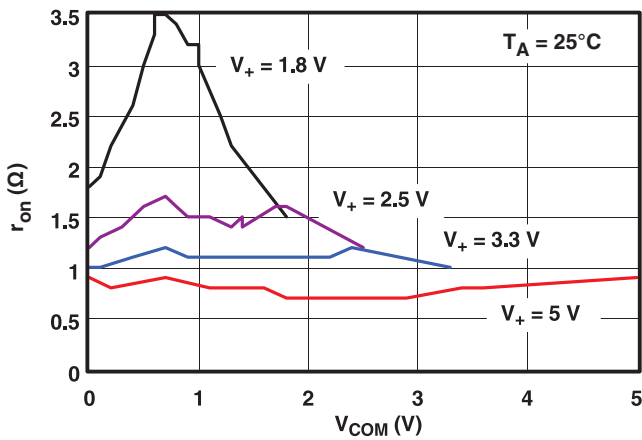


Figure 1. r_{on} vs V_{COM}

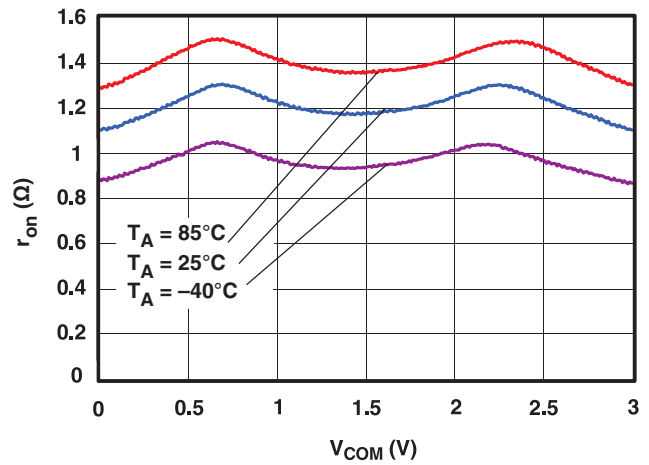


Figure 2. r_{on} vs V_{COM} ($V_+ = 3V$)

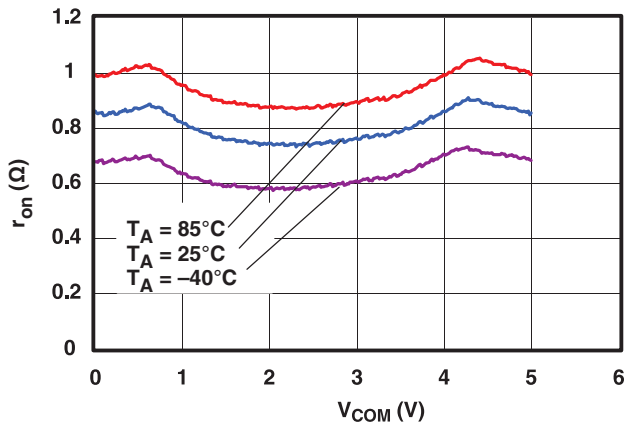


Figure 3. r_{on} vs V_{COM} ($V_+ = 5V$)

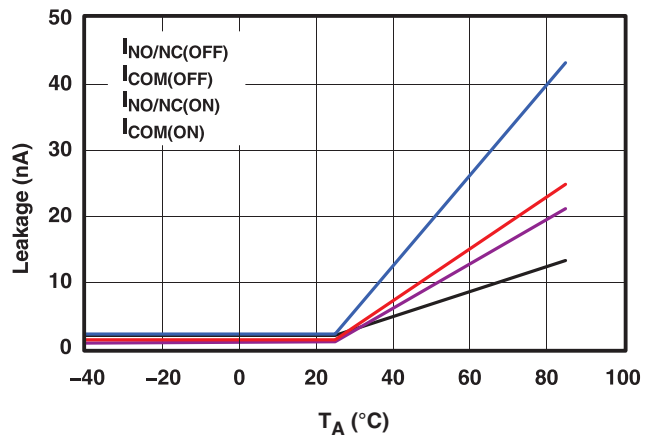


Figure 4. Leakage Current vs Temperature ($V_+ = 5.5V$)

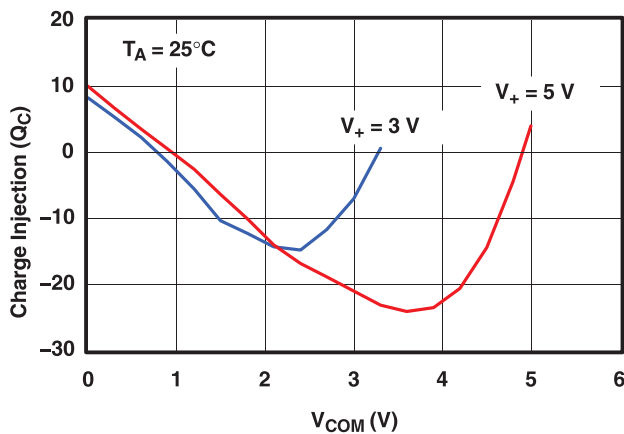


Figure 5. Charge Injection (Q_C) vs V_{COM}

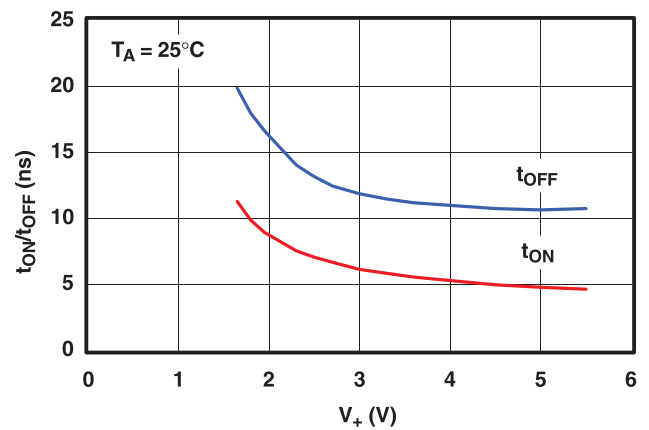


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE (continued)

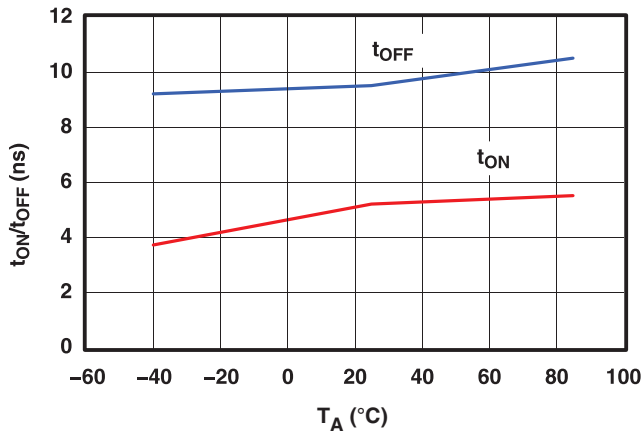


Figure 7. t_{ON} and t_{OFF} vs Temperature ($V_+ = 5\text{ V}$)

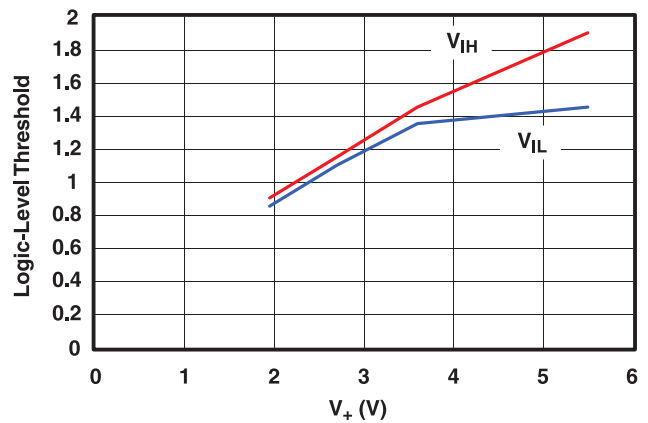


Figure 8. Logic-Level Threshold vs V_+

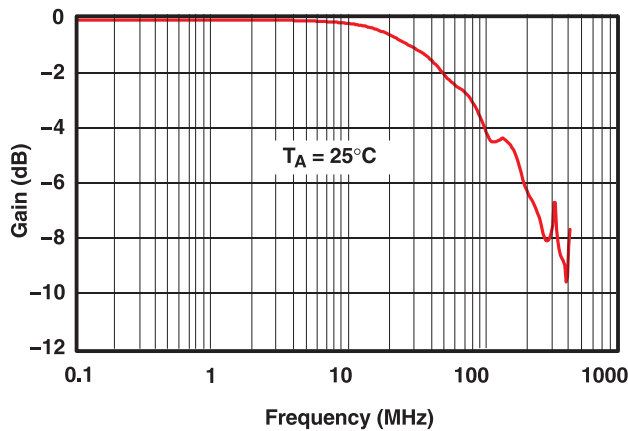


Figure 9. Bandwidth ($V_+ = 5\text{ V}$)

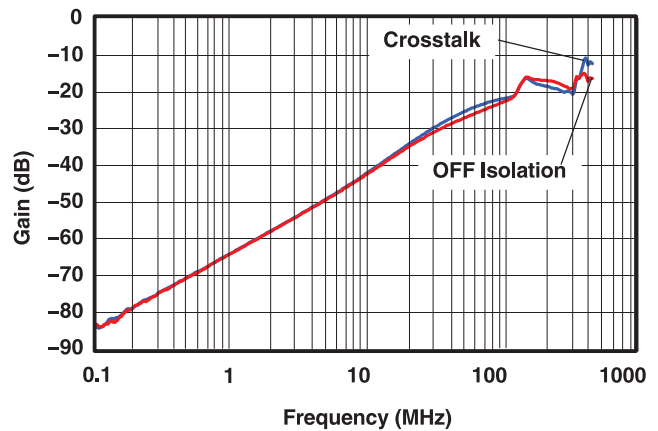


Figure 10. OFF Isolation and Crosstalk ($V_+ = 5\text{ V}$)

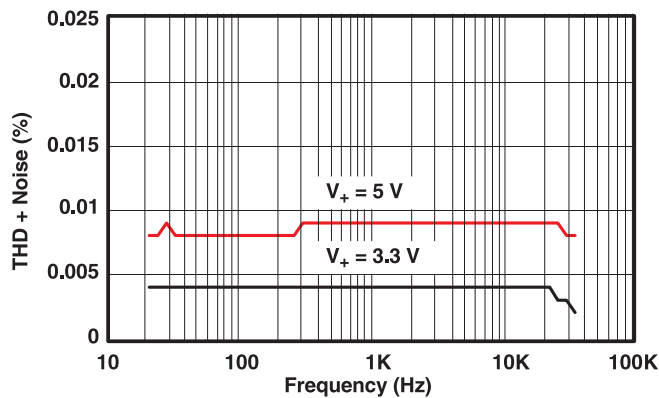


Figure 11. Total Harmonic Distortion (THD) vs Frequency

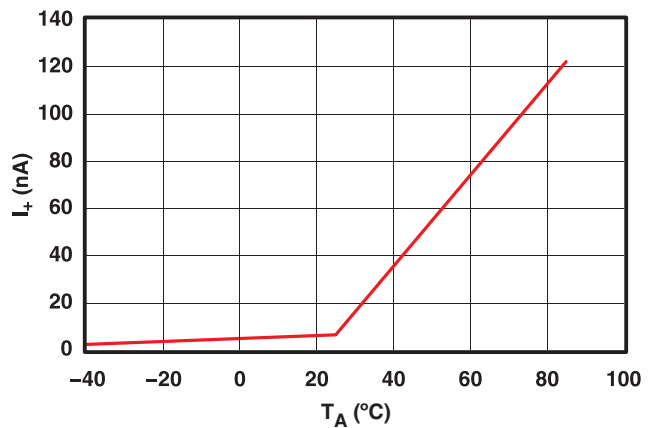


Figure 12. Power Supply Current vs Temperature ($V_+ = 5\text{ V}$)

PIN DESCRIPTION

| PIN NO. | NAME | DESCRIPTION |
|---------|------------------------|--|
| 1 | COM | Common |
| 2 | $\overline{\text{EN}}$ | Enable control input |
| 3 | GND | Digital ground |
| 4 | GND | Digital ground |
| 5 | IN | Digital control to connect the COM to NO or NC |
| 6 | NO | Normally open |
| 7 | NC | Normally closed |
| 8 | V_+ | Power supply |

PARAMETER DESCRIPTION

| SYMBOL | DESCRIPTION |
|--------------------------------|--|
| V_{COM} | Voltage at COM |
| V_{NC} | Voltage at NC |
| V_{NO} | Voltage at NO |
| r_{on} | Resistance between COM and NC or COM and NO ports when the channel is ON |
| Δr_{on} | Difference of r_{on} between channels in a specific device |
| $r_{\text{on(flat)}}$ | Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions |
| $I_{\text{NC(OFF)}}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state |
| $I_{\text{NO(OFF)}}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state |
| $I_{\text{NC(ON)}}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open |
| $I_{\text{NO(ON)}}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open |
| $I_{\text{COM(ON)}}$ | Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open |
| V_{IH} | Minimum input voltage for logic high for the control input (IN) |
| V_{IL} | Maximum input voltage for logic low for the control input (IN) |
| V_{I} | Voltage at the control input (IN) |
| $I_{\text{IH}}, I_{\text{IL}}$ | Leakage current measured at the control input (IN) |
| t_{ON} | Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON. |
| t_{OFF} | Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF. |
| t_{BBM} | Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state. |
| Q_{C} | Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_{\text{C}} = C_{\text{L}} \times \Delta V_{\text{COM}}$, C_{L} is the load capacitance and ΔV_{COM} is the change in analog output voltage. |
| $C_{\text{NC(OFF)}}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is OFF |
| $C_{\text{NO(OFF)}}$ | Capacitance at the NO port when the corresponding channel (NO to COM) is OFF |
| $C_{\text{NC(ON)}}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is ON |
| $C_{\text{NO(ON)}}$ | Capacitance at the NO port when the corresponding channel (NO to COM) is ON |
| $C_{\text{COM(ON)}}$ | Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON |
| C_{I} | Capacitance of control input (IN) |
| O_{ISO} | OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state. |
| X_{TALK} | Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB. |
| BW | Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the DC gain. |
| THD | Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of fundamental harmonic. |

PARAMETER DESCRIPTION (continued)

| SYMBOL | DESCRIPTION |
|--------|---|
| I_+ | Static power-supply current with the control (IN) pin at V_+ or GND |

PARAMETER MEASUREMENT INFORMATION

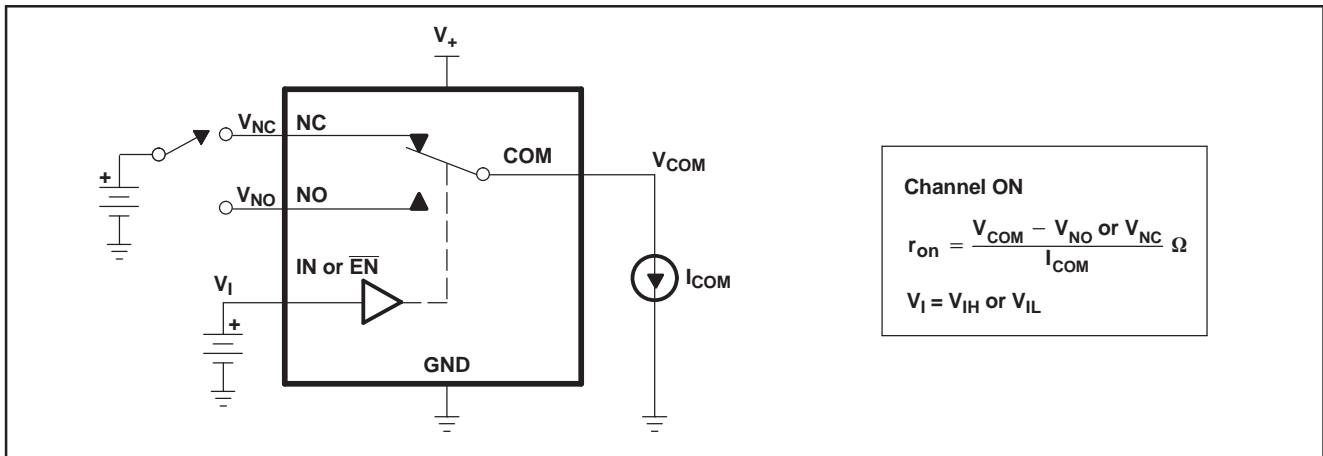


Figure 13. ON-State Resistance (r_{on})

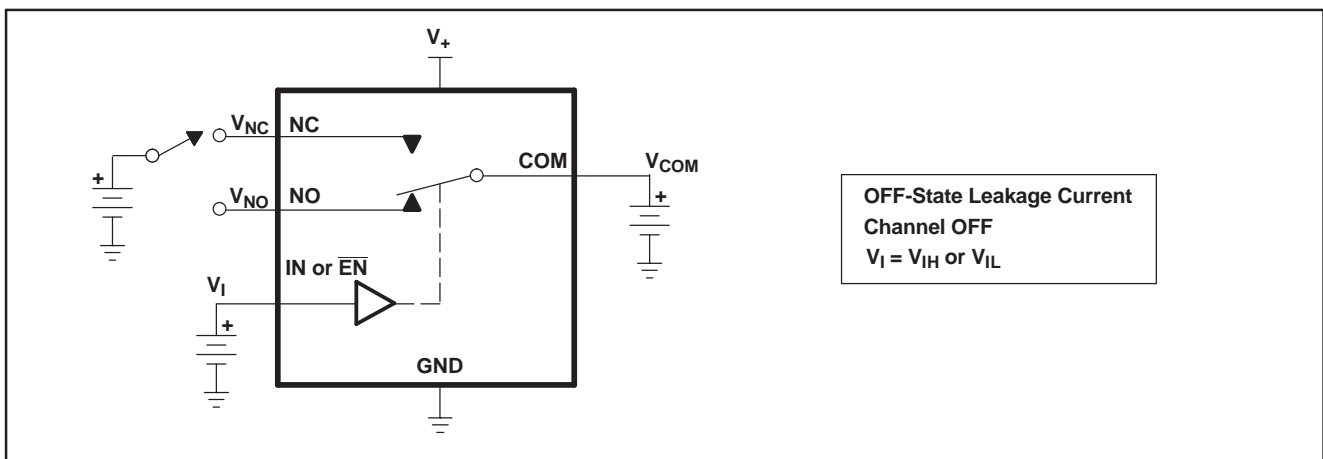


Figure 14. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(PWROFF)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

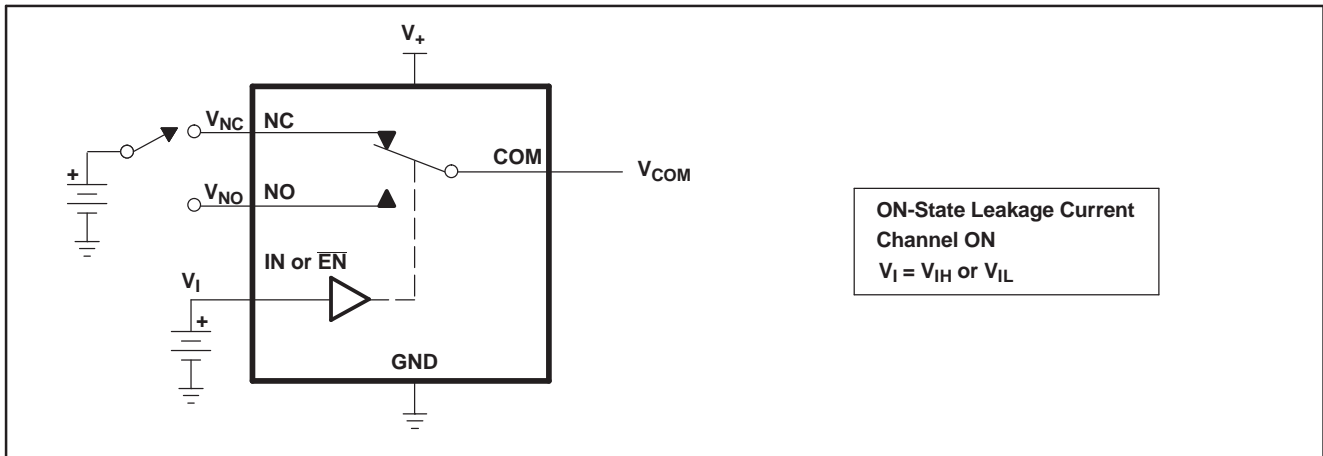


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

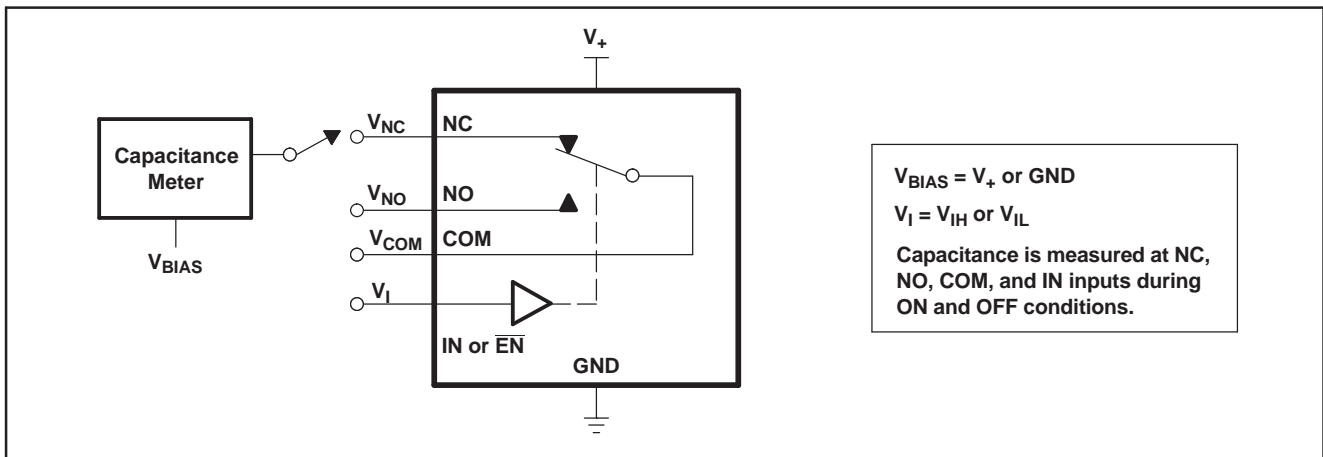
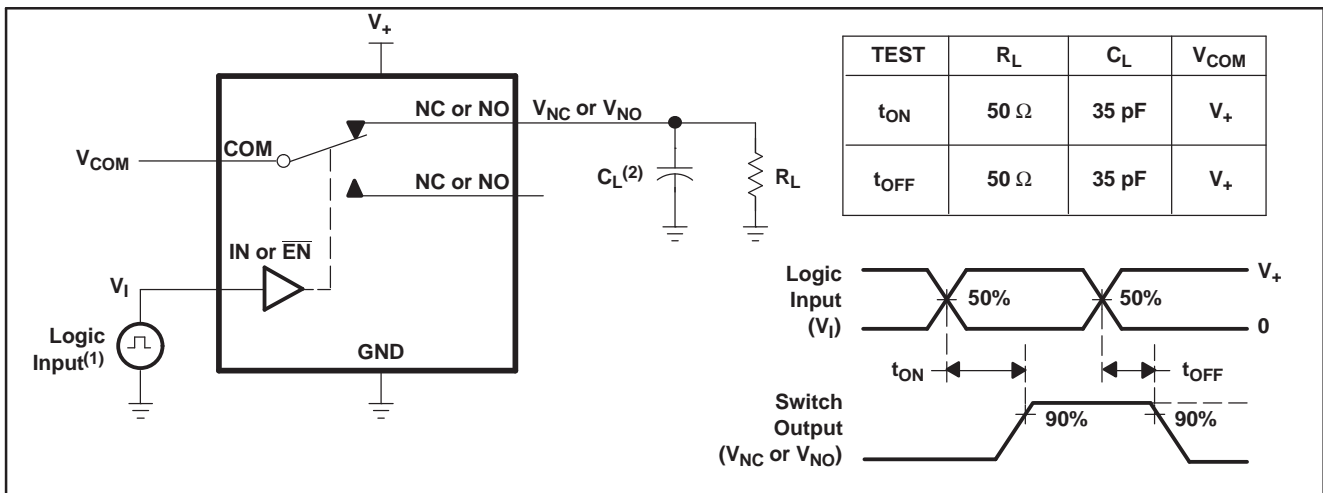


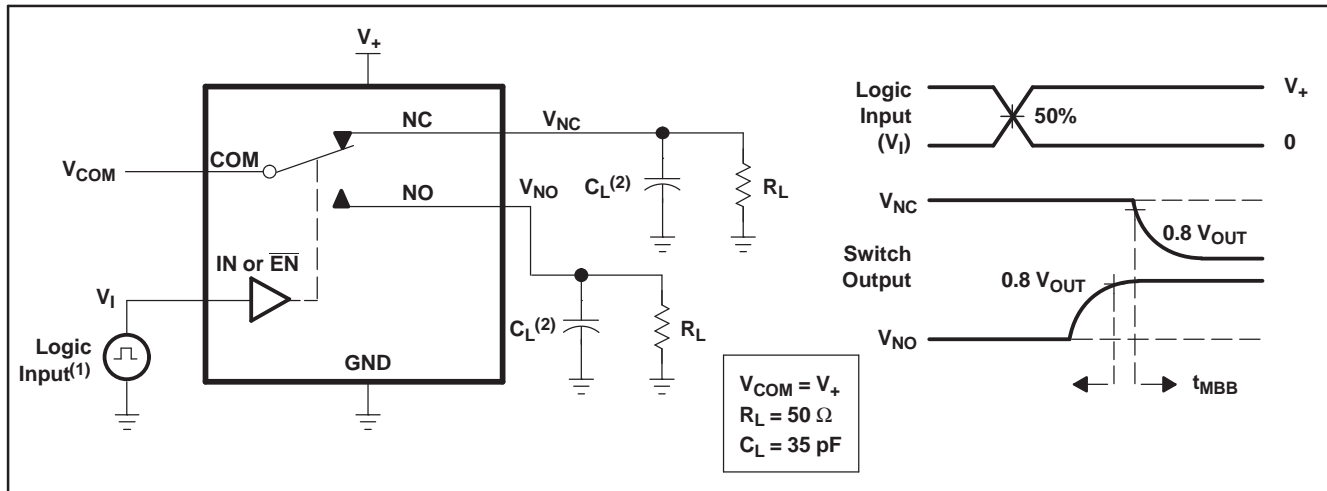
Figure 16. Capacitance (C_I , $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



(1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
 (2) C_L includes probe and jig capacitance.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
- (2) C_L includes probe and jig capacitance.

Figure 18. Make-Before-Break Time (t_{MBB})

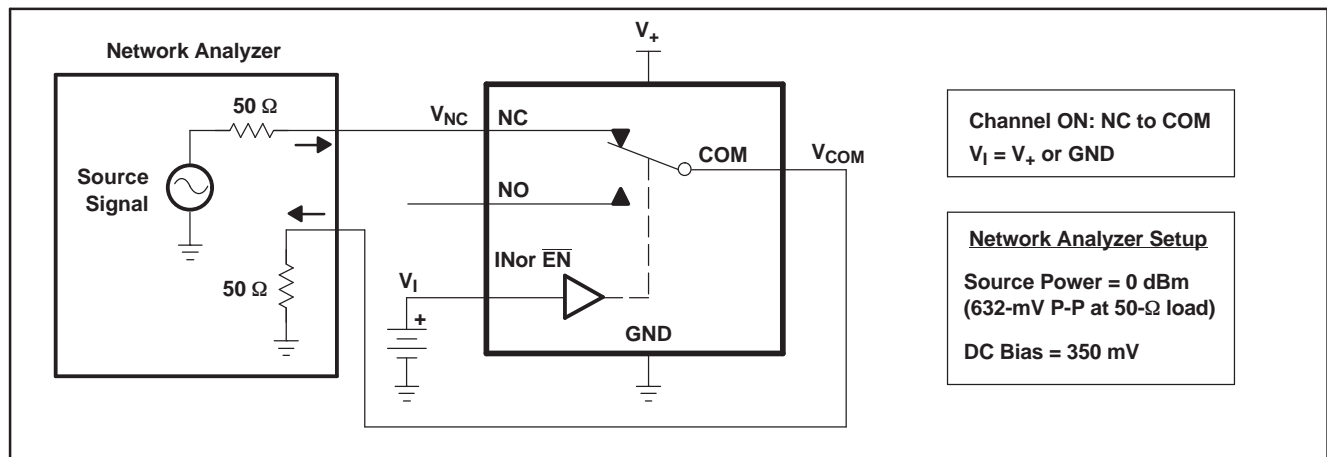


Figure 19. Bandwidth (BW)

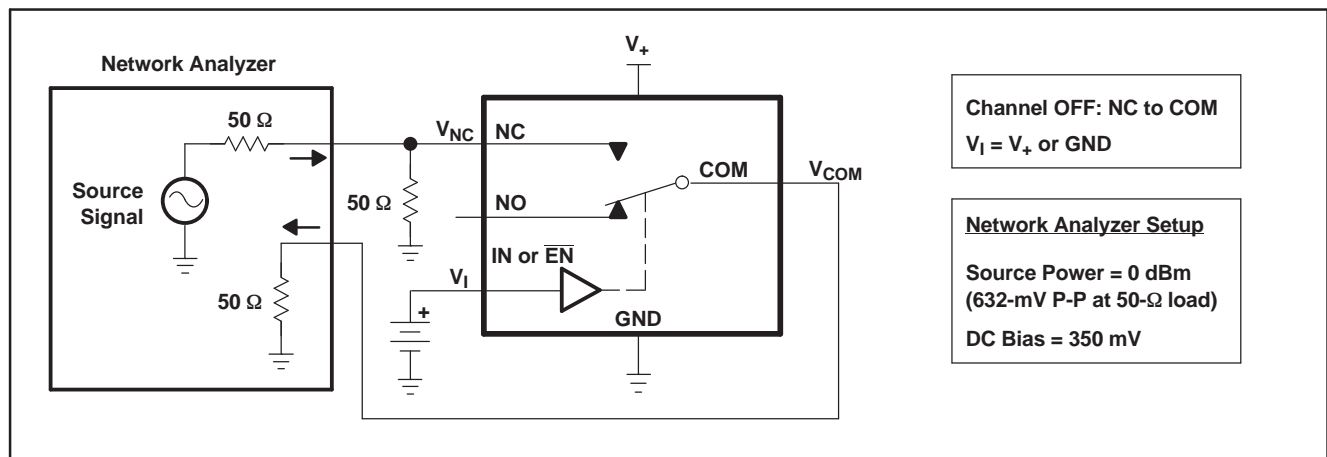


Figure 20. OFF Isolation (O_{ISO})

PARAMETER MEASUREMENT INFORMATION (continued)

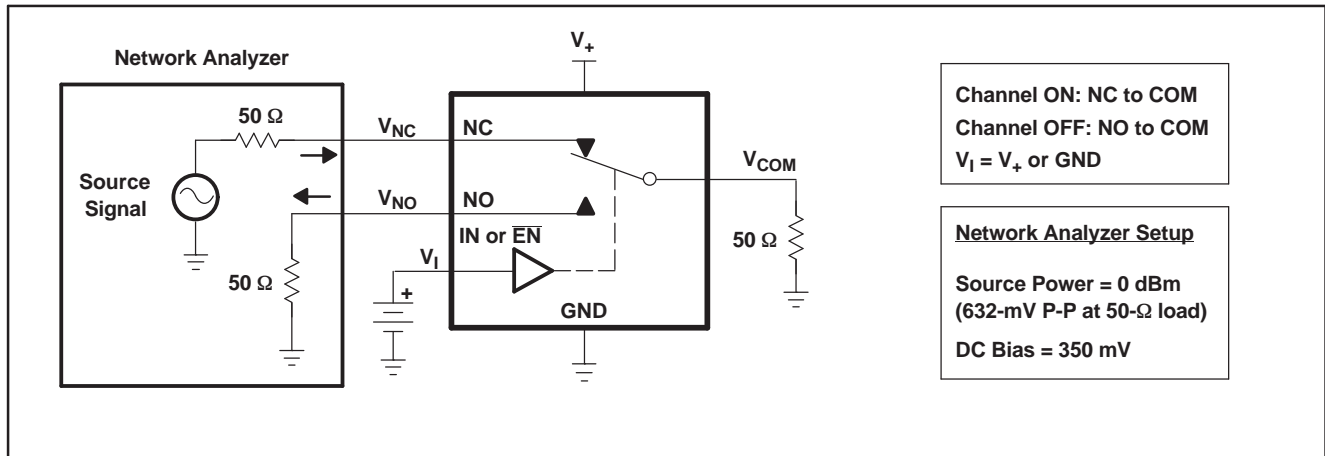
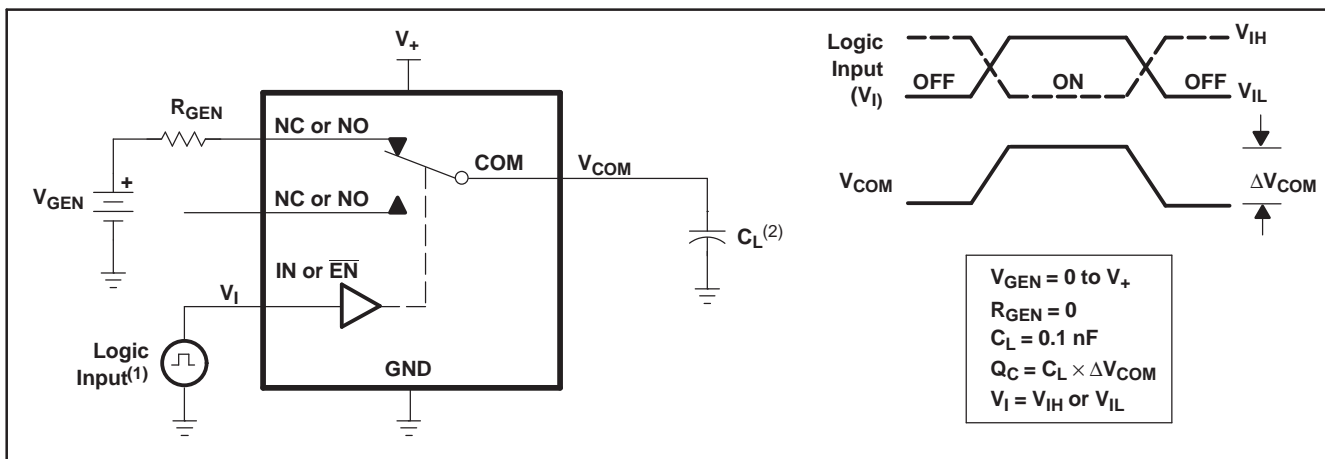


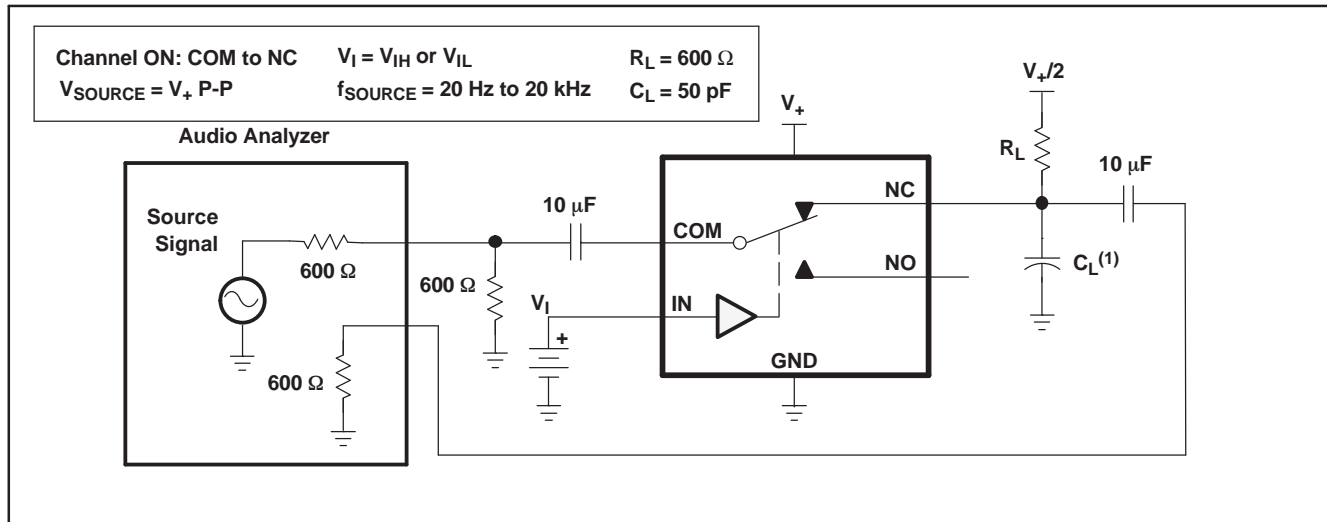
Figure 21. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
 (2) C_L includes probe and jig capacitance.

Figure 22. Charge Injection (Q_C)

PARAMETER MEASUREMENT INFORMATION (continued)



(1) C_L includes probe and jig capacitance.

Figure 23. Total Harmonic Distortion (THD)

REVISION HISTORY

| Changes from Revision B (May 2009) to Revision C | Page |
|--|------|
| • Changed ORDERING INFORMATION Table. | 1 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TS5A3154DCUR | ACTIVE | VSSOP | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | (CF, JCFQ, JCFR) JZ | Samples |
| TS5A3154DCURE6 | PREVIEW | VSSOP | DCU | 8 | 3000 | TBD | Call TI | Call TI | -40 to 85 | | |
| TS5A3154DCURG4 | ACTIVE | VSSOP | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | JCFR | Samples |
| TS5A3154YZPR | ACTIVE | DSBGA | YZP | 8 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (JX7, JXN) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TS5A3154DCUR | VSSOP | DCU | 8 | 3000 | 178.0 | 9.5 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| TS5A3154DCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| TS5A3154DCURG4 | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| TS5A3154YZPR | DSBGA | YZP | 8 | 3000 | 178.0 | 9.2 | 1.02 | 2.02 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TS5A3154DCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| TS5A3154DCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| TS5A3154DCURG4 | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| TS5A3154YZPR | DSBGA | YZP | 8 | 3000 | 220.0 | 220.0 | 35.0 |

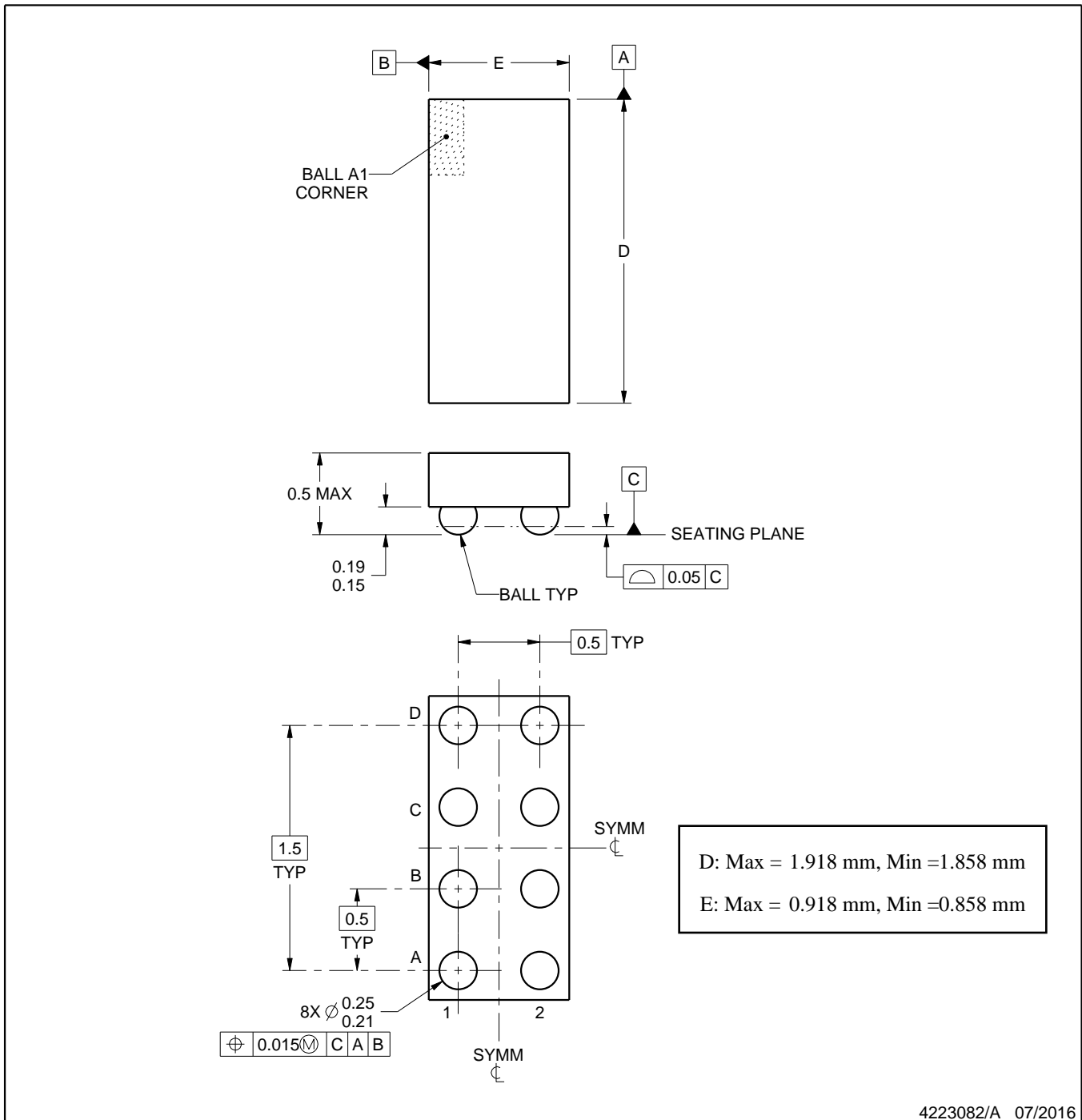
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



4210064/C 04/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated