

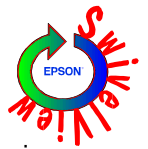
## S1D13742 Mobile Graphics Engine

August 2007

The S1D13742 is a color LCD graphics controller with an embedded 768K byte display buffer. The S1D13742 supports a 8/16-bit Intel 80 CPU architecture while providing high performance bandwidth into display memory allowing for fast screen updates.

Products requiring a rotated display image can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. Resolutions supported include 800x480 single buffered and 352x416 double buffered.

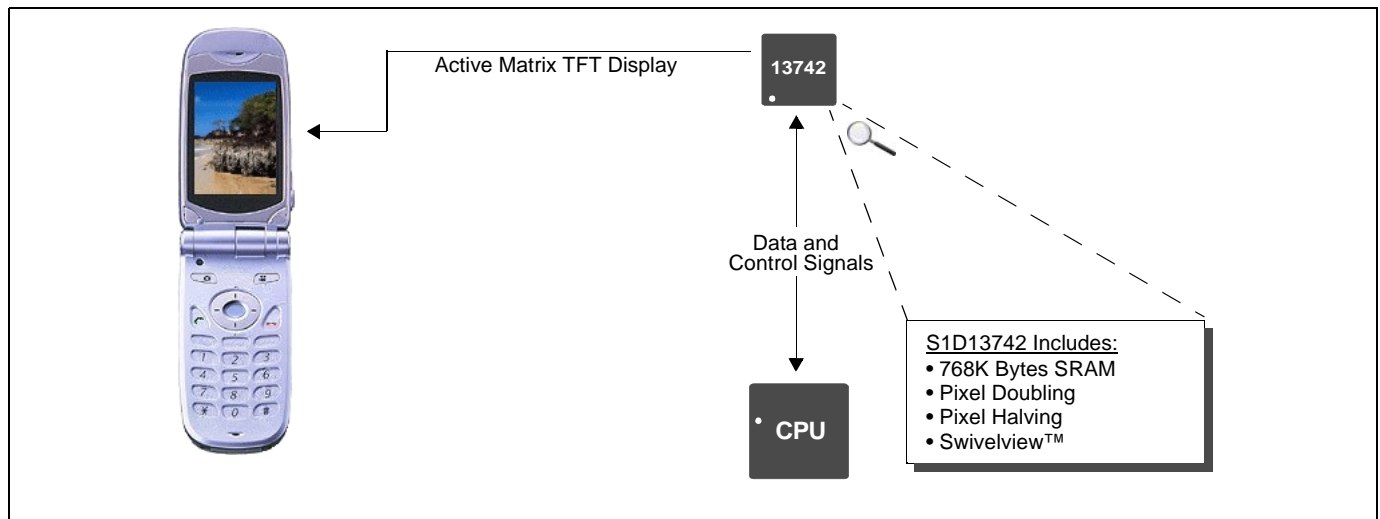
The S1D13742 uses a double-buffer architecture to prevent any visual tearing during streaming video screen updates.



### ■ FEATURES

- Embedded 768K byte SRAM Display Buffer
- Low Operating Voltage
- 8/16-bit Intel 80 interface (used for display or register data).
- RGB: 8:8:8, 6:6:6, 5:6:5 (8:8:8 will be truncated to 16 or 18 bpp).
- YUV 4:2:2, 4:2:0 (Internal YUV to RGB Converter stored as 16 or 18 bpp).
- Active Matrix TFT interface - 18/36-bit interface.
- Supports resolutions up to 800x480.
- Hardware / Software Power Save mode.
- 16/18 bit-per-pixel (bpp) color depths.
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image
- Double-Buffer available to prevent image tearing during streaming input
- Pixel Doubling: Horizontal and Vertical averaging for smooth doubling of a single window
- Pixel Halving: no limitation on number of windows
- Internal programmable PLL.
- Single MHz clock input: CLKI.
- General Purpose Input/Output pins.

### ■ SYSTEM BLOCK DIAGRAM



## S1D13742

### DESCRIPTION

#### Integrated Frame Buffer

- Embedded 768K byte SRAM display buffer.

#### CPU Interface

- 8/16-bit Intel 80 interface (used for display or register data).
- Chip select is used to select device. When inactive, any input data/command will be ignored.

#### Panel Support

- Active Matrix TFT interface.
- 18/36-bit interface.
- Supports resolutions up to 800x480.

#### Miscellaneous

- Internal programmable PLL.
- Single MHz clock input: CLKI.
- CLKI available as CLKOUT (separate CLKOUTEN pin associated with output).
- Hardware / Software Power Save mode.
- Input pin to Enable/Disable Power Save Mode.
- General Purpose Input/Output pins are available (GPIO[7:0]).
- COREVDD 1.5 volts and IOVDD 1.65 ~ 3.6 volts
- FCBGA 121-pin or QFP20 144-pin package

#### Digital Video

- RGB: 8:8:8, 6:6:6, 5:6:5 (8:8:8 will be truncated to 16 or 18 bpp).
- YUV 4:2:2, 4:2:0 (Internal YUV to RGB Converter stored as 16 or 18 bpp).

#### Display Features

- 16/18 bit-per-pixel (bpp) color depths.
- 16 bpp to 18 bpp Input Data conversion.
- All display writes are handled by window apertures/position for complete or partial display updates. All window coordinates are referenced to top left corner of the displayed image (even in a rotated display, the top-left corner is maintained and no host side translation need take place).
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image. All displayed windows can have independent rotation. No additional programming necessary when enabling these modes.
- Double-Buffer available to prevent image tearing during streaming input. Resolutions supported must fit inside 384K bytes (½ of total available display buffer). Typical resolution of 352x416.
- Pixel Doubling: Horizontal and Vertical averaging for smooth doubling of a single window.
- Pixel Halving: no limitation on number of windows.

### CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- S1D13742 Technical Documentation
- S1D13742 Evaluation Boards
- CPU Independent Software Utilities
- Royalty Free source level driver code

#### Japan

Seiko Epson Corporation  
IC International Sales Group  
421-8, Hino, Hino-shi  
Tokyo 191-8501, Japan  
Tel: 042-587-5812  
Fax: 042-587-5564  
<http://www.epson.co.jp/>

#### Hong Kong

Epson Hong Kong Ltd.  
20/F., Harbour Centre  
25 Harbour Road  
Wanchai, Hong Kong  
Tel: 2585-4600  
Fax: 2827-4346  
<http://www.epson.com.hk/>

#### North America

Epson Electronics America, Inc.  
2580 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: (408) 922-0200  
Fax: (408) 922-0238  
<http://www.eea.epson.com/>

#### Europe

Epson Europe Electronics GmbH  
Riesstrasse 15  
80992 Munich, Germany  
Tel: 089-14005-0  
Fax: 089-14005-110  
<http://www.epson-electronics.de/>

#### Taiwan

Epson Taiwan Technology & Trading Ltd.  
14F, No. 7  
Song Ren Road  
Taipei 110  
Tel: 02-8786-6688  
Fax: 02-8786-6677  
<http://www.epson.com.tw/>

#### Singapore

Epson Singapore Pte Ltd  
1 HarbourFront Place #03-02  
HarbourFront Tower One  
Singapore, 098633  
Tel: (65) 6586-5500  
Fax: (65) 6271-3182  
<http://www.epson.com.sg/>

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