

# NCS325, NCS2325, NCS4325

## 50 $\mu\text{V}$ Offset, 0.25 $\mu\text{V}/^\circ\text{C}$ , 35 $\mu\text{A}$ , Zero-Drift Operational Amplifier

The NCS325, NCS2325 and NCS4325 are CMOS operational amplifiers providing precision performance. The Zero-Drift architecture allows for continuous auto-calibration, which provides very low offset, near-zero drift over time and temperature, and near flat 1/f noise at only 35  $\mu\text{A}$  (max) quiescent current. These benefits make these devices ideal for precision DC applications. These op amps provide rail-to-rail input and output performance and are optimized for low voltage operation as low as 1.8 V and up to 5.5 V. The single channel NCS325 is available in the space-saving SOT23-5 package. The dual channel NCS2325 is available in Micro8, SOIC-8, and DFN-8. The quad channel NCS4325 is available in SOIC-14.

### Features

- Low Offset Voltage: 14  $\mu\text{V}$  typ, 50  $\mu\text{V}$  max at 25°C for NCS325
- Zero Drift: 0.25  $\mu\text{V}/^\circ\text{C}$  max
- Low Noise: 1  $\mu\text{Vpp}$ , 0.1 Hz to 10 Hz
- Quiescent Current: 21  $\mu\text{A}$  typ, 35  $\mu\text{A}$  max at 25°C
- Supply Voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input and Output
- Internal EMI Filtering
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

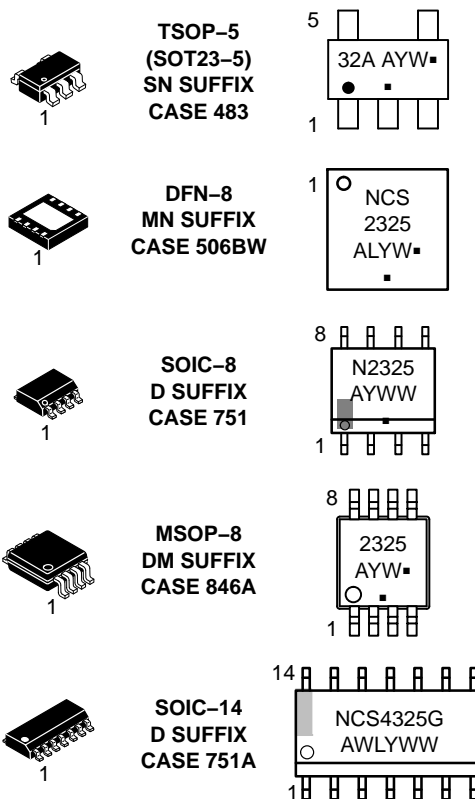
- Battery Powered Instruments
- Temperature Measurements
- Transducer Applications
- Electronic Scales
- Medical Instrumentation
- Current Sensing



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### MARKING DIAGRAMS



A = Assembly Location  
Y = Year  
WL = Wafer Lot  
W or WW = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

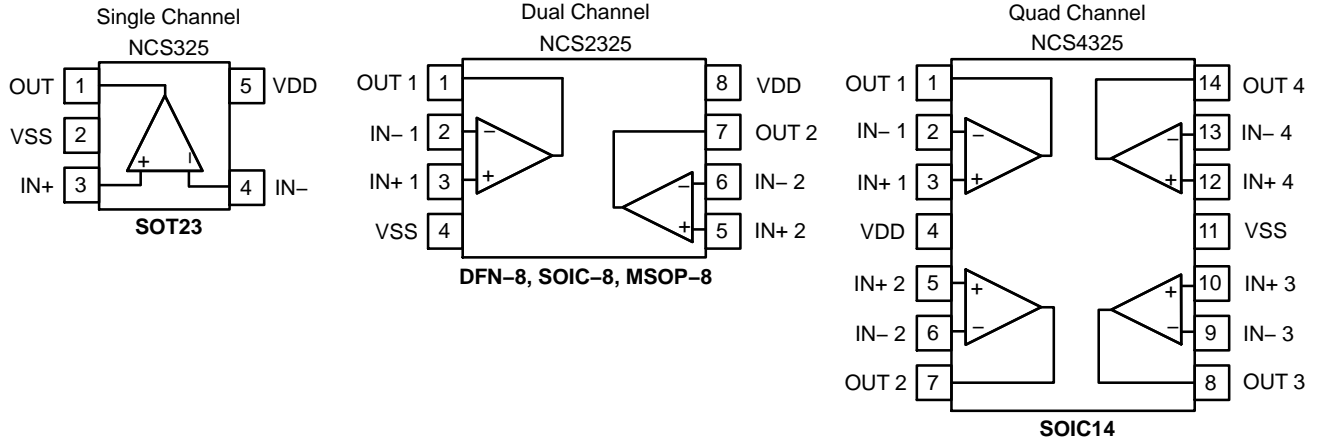
### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

# NCS325, NCS2325, NCS4325

## PIN CONNECTIONS



## ORDERING INFORMATION

Configuration	Device	Package	Shipping†
Single	NCS325SN2T1G	SOT23-5 / TSOP-5	3000 / Tape & Reel
Dual	NCS2325MNTXG* (In Development)	DFN8	3000 / Tape & Reel
	NCS2325DR2G	SOIC-8	3000 / Tape & Reel
	NCS2325DMR2G	Micro8 / MSOP-8	4000 / Tape & Reel
Quad	NCS4325DR2G	SOIC-14	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*Contact local sales office for more information

# NCS325, NCS2325, NCS4325

**ABSOLUTE MAXIMUM RATINGS** Over operating free-air temperature, unless otherwise stated.

Parameter	Rating	Unit
Supply Voltage	6	V

## INPUT AND OUTPUT PINS

Input Voltage (Note 1)	$(V_{SS}) - 0.3$ to $(V_{DD}) + 0.3$	V
Input Current (Note 1)	$\pm 10$	mA
Output Short Circuit Current (Note 2)	Continuous	

## TEMPERATURE

Operating Temperature	-40 to +150	°C
Storage Temperature	-65 to +150	°C
Junction Temperature	+150	°C

## ESD RATINGS (Note 3)

Human Body Model (HBM)	4000	V
Machine Model (MM)	200	V

## OTHER RATINGS

Latch-up Current (Note 4)	100	mA
MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less
- Short-circuit to ground.
- This device series incorporates ESD protection and is tested by the following methods:  
ESD Human Body Model tested per AEC-Q100-002 (JEDEC standard: JESD22-A114)  
ESD Machine Model tested per AEC-Q100-003 (JEDEC standard: JESD22-A115)
- Latch-up Current tested per JEDEC standard: JESD78.

## THERMAL INFORMATION

Thermal Metric	Symbol	Package	Value	Unit
Junction to Ambient (Note 5)	$\theta_{JA}$	SOT23-5 / TSOP-5	235	°C/W
		Micro8 / MSOP-8	298	
		SOIC-8	250	
		DFN-8	130	
		SOIC-14	216	

- As mounted on an 80x80x1.5 mm FR4 PCB with 650 mm<sup>2</sup> and 2 oz (0.034 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines

## OPERATING CONDITIONS

Parameter	Symbol	Range	Unit
Supply Voltage ( $V_{DD} - V_{SS}$ )	$V_S$	1.8 to 5.5	V
Specified Operating Range	$T_A$	-40 to 125	°C
Input Common Mode Voltage Range	$V_{ICMR}$	$V_{SS}-0.1$ to $V_{DD}+0.1$	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NCS325, NCS2325, NCS4325

## ELECTRICAL CHARACTERISTICS: $V_S = 1.8\text{ V}$ to $5.5\text{ V}$

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
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### INPUT CHARACTERISTICS

Offset Voltage	$V_{OS}$	NCS325	$V_S = +5\text{ V}$		14	50	$\mu\text{V}$
		NCS2325, NCS4325	$V_S = +5\text{ V}$		14	75	
Offset Voltage Drift vs Temp	$\Delta V_{OS}/\Delta T$	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$			<b>0.02</b>	<b>0.25</b>	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_{IB}$				$\pm 50$		$\text{pA}$
Input Offset Current	$I_{OS}$				$\pm 100$		$\text{pA}$
Common Mode Rejection Ratio	CMRR	NCS325	$V_{SS}+0.3 < V_{CM} < V_{DD} - 0.3$ , $V_S = 1.8\text{ V}$	<b>85</b>	108		dB
			$V_{SS}+0.3 < V_{CM} < V_{DD} - 0.3$ , $V_S = 5.5\text{ V}$	<b>90</b>	110		
		NCS2325, NCS4325	$V_{SS}+0.3 < V_{CM} < V_{DD} - 0.3$ , $V_S = 5\text{ V}$	<b>90</b>	110		
			$V_{SS}-0.1 < V_{CM} < V_{DD} + 0.1$ , $V_S = 1.8\text{ V}$		80		
			$V_{SS}-0.1 < V_{CM} < V_{DD} + 0.1$ , $V_S = 5.5\text{ V}$		92		
Input Resistance	$R_{IN}$				15		$\text{G}\Omega$
Input Capacitance	$C_{IN}$	NCS325	Differential		1.8		$\text{pF}$
			Common Mode		3.5		$\text{pF}$
		NCS2325, NCS4325	Differential		4.1		$\text{pF}$
			Common Mode		8.0		$\text{pF}$

### OUTPUT CHARACTERISTICS

Output Voltage High	$V_{OH}$	Output swing within $V_{DD}$		12	100	$\text{mV}$
Output Voltage Low	$V_{OL}$	Output swing within $V_{SS}$		8	100	$\text{mV}$
Short Circuit Current	$I_{SC}$			$\pm 5$		$\text{mA}$
Open Loop Output Impedance	$Z_{out-OL}$	$f = 350\text{ kHz}$ , $I_O = 0\text{ mA}$ , $V_S = 1.8\text{ V}$		1.4		$\text{k}\Omega$
		$f = 350\text{ kHz}$ , $I_O = 0\text{ mA}$ , $V_S = 5.5\text{ V}$		2.7		
Capacitive Load Drive	$C_L$			See Figure		

### NOISE PERFORMANCE

Voltage Noise Density	$e_N$	$f_{IN} = 1\text{ kHz}$		100		$\text{nV} / \sqrt{\text{Hz}}$
Voltage Noise	$e_{P-P}$	$f_{IN} = 0.01\text{ Hz}$ to $1\text{ Hz}$		0.3		$\mu\text{V}_{PP}$
		$f_{IN} = 0.1\text{ Hz}$ to $10\text{ Hz}$		1		$\mu\text{V}_{PP}$
Current Noise Density	$i_N$	$f_{IN} = 10\text{ Hz}$		0.3		$\text{pA} / \sqrt{\text{Hz}}$

### DYNAMIC PERFORMANCE

Open Loop Voltage Gain	$A_{VOL}$	$R_L = 10\text{ k}\Omega$ , $V_S = 5.5\text{ V}$				114		dB
Gain Bandwidth Product	GBWP	NCS325	$C_L = 100\text{ pF}$ , $R_L = 10\text{ k}\Omega$		350			kHz
		NCS2325, NCS4325	$C_L = 100\text{ pF}$ , $R_L = 10\text{ k}\Omega$		270			
Phase Margin	$\phi_M$	$C_L = 100\text{ pF}$				60		$^\circ$
Gain Margin	$A_M$	$C_L = 100\text{ pF}$				20		dB
Slew Rate	SR	$G = +1$ , $C_L = 100\text{ pF}$ , $V_S = 1.8\text{ V}$				0.10		$\text{V}/\mu\text{s}$
		$G = +1$ , $C_L = 100\text{ pF}$ , $V_S = 5.5\text{ V}$				0.16		

### POWER SUPPLY

Power Supply Rejection Ratio	PSRR		100	107		dB		
		$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	<b>95</b>					
Turn-on Time	$t_{ON}$	$V_S = 5\text{ V}$				100	$\mu\text{s}$	
Quiescent Current	$I_Q$	No load				21	<b>35</b>	$\mu\text{A}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NCS325, NCS2325, NCS4325

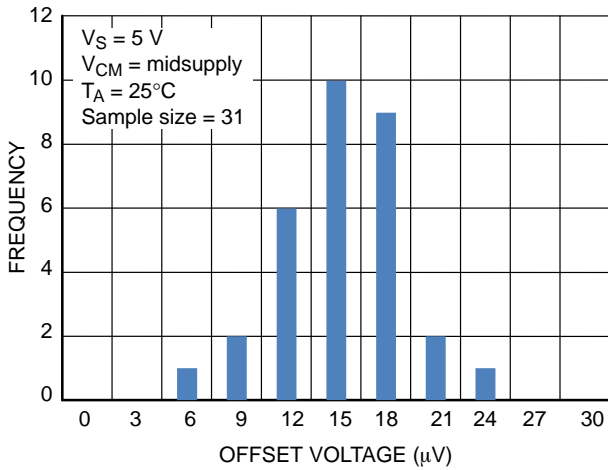


Figure 1. Offset Voltage Distribution

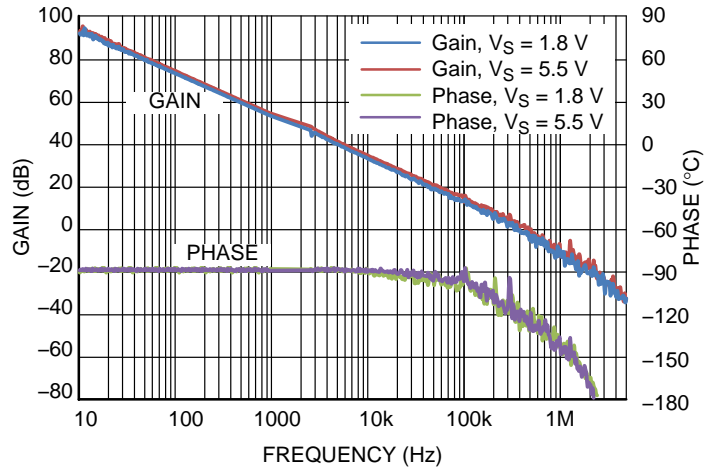


Figure 2. Gain and Phase vs. Frequency

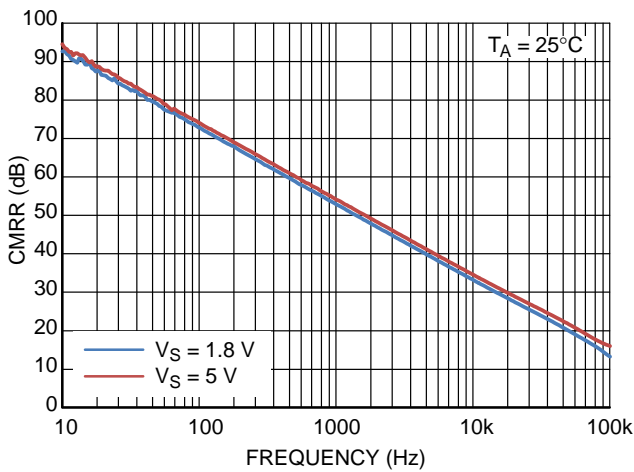


Figure 3. CMRR vs. Frequency

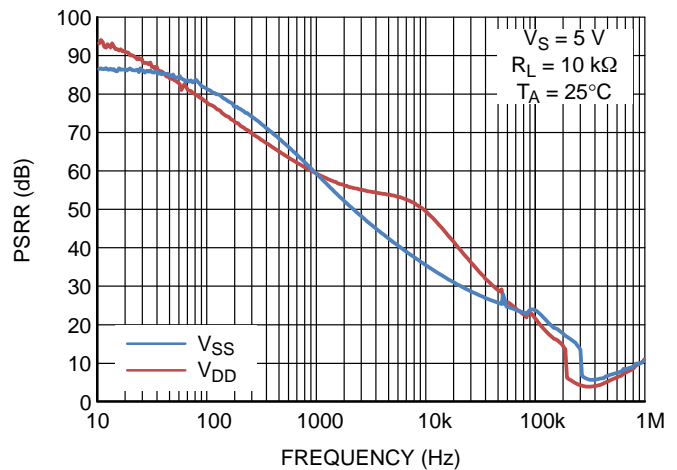


Figure 4. PSRR vs. Frequency

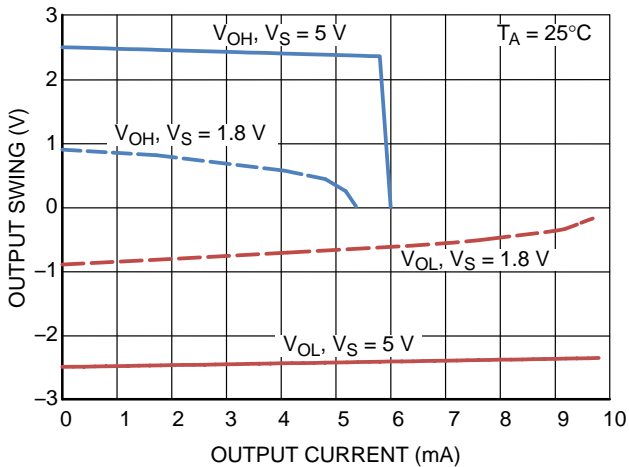


Figure 5. Output Voltage Swing vs. Output Current

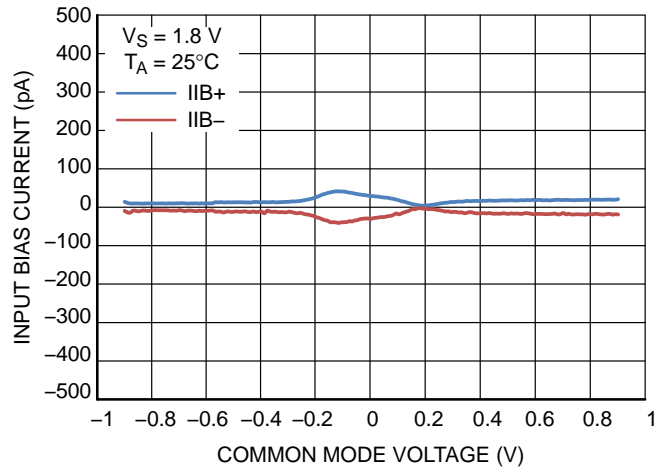
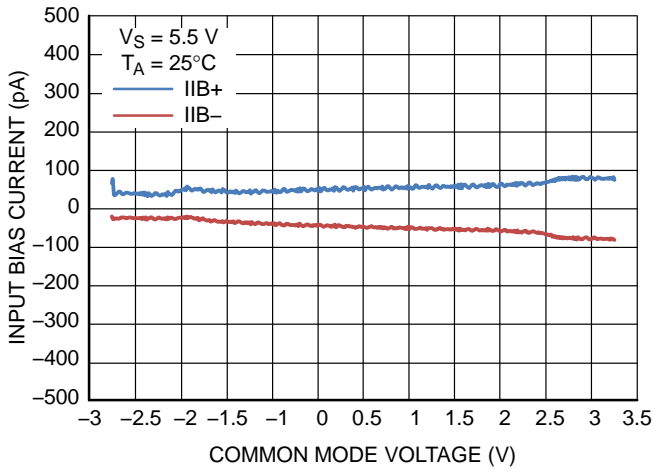
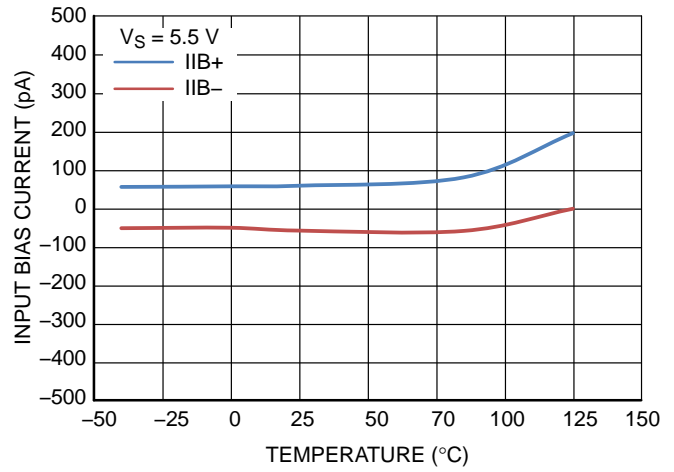


Figure 6. Input Bias Current vs. Common Mode Voltage,  $V_S = 1.8\text{ V}$

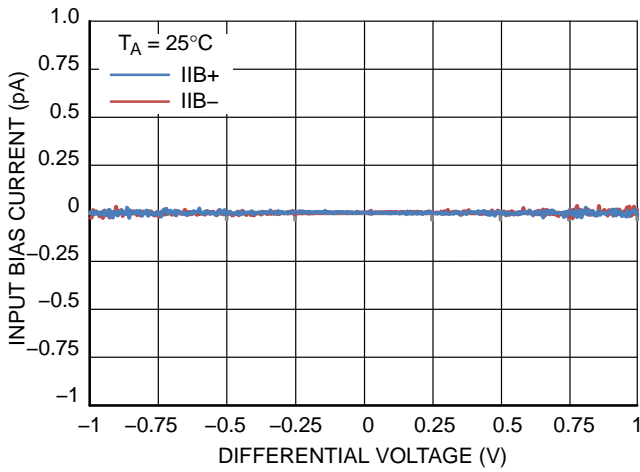
# NCS325, NCS2325, NCS4325



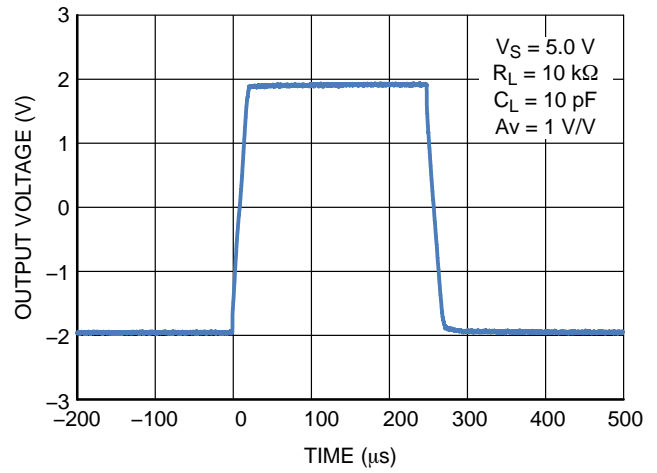
**Figure 7. Input Bias Current vs. Common Mode Voltage,  $V_S = 5.5\text{ V}$**



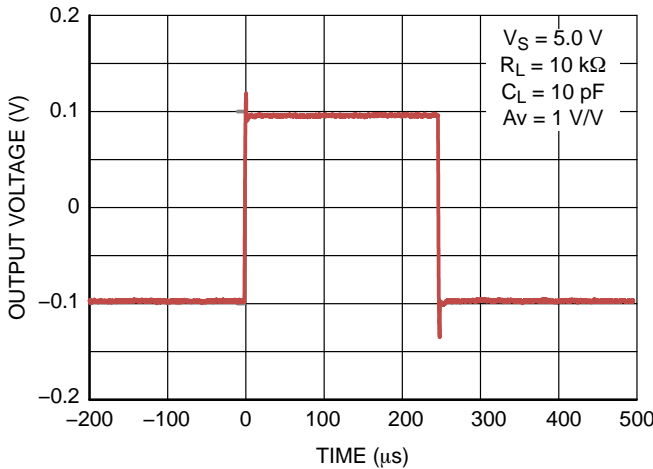
**Figure 8. Input Bias Current vs. Temperature**



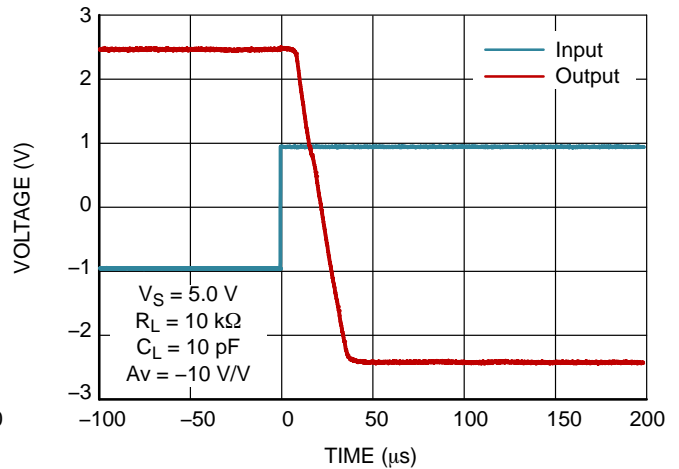
**Figure 9. Input Bias Current vs. Input Differential Voltage**



**Figure 10. Large Signal Step Response**



**Figure 11. Small Signal Step Response**



**Figure 12. Positive Over Voltage Recovery**

# NCS325, NCS2325, NCS4325

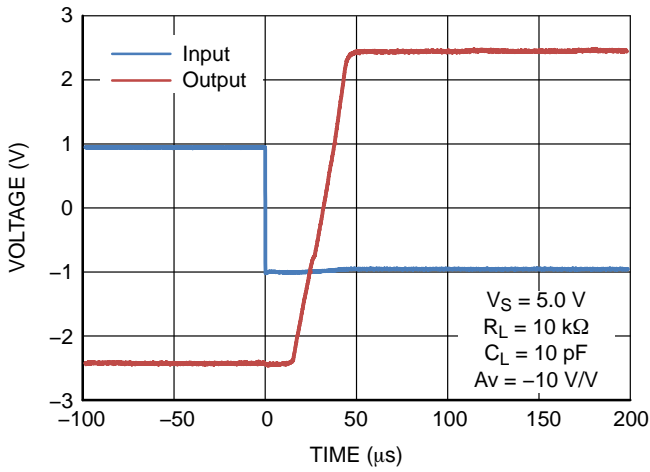


Figure 13. Negative Over Voltage Recovery

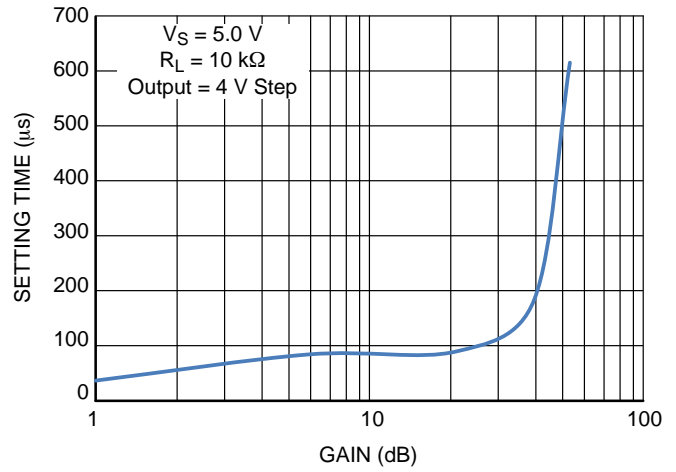


Figure 14. Setting Time vs. Closed Loop Gain

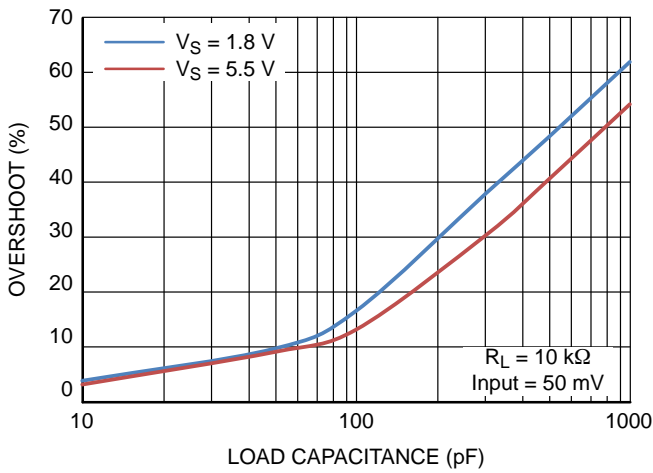


Figure 15. Small Signal Overshoot vs. Load Capacitance

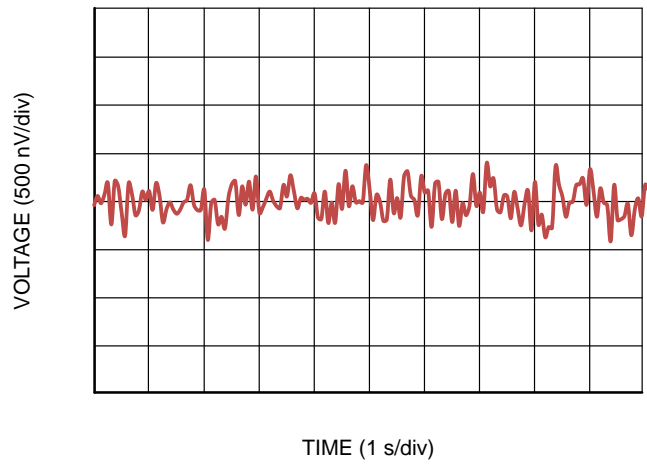


Figure 16. 0.1 Hz to 10 Hz Noise

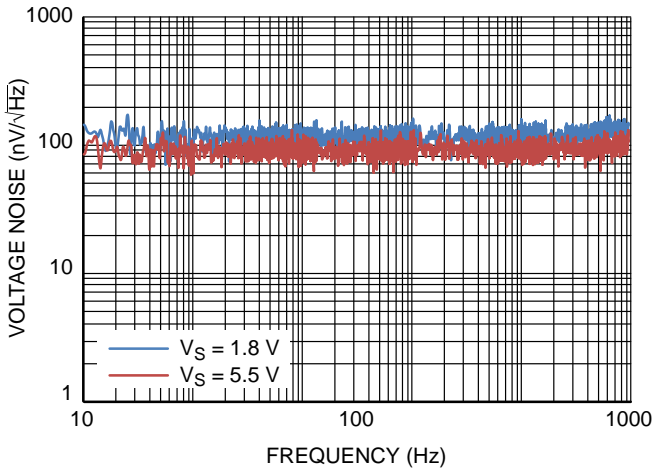


Figure 17. Voltage Noise Spectral Density vs. Frequency

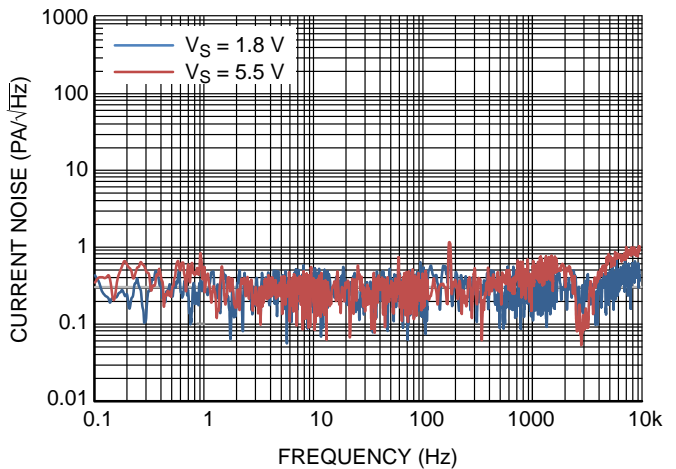


Figure 18. Current Noise Spectral Density vs. Frequency

# NCS325, NCS2325, NCS4325

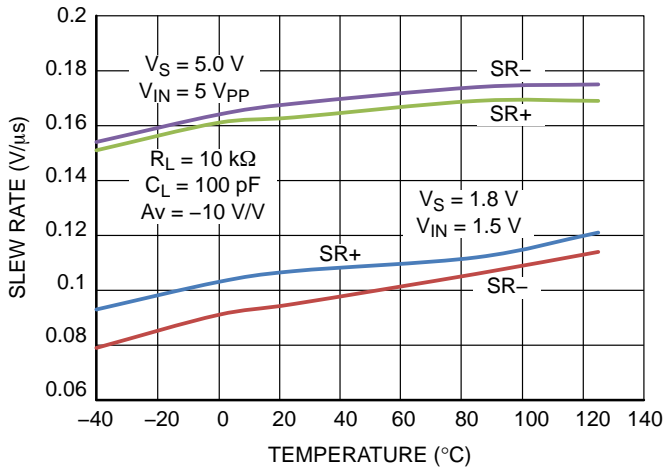


Figure 19. Slew Rate vs. Temperature

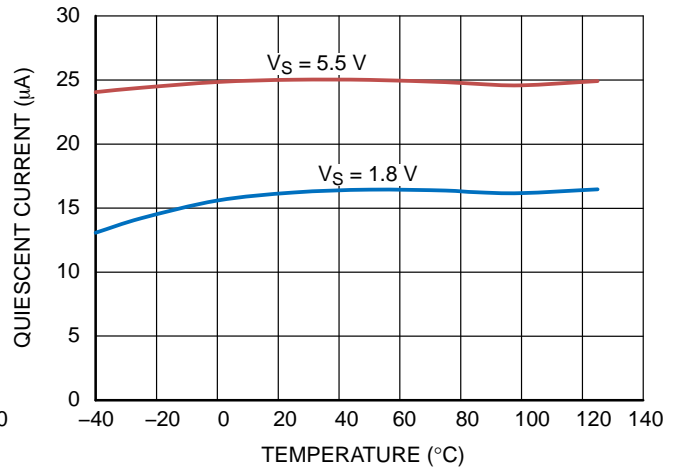


Figure 20. Quiescent Current vs. Temperature

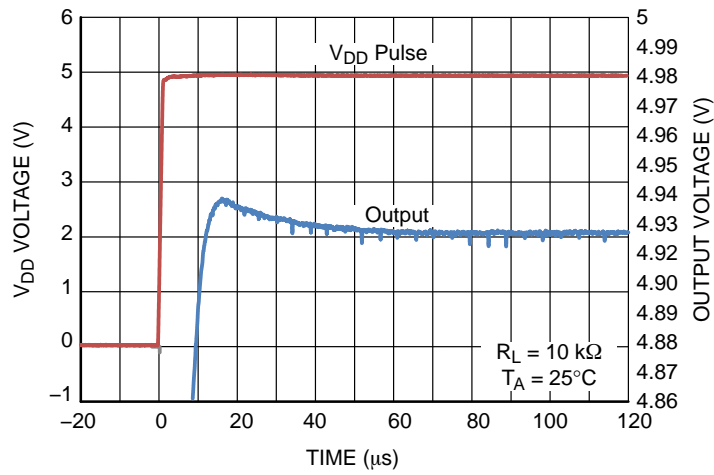


Figure 21. Turn-on Response



APPLICATIONS INFORMATION

INPUT VOLTAGE

The NCS325, NCS2325 and NCS4325 have rail-to-rail common mode input voltage range. Diodes between the inputs and the supply rails keep the input voltage from exceeding the rails.

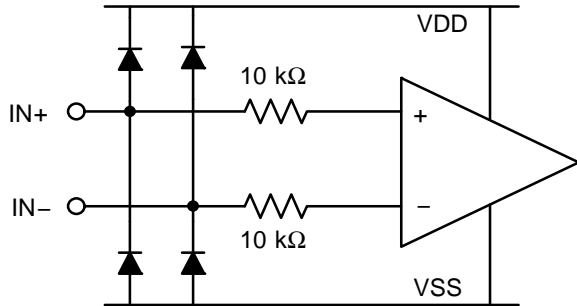


Figure 22. Equivalent Input Circuit

EMI SUSCEPTIBILITY AND INPUT FILTERING

Op amps have varying amounts of EMI susceptibility. Semiconductor junctions can pick up and rectify EMI signals, creating an EMI-induced voltage offset at the output, adding another component to the total error. Input pins are the most sensitive to EMI. The NCS325, NCS2325 and NCS4325 integrate a low-pass filter to decrease its sensitivity to EMI.

APPLICATION CIRCUITS

Low-Side Current Sensing

The goal of low-side current sensing is to detect over-current conditions or as a method of feedback control. A sense resistor is placed in series with the load to ground. Typically, the value of the sense resistor is less than 100 mΩ to reduce power loss across the resistor. The op amp amplifies the voltage drop across the sense resistor with a gain set by external resistors R1, R2, R3, and R4 (where R1 = R2, R3 = R4). Precision resistors are required for high accuracy, and the gain is set to utilize the full scale of the ADC for the highest resolution.

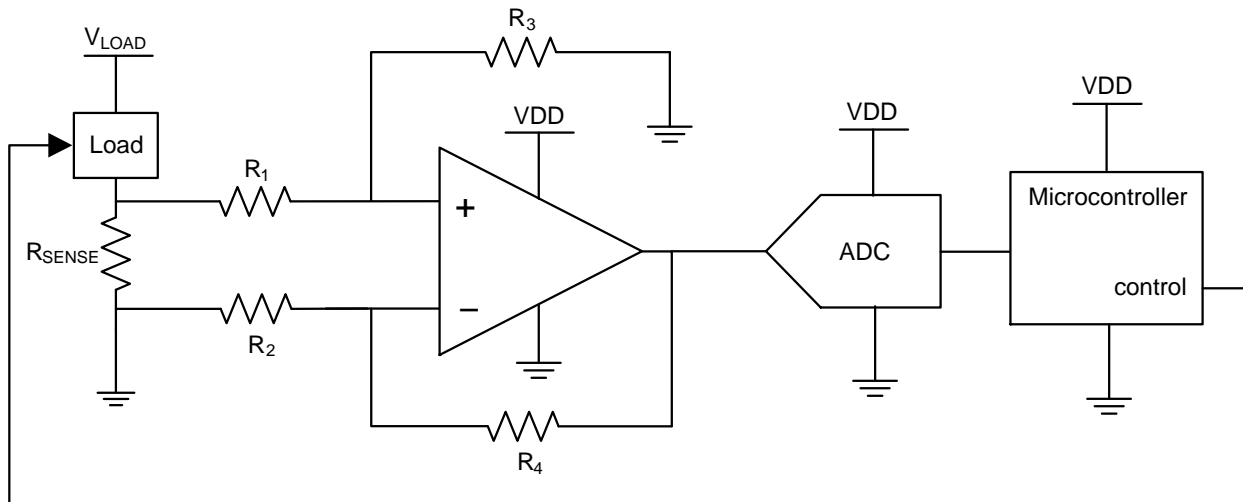


Figure 23. Low-Side Current Sensing

### Differential Amplifier for Bridged Circuits

Sensors to measure strain, pressure, and temperature are often configured in a Wheatstone bridge circuit as shown in Figure 24. In the measurement, the voltage change that is

produced is relatively small and needs to be amplified before going into an ADC. Precision amplifiers are recommended in these types of applications due to their high gain, low noise, and low offset voltage.

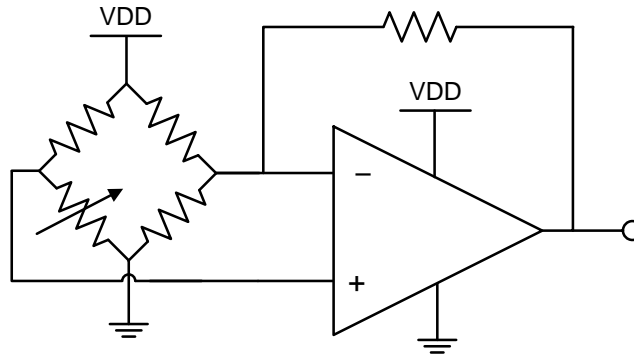


Figure 24. Bridge Circuit Amplification

### GENERAL LAYOUT GUIDELINES

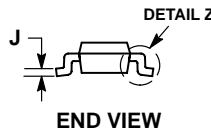
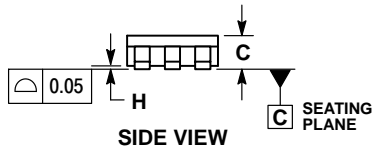
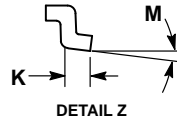
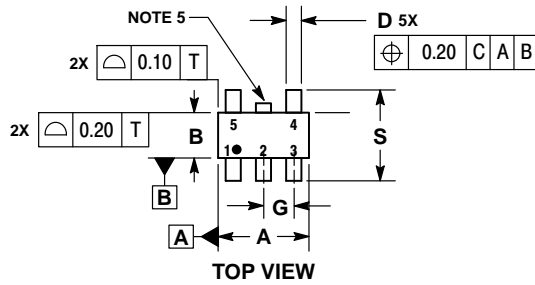
To ensure optimum device performance, it is important to follow good PCB design practices. Place 0.1  $\mu$ F decoupling capacitors as close as possible to the supply pins. Keep traces short, utilize a ground plane, choose surface-mount components, and place components as close as possible to

the device pins. These techniques will reduce susceptibility to electromagnetic interference (EMI). Thermoelectric effects can create an additional temperature dependent offset voltage at the input pins. To reduce these effects, use metals with low thermoelectric-coefficients and prevent temperature gradients from heat sources or cooling fans.

# NCS325, NCS2325, NCS4325

## PACKAGE DIMENSIONS

### TSOP-5 CASE 483-02 ISSUE K

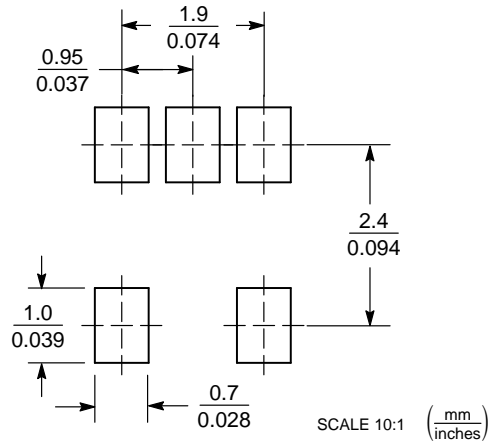


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	3.00	BSC
B	1.50	BSC
C	0.90	1.10
D	0.25	0.50
G	0.95	BSC
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

### SOLDERING FOOTPRINT\*

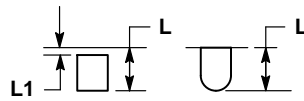
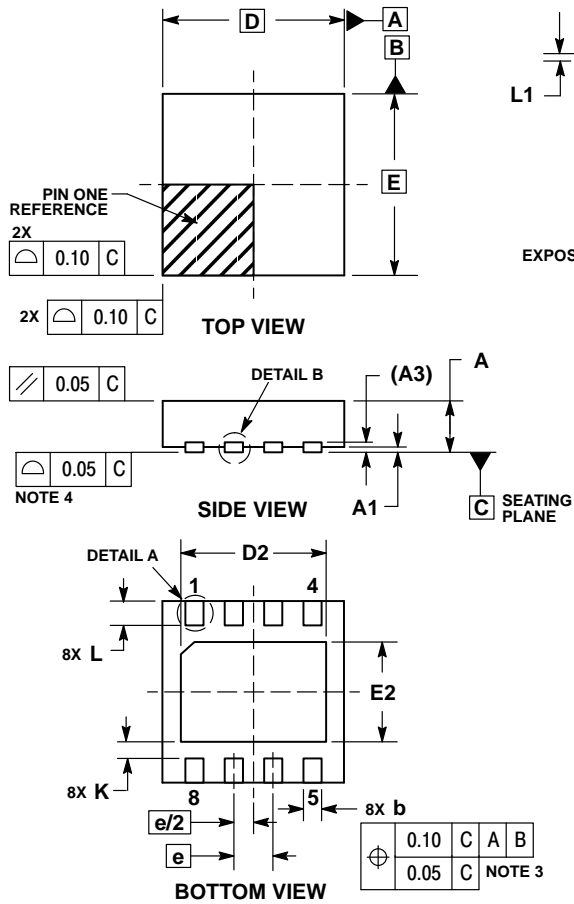


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

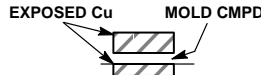
# NCS325, NCS2325, NCS4325

## PACKAGE DIMENSIONS

DFN8, 3x3, 0.65P  
CASE 506BW-01  
ISSUE O



DETAIL A  
OPTIONAL  
CONSTRUCTIONS



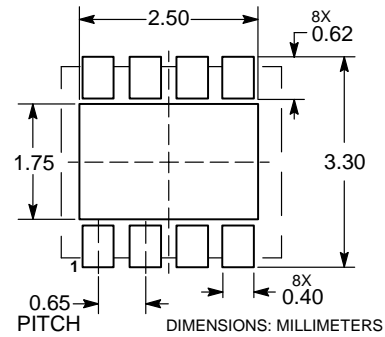
DETAIL B  
OPTIONAL  
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.25	0.35
D	3.00	BSC
D2	2.30	2.50
E	3.00	BSC
E2	1.55	1.75
e	0.65	BSC
K	0.20	---
L	0.35	0.45
L1	0.00	0.15

### RECOMMENDED SOLDERING FOOTPRINT\*

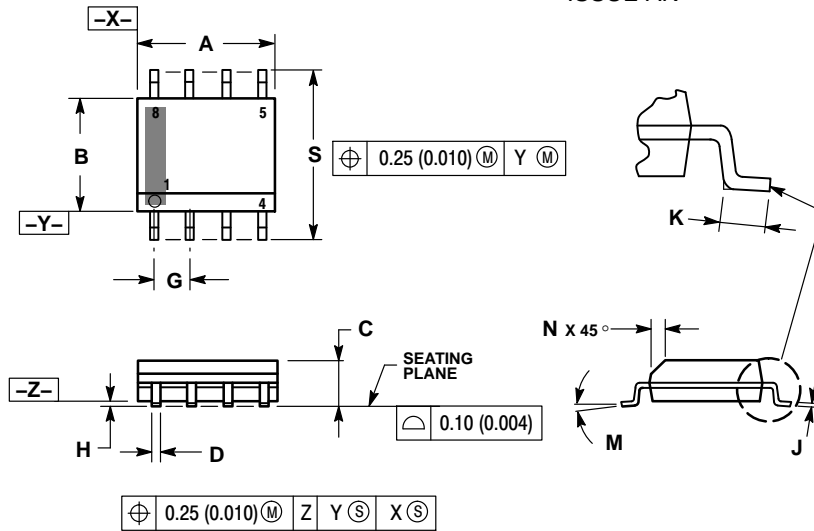


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NCS325, NCS2325, NCS4325

## PACKAGE DIMENSIONS

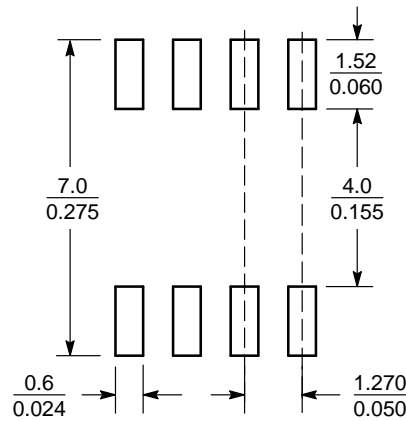
SOIC-8 NB  
CASE 751-07  
ISSUE AK



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



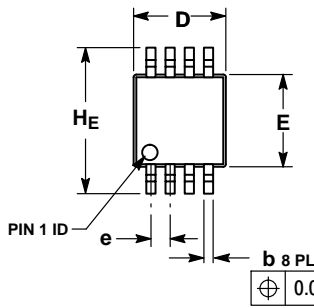
SCALE 6:1 ( $\frac{\text{mm}}{\text{inches}}$ )

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

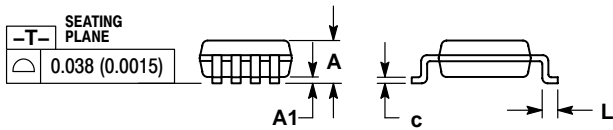
# NCS325, NCS2325, NCS4325

## PACKAGE DIMENSIONS

**Micro8™**  
CASE 846A-02  
ISSUE J



$\oplus$	0.08 (0.003)	$\textcircled{M}$	T	B	$\textcircled{S}$	A	$\textcircled{S}$
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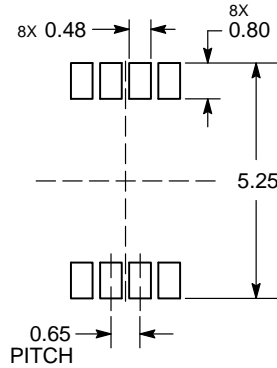


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
HE	4.75	4.90	5.05	0.187	0.193	0.199

### RECOMMENDED SOLDERING FOOTPRINT\*



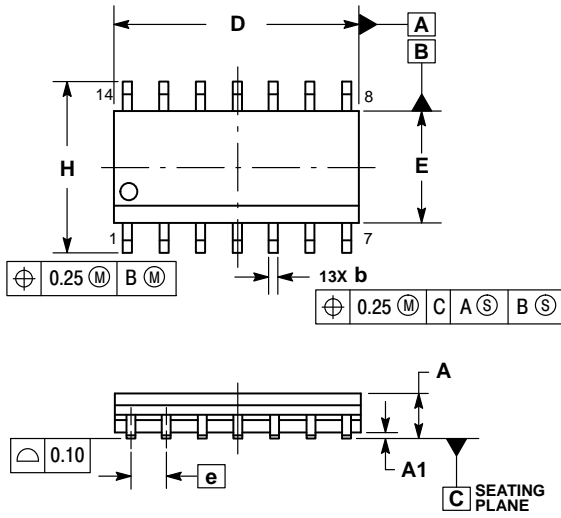
DIMENSION: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NCS325, NCS2325, NCS4325

## PACKAGE DIMENSIONS

### SOIC-14 NB CASE 751A-03 ISSUE L

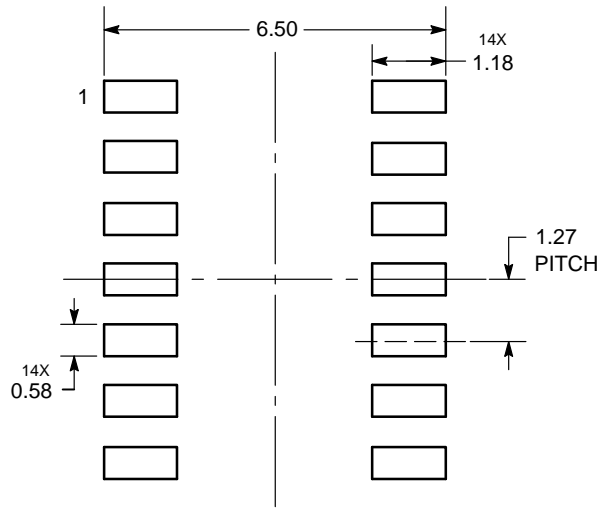


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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