SN74AVC16T245-Q1 16-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H3B (JESD 22 A114-A)
  - Device CDM ESD Classification Level C5 (JESD 22 C101)
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature – If Either V_{CC} Input is at GND, Both Ports Are in the High-Impedance State
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I_{off} Supports Partial-Power-Down Mode Operation
- I/Os Are 4.6-V Tolerant
- Maximum Data Rates
  - 380 Mbps (1.8-V to 3.3-V Translation)
  - 200 Mbps (<1.8-V to 3.3-V Translation)
  - 200 Mbps (Translate to 2.5 V or 1.8 V)
  - 150 Mbps (Translate to 1.5 V)
  - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Telematics
- Clusters
- Head Units
- Navigation Systems

3 Description

The SN74AVC16T245-Q1 is a 16-bit noninverting bus transceiver that uses two separate configurable power-supply rails. The SN74AVC16T245-Q1 is optimized to operate with V_{CCA} or V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA} or V_{CCB} as low as 1.2 V. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

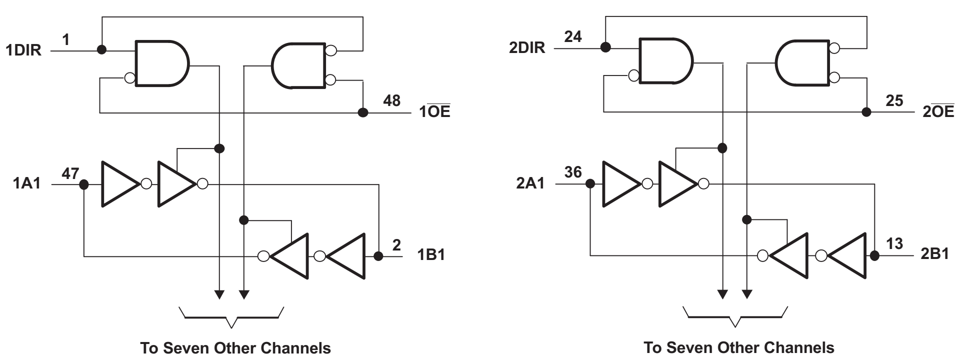
The SN74AVC16T245-Q1 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so the buses effectively are isolated.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVC16T245-Q1	TVSOP (48)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2008) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations*section,*Layout* section, *Device and Documentation Support*section, and*Mechanical, Packaging, and Orderable Information* section 1
- Deleted *Ordering Information* table; see the POA at the end of the data sheet 1
- Deleted Overvoltage-Tolerant Inputs/Outputs Allow Mixed- Voltage-Mode Data Communications bullet from *Features* 1
- Deleted ESD Protection Exceeds JESD 22 from *Features* 1
- Changed the *Thermal Information* table 7

5 Description (continued)

The SN74AVC16T245-Q1 is designed so that the control pins (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) are supplied by V_{CCA}.

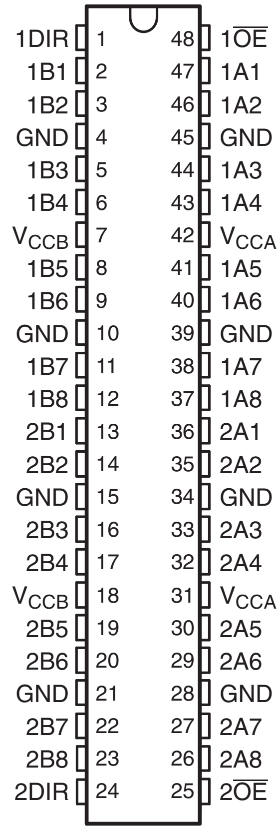
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6 Pin Configuration and Functions

DGV Package
48-Pin TVSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A1	47	I/O	Input and output. Referenced to V_{CCA}
1A2	46		
1A3	44		
1A4	43		
1A5	41		
1A6	40		
1A7	38		
1A8	37		
1B1	2	I/O	Input and output. Referenced to V_{CCB}
1B2	3		
1B3	5		
1B4	6		
1B5	8		
1B6	9		
1B7	11		
1B8	12		

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
2A1	36	I/O	Input and output. Referenced to V_{CCA}
2A2	35		
2A3	33		
2A4	32		
2A5	30		
2A6	29		
2A7	27		
2A8	26		
2B1	13	I/O	Input and output. Referenced to V_{CCB}
2B2	14		
2B3	16		
2B4	17		
2B5	19		
2B6	20		
2B7	22		
2B8	23		
1DIR	1	I	Direction-control signal
2DIR	24		
1$\overline{OE}$	48	—	Tri-State output-mode enables. Pull $\overline{OE}$ high to place all outputs in Tri-State mode. Referenced to V_{CCA}
2$\overline{OE}$	25		
GND	4, 10, 15, 21, 45, 39, 34, 28	—	Ground
V_{CCA}	42, 31	—	A-port supply voltage. 1.2 V ≤ V_{CCB} ≤ 3.6 V
V_{CCB}	7, 18	—	B-port supply voltage. 1.2 V ≤ V_{CCB} ≤ 3.6 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage [2]	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state[2]	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state[2][3]	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA}, V_{CCB}, and GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	
		Machine model (MM), per JEDEC specification JESD22-A115-A	±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1][2][3]

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}, V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs[4]	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs[4]	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})[5]	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})[5]	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(5) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

7.4 Thermal Information

THERMAL METRIC[1]		SN74AVC16T245-Q1 DGV (TVSOP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to 125°C	V_{CCO} – 0.2			V
		I_{OH} = –3 mA		1.2 V	1.2 V	T_A = 25°C		0.95		
		I_{OH} = –6 mA		1.4 V	1.4 V	T_A = –40°C to 125°C	1			
		I_{OH} = –8 mA		1.65 V	1.65 V	T_A = –40°C to 125°C	1.15			
		I_{OH} = –9 mA		2.3 V	2.3 V	T_A = –40°C to 125°C	1.75			
		I_{OH} = –12 mA		3 V	3 V	T_A = –40°C to 125°C	2.3			
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to 125°C			0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V	T_A = 25°C		0.15		
		I_{OL} = 6 mA		1.4 V	1.4 V	T_A = –40°C to 125°C			0.4	
		I_{OL} = 8 mA		1.65 V	1.65 V	T_A = –40°C to 125°C			0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V	T_A = –40°C to 125°C			0.55	
		I_{OL} = 12 mA		3 V	3 V	T_A = –40°C to 125°C			0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = 25°C		±0.025	±0.25	µA
						T_A = –40°C to 125°C			±2	
I_{off}	A or B port	V_I or V_O= 0 to 3.6 V		0 V	0 to 3.6 V	T_A = 25°C		±0.1	±2.5	µA
						T_A = –40°C to 125°C			±10	
	A or B port			0 to 3.6 V	0 V	T_A = 25°C		±0.5	±2.5	
						T_A = –40°C to 125°C			±10	
I_{OZ}(3)	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V	T_A = 25°C		±0.5	±2.5	µA
						T_A = –40°C to 125°C			±10	
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to 125°C			30	µA
				0 V	3.6 V	T_A = –40°C to 125°C			–40	
				3.6 V	0 V	T_A = –40°C to 125°C			30	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to 125°C			30	µA
				0 V	3.6 V	T_A = –40°C to 125°C			30	
				3.6 V	0 V	T_A = –40°C to 125°C			–40	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to 125°C			60	µA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V	T_A = 25°C		3.5		pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V	T_A = 25°C		7		pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

7.6 Switching Characteristics: V_{CCA}= 1.2 V

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V			V_{CCB} = 1.5 V			V_{CCB} = 1.8 V			V_{CCB} = 2.5 V			V_{CCB} = 3.3 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	B		4.1			3.3			3			2.8			3.2		ns
t_{PHL}				4.1			3.3			3			2.8			3.2		
t_{PLH}	B	A		4.4			4			3.8			3.6			3.5		ns
t_{PHL}				4.4			4			3.8			3.6			3.5		
t_{PZH}	$\overline{OE}$	A		6.4			6.4			6.4			6.4			6.4		ns
t_{PZL}				6.4			6.4			6.4			6.4			6.4		
t_{PZH}	$\overline{OE}$	B		6			4.6			4			3.4			3.2		ns
t_{PZL}				6			4.6			4			3.4			3.2		
t_{PHZ}	$\overline{OE}$	A		6.6			6.6			6.6			6.6			6.8		ns
t_{PLZ}				6.6			6.6			6.6			6.6			6.8		
t_{PHZ}	$\overline{OE}$	B		6			4.9			4.9			4.2			5.3		ns
t_{PLZ}				6			4.9			4.9			4.2			5.3		

7.7 Switching Characteristics: V_{CCA}= 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V			V_{CCB} = 1.5 V ± 0.1 V			V_{CCB} = 1.8 V ± 0.15 V			V_{CCB} = 2.5 V ± 0.2 V			V_{CCB} = 3.3 V ± 0.3 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	B		3.6		0.5		9.2	0.5		8.2	0.5		7.1	0.5		6.7	ns
t_{PHL}				3.6		0.5		9.2	0.5		8.2	0.5		7.1	0.5		6.7	
t_{PLH}	B	A		3.3		0.5		9.2	0.5		8.9	0.5		8.6	0.5		8.5	ns
t_{PHL}				3.3		0.5		9.2	0.5		8.9	0.5		8.6	0.5		8.5	
t_{PZH}	$\overline{OE}$	A		4.3		0.5		13.1	0.5		13.1	0.5		13.1	0.5		13.1	ns
t_{PZL}				4.3		0.5		13.1	0.5		13.1	0.5		13.1	0.5		13.1	
t_{PZH}	$\overline{OE}$	B		5.6		0.5		13.1	0.5		11.1	0.5		8.9	0.5		8.2	ns
t_{PZL}				5.6		0.5		13.1	0.5		11.1	0.5		8.9	0.5		8.2	
t_{PHZ}	$\overline{OE}$	A		4.5		0.5		12.1	0.5		12.1	0.5		12.1	0.5		12.1	ns
t_{PLZ}				4.5		0.5		12.1	0.5		12.1	0.5		12.1	0.5		12.1	
t_{PHZ}	$\overline{OE}$	B		5.5		0.5		11.7	0.5		10.5	0.5		9.5	0.5		9.3	ns
t_{PLZ}				5.5		0.5		11.7	0.5		10.5	0.5		9.5	0.5		9.3	

7.8 Switching Characteristics: V_{CCA}= 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V			V_{CCB} = 1.5 V ± 0.1 V			V_{CCB} = 1.8 V ± 0.15 V			V_{CCB} = 2.5 V ± 0.2 V			V_{CCB} = 3.3 V ± 0.3 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	B		3.4		0.5		8.9	0.5		7.8	0.5		6.7	0.5		6.3	ns
t_{PHL}				3.4		0.5		8.9	0.5		7.8	0.5		6.7	0.5		6.3	
t_{PLH}	B	A		3		0.5		8.2	0.5		7.8	0.5		7.5	0.5		7.4	ns
t_{PHL}				3		0.5		8.2	0.5		7.8	0.5		7.5	0.5		7.4	
t_{PZH}	$\overline{OE}$	A		3.4		0.5		10.8	0.5		10.8	0.5		10.8	0.5		10.8	ns
t_{PZL}				3.4		0.5		10.8	0.5		10.8	0.5		10.8	0.5		10.8	
t_{PZH}	$\overline{OE}$	B		5.4		0.5		12.2	0.5		10.4	0.5		8.3	0.5		7.5	ns
t_{PZL}				5.4		0.5		12.2	0.5		10.4	0.5		8.3	0.5		7.5	
t_{PHZ}	$\overline{OE}$	A		4.2		0.5		10.7	0.5		10.7	0.5		10.7	0.5		10.7	ns
t_{PLZ}				4.2		0.5		10.7	0.5		10.7	0.5		10.7	0.5		10.7	
t_{PHZ}	$\overline{OE}$	B		5.2		0.5		11.4	0.5		8.9	0.5		8.9	0.5		8.7	ns
t_{PLZ}				5.2		0.5		11.4	0.5		8.9	0.5		8.9	0.5		8.7	

7.9 Switching Characteristics: V_{CCA}= 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V			V_{CCB} = 1.5 V ± 0.1 V			V_{CCB} = 1.8 V ± 0.15 V			V_{CCB} = 2.5 V ± 0.2 V			V_{CCB} = 3.3 V ± 0.3 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	B		3.2		0.5		9.6	0.5		7.5	0.5		6.3	0.5		5.8	ns
t_{PHL}				3.2		0.5		8.6	0.5		7.5	0.5		6.3	0.5		5.8	
t_{PLH}	B	A		2.6		0.5		7.1	0.5		6.7	0.5		6.3	0.5		6.2	ns
t_{PHL}				2.6		0.5		7.1	0.5		6.7	0.5		6.3	0.5		6.2	
t_{PZH}	$\overline{OE}$	A		2.5		0.5		8.3	0.5		8.3	0.5		8.3	0.5		8.3	ns
t_{PZL}				2.5		0.5		8.3	0.5		8.3	0.5		8.3	0.5		8.3	
t_{PZH}	$\overline{OE}$	B		5.2		0.5		12.4	0.5		10.3	0.5		8.1	0.5		7.5	ns
t_{PZL}				5.2		0.5		12.4	0.5		10.3	0.5		8.1	0.5		7.5	
t_{PHZ}	$\overline{OE}$	A		3		0.5		9.1	0.5		9.1	0.5		9.1	0.5		9.1	ns
t_{PLZ}				3		0.5		9.1	0.5		9.1	0.5		9.1	0.5		9.1	
t_{PHZ}	$\overline{OE}$	B		5		0.5		10.9	0.5		9.6	0.5		9.1	0.5		8.2	ns
t_{PLZ}				5		0.5		10.9	0.5		9.6	0.5		9.1	0.5		8.2	

7.10 Switching Characteristics: V_{CCA}= 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V			V_{CCB} = 1.5 V ± 0.1 V			V_{CCB} = 1.8 V ± 0.15 V			V_{CCB} = 2.5 V ± 0.2 V			V_{CCB} = 3.3 V ± 0.3 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	B		3.2		0.5		8.5	0.5		7.4	0.5		6.2	0.5		5.7	ns
t_{PHL}				3.2		0.5		8.5	0.5		7.4	0.5		6.2	0.5		5.7	
t_{PLH}	B	A		2.8		0.5		6.7	0.5		6.3	0.5		5.8	0.5		5.7	ns
t_{PHL}				2.8		0.5		6.7	0.5		6.3	0.5		5.8	0.5		5.7	
t_{PZH}	$\overline{OE}$	A		2.2		0.5		7.3	0.5		7.2	0.5		7.1	0.5		7	ns
t_{PZL}				2.2		0.5		7.3	0.5		7.2	0.5		7.1	0.5		7	
t_{PZH}	$\overline{OE}$	B		5.1		0.5		12.3	0.5		10.2	0.5		7.9	0.5		7	ns
t_{PZL}				5.1		0.5		12.3	0.5		10.2	0.5		7.9	0.5		7	
t_{PHZ}	$\overline{OE}$	A		3.4		0.5		8	0.5		8	0.5		8	0.5		8	ns
t_{PLZ}				3.4		0.5		8	0.5		8	0.5		8	0.5		8	
t_{PHZ}	$\overline{OE}$	B		4.9		0.5		10.7	0.5		9.5	0.5		8.2	0.5		8	ns
t_{PLZ}				4.9		0.5		10.7	0.5		9.5	0.5		8.2	0.5		8	

7.11 Operating Characteristics

T_A= 25°C

PARAMETER			TEST CONDITIONS	V_{CCA} = V_{CCB}= 1.2 V			V_{CCA} = V_{CCB}= 1.5 V			V_{CCA} = V_{CCB}= 1.8 V			V_{CCA} = V_{CCB}= 2.5 V			V_{CCA} = V_{CCB}= 3.3 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
C_{pdA} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns		1			1			1			1			2		pF
		Outputs disabled			1			1			1			1			1		
	B to A	Outputs enabled			13			13			14			15			16		
		Outputs disabled			1			1			1			1			1		
C_{pdB} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns		13			13			14			15			16		pF
		Outputs disabled			1			1			1			1			1		
	B to A	Outputs enabled			1			1			1			1			2		
		Outputs disabled			1			1			1			1			1		

(1) Power dissipation capacitance per transceiver

7.12 Typical Characteristics

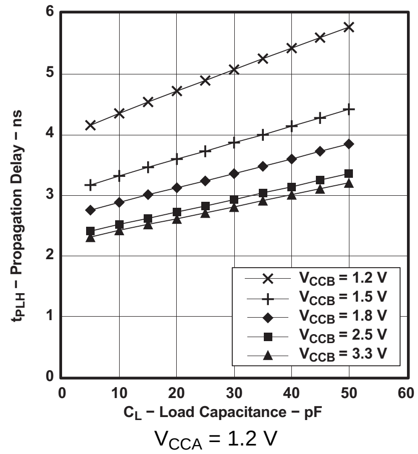


Figure 1. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

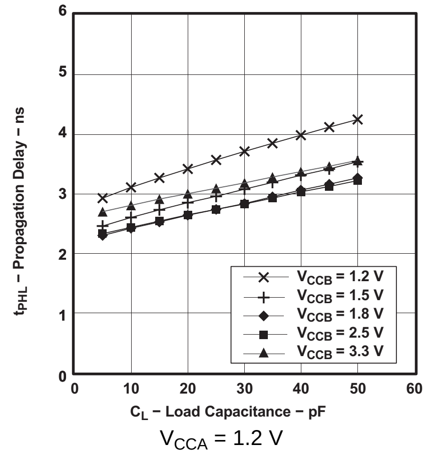


Figure 2. Typical Propagation Delay t_{PHL} (A to B) vs Load Capacitance

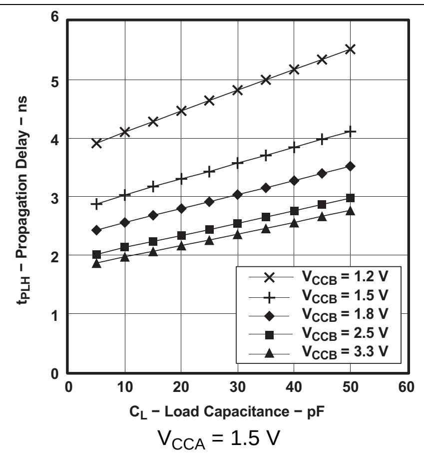


Figure 3. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

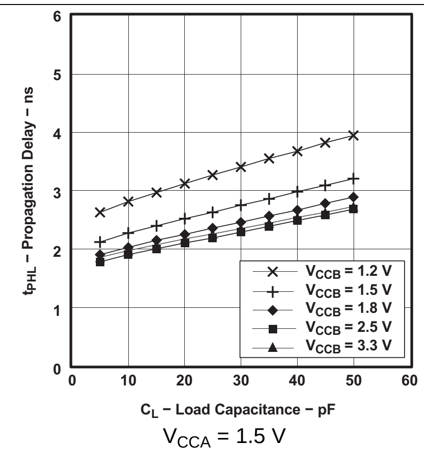


Figure 4. Typical Propagation Delay t_{PHL} (A to B) vs Load Capacitance

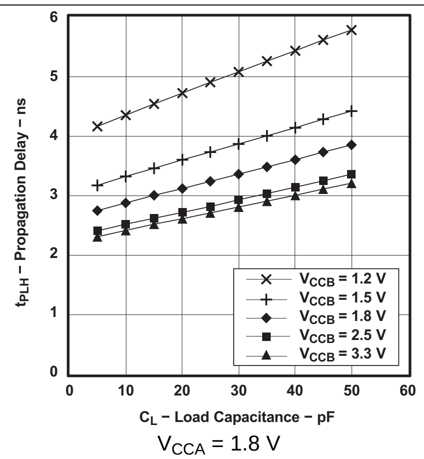


Figure 5. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

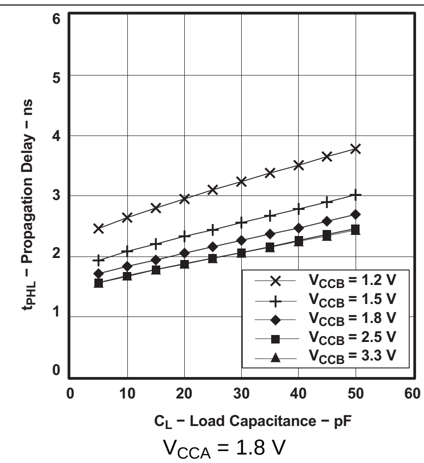


Figure 6. Typical Propagation Delay t_{PHL} (A to B) vs Load Capacitance

Typical Characteristics (continued)

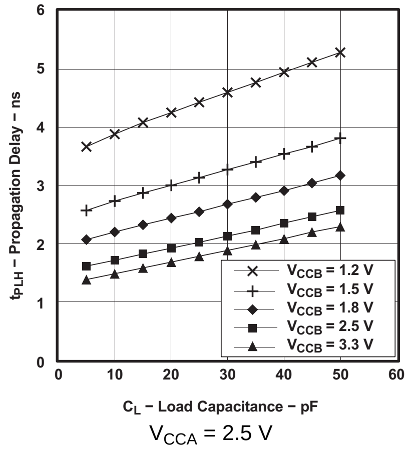


Figure 7. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

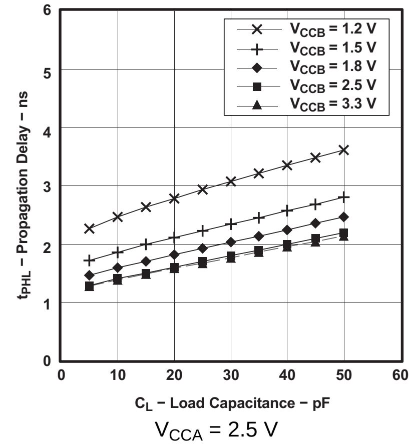


Figure 8. Typical Propagation Delay t_{PHL} (A to B) vs Load Capacitance

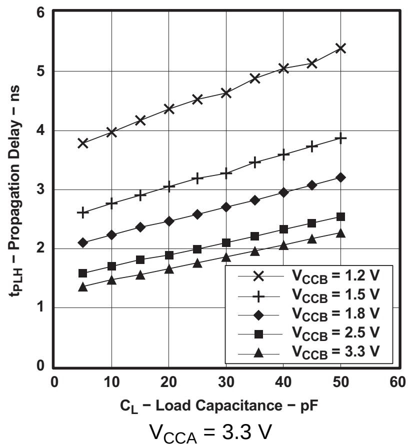


Figure 9. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

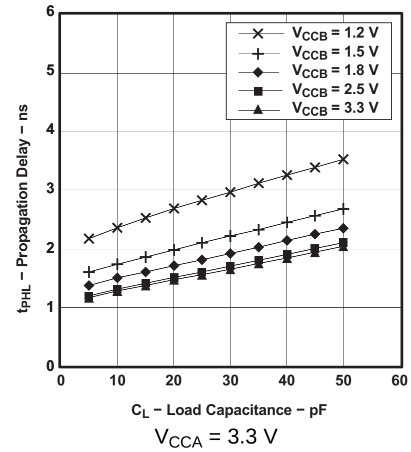
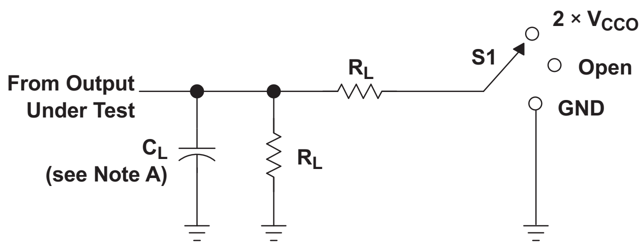


Figure 10. Typical Propagation Delay t_{PHL} (A to B) vs Load Capacitance

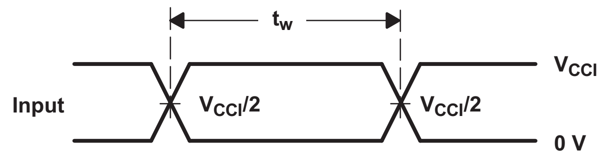
8 Parameter Measurement Information



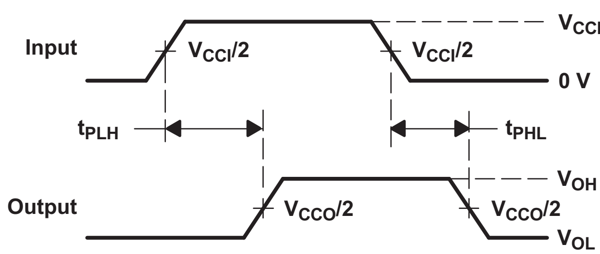
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

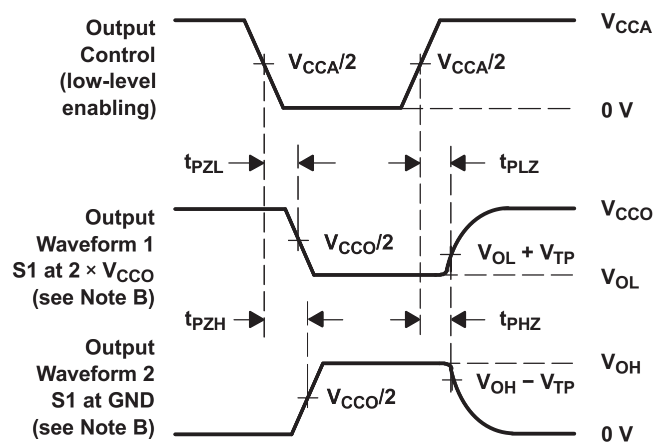
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 11. Load Circuit and Voltage Waveforms

9 Detailed Description

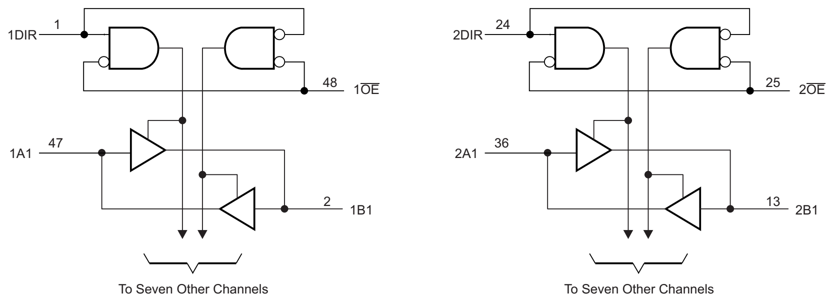
9.1 Overview

The SN74AVC16T245-Q1 is a 16-bit, dual-supply, noninverting, bidirectional voltage level translation. Pins A and control pins (DIR and OE) are supported by V_{CCA} and B pins are supported by V_{CCB}. The A port can accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when OE is set to low. When OE is set to high, both A and B are in the high-impedance state.

This device is fully specified for partial-power-down applications using off output current (I_{off}).

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are put in a high-impedance state.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 1.2 V to 3.6 V, making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

9.3.2 Partial-Power-Down Mode Operation

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry prevents backflow current by disabling I/O output circuits when device is in partial power-down mode.

9.3.3 V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND, both ports are in a high-impedance state (I_{OZ} shown in *Electrical Characteristics*). This prevents false logic levels from being presented to either bus.

9.4 Device Functional Modes

The SN74AVC16T245-Q1 is a voltage level translator that can operate from 1.2 V to 3.6 V (V_{CCA}) and 1.2 V to 3.6 V (V_{CCB}). The signal translation between 1.2 V and 3.6 V requires direction control and output enable control. When OE is low and DIR is high, data transmission is from A to B. When OE is low and DIR is low, data transmission is from B to A. When OE is high, both output ports will be high-impedance. Table 1 lists the functions.

Table 1. Function Table (Each 16-Bit Section)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AVC16T245-Q1 device can be used in level-shifting applications for interfacing devices and addressing mixed voltage incompatibility. The SN74AVC16T245-Q1 device is ideal for data transmission where direction is different for each channel.

10.1.1 Enable Times

Calculate the enable times for the SN74AVC16T45 using the following formulas:

$$t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)} \quad (1)$$

$$t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)} \quad (2)$$

$$t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)} \quad (3)$$

$$t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)} \quad (4)$$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC16T245-Q1 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

10.2 Typical Application

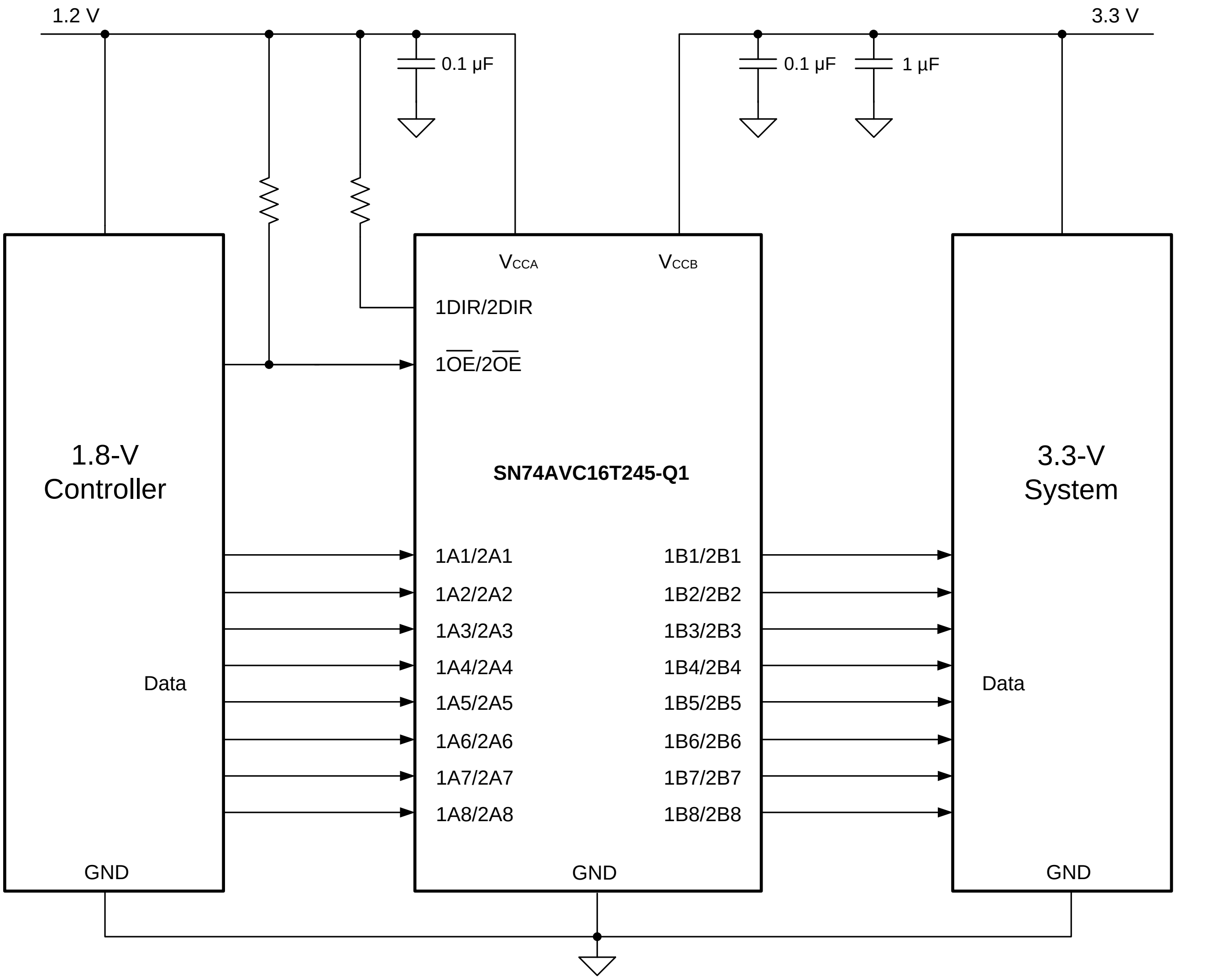


Figure 12. Typical Application Schematic

10.2.1 Design Requirements

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Tie any unused input and output ports directly to ground.

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V
Output voltage range	3.3 V

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  – Use the supply voltage of the device that is driving the SN74AVC16T245-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  – Use the supply voltage of the device that the SN74AVC16T245-Q1 device is driving to determine the output voltage range.

10.2.3 Application Curve

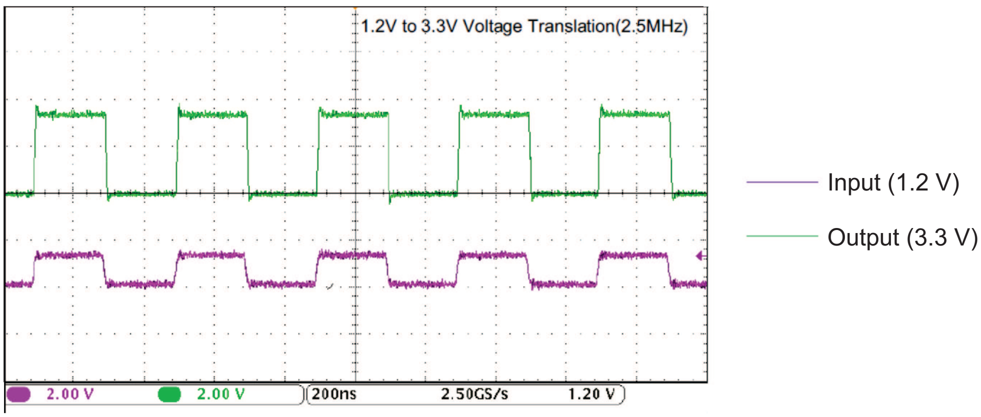


Figure 13. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

11 Power Supply Recommendations

The SN74AVC16T245-Q1 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V and V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB}, respectively, allowing for low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The output-enable $\overline{OE}$ input circuit is designed so that it is supplied by V_{CCA} and when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

12 Layout

12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended:

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

12.2 Layout Example

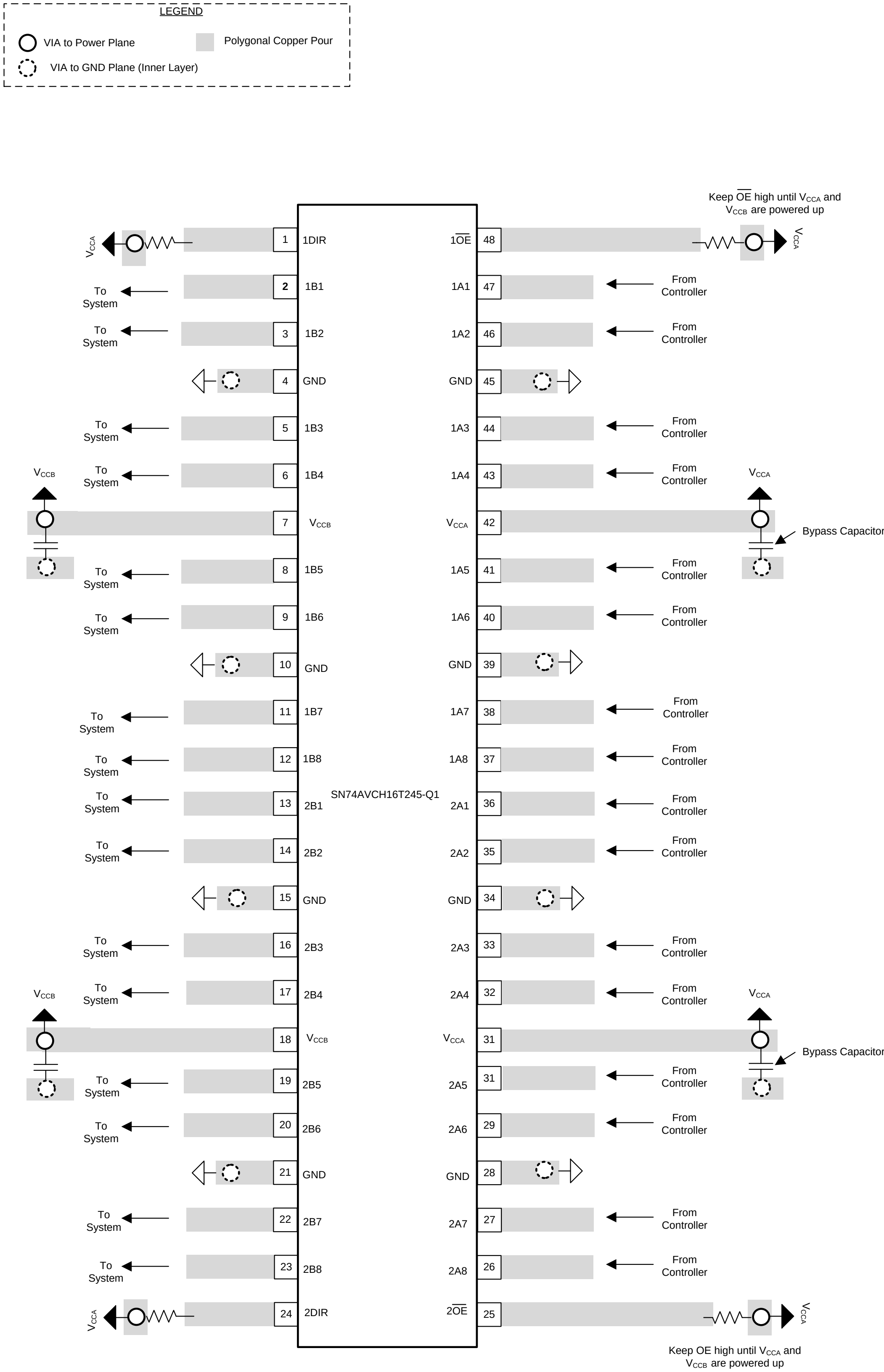


Figure 14. Recommended Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *CMOS Power Consumption and Cpd Calculation*
- *IC Package Thermal Metrics application report*
- *Implications of Slow or Floating CMOS Inputs*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAVC16T245QDGVRQ1	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WF245Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AVC16T245-Q1 :

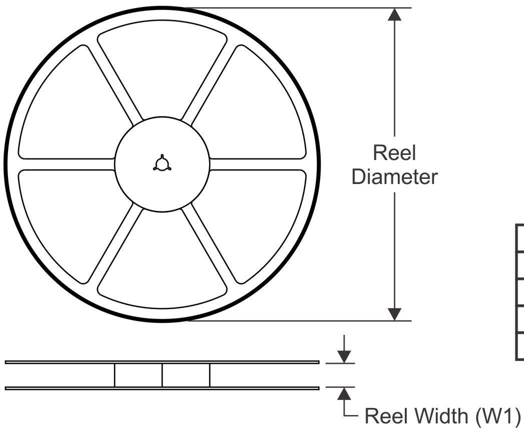
- Catalog: SN74AVC16T245

NOTE: Qualified Version Definitions:

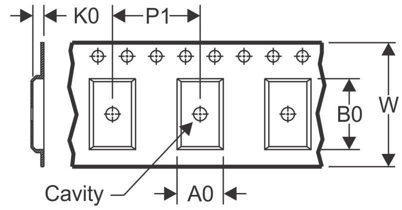
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

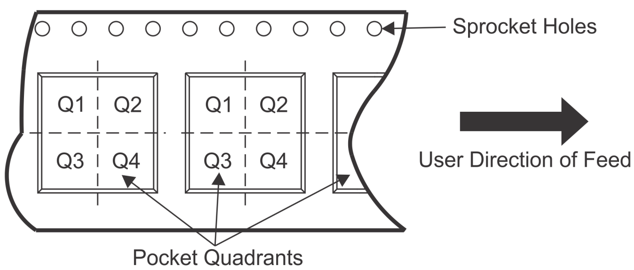


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

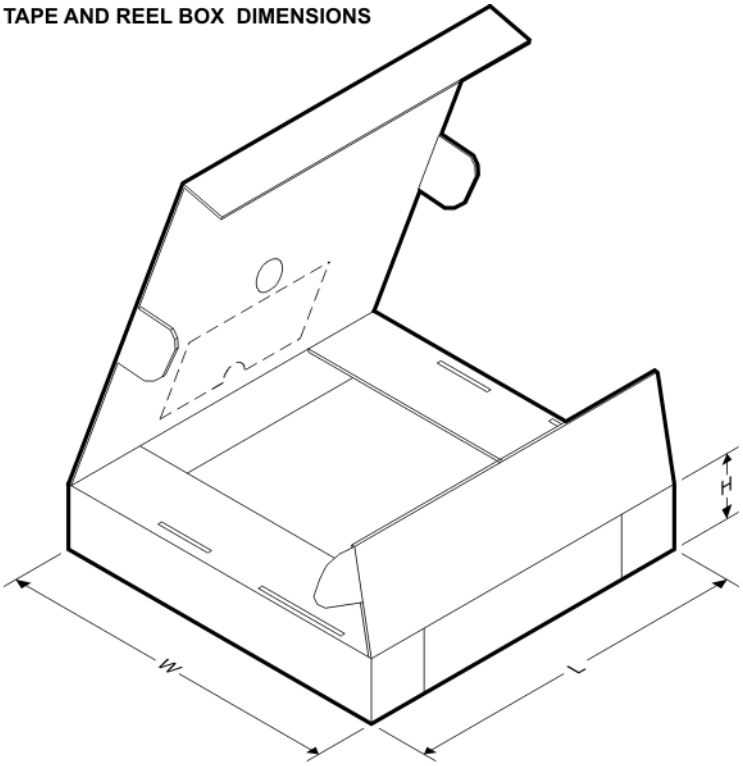
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAVC16T245QDGVRQ1	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

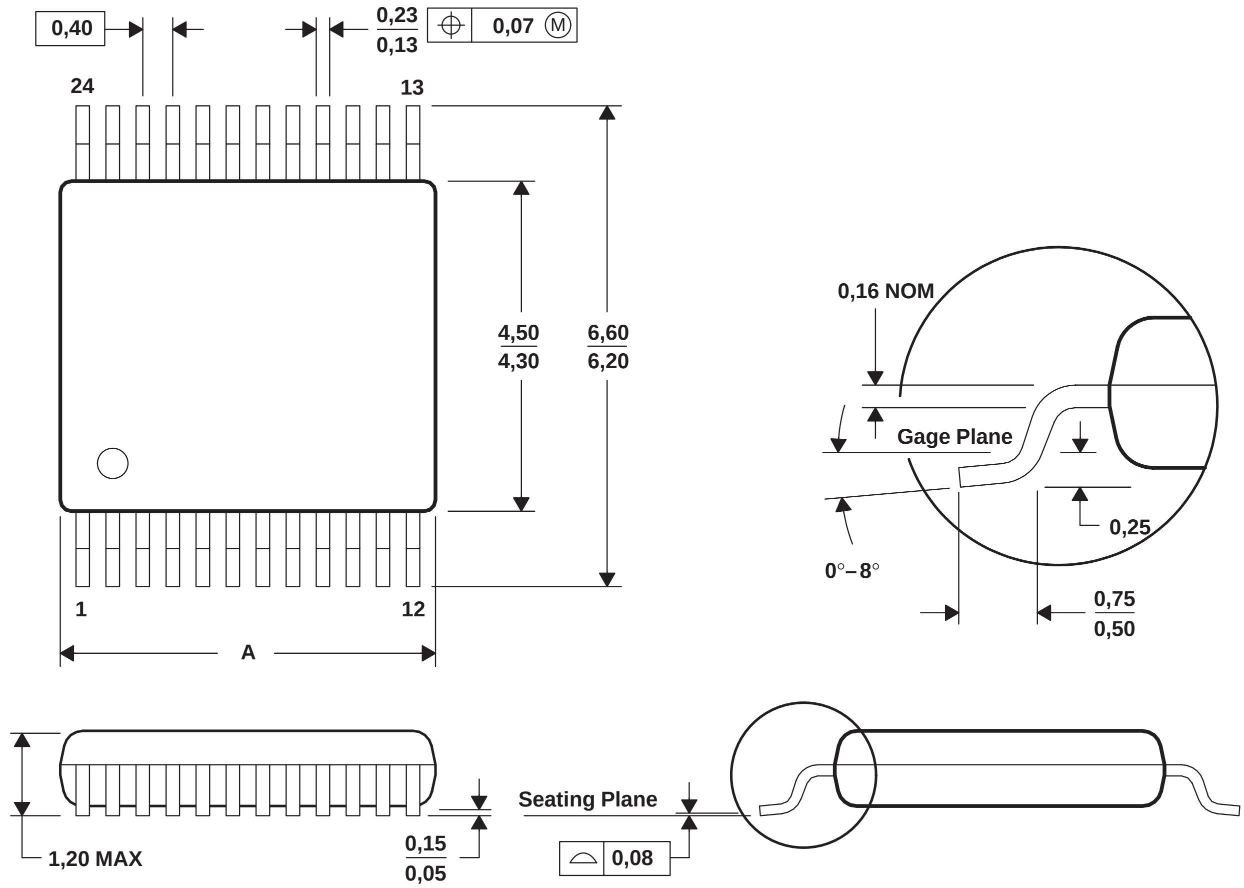


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAVC16T245QDGVRQ1	TVSOP	DGV	48	2000	367.0	367.0	38.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

IMPORTANT NOTICE AND DISCLAIMER