Burr-Brown Products
from Texas Instruments

OPA234
OPA2234
OPA4234

SBOS055B – MAY 1996 – REVISED APRIL 2008

Low-Power, Precision SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

FEATURES

- **WIDE SUPPLY RANGE:**
  Single Supply: V_S = +2.7V to +36V
  Dual Supply: V_S = ±1.35V to ±18V
- **SPECIFIED PERFORMANCE:**
  +2.7V, +5V, and ±15V
- **LOW QUIESCENT CURRENT: 250μA/amp**
- **LOW INPUT BIAS CURRENT: 25nA max**
- **LOW OFFSET VOLTAGE: 100μV max**
- **HIGH CMRR, PSRR, and A_{OL}**
- **SINGLE, DUAL, and QUAD VERSIONS**

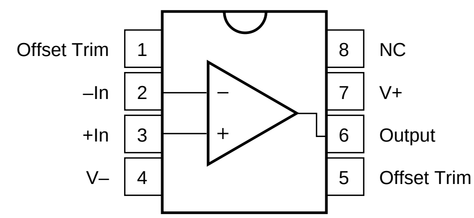
DESCRIPTION

The OPA234 series low-cost op amps are ideal for single-supply, low-voltage, low-power applications. The series provides lower quiescent current than older "1013"-type products and comes in current industry-standard packages and pinouts. The combination of low offset voltage, high common-mode rejection, high power-supply rejection, and a wide supply range provides excellent accuracy and versatility. Single, dual, and quad versions have identical specifications for maximum design flexibility. These general-purpose op amps are ideal for portable and battery-powered applications.

The OPA234 series op amps operate from either single or dual supplies. In single-supply operation, the input common-mode range extends below ground and the output can swing to within 50mV of ground. Excellent phase margin makes the OPA234 series ideal for demanding applications, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

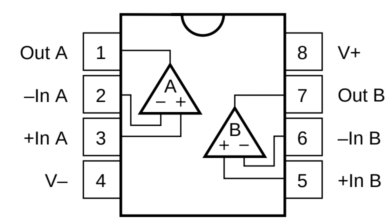
Single version packages are in an SO-8 surface-mount and a space-saving MSOP-8 surface-mount. Dual packages are in an SO-8 surface-mount. Quad packages are in an SO-14 surface-mount. All are specified for –40°C to +85°C operation.

OPA234



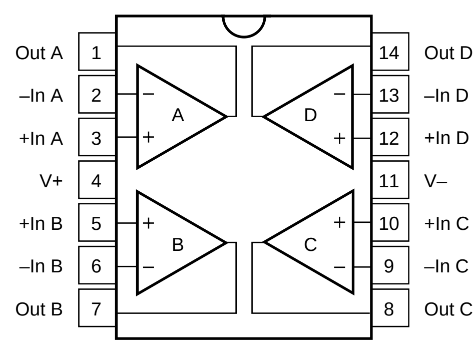
SO-8, MSOP-8

OPA2234



SO-8

OPA4234



SO-14

ELECTRICAL CHARACTERISTICS: V_S = +5V

At T_A = 25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER		CONDITION	OPA234U, E OPA2234U MIN	TYP	MAX	OPA234UA, EA OPA2234UA OPA4234UA, U MIN	TYP	MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{OS}	V_{CM} = 2.5V		±40	±100		*	±250	µV
OPA234E, EA				±100	±150		*	±350	µV
vs Temperature(1)	dV_{OS}/dT	Operating Temperature Range		±0.5	±3		*	*	µV/°C
vs Power Supply	PSRR	V_S = +2.7V to +30V, V_{CM} = 1.7V		3	10		*	20	µV/V
vs Time				0.2			*		µV/mo
Channel Separation (Dual, Quad)				0.3			*		µV/V
INPUT BIAS CURRENT									
Input Bias Current(2)	I_B	V_{CM} = 2.5V		–15	–30		*	–50	nA
Input Offset Current	I_{OS}	V_{CM} = 2.5V		±1	±5		*	*	nA
NOISE		f = 1kHz							
Input Voltage Noise Density	v_n			25			*		$nV/\sqrt{Hz}$
Current Noise Density	i_n			80			*		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range			–0.1		(V+) –1	*		*	V
Common-Mode Rejection	CMRR	V_{CM} = –0.1V to 4V	91	106		86	*		dB
INPUT IMPEDANCE									
Differential				10^7 || 5			*		Ω || pF
Common-Mode		V_{CM} = 2.5V		10^{10} || 6			*		Ω || pF
OPEN-LOOP GAIN		V_O = 0.25V to 4V							
Open-Loop Voltage Gain	A_{OL}	R_L = 10kΩ	108	120		100	*		dB
		R_L = 2kΩ	86	96		*	*		dB
FREQUENCY RESPONSE									
Gain-Bandwidth Product	GBW	C_L = 100pF		0.35			*		MHz
Slew Rate	SR			0.2			*		V/µs
Settling Time: 0.1%		G = 1, 3V Step, C_L = 100pF		15			*		µs
0.01%		G = 1, 3V Step, C_L = 100pF		25			*		µs
Overload Recovery Time		(V_{IN}) (Gain) = V_S		16			*		µs
OUTPUT									
Voltage Output: Positive		R_L = 10kΩ to $V_S/2$	(V+) –1	(V+) –0.65		*	*		V
Negative		R_L = 10kΩ to $V_S/2$	0.25	0.05		*	*		V
Positive		R_L = 10kΩ to Ground	(V+) –1	(V+) –0.65		*	*		V
Negative		R_L = 10kΩ to Ground	0.1	0.05		*	*		V
Short-Circuit Current	I_{SC}			±11			*		mA
Capacitive Load Drive (Stable Operation)(3)		G = +1		1000			*		pF
POWER SUPPLY									
Specified Operating Voltage				+5			*		V
Operating Voltage Range			+2.7		+36	*		*	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		250	300		*	*	µA
TEMPERATURE RANGE									
Specified Range			–40		+85	*		*	°C
Operating Range			–40		+125	*		*	°C
Storage			–55		+125	*		*	°C
Thermal Resistance	θ_{JA}								
8-Pin DIP				100			*		°C/W
SO-8 Surface-Mount				150			*		°C/W
MSOP-8 Surface-Mount				220			*		°C/W
14-Pin DIP				80			*		°C/W
SO-14 Surface-Mount				110			*		°C/W

* Specifications same as OPA234U, E.

NOTES: (1) Wafer-level tested to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.

ELECTRICAL CHARACTERISTICS: V_S = +2.7V

At T_A = 25°C, V_S = +2.7V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER	CONDITION	OPA234U, E OPA2234U MIN	TYP	MAX	OPA234UA, EA OPA2234UA OPA4234UA, U MIN	TYP	MAX	UNITS
OFFSET VOLTAGE								
Input Offset Voltage V_{OS}	V_{CM} = 1.35V		±40	±100		∗	±250	µV
OPA234E, EA			±100	±150		∗	±350	µV
vs Temperature(1) dV_{OS}/dT	Operating Temperature Range		±0.5	±3		∗	∗	µV/°C
vs Power Supply PSRR	V_S = +2.7V to +30V, V_{CM} = 1.7V		3	10		∗	20	µV/V
vs Time			0.2			∗		µV/mo
Channel Separation (Dual, Quad)			0.3			∗		µV/V
INPUT BIAS CURRENT								
Input Bias Current(2) I_B	V_{CM} = 1.35V		–15	–30		∗	–50	nA
Input Offset Current I_{OS}	V_{CM} = 1.35V		±1	±5		∗	∗	n
NOISE	f = 1kHz							
Input Voltage Noise Density v_n			25			∗		nV/√Hz
Current Noise Density i_n			80			∗		fA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range		–0.1		(V+) –1	∗		∗	V
Common-Mode Rejection CMRR	V_{CM} = –0.1V to 1.7V	91	106		86	∗		dB
INPUT IMPEDANCE								
Differential			10^7 ǁ 5			∗		Ω ǁ pF
Common-Mode	V_{CM} = 1.35V		10^{10} ǁ 6			∗		Ω ǁ pF
OPEN-LOOP GAIN	V_O = 0.25V to 1.7V							
Open-Loop Voltage Gain A_{OL}	R_L = 10kΩ	108	125		100	∗		dB
	R_L = 2kΩ	86	96		86	∗		dB
FREQUENCY RESPONSE								
Gain-Bandwidth Product GBW	C_L = 100pF		0.35			∗		MHz
Slew Rate SR			0.2			∗		V/µs
Settling Time: 0.1%	G = 1, 1V Step, C_L = 100pF		6			∗		µs
0.01%	G = 1, 1V Step, C_L = 100pF		16			∗		µs
Overload Recovery Time	(V_{IN}) (Gain) = V_S		8			∗		µs
OUTPUT								
Voltage Output: Positive	R_L = 10kΩ to V_S/2	(V+) –1	(V+) –0.6		∗	∗		V
Negative	R_L = 10kΩ to V_S/2	0.25	0.05		∗	∗		V
Positive	R_L = 10kΩ to Ground	(V+) –1	(V+) –0.65		∗	∗		V
Negative	R_L = 10kΩ to Ground	0.1	0.05		∗	∗		V
Short-Circuit Current I_{SC}			±8			∗		mA
Capacitive Load Drive (Stable Operation)(3)	G = +1		1000			∗		pF
POWER SUPPLY								
Specified Operating Voltage			+2.7			∗		V
Operating Voltage Range		+2.7		+36	∗		∗	V
Quiescent Current (per amplifier) I_Q	I_O = 0		250	300		∗	∗	µA
TEMPERATURE RANGE								
Specified Range		–40		+85	∗		∗	°C
Operating Range		–40		+125	∗		∗	°C
Storage		–55		+125	∗		∗	°C
Thermal Resistance θ_{JA}								
8-Pin DIP			100			∗		°C/W
SO-8 Surface-Mount			150			∗		°C/W
MSOP-8 Surface-Mount			220			∗		°C/W
14-Pin DIP			80			∗		°C/W
SO-14 Surface-Mount			110			∗		°C/W

∗ Specifications same as OPA234U, E.

NOTES: (1) Wafer-level tested to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.

ELECTRICAL CHARACTERISTICS: V_S = ±15V

At T_A = 25°C, V_S = ±15V, and R_L = 10kΩ connected to ground, unless otherwise noted.

PARAMETER	CONDITION	OPA234U, E OPA2234U MIN	TYP	MAX	OPA234UA, EA OPA2234UA OPA4234UA, U MIN	TYP	MAX	UNITS
OFFSET VOLTAGE								
Input Offset Voltage V_{OS}	V_{CM} = 0V		±70	±250		*	±500	µV
OPA4234U Model						±70	±250	µV
vs Temperature(1) dV_{OS}/dT	Operating Temperature Range		±0.5	±5		*	*	µV/°C
vs Power Supply PSRR	V_S = ±1.35V to ±18V, V_{CM} = 0V		3	10		*	20	µV/V
vs Time			0.2			*		µV/mo
Channel Separation (Dual, Quad)			0.3			*		µV/V
INPUT BIAS CURRENT								
Input Bias Current(2) I_B	V_{CM} = 0V		–12	–25		*	–50	nA
Input Offset Current I_{OS}	V_{CM} = 0V		±1	±5		*	*	nA
NOISE	f = 1kHz							
Input Voltage Noise Density v_n			25			*		nV/√Hz
Current Noise Density i_n			80			*		fA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range		(V–)		(V+) –1	*		*	V
Common-Mode Rejection CMRR	V_{CM} = –15V to 14V	91	106		86	*		dB
INPUT IMPEDANCE								
Differential			$10^7 \parallel 5$			*		Ω ∥ pF
Common-Mode	V_{CM} = 0V		$10^{10} \parallel 6$			*		Ω ∥ pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain A_{OL}	V_O = –14.5V to 14V	110	120		100	*		dB
FREQUENCY RESPONSE								
Gain-Bandwidth Product GBW	C_L = 100pF		0.35			*		MHz
Slew Rate SR			0.2			*		V/µs
Settling Time: 0.1%	G = 1, 10V Step, C_L = 100pF		41			*		µs
0.01%	G = 1, 10V Step, C_L = 100pF		47			*		µs
Overload Recovery Time	(V_{IN}) (Gain) = V_S		22			*		µs
OUTPUT								
Voltage Output: Positive		(V+) –1	(V+) –0.7		*	*		V
Negative		(V–) +0.5	(V–) +0.15		*	*		V
Short-Circuit Current I_{SC}			±22			*		mA
Capacitive Load Drive (Stable Operation)(3)	G = +1		1000			*		pF
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±1.35		±18	*		*	V
Quiescent Current (per amplifier) I_Q	I_O = 0		±275	±350		*	*	µA
TEMPERATURE RANGE								
Specified Range		–40		+85	*		*	°C
Operating Range		–40		+125	*		*	°C
Storage		–55		+125	*		*	°C
Thermal Resistance θ_{JA}								
8-Pin DIP			100			*		°C/W
SO-8 Surface-Mount			150			*		°C/W
MSOP-8 Surface-Mount			220			*		°C/W
14-Pin DIP			80			*		°C/W
SO-14 Surface-Mount			110			*		°C/W

* Specifications same as OPA234U, E.

NOTES: (1) Wafer-level tested to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE MARKING
Single		
OPA234EA	MSOP-8 Surface-Mount	A34
OPA234E	"	"
OPA234UA	SO-8 Surface-Mount	OPA234UA
OPA234U	"	OPA234U
Dual		
OPA2234UA	SO-8 Surface-Mount	OPA2234UA
OPA2234U	"	OPA2234U
Quad		
OPA4234UA	SO-8 Surface-Mount	OPA4234UA
OPA4234U	"	OPA4234U

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

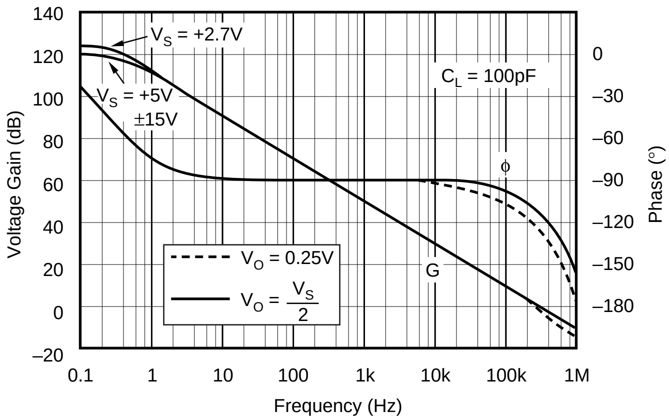
Supply Voltage, V+ to V–	36V
Input Voltage	(V–) –0.7V to (V+) +0.7V
Output Short-Circuit(1)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Short-circuit to ground, one amplifier per package.

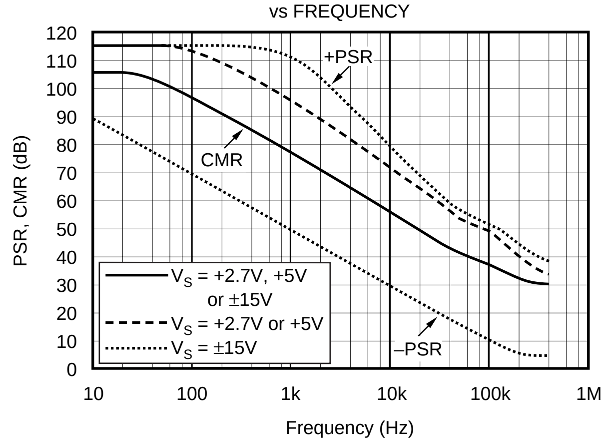
TYPICAL CHARACTERISTIC CURVES

At $T_A = +25°C$ and $R_L = 10k\Omega$, unless otherwise noted.

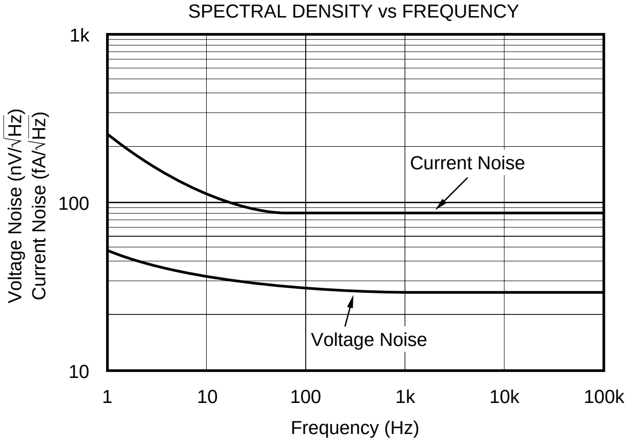
OPEN-LOOP GAIN/PHASE vs FREQUENCY



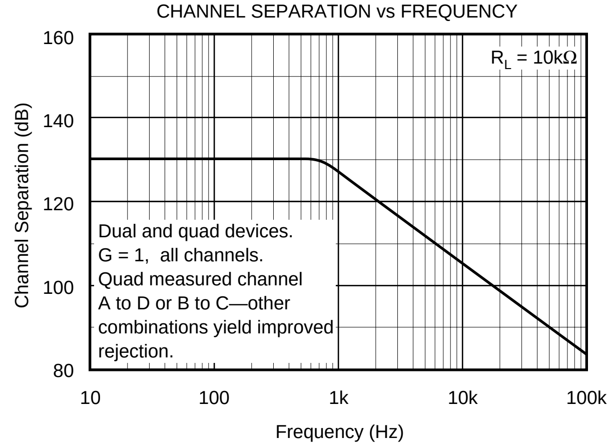
POWER-SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



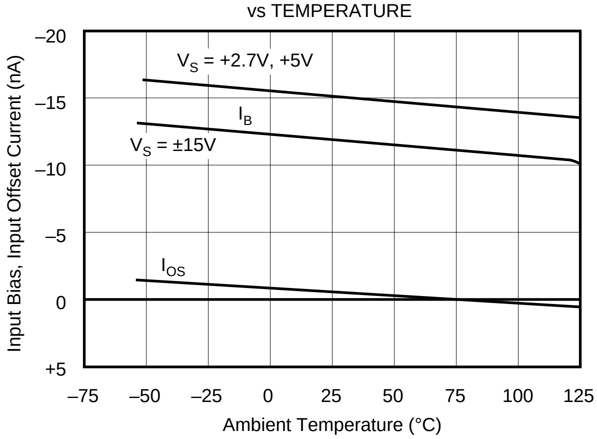
INPUT NOISE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



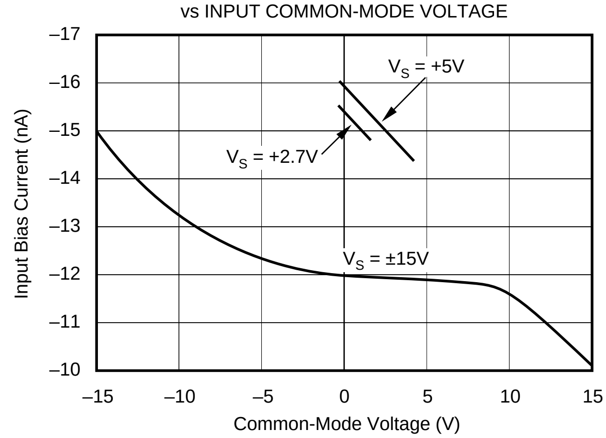
CHANNEL SEPARATION vs FREQUENCY



INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE

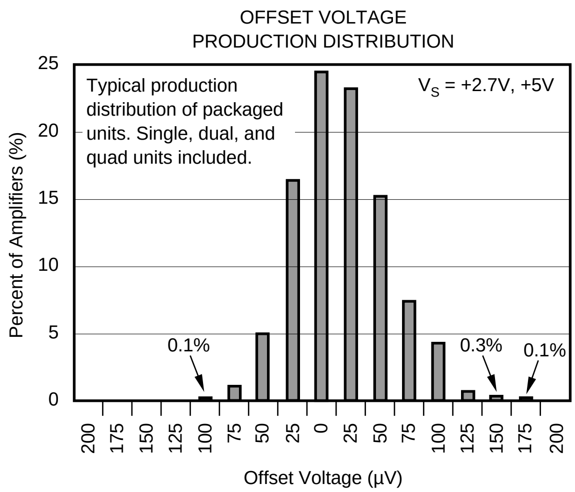


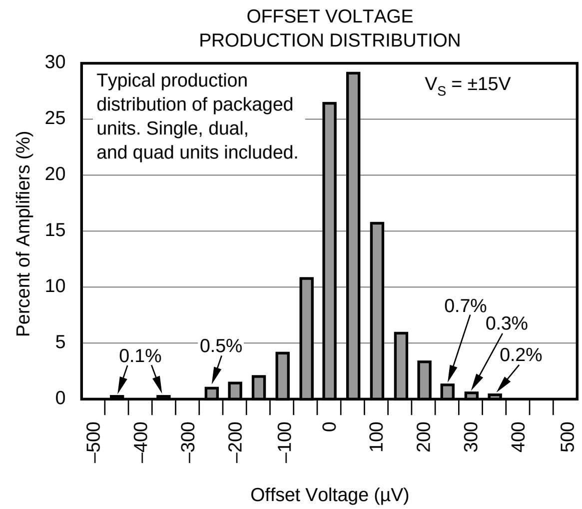
INPUT BIAS CURRENT vs INPUT COMMON-MODE VOLTAGE

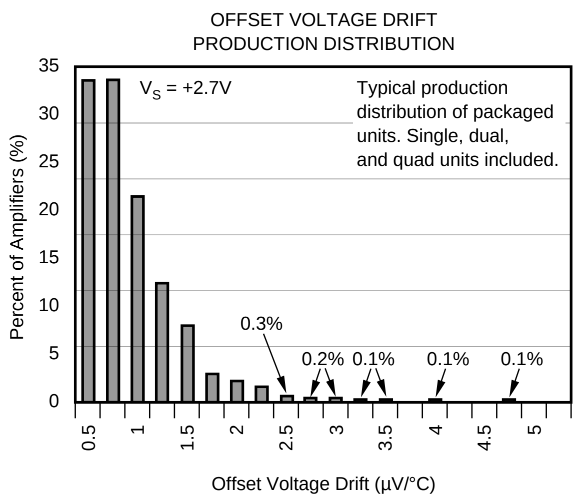


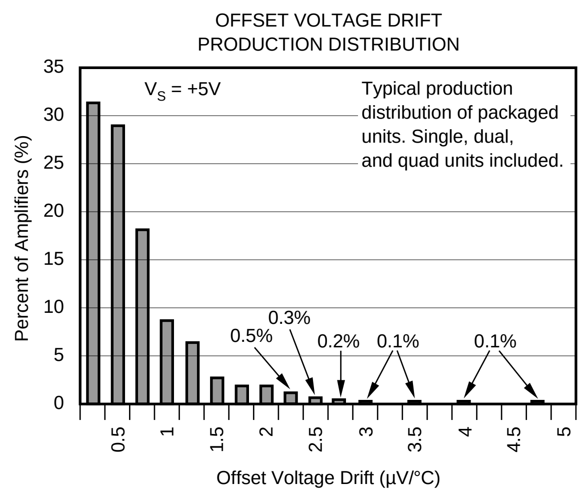
TYPICAL CHARACTERISTIC CURVES (Cont.)

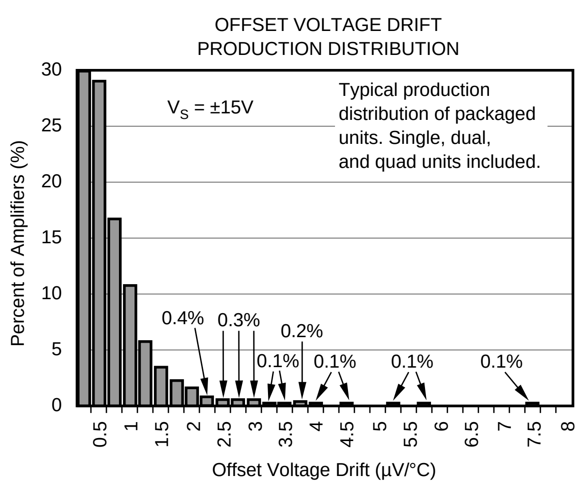
At T_A = +25°C and R_L = 10kΩ, unless otherwise noted.

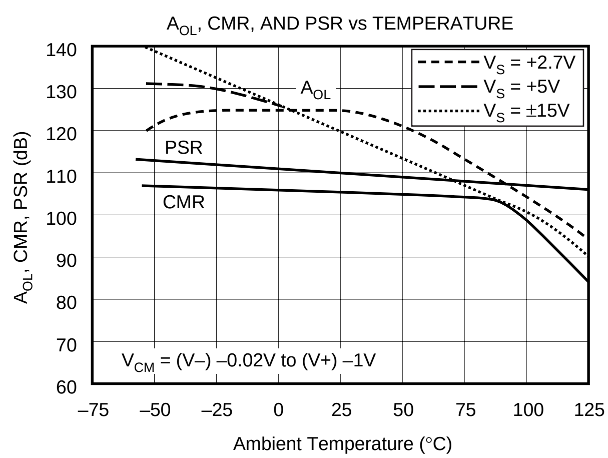








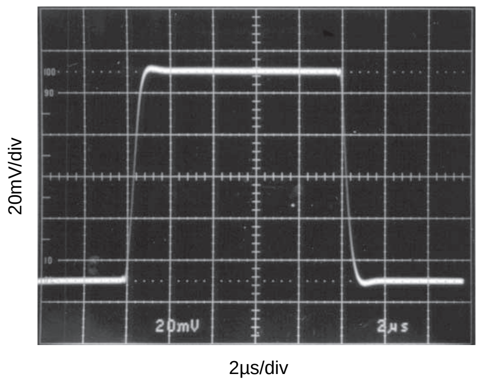




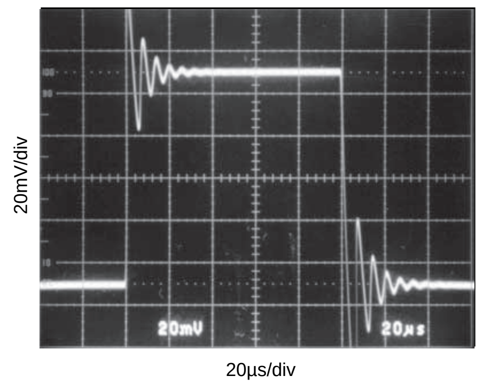
TYPICAL CHARACTERISTIC CURVES (Cont.)

At T_A = +25°C and R_L = 10kΩ, unless otherwise noted.

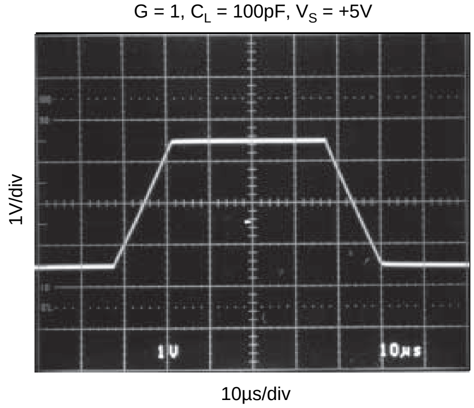
SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 100pF, V_S = +5V



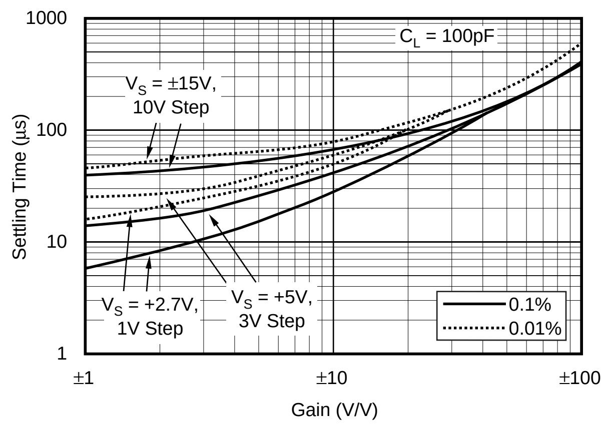
SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 10,000pF, V_S = +5V



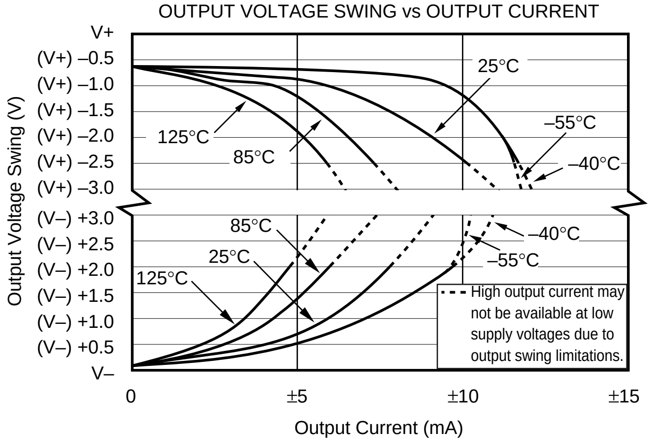
LARGE-SIGNAL STEP RESPONSE
G = 1, C_L = 100pF, V_S = +5V



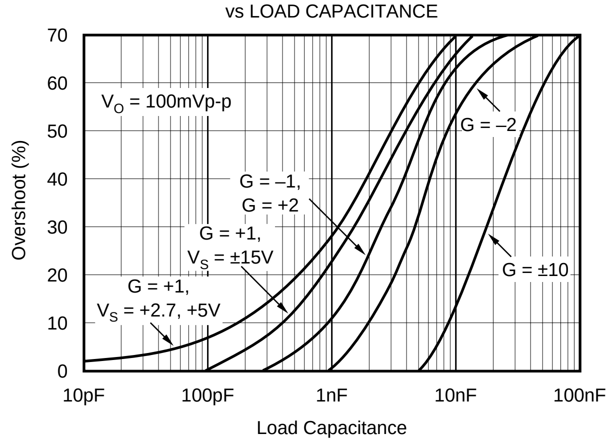
SETTLING TIME vs CLOSED-LOOP GAIN



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

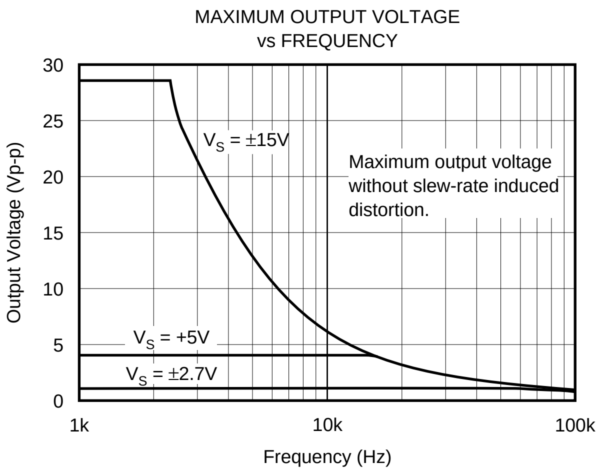


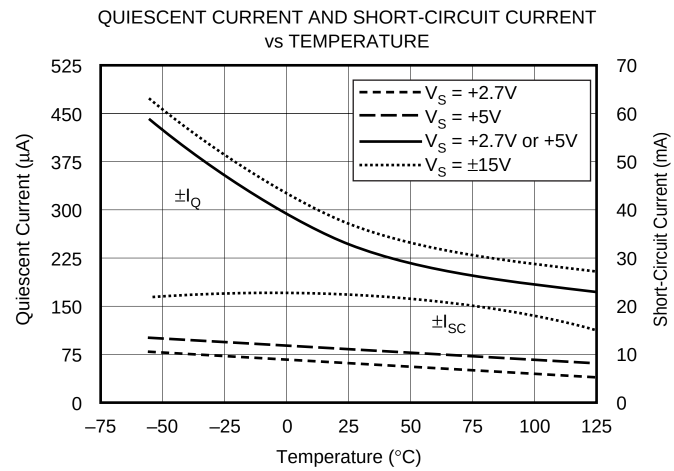
SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



TYPICAL CHARACTERISTIC CURVES (Cont.)

At T_A = +25°C and R_L = 10kΩ, unless otherwise noted.





APPLICATIONS INFORMATION

The OPA234 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 10nF ceramic capacitors.

OPERATING VOLTAGE

The OPA234 series op amps operate from single (+2.7V to +36V) or dual (±1.35V to ±18V) supplies with excellent performance. Specifications are production tested with +2.7V, +5V, and ±15V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Characterisitc curves.

OFFSET VOLTAGE TRIM

Offset voltage of the OPA234 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA234 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer, as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

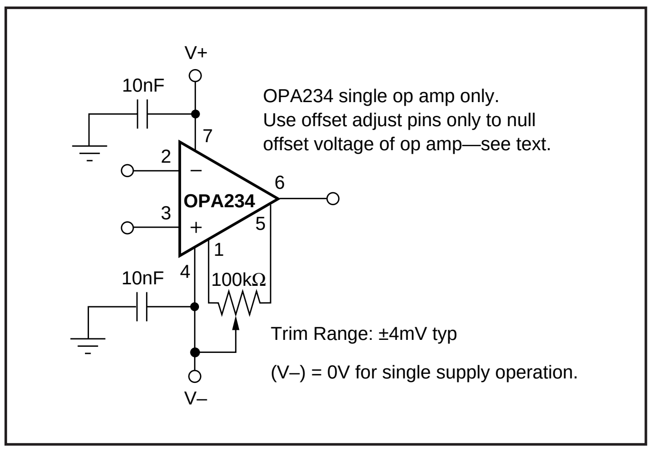


FIGURE 1. OPA234 Offset Voltage Trim Circuit.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2234U	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U	
OPA2234U/2K5	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U	
OPA2234UA	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U A	
OPA2234UA/2K5	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U A	
OPA2234UA/2K5G4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U A	
OPA2234UG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 2234U	
OPA234E/250	NRND	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 125	A34	
OPA234E/250G4	NRND	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 125	A34	
OPA234E/2K5	NRND	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 125	A34	
OPA234EA/250	NRND	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 125	A34	
OPA234EA/250G4	NRND	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 125	A34	
OPA234EA/2K5	NRND	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 125	A34	
OPA234U	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	OPA 234U	
OPA234U/2K5	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	OPA 234U	
OPA234UA	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	OPA 234U A	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA234UA/2K5	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	OPA 234U A	
OPA4234U	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U	
OPA4234U/2K5	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U	
OPA4234UA	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U A	
OPA4234UA/2K5	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U A	
OPA4234UA/2K5G4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U A	
OPA4234UAG4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U A	
OPA4234UG4	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4234U	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

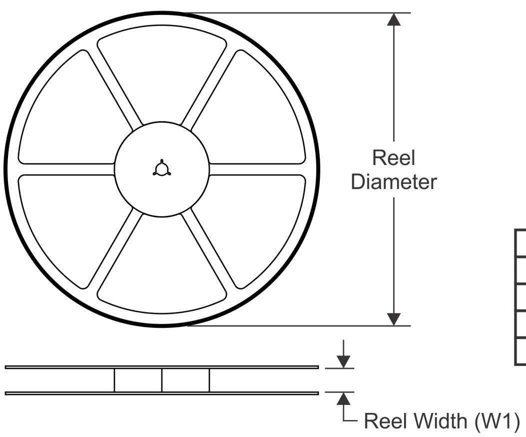
OTHER QUALIFIED VERSIONS OF OPA2234 :

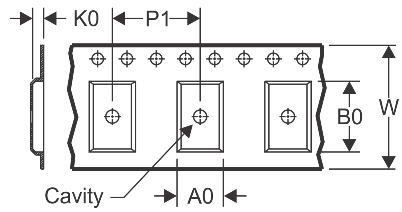
- Military: OPA2234M

NOTE: Qualified Version Definitions:

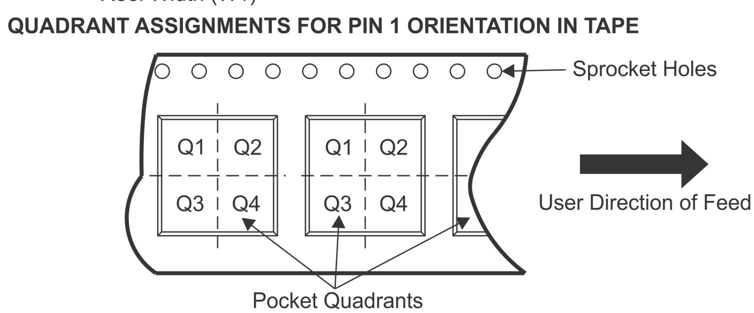
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION





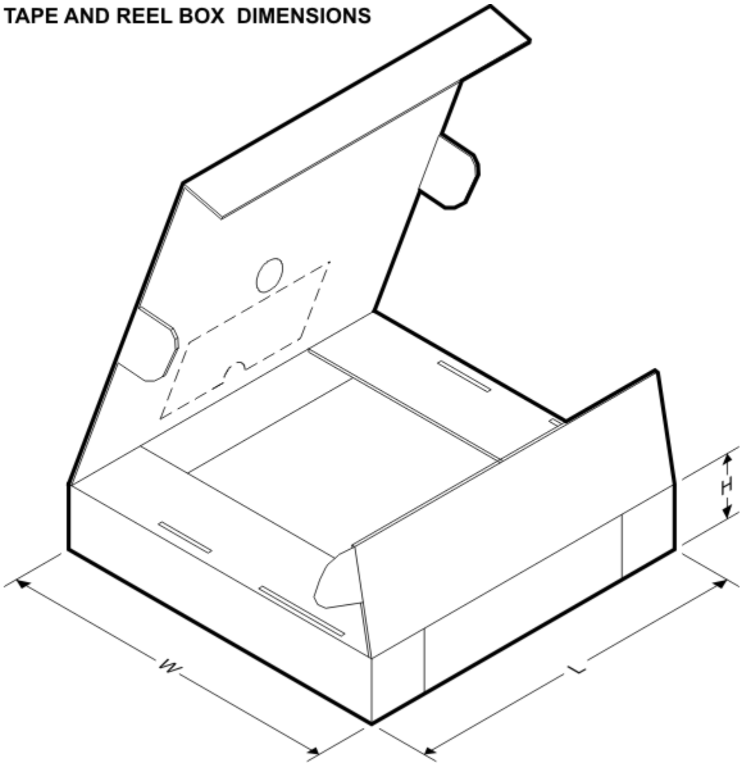
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2234U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2234UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA234E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA234E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA234EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA234EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA234U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA234UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4234U/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4234UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

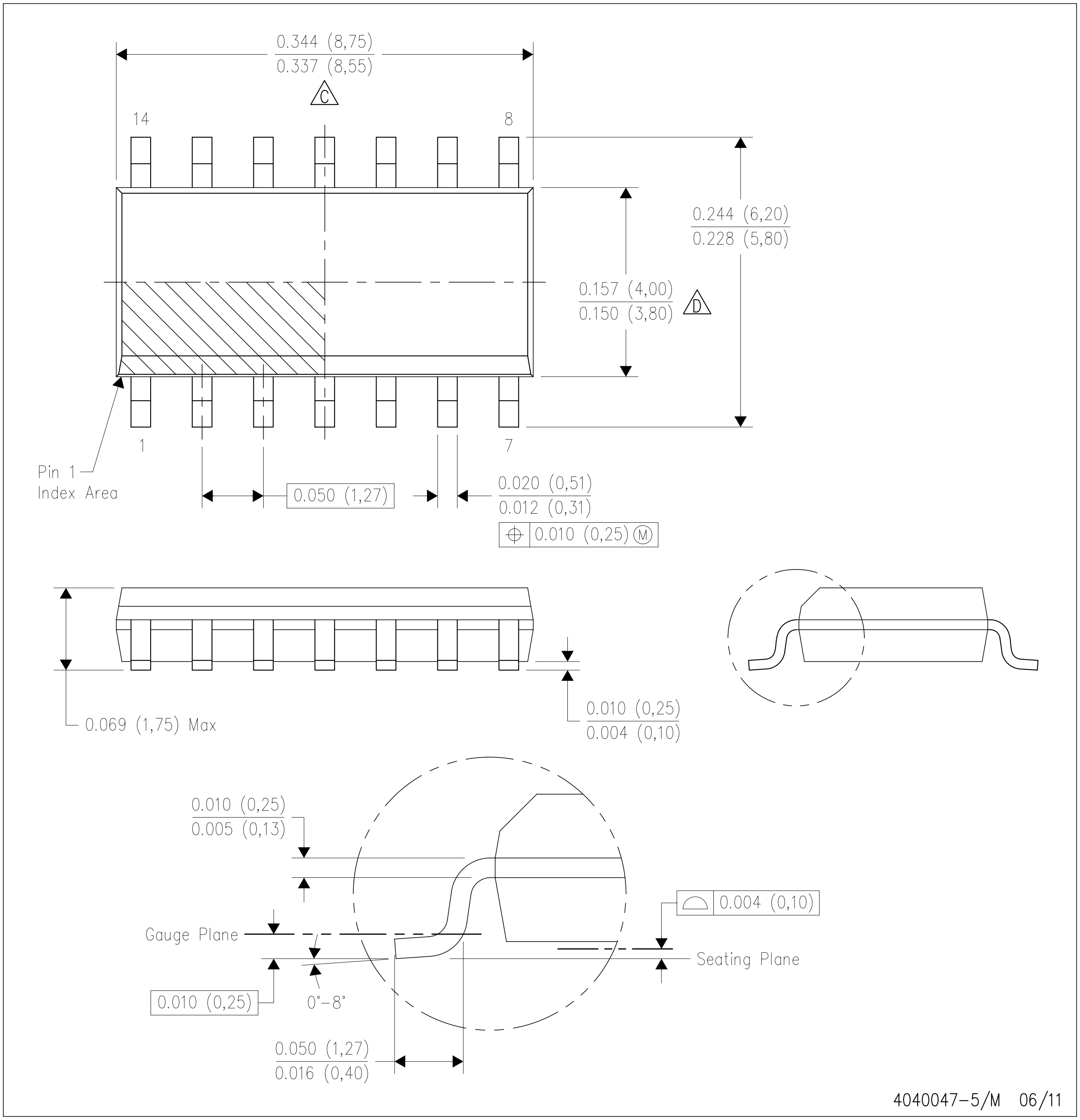
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

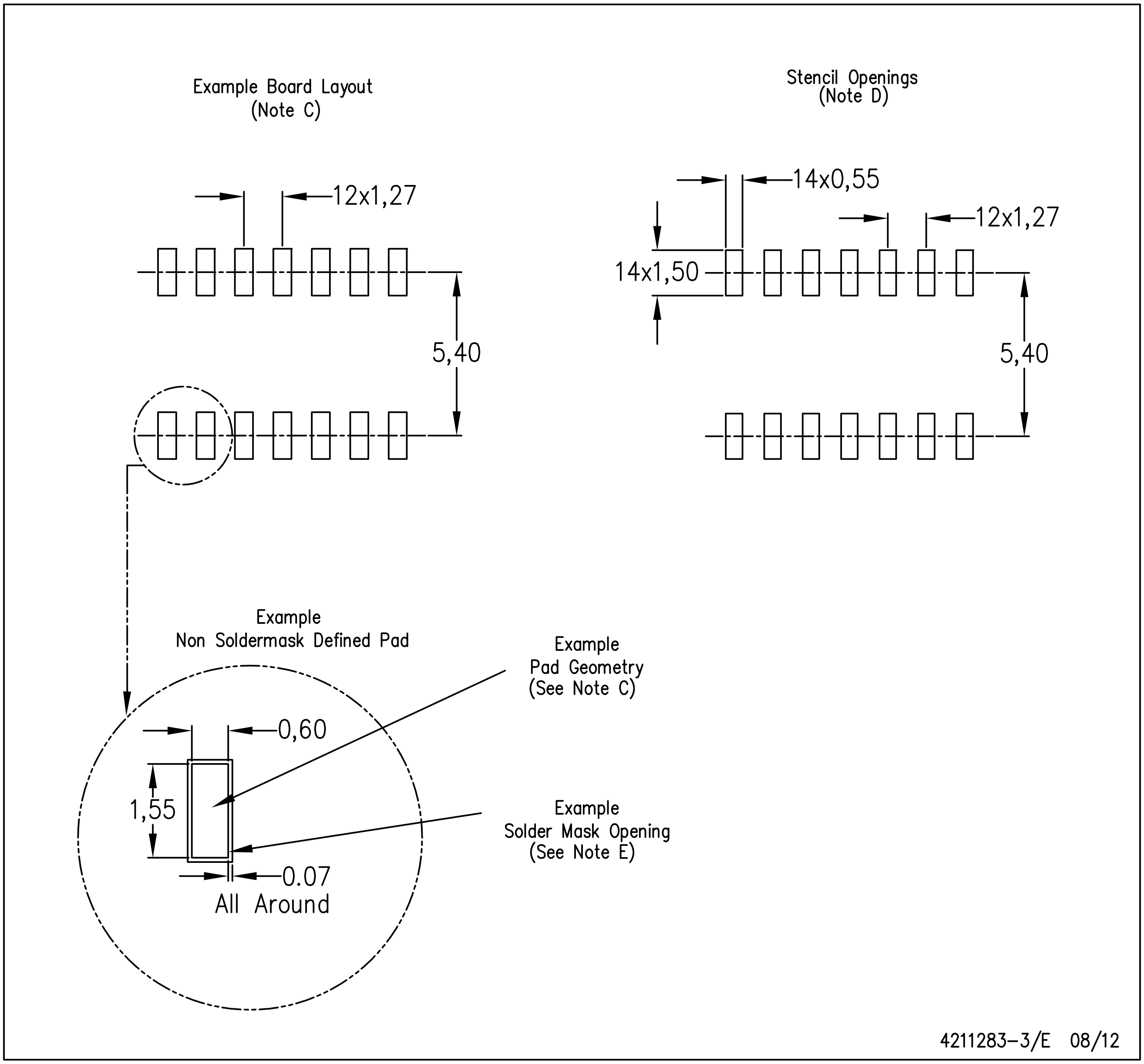
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2234U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2234UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA234E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA234E/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA234EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA234EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA234U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA234UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4234U/2K5	SOIC	D	14	2500	367.0	367.0	38.0
OPA4234UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

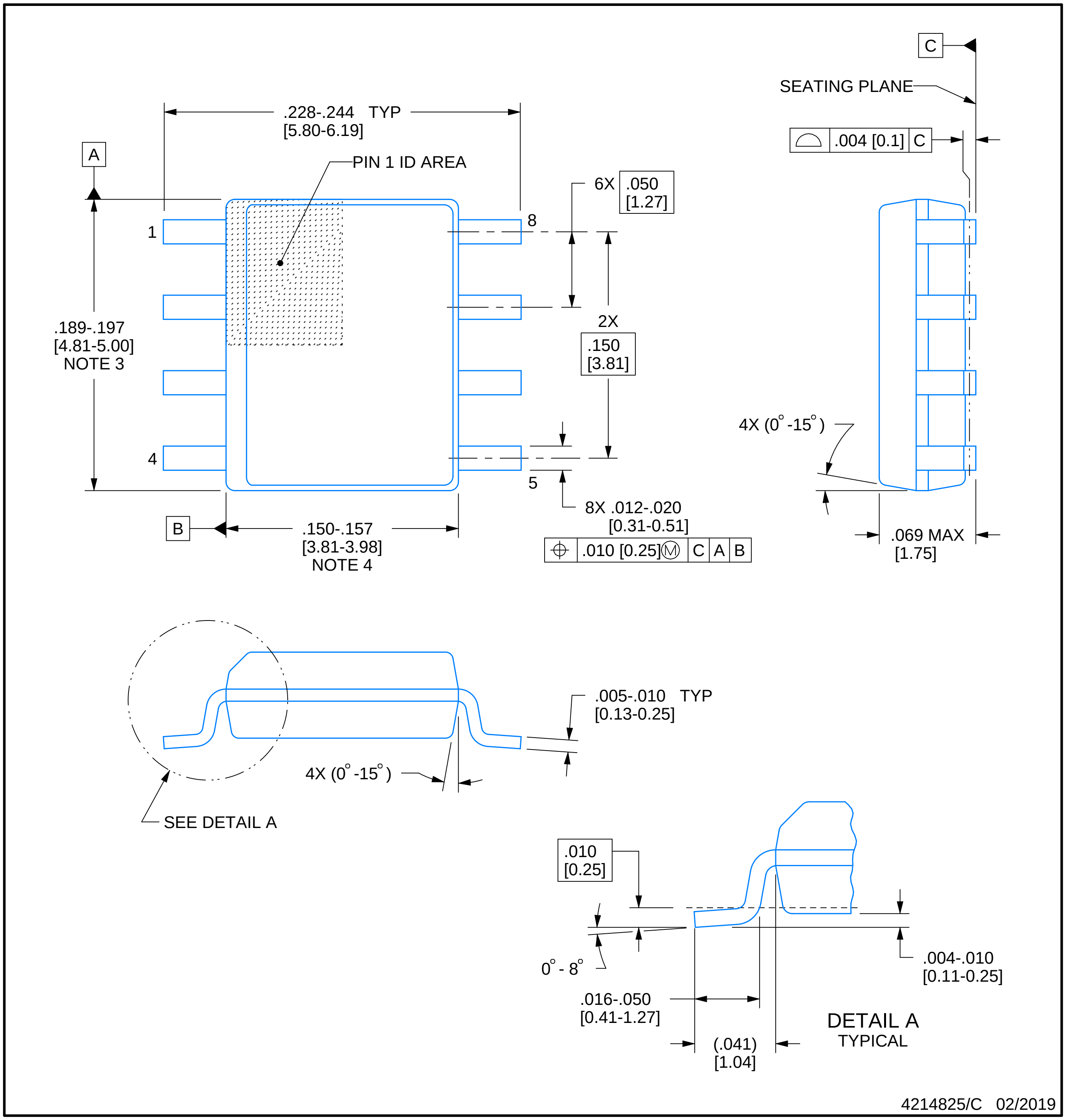


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

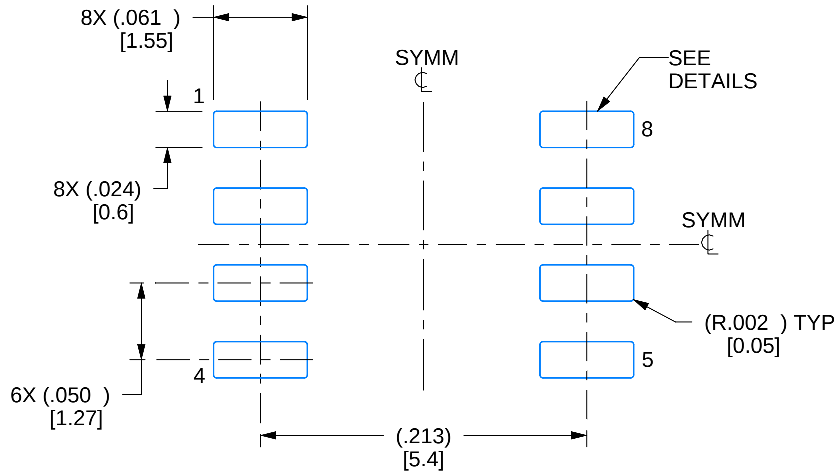


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

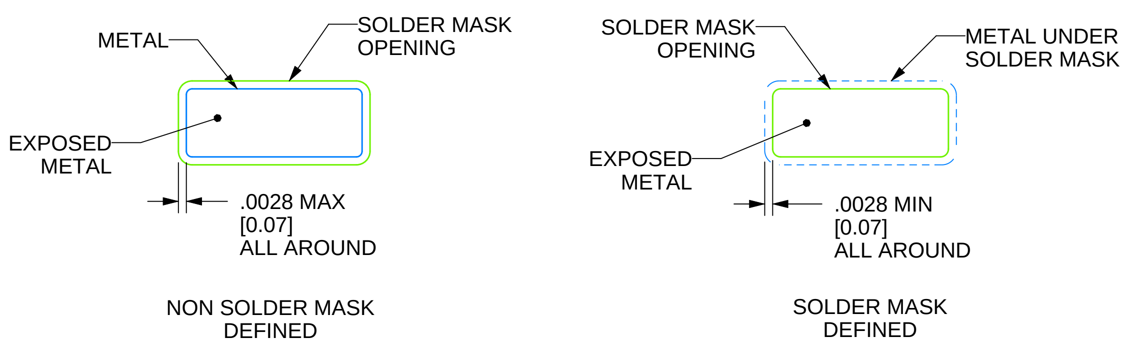


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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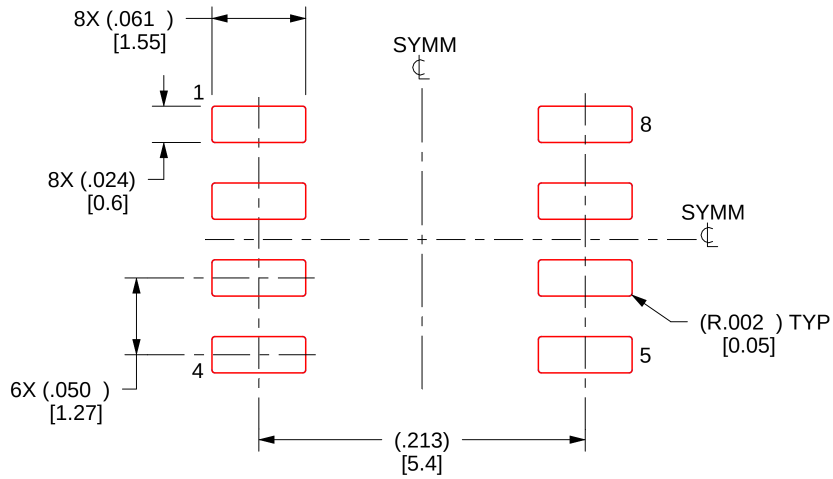
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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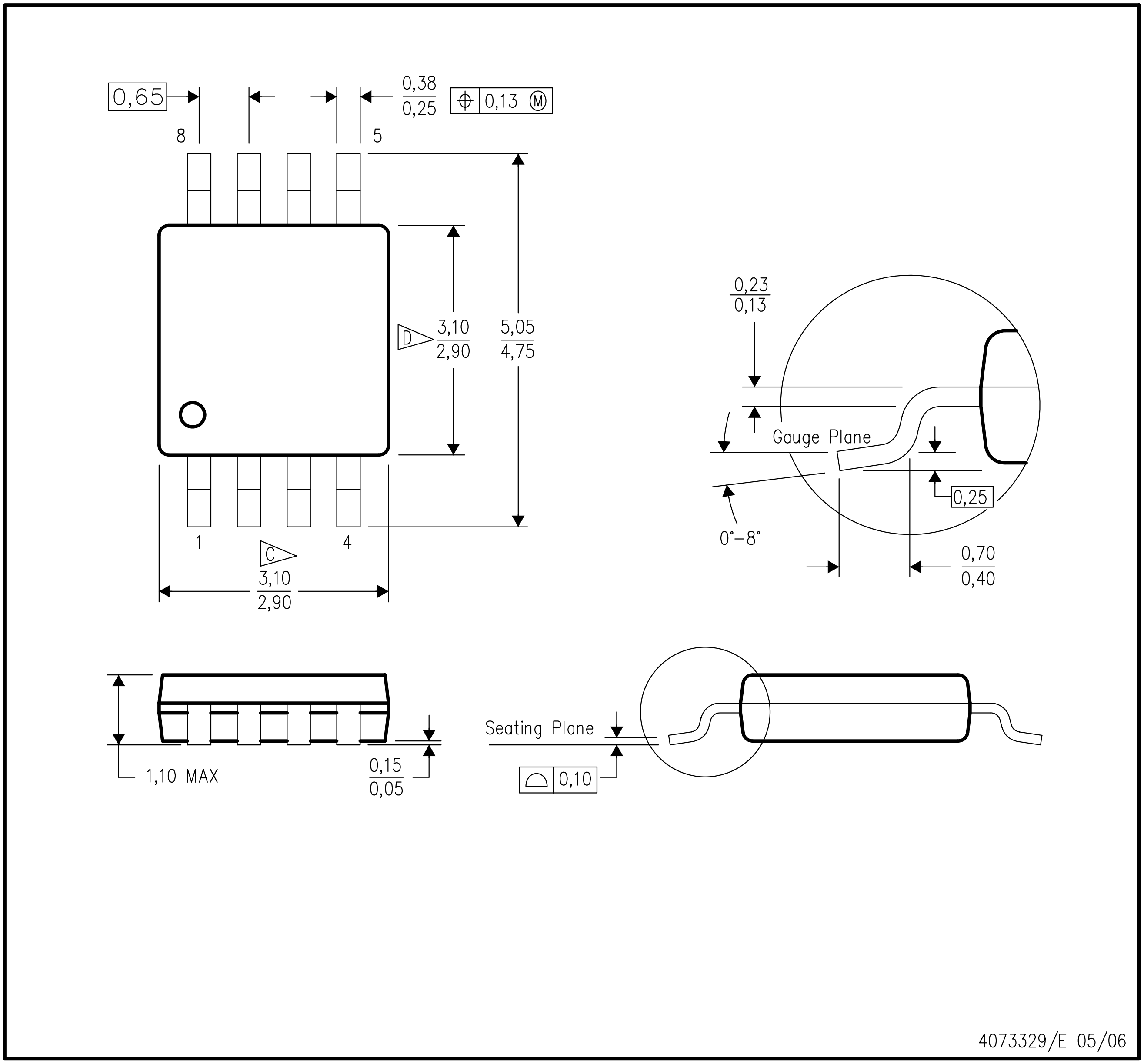
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.