

FULLY INTEGRATED 8-CHANNEL DC/DC CONVERTER FOR DIGITAL STILL CAMERAS

FEATURES

- 8-Channel DC/DC Converter and Low Dropout (LDO)
- Integrated Power MOSFET Switch Except CH8
 - Boost (CH5/7)
 - Buck (CH1/3)
 - Buck-Boost (CH2/4)
 - Invert (CH6)
- Low-Power Suspend Mode (Sleep Mode)
- Power ON/OFF Sequence (CH1/2/3 and CH5/6)
- LED-Back Light Brightness Control (CH7)
- Fixed Switching Frequency (CH1–4: 1.5 MHz, CH5–8: 750 kHz)
- Fixed Max Duty Cycle Internally
- Soft Start
- Undervoltage Lockout (UVLO)
- Protection
 - Thermal Shutdown (TSD)
 - Overvoltage Protection (OVP)
 - Overcurrent Protection (OCP) Except CH8
- Supply Voltage Range: 1.5 V to 5.5 V
- Operating Temperature Range: –25°C to 85°C
- 6 × 6 mm, 0.4-mm Pitch, 48-Pin QFN Package

APPLICATIONS

- Digital Still Cameras (DSCs)
- Portable Electronics Equipment

DESCRIPTION/ ORDERING INFORMATION

The TPS65530A is a fully integrated 8-channel switching dc/dc converter, and seven channels have integrated power FET.

CH2/4 are configured for H bridge for buck-boost topology and single inductor supports. These channels achieve higher efficiency in spite of input/output voltage conditions.

CH7 has a brightness control and drives white LED by constant current. Also, CH7 supports overvoltage protection (OVP) for open load.

CH1/2/3 have a power ON/OFF sequence suitable for a digital still camera (DSC) system. CH5/6 have a power ON/OFF sequence, depending on the CCD. Power ON/OFF for CCD block (CH5/6) is selectable by the input voltage level at the SEQ56 pin. CH4 and CH7 have individual ON/OFF sequences.

The TPS65530A high switching frequency is achieved by an integrated power MOSFET switch. It reduces external parts dynamically. Shutdown current consumption is less than 1 μ A as a typical value.

ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾⁽²⁾ | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------------------|-----------------------|------------------|
| –25°C to 85°C | QFN | Reel of 250 | TPS65530ARSLT |
| | | Reel of 2500 | TPS65530ARSLR |
| | | | TPS65530A |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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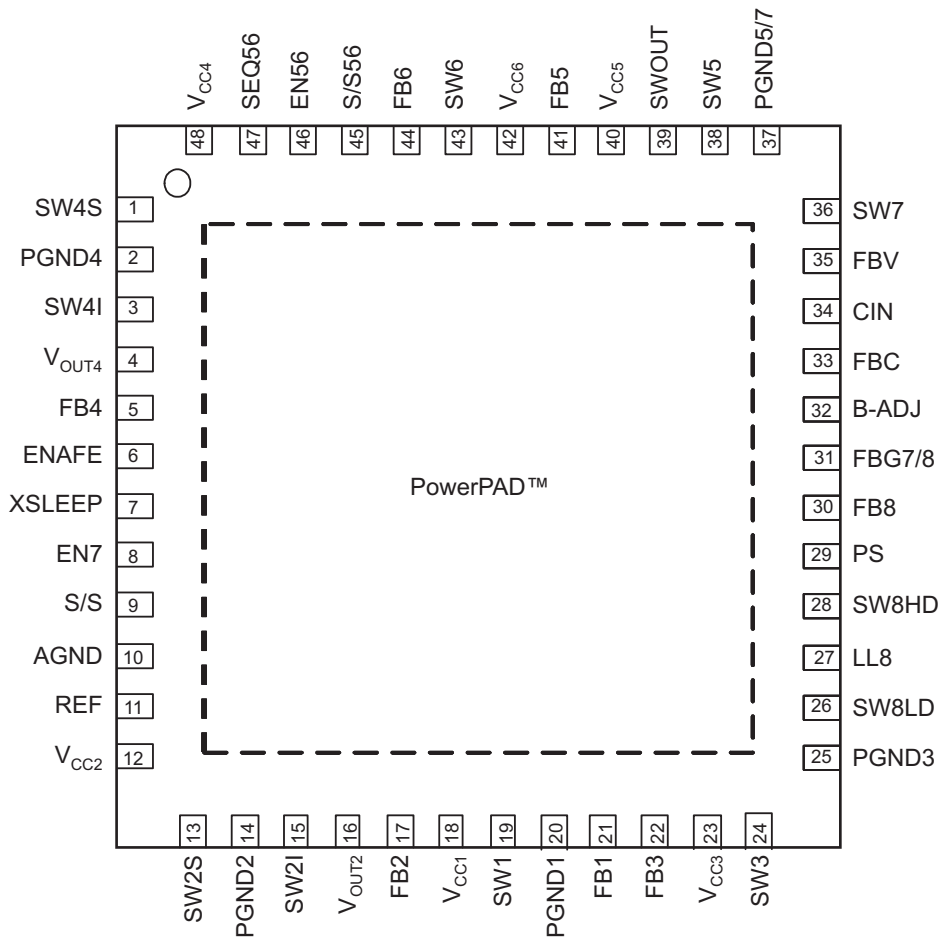


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CHANNEL CONFIGURATION

| CHANNEL | OPERATION MODE | RECTIFY MODE | CONTROL METHOD | OUTPUT VOLTAGE (V) | APPLICATION | MAXIMUM SUPPLY CURRENT (mA) |
|---------|---------------------|----------------|-----------------|--------------------|--------------------------------------|-----------------------------|
| CH1 | Buck SW | Synchronous | Voltage | 0.9 to 2.5 | Engine core | 600 |
| CH2 | Buck-boost SW | Synchronous | Average current | 2.5 to 3.6 | Engine I/O (DSP I/F) | 600 |
| CH3 | Buck SW | Synchronous | Voltage | 0.9 to 2.5 | External memory | 300 |
| CH4 | Buck-boost SW | Synchronous | Average current | 2.2 to 3.6 | AFE | 300 |
| CH5 | Boost SW | Nonsynchronous | Peak current | Up to 18 | CCD+ | 50 |
| CH6 | Invert SW | Nonsynchronous | Voltage | -10 to -5 | CCD- | 100 |
| CH7 | Boost SW | Nonsynchronous | Voltage | 3 to 20 | Backlight LED | 25 |
| CH8 | Boost SW | Synchronous | Voltage | 3.3 to 5.5 | Motor controller and IC drive supply | - |
| REF | Low dropout voltage | - | - | 2.8 | Internal supply for logic | 15 |

QFN PACKAGE (TOP VIEW)



TERMINAL FUNCTIONS

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|----------|-------------------|--------------------|--|
| NO. | NAME | | |
| 1 | SW4S | O | Buck-side terminal of coil for CH4 |
| 2 | PGND4 | G | GND for CH4 low-side FET |
| 3 | SW4I | I | Boost-side terminal of coil for CH4 |
| 4 | V _{OUT4} | O | Output of CH4 |
| 5 | FB4 | I | Output voltage feedback for CH4. The external resistors should be connected as close as possible to the terminal. |
| 6 | ENAFE | I | Enable for CH4 (L: Disable, H: Enable) |
| 7 | XSLEEP | I | Control for sleep mode/normal operation (L: Sleep mode, H: Normal operation) |
| 8 | EN7 | I | Enable for CH7 (L: Disable, H: Enable) |
| 9 | S/S | I/O | Soft-start time adjustment. The time is programmable by an external capacitor (see the Soft Start description). |
| 10 | AGND | G | Analog ground |
| 11 | REF | O | Output of LDO. From 2.2 μ F to 4.7 μ F, capacitor should be connected to AGND. |
| 12 | V _{CC2} | P | Power supply at CH2 buck-side FET from battery |
| 13 | SW2S | O | Buck-side terminal of coil for CH2 |
| 14 | PGND2 | G | GND for CH2 low-side FET |
| 15 | SW2I | I | Boost-side terminal of coil for CH2 |
| 16 | V _{OUT2} | O | Output of CH2 |
| 17 | FB2 | O | Output voltage feedback for CH2. The external resistors should be connected as close as possible to the terminal. |
| 18 | V _{CC1} | P | Power supply at CH1 high-side FET from battery |
| 19 | SW1 | O | Output of CH1. The terminal should be connected to the external inductor. |
| 20 | PGND1 | G | GND for CH1 low-side FET |
| 21 | FB1 | I | Output voltage feedback for CH1. The external resistors should be connected as close as possible to the terminal. |
| 22 | FB3 | I | Output voltage feedback for CH3. The external resistors should be connected as close as possible to the terminal. |
| 23 | V _{CC3} | P | Power supply at CH3 high-side FET from battery |
| 24 | SW3 | O | Output of CH3. The terminal should be connected to the external inductor. |
| 25 | PGND3 | G | GND for CH3 low-side FET |
| 26 | SW8LD | O | Output for CH8 external low-side FET drive. The terminal is connected to the gate of the low-side external FET. |
| 27 | LL8 | O | Switching output for CH8 at wake mode. The terminal is switched when the output voltage of CH8 is less than 2.5 V. |
| 28 | SW8HD | O | Output for CH8 external high-side FET drive. The terminal is connected to the gate of the high-side external FET. |
| 29 | PS | I | Power input for IC inside. The terminal should be connected to CH8 output voltage. |
| 30 | FB8 | I | Output voltage feedback for CH8. The external resistors should be connected as close as possible to the terminal. |
| 31 | FBG7/8 | I | GND for CH7/8 feedback resistors |
| 32 | B-ADJ | I | Brightness adjustment for W-LED |
| 33 | FBC | I | Output current feedback for CH7 |
| 34 | CIN | I | Input current at CH7 load switch |
| 35 | FBV | I | Output voltage feedback for CH7. The external resistors should be connected as close as possible to the terminal. |
| 36 | SW7 | O | Output of CH7. The terminal should be connected to the external inductor. |
| 37 | PGND5/7 | G | Power GND for CH5/7. The terminal should be connected by power ground layer at PCB via a through hole. |
| 38 | SW5 | O | Low-side terminal of coil for CH5 |

(1) I = input, O = output, I/O = input/output, P = power supply, G = GND

TERMINAL FUNCTIONS (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------|------------------|--------------------|--|
| NO. | NAME | | |
| 39 | SWOUT | O | High-side terminal of coil for CH5 |
| 40 | V _{CC5} | P | Power supply at CH5 high-side FET from battery |
| 41 | FB5 | I | Output voltage feedback for CH5. The external resistors should be connected as close as possible to the terminal. |
| 42 | V _{CC6} | P | Power supply at CH6 load switch from battery |
| 43 | SW6 | O | Output of CH6. The terminal should be connected to the external inductor. |
| 44 | FB6 | I | Output voltage feedback for CH6. The external resistors should be connected as close as possible to the terminal. |
| 45 | S/S56 | I/O | Soft-start time adjustment for CH5/6. The time is programmable by external capacitor (see the Soft Start description). |
| 46 | EN56 | I | Enable for CH5/6 (L: Disable, H: Enable) |
| 47 | SEQ56 | I | Sequence select for CH5/6 (see the Power ON/OFF Sequence description) |
| 48 | V _{CC4} | P | Power supply at CH4 high-side FET from battery |
| Back side | PowerPAD™ | G | Must be soldered to achieve appropriate power dissipation. Should be connected to PGND to use a $\Phi 0.3$ -mm through hole. |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | UNIT |
|---|---|-------------|------|
| Input voltage range | V _{CC1} , V _{CC2} , V _{CC3} , V _{CC4} , V _{CC5} , V _{CC6} , SWOUT, FB2, FB4, FB5, FB8, FBC, FBV, PS, XSLEEP, ENAFE, SEQ56, EN56, EN7, SW4S, SW4I, V _{OUT4} , V _{OUT2} , SW1, SW3, SW8LD, SW8HD, FBG78 (based on PGND or AGND) | –0.3 to 6 | V |
| | SW2S, SW2I | –0.3 to 7 | |
| | BADJ, SS, FB1, FB3, FB6, SS56 | –0.3 to 3 | |
| | LL8 | –0.3 to 7 | |
| | REF | –0.3 to 3.6 | |
| | SW5 | –0.3 to 22 | |
| | SW7, CIN | –0.3 to 27 | |
| | SW6 (based on V _{CC6}) | –20 | |
| | PGND1, PGND2, PGND3, PGND4, PGND57, AGND | –0.3 to 0.3 | |
| Switching current | CIN | 0.05 | A |
| | SW2S, SW2I | 3.3 | |
| | SW4S, SW4I | 1.65 | |
| | SW1 | 1.9 | |
| | SW3 | 1 | |
| | SW5 | 1.6 | |
| | SW6 | –1.35 | |
| | SW7 | 1.2 | |
| | LL8 | 1 | |
| | SW8LD, SW8HD | 0.6 | |
| T _J Maximum junction temperature range | | –30 to 150 | °C |
| T _{stg} Storage temperature range | | –40 to 150 | °C |
| ESD rating, Human-Body Model (HBM) | JEDEC JESD22A-A114 | 2 | kV |
| ESD rating, Charged-Device Model (CDM) | JEDEC JESD22A-C101 | 500 | V |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

| PACKAGE | R _{θJA} ⁽¹⁾ | POWER RATINGS T _A < 25°C | POWER RATINGS RATE T _A > 25°C |
|------------|---------------------------------|--|---|
| 48-pin QFN | 27°C/W | 2.9 W | 0.029°C/W |

(1) The thermal resistance, R_{θJA}, is based on a soldered PowerPAD package on a 2S2P JEDEC board (3-in × 3-in, four layers) using thermal vias (0.3-mm diameter × 12 vias)

RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|--------------------------|---|-----|-----|------|
| Supply voltage | V _{CC1} , V _{CC2} , V _{CC4} , V _{CC5} | 1.5 | 5.5 | V |
| | V _{CC3} , V _{CC6} | 2.5 | 5.5 | |
| High-level input voltage | XSLEEP, ENAFE, EN56, EN7 | 1.4 | | V |
| | SEQ56 | 1.4 | REF | |
| Low-level input voltage | XSLEEP, ENAFE, EN56, EN7, SEQ56 | | 0.4 | V |
| Operating temperature | | –25 | 85 | °C |

ELECTRICAL CHARACTERISTICS

0°C ≤ T_J ≤ 125°C, 1.8 V ≤ V_{CC2} ≤ 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------------|---|--|-------|--------------------|-------|------|
| For All Circuits | | | | | | |
| I _{CC_Iq} | Consumption current at PS (pin 29) | V _{CC2} = VPS = 3.6 V, XSLEEP = AGND | | 1 | 10 | μA |
| I _{CC_sleep} | | V _{CC2} = 3.6 V, VPS = 5 V, XSLEEP = AGND, ENAFE = V _{CC2} | | 40 | 70 | |
| I _{CC_PWM} | | V _{CC2} = 3.6 V, VPS = 5 V, XSLEEP = V _{CC2} , ENAFE = V _{CC2} , EN56 = V _{CC2} , EN7 = V _{CC2} | | 20 | 30 | |
| I _{CC_Iq2} | Consumption current at V _{CC2} (pin 12) | V _{CC2} = VPS = 3.6 V, XSLEEP = AGND | | 1 | 10 | μA |
| I _{CC_sleep2} | | V _{CC2} = 3.6 V, VPS = 5 V, XSLEEP = AGND, ENAFE = V _{CC2} | | 12 | 30 | |
| I _{CC_PWM2} | | V _{CC2} = 3.6 V, VPS = 5 V, XSLEEP = V _{CC2} , ENAFE = V _{CC2} , EN56 = V _{CC2} , EN7 = V _{CC2} | | 0.3 | 1 | |
| TSD | Thermal shutdown temperature ⁽²⁾ | | | 150 | | °C |
| V _(UV_ON) | UVLO detect level | V _{CC2} from 0 V to 5.5 V, XSLEEP = V _{CC2} | 1.25 | 1.4 | 1.55 | V |
| V _(UV_OFF) | UVLO hysteresis | V _{CC2} from 5.5 V to 0 V | 50 | 100 | 150 | mV |
| OSC | Internal OSC frequency | V _{CC2} = 3.6 V | 1.35 | 1.5 | 1.65 | MHz |
| O _{SC_SUB} | CH5–8 switching frequency | OSC = 1.5 MHz, VPS = 5 V | | 750 | | KHz |
| | REF output voltage | XSLEEP = V _{CC2} | 2.72 | 2.8 | 3.03 | V |
| I _{SS} | SS source current | S/S = AGND | 6 | 10 | 14 | μA |
| | Pull-down resistance at XSLEEP, ENAFE, EN56, EN7, SEQ56 | XSLEEP = ENAFE = EN56 = EN7 = SEQ56 = 3 V | | 200 | | kΩ |
| CH1 | | | | | | |
| V _{CC1} | Supply voltage | | 1.5 | | 5.5 | V |
| V _{OUT1} | Output voltage ⁽²⁾ | | 0.9 | | 2.5 | V |
| I _{OUT1} | Output current ⁽²⁾ | V _{CC1} > 2.4 V, V _{OUT1} = 1.2 V, Feedback resistance: R1 = 330 kΩ, R2 = 330 kΩ | | | 600 | mA |
| V _{FB1} | FB1 reference voltage | No load | 0.59 | 0.6 | 0.61 | V |
| | Overcurrent protection threshold | | | 0.9 | 1.9 | A |
| | Overvoltage protection threshold (sensing at FB1 pin) | | 0.67 | 0.75 | 0.83 | V |
| | High-side Nch FET ON resistance ⁽³⁾ | VPS = 5 V | | 320 | 500 | mΩ |
| | Low-side Nch FET ON resistance ⁽³⁾ | VPS = 5 V | | 200 | 250 | mΩ |
| | Trigger voltage to start CH3 | | | 0.48 | | V |
| | Trigger voltage to power off LDO | | | 0.25 | | V |
| CH2 | | | | | | |
| V _{CC2} | Supply voltage | | 1.5 | | 5.5 | V |
| V _{OUT2} | Output voltage ⁽²⁾ | | 2.5 | | 3.6 | V |
| I _{OUT2} | Output current ⁽²⁾ | V _{CC2} > 2.4 V, V _{OUT2} = 3.3 V, Feedback resistance: R1 = 180 kΩ, R2 = 820 kΩ | | | 600 | mA |
| V _{FB2} | FB2 reference voltage | No load | 0.595 | 0.605 | 0.615 | V |
| | Overcurrent protection threshold | | | 2.6 | 3.3 | A |
| | Overvoltage protection threshold (sensing at FB2 pin) | | 0.67 | 0.75 | 0.83 | V |
| Buck side ⁽³⁾ | High-side FET ON resistance | VPS = 5 V | | 100 | 210 | mΩ |
| | Low-side FET ON resistance | VPS = 5 V | | 450 | 600 | |

(1) T_A = 25°C

(2) Specified by design

(3) The value of FET ON resistance includes the resistance of bonding wire.

ELECTRICAL CHARACTERISTICS (continued)
 $0^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$, $1.8\text{ V} \leq V_{\text{CC}2} \leq 5\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---|-------------------------------|--|------------------|--------------------|-------|------|
| Boost side ⁽³⁾ | High-side FET ON resistance | VPS = 5 V | | 130 | 240 | mΩ |
| | Low-side FET ON resistance | VPS = 5 V | | 80 | 140 | |
| Trigger voltage to power off CH3 | | V _{OUT2} = 0.5 V | | 0.5 | | V |
| V _{OUT2} leakage current | | V _{OUT2} = 0.5 V | | | 1 | μA |
| Nch FET ON resistance for discharge | | XSLEEP = AGND, ENAFE = AGND | | 1 | 2 | kΩ |
| CH3 | | | | | | |
| V _{CC3} | Supply voltage | | 2.5 | | 5.5 | V |
| V _{OUT3} | Output voltage ⁽²⁾ | | 0.9 | | 2.5 | V |
| I _{OUT3} | Output current ⁽²⁾ | V _{CC3} > 2.5 V, V _{OUT3} = 1.8 V, Feedback resistance: R1 = 220 kΩ, R2 = 470 kΩ | | | 300 | mA |
| V _{FB3} | FB3 reference voltage | No load | 0.59 | 0.6 | 0.61 | V |
| Overcurrent protection threshold | | | | 0.6 | 1 | A |
| Overvoltage protection threshold (sensing at FB3 pin) | | | 0.67 | 0.75 | 0.83 | V |
| High-side Nch FET ON resistance ⁽⁴⁾ | | VPS = 5 V | | 370 | 750 | mΩ |
| Low-side Nch FET ON resistance ⁽⁴⁾ | | VPS = 5 V | | 300 | 600 | mΩ |
| Nch FET ON resistance for discharge | | XSLEEP = AGND, ENAFE = AGND | | 1 | 2 | kΩ |
| Trigger voltage to start CH2 | | | | 0.48 | | V |
| Trigger voltage to power off CH1 | | | | 0.2 | | V |
| CH4 | | | | | | |
| V _{CC4} | Supply voltage | | 1.5 | | 5.5 | V |
| V _{OUT4} | Output voltage ⁽⁵⁾ | | 2.2 | | 3.6 | V |
| I _{OUT4} | Output current ⁽⁵⁾ | V _{CC4} > 2.4 V, V _{OUT4} = 3.3 V, Feedback resistance: R1 = 82 kΩ, R2 = 330 kΩ | | 100 | 300 | mA |
| V _{FB4} | FB4 reference voltage | No load | 0.595 | 0.605 | 0.615 | V |
| Overcurrent protection threshold | | | | 1.4 | 1.65 | A |
| Overvoltage protection threshold (sensing at FB4 pin) | | | 0.67 | 0.75 | 0.83 | V |
| Buck side ⁽⁴⁾ | High-side FET ON resistance | VPS = 5 V | | 130 | 310 | mΩ |
| | Low-side FET ON resistance | VPS = 5 V | | 600 | 730 | |
| Boost side ⁽⁴⁾ | High-side FET ON resistance | VPS = 5 V | | 170 | 270 | mΩ |
| | Low-side FET ON resistance | VPS = 5 V | | 130 | 250 | |
| V _{OUT4} leakage current | | V _{OUT4} = 0.5 V | | | 1 | μA |
| Nch FET ON resistance for discharge | | XSLEEP = AGND, ENAFE = AGND | | 1 | 2 | kΩ |
| CH5 | | | | | | |
| V _{CC5} | Supply voltage | | 1.5 | | 5.5 | V |
| V _{OUT5} | Output voltage ⁽⁵⁾ | | V _{CC5} | | 18 | V |
| V _{FB5} | FB5 reference voltage | No load | 0.98 | 1 | 1.02 | V |
| I _{OUT5} | Output current ⁽⁵⁾ | V _{CC5} > 2.4 V, V _{OUT5} = 15 V, Feedback resistance: R1 = 40 kΩ, R2 = 560 kΩ | | | 50 | mA |

(4) The value of FET ON resistance includes the resistance of bonding wire.

(5) Specified by design

ELECTRICAL CHARACTERISTICS (continued)

0°C ≤ T_J ≤ 125°C, 1.8 V ≤ V_{CC2} ≤ 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---------------------|--|--|-------|--------------------|------|------|
| | Overcurrent protection threshold | | | 1.3 | 1.6 | A |
| | Overvoltage protection threshold (sensing at FB5 pin) | | 1.09 | 1.25 | 1.38 | V |
| | Nch FET ON resistance ⁽⁴⁾ | VPS = 5 V | | 610 | 900 | mΩ |
| | Load switch ON resistance (between V _{CC5} and SW5) | 1.5 V < V _{CC5} < 5.5 V | | 100 | 470 | mΩ |
| | Load switch ramp-up time (between V _{CC5} and SW5) ⁽⁵⁾ | 1.5 V < V _{CC5} < 5.5 V, SWOUT capacitance = 4.7 μF | | 200 | | μS |
| | Load switch leakage current (between V _{CC5} and SW5) | | | | 1 | μA |
| | Max duty cycle | | 96 | 98 | | % |
| | Trigger voltage to start up CH6 | SEQ56 = AGND | | 0.8 | | V |
| CH6 | | | | | | |
| V _{CC6} | Supply voltage | | 2.5 | | 5.5 | V |
| V _{OUT6} | Output voltage ⁽⁵⁾ | | -10 | | -5 | V |
| I _{OUT6} | Output current ⁽⁵⁾ | V _{CC6} > 2.8 V, V _{OUT6} = -7.5 V, Feedback resistance: R1 = 136 kΩ, R2 = 820 kΩ | | | 100 | mA |
| V _{FB6} | FB6 reference voltage | No load | -0.02 | 0 | 0.02 | V |
| | Overcurrent protection threshold | V _{CC6} > 2.8 V | | 1.1 | 1.35 | A |
| | Overvoltage protection threshold (sensing at FB6 pin) | | -0.3 | -0.2 | -0.1 | V |
| | Pch FET ON resistance ⁽⁶⁾ | V _{CC6} = 3.6 V | | 640 | 1100 | mΩ |
| | Max duty cycle | | 84 | 91 | 98 | % |
| | Trigger voltage to power off CH6 | SEQ56 = AGND | 0.5 | 0.53 | 0.56 | V |
| V _{S/S56} | S/S56 pin voltage | | 1.22 | 1.25 | 1.28 | V |
| I _{S/S56} | S/S56 pin source current | S/S56 = AGND | 170 | 200 | 230 | μA |
| CH7 | | | | | | |
| V _{CC7} | Supply voltage ⁽⁷⁾ | | 1.5 | | 5.5 | V |
| V _{OUT7} | Output voltage ⁽⁸⁾ | V _{CC7} < V _{OUT7} | 3 | | 20 | V |
| I _{OUT7_L} | Lower output current ⁽⁷⁾ | V _{CC7} > 2.4 V, V _{OUT7} = 15 V, Feedback resistance: R1 = 47 kΩ, R2 = 680 kΩ, R _{sense} = 10 Ω, B_ADJ pin voltage = 0 V | 3.7 | 5 | 6.3 | mA |
| I _{OUT7_H} | Higher output current ⁽⁷⁾ | V _{CC7} > 2.4 V, V _{OUT7} = 15 V, Feedback resistance: R1 = 47 kΩ, R2 = 680 kΩ, R _{sense} = 10 Ω, B_ADJ pin voltage = 1 V | 23.7 | 25 | 26.3 | mA |
| V _{FBV} | FBV reference voltage | No load | 0.97 | 1 | 1.03 | V |
| | Overvoltage protection threshold (sensing at FBV pin) | | 1.15 | 1.25 | 1.35 | V |
| | Overcurrent protection threshold | | | 0.8 | 1.2 | A |
| | Nch FET ON resistance ⁽⁶⁾ | | | 700 | 1200 | mΩ |
| | Max duty cycle | | 86 | 91 | 99 | % |
| | Load switch ON resistance | | | 2 | 4 | Ω |
| | Load switch leakage current (between C-IN and FBC) | | | | 1 | μA |
| R _{B-ADJ} | B-ADJ pin input impedance | | | 1 | | MΩ |

(6) The value of FET ON resistance includes the resistance of bonding wire.

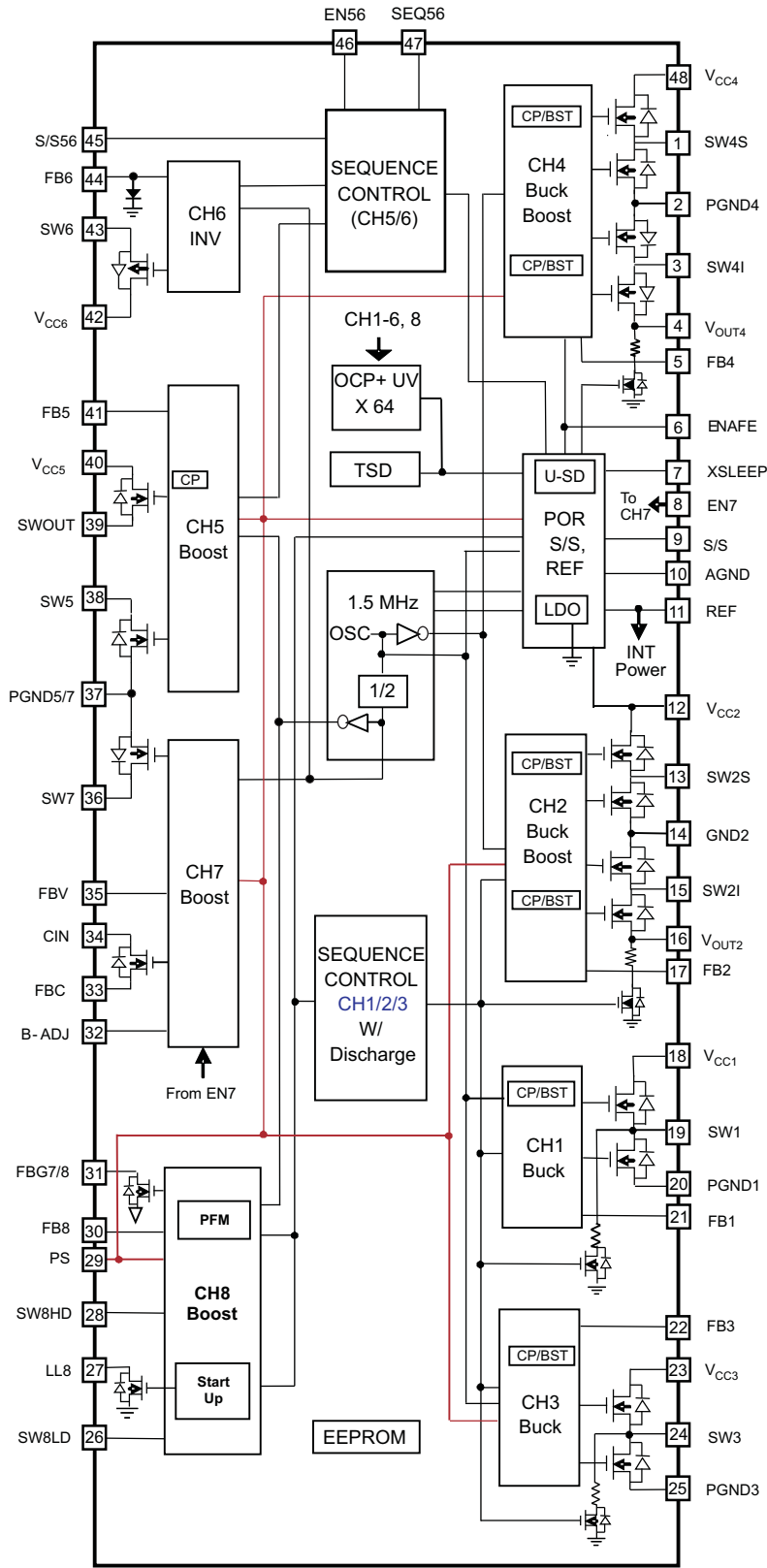
(7) Specified by design

(8) Due to constant current control for CH7, the operating condition is that Input voltage is less than LED supply voltage (output voltage).

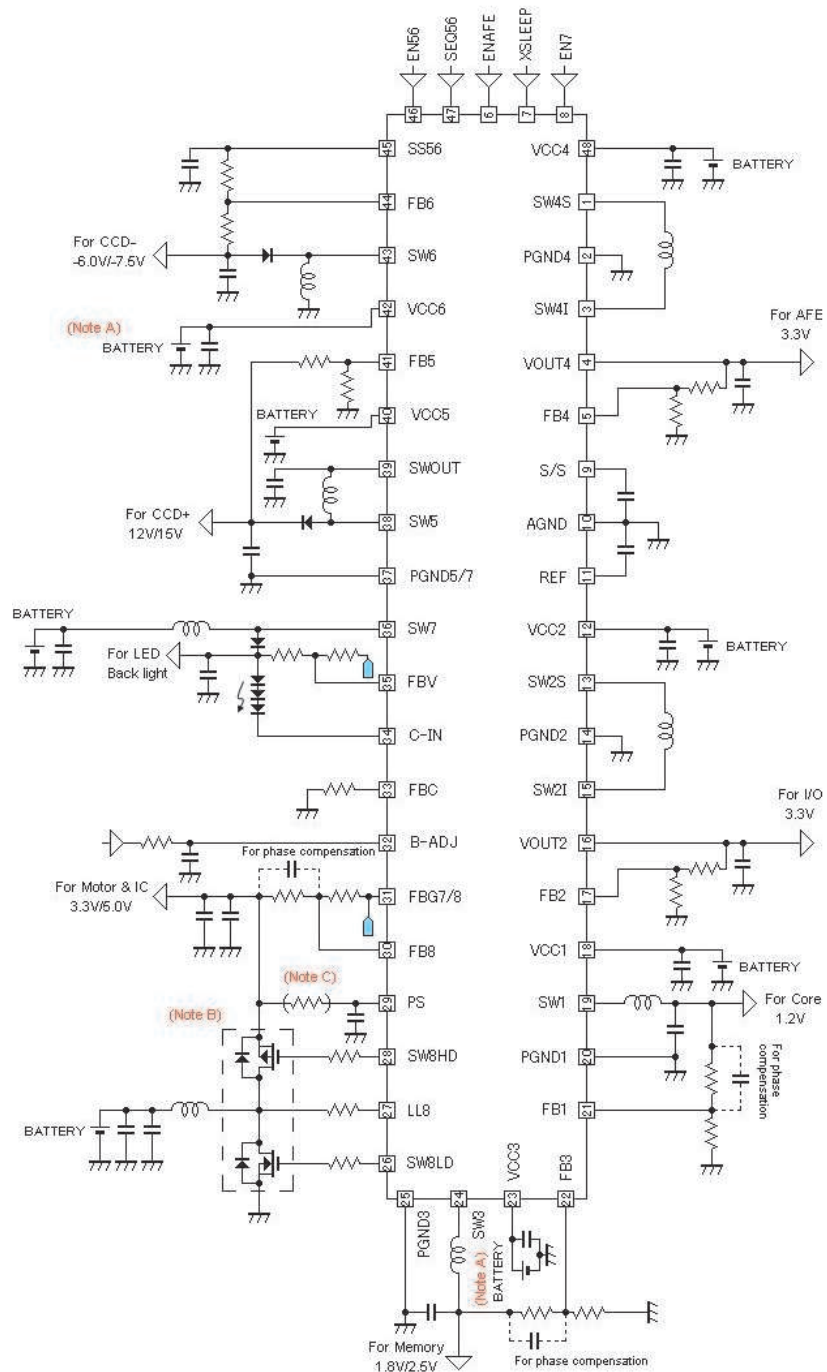
ELECTRICAL CHARACTERISTICS (continued)
 $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, $1.8\text{ V} \leq V_{\text{CC2}} \leq 5\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---|-------------------------------|--|------|--------------------|------|---------------|
| CH8 | | | | | | |
| Supply voltage ⁽⁷⁾ | | $T_A = 25^{\circ}\text{C}$, Start up (XSLEEP from AGND to V_{CC2}) | 1.8 | | 5.5 | V |
| | | XSLEEP = V_{CC2} | 1.5 | | 5.5 | |
| VPS | Output voltage ⁽⁷⁾ | | 3.3 | | 5.5 | V |
| V_{FB8} | FB8 reference voltage | XSLEEP = H, ENAFE = AGND, No load | 1.23 | 1.25 | 1.27 | V |
| | | CH8 operation mode: PFM mode, No load | 1.2 | 1.25 | 1.35 | |
| Fixed ON time at PFM mode | | $V_{\text{CC2}} = 3.6\text{ V}$ | | 250 | | ns |
| Max duty cycle | | | 76 | 85 | 92 | % |
| SW8LD driver | Source impedance | VPS = 5 V, ISW = 100 mA | | 5 | 7.5 | Ω |
| | Sink impedance | VPS = 5 V, ISW = -100 mA | | 1 | 1.5 | |
| SW8HD driver | Source impedance | VPS = 5 V, ISW = 100 mA | | 10 | 15 | Ω |
| | Sink impedance | VPS = 5 V, ISW = -100 mA | | 5 | 7.5 | |
| Overvoltage protection threshold (sensing at FB8 pin) | | | 1.3 | 1.56 | 1.8 | V |
| FBG7/8 FET ON resistance | | VPS = 5 V, XSLEEP = V_{CC2} | | 0.6 | | k Ω |
| FBG7/8 leakage current | | XSLEEP = AGND, ENAFE = AGND | | | 1 | μA |

BLOCK DIAGRAM



APPLICATION INFORMATION



- A. When output voltage is higher than input voltage at 2AA battery models, V_{CC1} and V_{CC3} should be connected to the CH8 output. When the 2AA battery is connected, V_{CC6} should be connected to the CH8 output.
- B. The external FET for CH8 is dependent on the load. When the motor is connected to CH8, the external FET is large.
- C. It is acceptable to connect directly to PS without resistor.

FUNCTIONAL DESCRIPTION

Logic True Table

The enable/disable of each channel is controlled by logic input signals level at XSLEEP (pin 7 for all channels), ENAFE (pin 6 for CH4), EN56 (pin 46 for CH5/6) and EN7 (pin 8 for CH7). Table 1 is the summary of the enable/disable mode.

Table 1. Control Pin vs Enable/Disable

| NO. OF STATE | XSLEEP | ENAFE | EN56 | EN7 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 | CH8 ⁽¹⁾ | LDO |
|-------------------|--------|-------|------|-----|-----|-----|-----|-----|-----|-----|-----|--------------------|-----|
| 1 | L | L | – | – | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| 2 | H | L | L | L | ON | ON | ON | OFF | OFF | OFF | OFF | PWM | ON |
| 3 | H | L | L | H | ON | ON | ON | OFF | OFF | OFF | ON | PWM | ON |
| 4 | H | L | H | L | ON | ON | ON | OFF | ON | ON | OFF | PWM | ON |
| 5 | H | L | H | H | ON | ON | ON | OFF | ON | ON | ON | PWM | ON |
| 6 | H | H | L | L | ON | ON | ON | ON | OFF | OFF | OFF | PWM | ON |
| 7 | H | H | L | H | ON | ON | ON | ON | OFF | OFF | ON | PWM | ON |
| 8 | H | H | H | L | ON | ON | ON | ON | ON | ON | OFF | PWM | ON |
| 9 | H | H | H | H | ON | ON | ON | ON | ON | ON | ON | PWM | ON |
| 10 ⁽²⁾ | L | H | – | – | OFF | OFF | OFF | OFF | OFF | OFF | OFF | PFM | OFF |

- (1) PWM = pulse width modulation, PFM = pulse frequency modulation
- (2) State 10 (CH8: PFM mode) must go through State 2.

Power ON/OFF Sequence

This device has the power ON/OFF sequence of CH1/2/3/8/REF and CH5/6 for DSC application. The CH1/2/3/8/REF sequence is shown in Figure 1. The CH5/6 sequence is shown in Figure 2. CH4 and CH7 have individual sequences but CH4–6 have the subordinate relationship with CH1–3 because the slope of soft start is the same and puts high priority of CH1–3 to avoid the functional conflict (see the Soft Start description). Due to this, CH4–6 should not be ON before CH1–3 are ON. When XSLEEP is forced low, all channels turn OFF with the power OFF sequence.

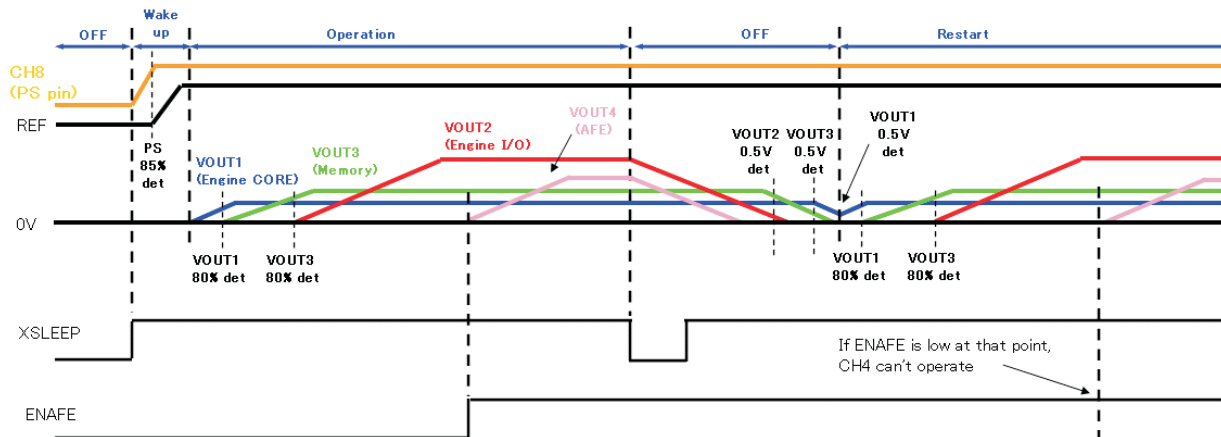


Figure 1. CH1/CH2/CH3/CH8/REF Power ON/OFF Sequence

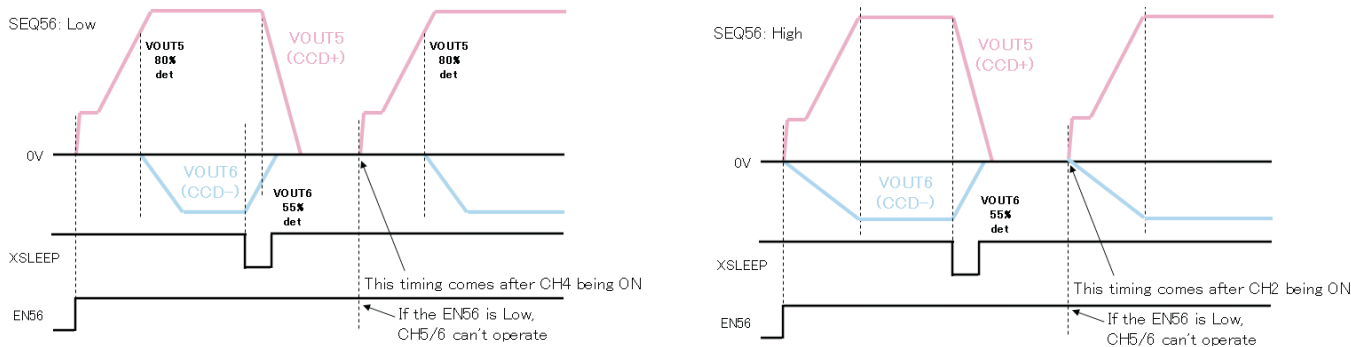


Figure 2. CH5/6 Power ON/OFF Sequence

Soft Start

This function reduces the rush current from the battery at start-up. This device has two slopes defined by S/S (pin 9) and S/S56 (pin 45). The slopes of CH1–4 are defined by S/S; the slopes of CH5/6 depend on SEQ56 (pin 47) signal level. When SEQ56 is low, the slope of CH5 is defined by S/S; the slope of CH6 is defined by S/S56. When SEQ56 is high, the slopes of CH5/6 are defined by S/S56. The soft-start time is calculated by Equation 1 and Equation 2.

$$T_{S/S} = C_{S/S} \times 60 \tag{1}$$

$$T_{S/S56} = C_{S/S56} \times 6.25 \tag{2}$$

Where:

- $C_{S/S}$ = Capacitance at S/S [μ F]
- $T_{S/S}$ = Soft-start duration defined by S/S [ms]
- $C_{S/S56}$ = Capacitance at S/S56 [μ F]
- $T_{S/S56}$ = Soft-start duration defined by S/S56 [ms]

The recommended capacitances are $C_{S/S} = 0.1 \mu\text{F}$ or $T_{S/S} = 6.0 \text{ ms}$, $C_{S/S56} = 1.0 \mu\text{F}$ or $T_{S/S56} = 6.25 \text{ ms}$.

Undervoltage Lockout (UVLO)

This device monitors the battery voltage level at V_{CC2} (pin 12) When XSLEEP is high and V_{CC2} is less than the threshold (defined in Electrical Characteristics as UVLO detect level), the operation shuts down immediately without the power OFF sequence. UVLO has a hysteresis as shown in Figure 3. This factor is defined in Electrical Characteristics as UVLO hysteresis.

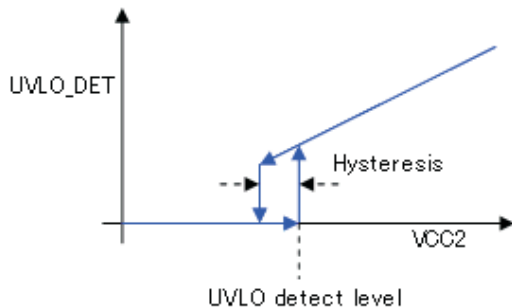


Figure 3. UVLO Hysteresis

Protection

The TPS65530A has three protection conditions: overcurrent protection (OCP), overvoltage protection (OVP), and thermal shutdown (TSD) (see Table 2).

Table 2. Protection Conditions

| PROTECTION | | CH1–CH6 | CH7 | CH8 | REF (LDO) |
|------------|--------------------|---|--|--|--|
| OCP | Change mode | All CH shutdown (latch-off) (without power OFF sequence) | Forced OFF at MOSFET | All CH shutdown (latch-off) (without power OFF sequence) | All CH shutdown (latch-off) (without power OFF sequence) |
| | Detect condition | Current over the threshold, V_{OUT} less than 80% to compare the target, and count 64 cycle \times 1.5 MHz | Current over the threshold | V_{OUT} less than 70% to compare the target | V_{OUT} less than 80% to compare the target |
| | Comeback condition | XSLEEP: Change level from Low to High ENAFE: Change level from Low to High (for CH4) EN56: Change level from Low to High (for CH5/6) or V_{CC2} : Apply more than UVLO threshold (1.4 V) after removing V_{CC2} | Current less than the threshold (automatic restoration) or V_{CC2} : Apply more than UVLO threshold (1.4 V) after removing V_{CC2} | XSLEEP: Change level from Low to High ENAFE: Change level from Low to High or V_{CC2} : Apply more than UVLO threshold (1.4 V) after removing V_{CC2} | XSLEEP: Change level from Low to High ENAFE: Change level from Low to High or V_{CC2} : Apply more than UVLO threshold (1.4 V) after removing V_{CC2} |
| OVP | Change mode | Forced OFF at applicable CH MOSFET | Forced OFF at MOSFET, load switch turns ON | Forced OFF at MOSFET | No OVP function |
| | Detect condition | Voltage over the threshold at feedback | Voltage over the threshold at feedback | Voltage over the threshold at feedback | |
| | Comeback condition | Voltage less than the threshold at feedback (auto-recovery) | EN7: Change level from Low to High | Voltage less than the threshold at feedback (auto-recovery) | |
| TSD | Change mode | All CH shutdown (without power OFF sequence) | | | |
| | Detect condition | The junction temperature is more than the threshold. | | | |
| | Comeback condition | XSLEEP: Change level from Low to High, ENAFE: Change level from Low to High (for CH4), EN56: Change level from Low to High (for CH5/6), or V_{CC2} : More than 1.4 V | | | |

CHANNEL DESCRIPTIONS

CH1/3 Description

Both CH1 and CH3 are the same topology. CH1/3 are the voltage-mode-controlled synchronous buck converters for engine core (CH1) or external memory (CH3). Both high-side and low-side switches are integrated into the device and consist of NMOS-FET only. The gate of the high-side switch is driven by bootstrap circuit. The capacitance of the bootstrap is included in the device. These channels are able to operate up to 100% duty cycle.

This device has a discharge path to use the switch (Q_Discharge1/3) for the CH1/3 output capacitor via the inductor. The switch is activated after the power OFF sequence has started. Typical resistance at the discharge circuit is 1 k Ω . When the device detects the threshold at FB1/3 after the power OFF sequence has started, the MOSFET turns OFF and the output is fixed with high impedance.

It is acceptable to connect the battery to V_{CC1}/V_{CC3} (pins 18/23) directly when the battery voltage is more than 2.5 V. When the battery voltage is less than 2.5 V, the CH8 output should be connected to V_{CC1}/V_{CC3} .

The output voltage is programmed from 0.9 V to 2.5 V (both CH1 and CH3) to use the feedback loop sensed by the external resistances. The output voltage is calculated by Equation 3. The block diagram is shown in Figure 4.

$$V_{OUT} = (1 + R2/R1) \times 0.6 [V] \tag{3}$$

Where:

V_{OUT} = Output voltage [V]

R1, R2 = Feedback resistance (see Figure 4)

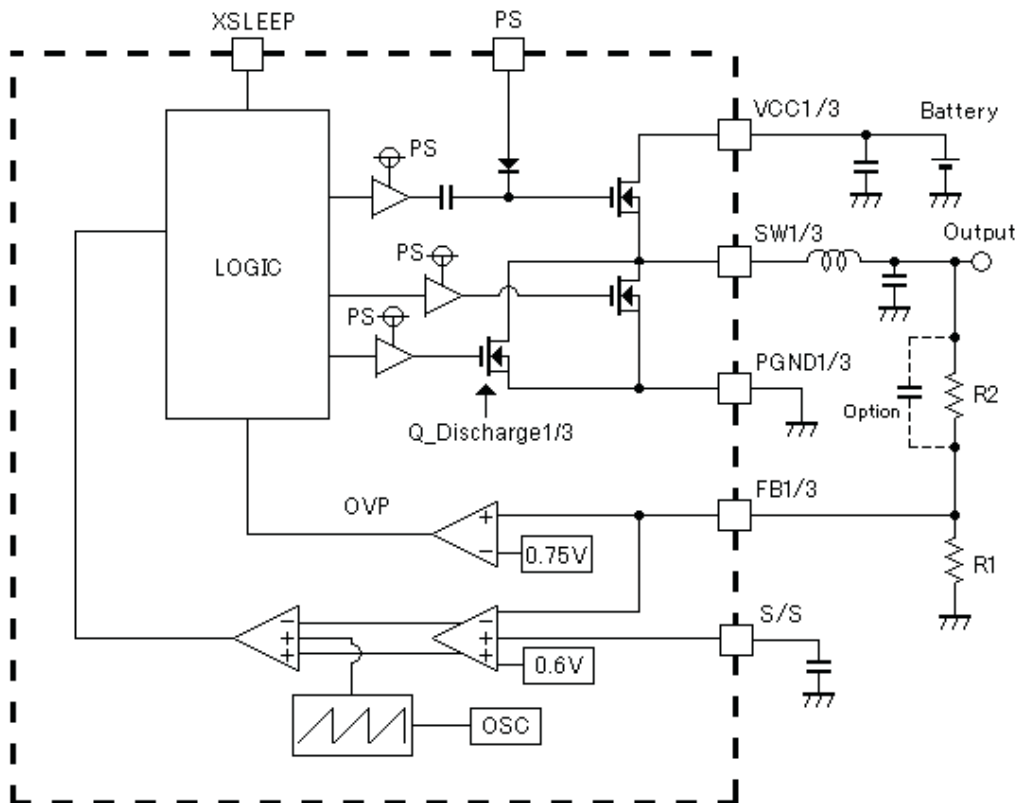


Figure 4. CH1/3 Block Diagram

CH1/3 Recommended Parts

Table 3. Recommended Parts for Inductor (CH1/3)

| VENDOR | TYPE NO. | INDUCTANCE (μH) | DCR (mΩ) | SIZE (mm) |
|--------|---------------------|-----------------|----------|-----------------|
| TOKO | DE2812C-1098AS-4R7M | 4.7 | 130 | 2.8 × 3.0 × 1.2 |

Table 4. Recommended Parts for Capacitor (Input, CH1/3)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|--------|-------------------|------------------|---------------|------------------------------------|
| Murata | GRM21BB30J226ME38 | 22.0 | 20 | 2.0 × 1.25 × 1.25 (EIA code: 0805) |

Table 5. Recommended Parts for Capacitor (Output, CH1/3)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|--------|----------------|------------------|---------------|------------------------------------|
| TDK | C2012X5R0J106M | 10.0 | 20 | 2.0 × 1.25 × 1.25 (EIA code: 0805) |

CH2/4 Description

Both CH2 and CH4 are the same topology. CH2/4 are the average current-mode-controlled synchronous back-boost converters for engine I/O (CH2) or AFE (CH4). This converter is an adapted H-bridge circuit to use four switches. These switches are integrated into the device and consist of NMOS-FET only. The gate of the high-side switch is controlled by the bootstrap circuit. The capacitance of the bootstrap is included in the device.

The device automatically switches from buck operation to boost operation or from boost operation to buck operation as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all four switches are permanently switching.

This device has a discharge switch (Q_Discharge2/4) for the CH2/4 output capacitor. The typical ON resistance at the discharge switch is 1 kΩ. The discharge switch is activated when XSLEEP turns low. For CH4 only, the switch is also activated when ENAFE turns low. After output voltage reaches approximately 0.5 V, the discharge switch turns OFF and V_{OUT2}/V_{OUT4} is changed into high impedance. The output voltage is programmable from 2.5 V to 3.6 V (for CH2) or from 2.2 V to 3.6 V (for CH4) to use the feedback loop sensed by the external resistances. The output voltage is calculated by Equation 4. The block diagram is shown in Figure 5.

$$V_{OUT} = (1 + R2/R1) \times 0.6 \text{ [V]} \tag{4}$$

Where:

V_{OUT} = Output voltage [V]

R1, R2 = Feedback resistance (see Figure 5)

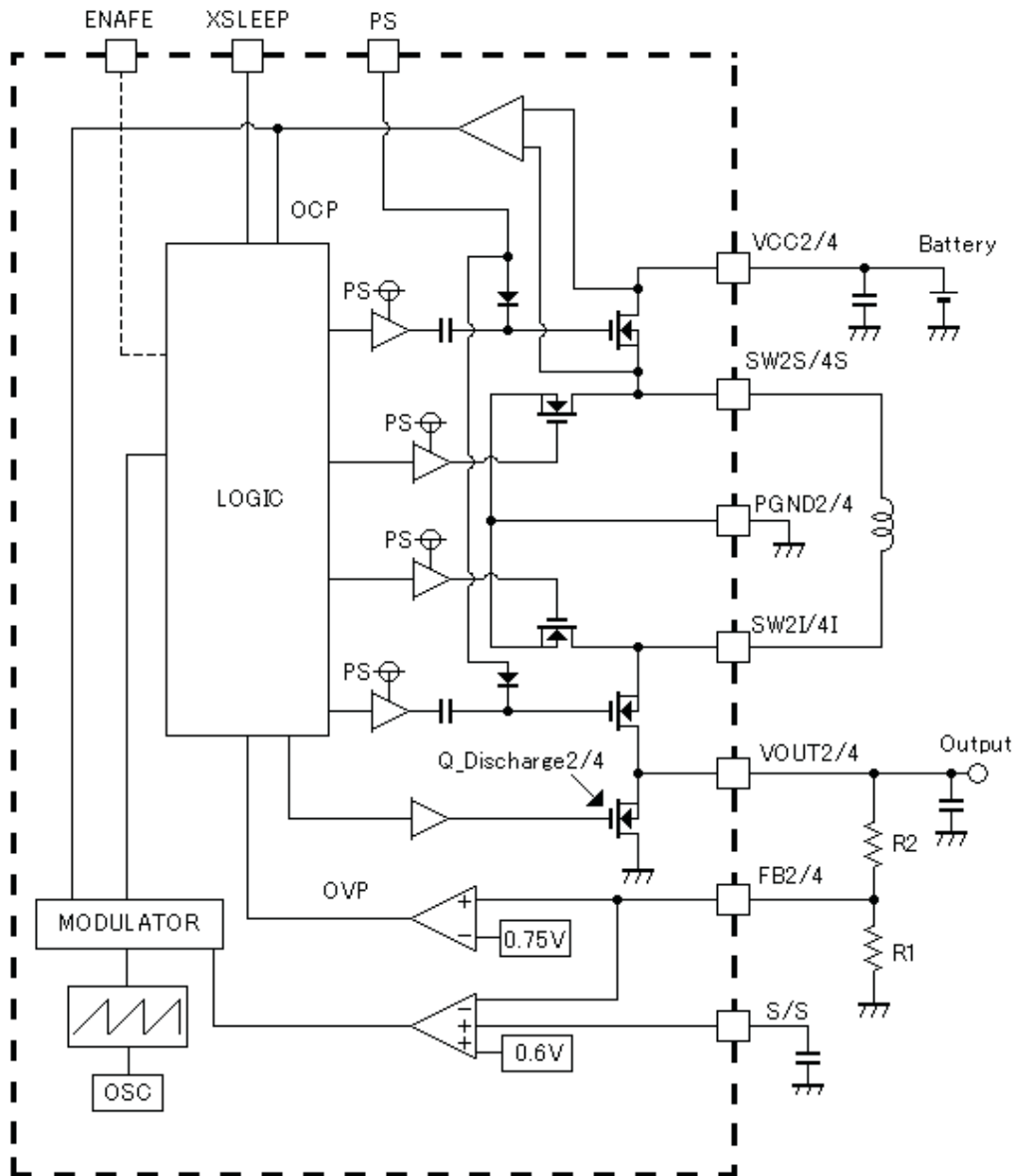


Figure 5. CH2/4 Block Diagram

CH2/4 Recommended Parts
Table 6. Recommended Parts for Inductor (CH2)

| VENDOR | TYPE NO. | INDUCTANCE (μH) | DCR (mΩ) | SIZE (mm) |
|--------|---------------------|-----------------|----------|-----------------|
| TOKO | DE2812C-1098AS-2R7M | 2.7 | 72 | 2.8 × 3.0 × 1.2 |

Table 7. Recommended Parts for Inductor (CH4)

| VENDOR | TYPE NO. | INDUCTANCE (μH) | DCR (mΩ) | SIZE (mm) |
|--------|---------------------|-----------------|----------|-----------------|
| TOKO | DE2812C-1098AS-4R7M | 4.7 | 130 | 2.8 × 3.0 × 1.2 |

Table 8. Recommended Parts for Capacitor (Input, CH2/4)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|--------|-------------------|------------------|---------------|------------------------------------|
| Murata | GRM21BB30J226ME38 | 22.0 | 20 | 2.0 × 1.25 × 1.25 (EIA code: 0805) |

Table 9. Recommended Parts for Capacitor (Output, CH2/4)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|-------------|-----------------|------------------|---------------|------------------------------------|
| Taiyo Yuden | JMK212BJ476MG-T | 47.0 | 20 | 2.0 × 1.25 × 1.25 (EIA code: 0805) |

CH5 Description

CH5 is the peak current-mode-controlled nonsynchronous boost converter for CCD+. The switch between inductor and power GND is integrated into the device and consists of NMOS-FET. Also, this device has a load switch between the battery and inductor and consists of NMOS-FET. The gate of the switch is controlled by a charge-pump circuit. The output voltage is programmable up to 18 V to use the feedback loop sensed by the external resistances. The output voltage is calculated by [Equation 5](#). The block diagram is shown in [Figure 6](#).

$$V_{OUT5} = (1 + R2/R1) \times 1.0 \text{ [V]} \quad (5)$$

Where:

V_{OUT5} = Output voltage of CH5 [V]

R1, R2 = Feedback resistance (see [Figure 6](#))

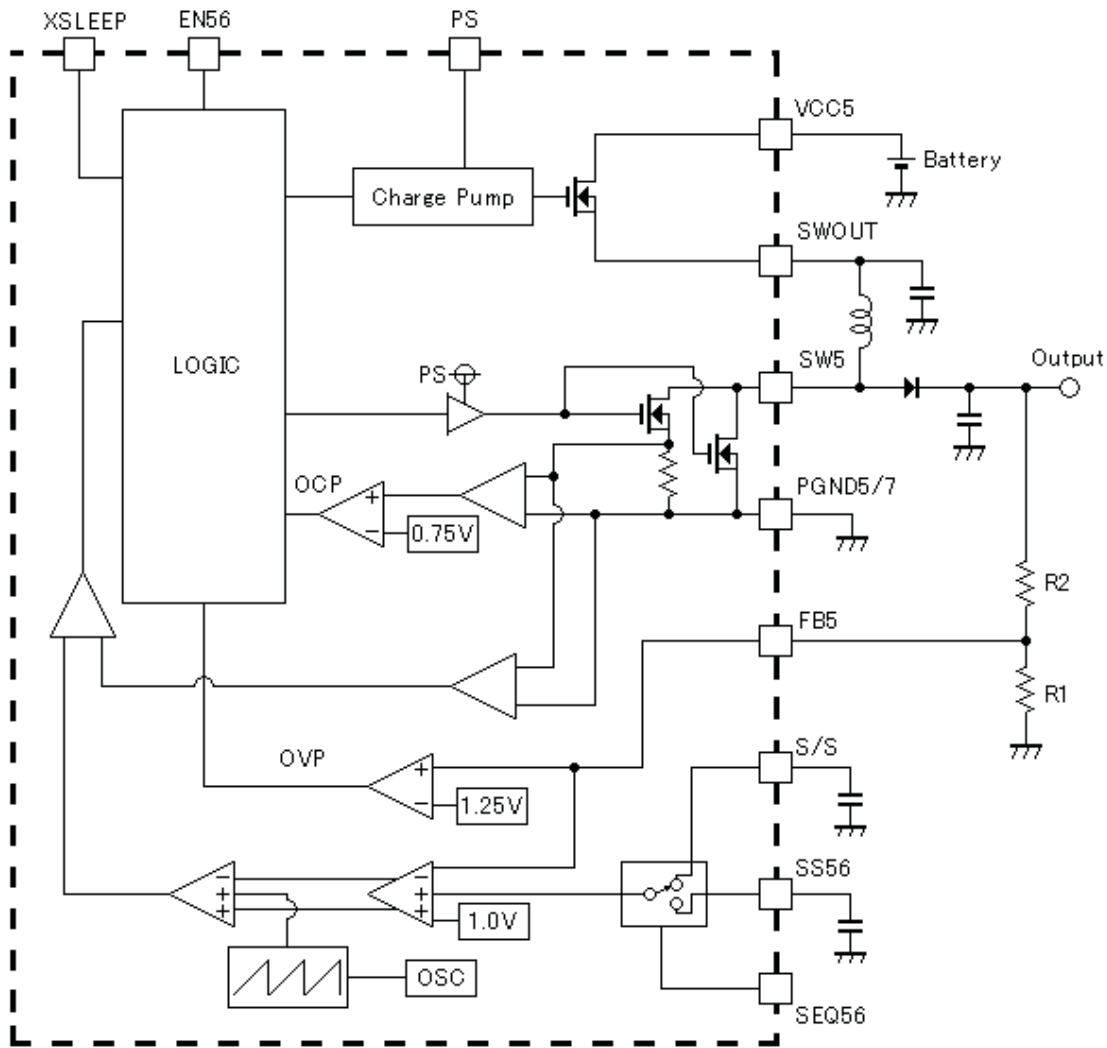


Figure 6. CH5 Block Diagram

CH5 Recommended Parts

Table 10. Recommended Parts for Inductor (CH5)

| VENDOR | TYPE NO. | INDUCTANCE (μH) | DCR (mΩ) | SIZE (mm) |
|--------|---------------------|-----------------|----------|-----------------|
| TOKO | DE2812C-1098AS-120M | 12.0 | 340 | 2.8 × 3.0 × 1.2 |

Table 11. Recommended Parts for Capacitor (Output, CH5)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|--------|-------------------|------------------|---------------|----------------------------------|
| Murata | GRM31CB31E106KA75 | 10.0 | 10 | 3.2 × 1.6 × 1.6 (EIA code: 1206) |

Table 12. Recommended Parts for Capacitor (SWOUT, CH5)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|--------|----------------|------------------|---------------|------------------------------------|
| TDK | C2012X5R1A335M | 3.3 | 20 | 2.0 × 1.25 × 1.25 (EIA code: 0805) |

Table 13. Recommended Parts for Diode (CH5)

| VENDOR | TYPE NO. | VR (V) | IF (mA) | VF (V)/IF (A) | CAPACITANCE (pF) | SIZE (mm) |
|--------|----------|--------|---------|---------------|------------------|-----------------|
| Sanyo | SB0503EJ | 30 | 500 | 0.55/0.5 | 16.5 | 1.6 × 0.8 × 0.6 |

CH6 Description

CH6 is the voltage-mode-controlled nonsynchronous inverting converter for CCD-. The switch between the input voltage and inductor is integrated into the device and consists of PMOS-FET. It is acceptable to connect the battery to V_{CC6} (pin 42) directly when the battery voltage is more than 2.5 V. When the battery voltage is less than 2.5 V, the CH8 output should be connected to V_{CC6}. The output voltage is programmable from -10 V to -5 V to use the feedback loop sensed by the external resistances. The output voltage is calculated by Equation 6. The block diagram is shown in Figure 7.

$$V_{OUT6} = 1.25 - (1 + R2/R1) \times 1.25 [V] \tag{6}$$

Where:

V_{OUT} = Output voltage of CH6 [V]

R1, R2 = Feedback resistance (see Figure 7)

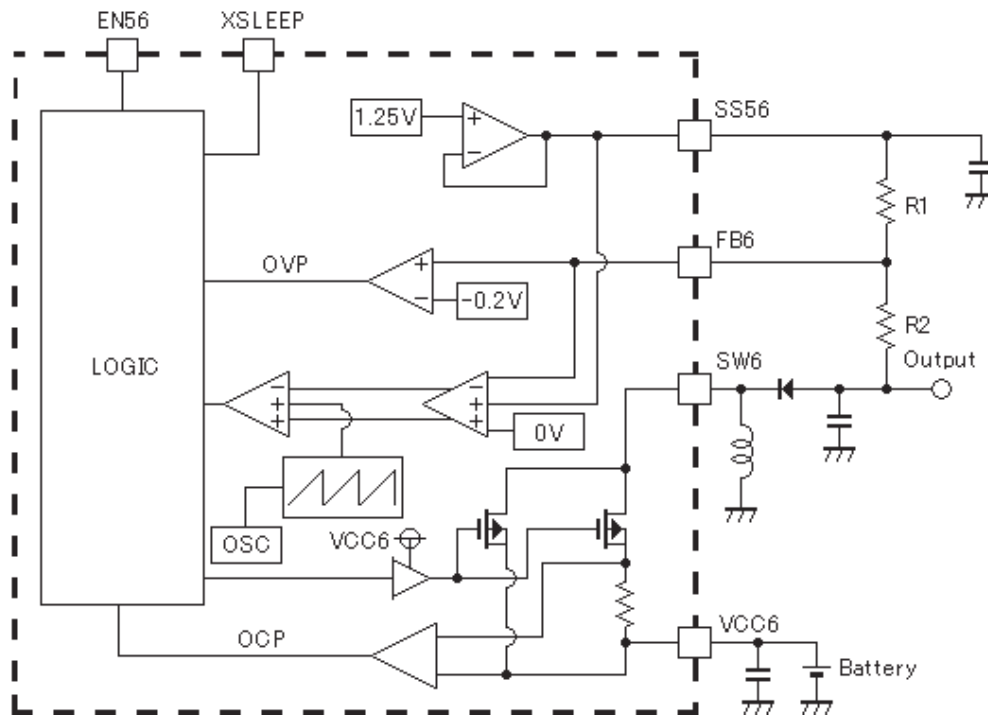


Figure 7. CH6 Block Diagram

CH6 Recommended Parts

Table 14. Recommended Parts for Inductor (CH6)

| VENDOR | TYPE NO. | INDUCTANCE (μH) | DCR (mΩ) | SIZE (mm) |
|--------|---------------------|-----------------|----------|-----------------|
| TOKO | DE2815C-1071AS-120M | 12.0 | 240 | 2.8 × 3.0 × 1.2 |

Table 15. Recommended Parts for Capacitor (Input, CH6)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|--------|-------------------|------------------|---------------|------------------------------------|
| Murata | GRM21BB31A106KE18 | 10.0 | 10 | 2.0 × 1.25 × 1.25 (EIA code: 0805) |

Table 16. Recommended Parts for Capacitor (Output, CH6)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|--------|-------------------|------------------|---------------|----------------------------------|
| Murata | GRM31CB31E106KA75 | 10.0 | 10 | 3.2 × 1.6 × 1.6 (EIA code: 1206) |

Table 17. Recommended Parts for Diode (CH6)

| VENDOR | TYPE NO. | VR (V) | IF (mA) | VF (V)/IF (A) | CAPACITANCE (pF) | SIZE (mm) |
|--------|----------|--------|---------|---------------|------------------|-----------------|
| Sanyo | SB0503EJ | 30 | 500 | 0.55/0.5 | 16.5 | 1.6 × 0.8 × 0.6 |

CH7 Description

CH7 is the voltage-mode-controlled nonsynchronous boost converter for the backlight LED. The switch between the inductor and power GND is integrated into the device and consists of NMOS-FET. Also, this device has a load switch to control the output current and consists of NMOS-FET. The output current is constant and is calculated by Equation 7. It is controlled by the B_ADJ (pin 32) input voltage as shown in Figure 8. The B_ADJ input voltage is required as an analog input. When it is required to input PWM signal for B_ADJ, the RC filter is needed.

$$I_{LED} = \frac{0.2}{R_{SENSE}} \cdot V_{BADJ} + \frac{0.05}{R_{SENSE}} \tag{7}$$

Where:

I_{LED} = Output current of CH7 [A]

R_{SENSE} = Sense resistor between FBC and PGND5/7 [Ω]

V_{BADJ} = B_ADJ input voltage ($0 < V_{BADJ} < 1$) [V]

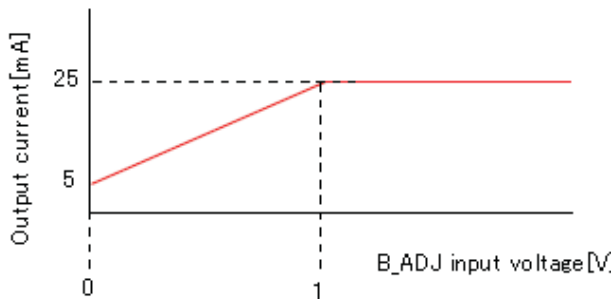


Figure 8. Output Current vs B_ADJ Input Voltage (RSENSE = 10 Ω)

The principle of the operation is to adjust the duty cycle of the MOSFET. When the B_ADJ input voltage is changed, the level of “A” point shown in Figure 9 is changed to get the desired duty cycle compared to the sense current.

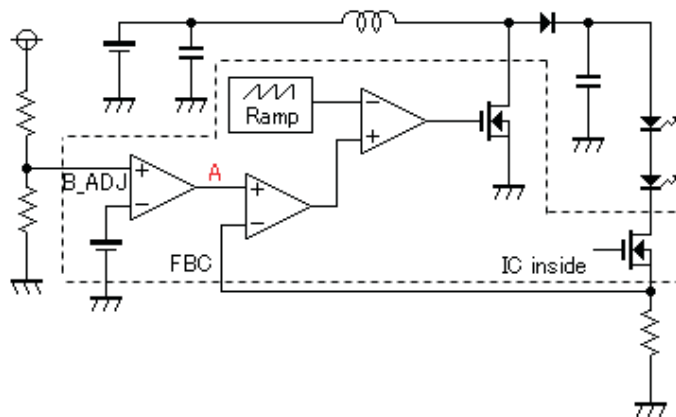


Figure 9. LED Brightness Control Block Diagram

At first, CH7 operates as pulse frequency modulation (PFM) mode at start-up. After reaching the target output voltage, CH7 operation is changed from PFM mode to pulse width modulation (PWM) mode automatically. The output voltage is programmable up to 20 V to use the feedback loop sensed by the external resistances. The maximum output voltage is calculated by [Equation 8](#). The block diagram is shown in [Figure 10](#).

$$V_{OUT7\ MAX} = 1 + (R2/R1) \times 1.25 \text{ [V]} \quad (8)$$

Where:

$V_{OUT7\ MAX}$ = Maximum output voltage of CH7 [V]

R1, R2 = Feedback resistance (see [Figure 10](#))

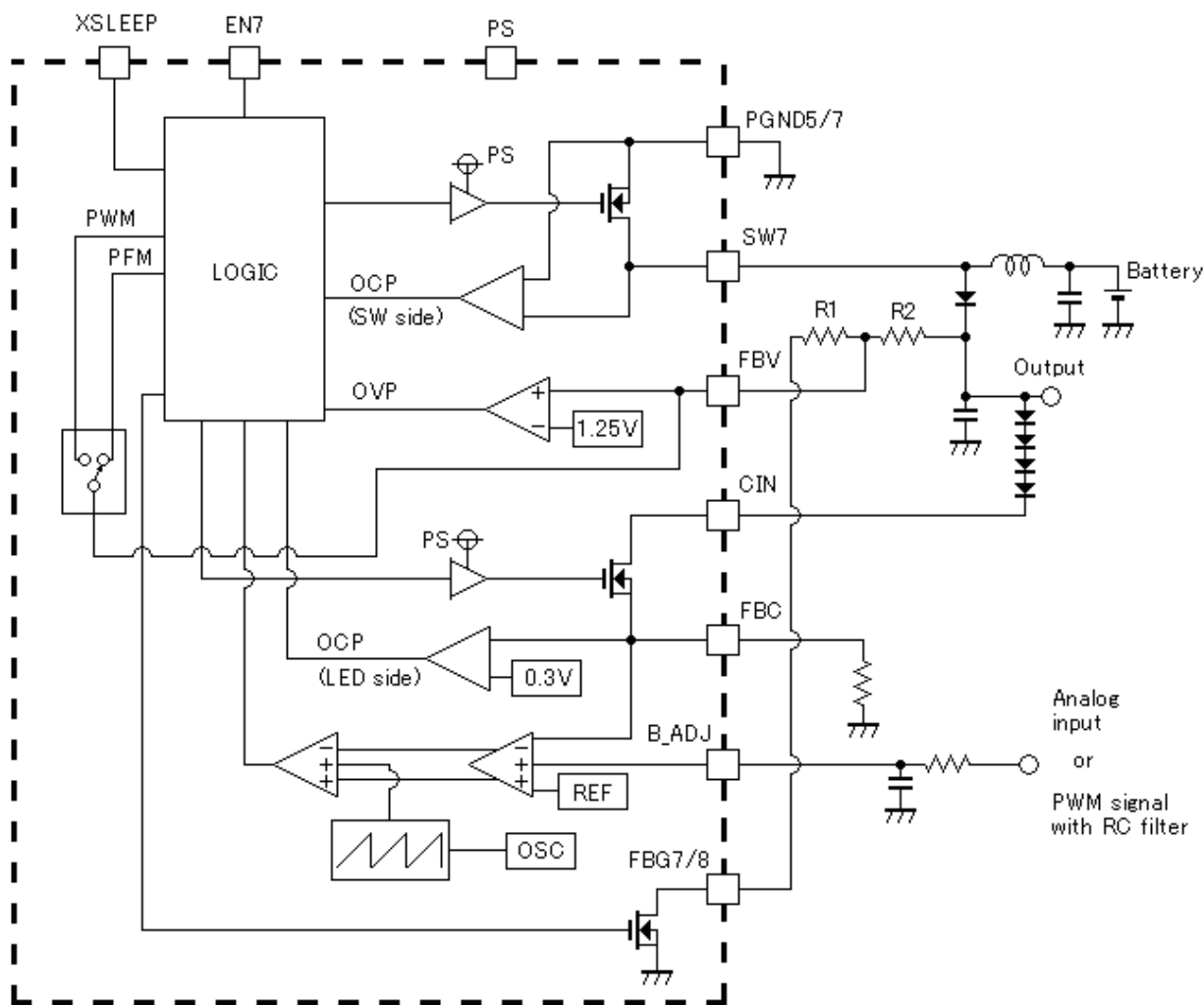


Figure 10. CH7 Block Diagram

CH7 Recommended Parts

Table 18. Recommended Parts for Inductor (CH7)

| VENDOR | TYPE NO. | INDUCTANCE (μH) | DCR (mΩ) | SIZE (mm) |
|--------|---------------------|-----------------|----------|-----------------|
| TOKO | DE2815C-1071AS-120M | 12.0 | 240 | 2.8 × 3.0 × 1.2 |

Table 19. Recommended Parts for Capacitor (Input, CH7)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|--------|-------------------|------------------|---------------|------------------------------------|
| Murata | GRM21BB31A106KE18 | 10.0 | 10 | 2.0 × 1.25 × 1.25 (EIA code: 0805) |

Table 20. Recommended Parts for Diode (CH7)

| VENDOR | TYPE NO. | VR (V) | IF (mA) | VF (V)/IF (A) | CAPACITANCE (μF) | SIZE (mm) |
|--------|----------|--------|---------|---------------|------------------|-----------------|
| Sanyo | SB0503EJ | 30 | 500 | 0.55/0.5 | 16.5 | 1.6 × 0.8 × 0.6 |

Table 21. Recommended Parts for Capacitor (Output, CH7)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|--------|-------------------|------------------|---------------|----------------------------------|
| Murata | GRM31CB31E106KA75 | 10.0 | 10 | 3.2 × 1.6 × 1.6 (EIA code: 1206) |

CH8 Description

CH8 uses an external FET. It is based on voltage-mode-controlled synchronous boost converter topology used for motor control and an IC inside driver. CH8 output should connect to PS (pin 29) because PS is the path to supply the power for the driver of each channel. This channel has two operation modes – PWM and PFM. The operation depends on the XSLEEP (pin 7) and ENAFE (pin 6) signal level.

When XSLEEP turns high, CH8 operates as PWM mode. The ENAFE signal level does not matter. For start-up (less than 2.5 V at CH8 output), CH8 operates as WAKE mode to use the internal MOSFET switch connected to LL8 (pin 27). The duty cycle of WAKE mode is fixed. After PS voltage reaches 2.5 V, CH8 operation is changed from WAKE mode to PFM mode automatically. PFM mode is driven by the external MOSFET switch. When PS voltage reaches 90% of the target voltage, the operation mode is changed from PFM mode to PWM mode automatically. To operate CH8 in PFM mode only, XSLEEP must be high at first. After that, XSLEEP goes low and ENAFE is high for PFM mode. PFM operation is recommended for the IC drive only from an efficiency point of view.

CH8 has reversed current protection to monitor the different voltage between LL8 and PS. The protection monitors the difference between both PFM mode and PWM mode. When LL8 voltage is larger than PS voltage, the function is activated. When the function is activated, SW8HD (pin 28) level is changed from high to low; SW8LD (pin 26) level stays low. This means that LL8 voltage converges the battery voltage naturally.

The recovery condition is dependent on the operation mode. When CH8 operates as PFM mode, the condition is that FB8 (pin 30) voltage is less than 1.25 V. When CH8 operates as PWM mode, the condition is that LL8 voltage is smaller than PS voltage at the rising edge of the internal clock.

The output voltage is programmable from 3.3 V to 5.5 V to use the feedback loop sensed by the external resistances. The output voltage is calculated by [Equation 9](#). The block diagram is shown in [Figure 11](#).

$$V_{OUT8} = (1 + R1/R2) \times 1.25 \text{ [V]} \quad (9)$$

Where:

V_{OUT8} = Output voltage of CH8 [V]

R1, R2 = Feedback resistance (see [Figure 11](#))

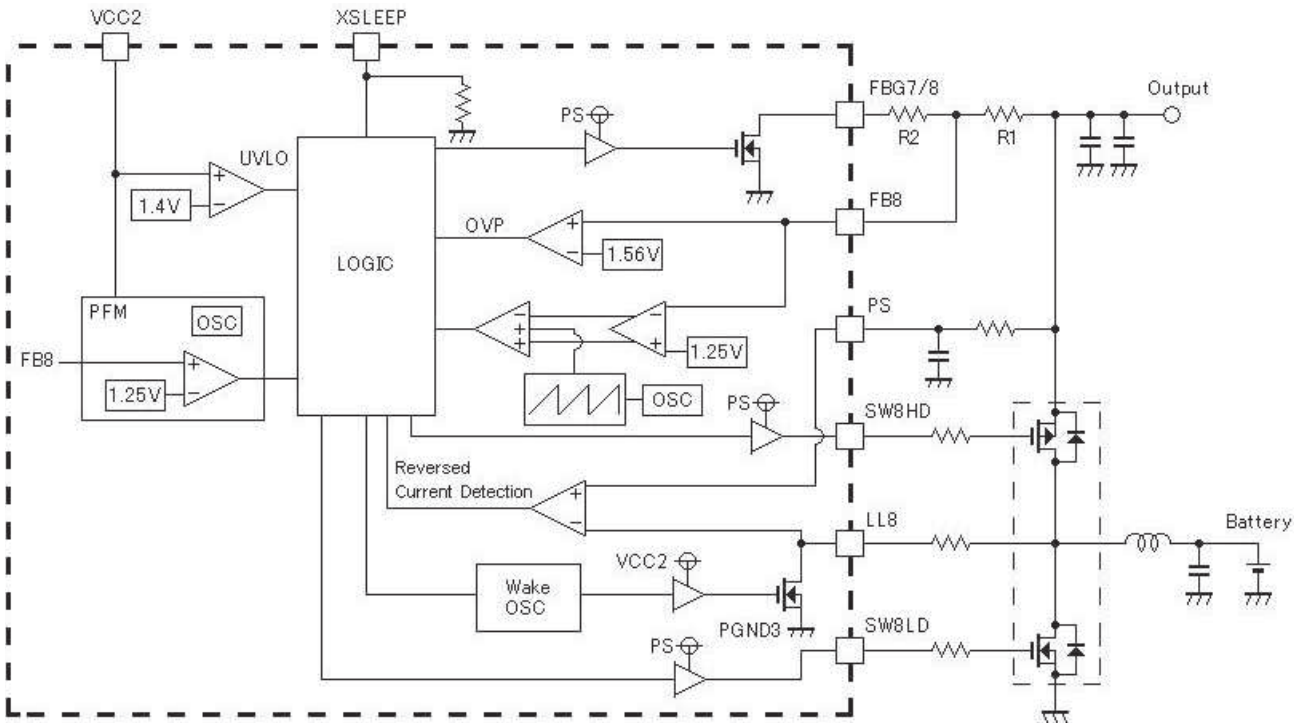


Figure 11. CH8 Block Diagram

CH8 Recommended Parts

For Motor Control and IC Inside Driver

Table 22. Recommended Parts for Inductor (CH8)

| VENDOR | TYPE NO. | INDUCTANCE (μH) | DCR (mΩ) | SIZE (mm) |
|--------|------------------|-----------------|----------|-----------------|
| TOKO | DE4518-1124-4R3M | 4.3 | 54 | 4.5 × 4.7 × 1.8 |

Table 23. Recommended Parts for Capacitor (Input, CH8)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|--------|----------------|------------------|---------------|-----------------------------------|
| TDK | C3216X5R0J226M | 22.0 × 2 pcs | 20 | 3.2 × 1.6 × 0.85 (EIA code: 1206) |

Table 24. Recommended Parts for Capacitor (Output, CH8)

| VENDOR | TYPE NO. | CAPACITANCE (μF) | TOLERANCE (%) | SIZE (mm) |
|--------|-------------------|------------------|---------------|-----------------------------------|
| Murata | GRM31MB31A106KE18 | 10.0 × 2 pcs | 10 | 3.2 × 1.6 × 1.15 (EIA code: 1206) |

Table 25. Recommended Parts for FET (CH8)

| VENDOR | TYPE NO. | ID (DC) (N-ch) (A) | ID (DC) (P-ch) (A) | Rds(on) (N-ch) (Ω) | Rds(on) (P-ch) (Ω) | QG (N-ch) (nC) | QG (P-ch) (nC) |
|--------|----------|--------------------|--------------------|--------------------|--------------------|----------------|----------------|
| Sanyo | VEC2607 | 4.5 | -4.0 | 0.032/4 V | 0.037/-4.5 V | 7.6 | 11.0 |
| | VEC2611 | 3.0 | -2.6 | 0.053/4 V | 0.080/-4.5 V | 8.8 | 6.5 |

For IC Inside Driver Only
Table 26. Recommended Parts for Inductor (CH8)

| VENDOR | TYPE NO. | INDUCTANCE (μ H) | DCR (m Ω) | SIZE (mm) |
|-------------|------------|-----------------------|-------------------|-----------------|
| Taiyo Yuden | LB2518T330 | 33 | 700 | 1.8 × 2.5 × 1.8 |

Table 27. Recommended Parts for Capacitor (Input, CH8)

| VENDOR | TYPE NO. | CAPACITANCE (μ F) | TOLERANCE (%) | SIZE (mm) |
|--------|----------------|------------------------|---------------|-----------------------------------|
| TDK | C3216X5R0J226M | 22 | 20 | 3.2 × 1.6 × 0.85 (EIA code: 1206) |

Table 28. Recommended Parts for Capacitor (Output, CH8)

| VENDOR | TYPE NO. | CAPACITANCE (μ F) | TOLERANCE (%) | SIZE (mm) |
|--------|----------------|------------------------|---------------|----------------------------------|
| TDK | C1608X5R0J475M | 4.7 | 20 | 1.6 × 0.8 × 0.8 (EIA code: 0603) |



Table 29. Recommended Parts for FET (CH8)

| VENDOR | TYPE NO. | ID (DC) (N-ch) (A) | ID (DC) (P-ch) (A) | Rds(on) (N-ch) (Ω) | Rds(on) (P-ch) (Ω) | QG (N-ch) (nQ) | QG (P-ch) (nQ) |
|------------------|-----------|-----------------------|-----------------------|--------------------------------|--------------------------------|----------------|----------------|
| ON Semiconductor | NTZD3155C | 0.54 | –0.43 | 0.4/4.5 V | 0.5 /–4.5 V | 1.5 | 1.7 |
| Sanyo | SCH2615 | 1.2 | –0.9 | 0.28/4 V | 0.47/–4.5 V | 1.15 | 1.43 |

Layout Consideration

To avoid ground shift problems due to the high currents in the switches, separate AGND (pin 10) from PGND1 (pin 20), PGND2 (pin 14), PGND3 (pin 25), PGND4 (pin 2), and PGND5/7 (pin 37). The reference GND for all control signals, such as XSLEEP, is AGND. The power switches inside the IC are connected to PGND1, PGND2, PGND3, PGND4, and PGND5/7. Both grounds must be connected on the printed circuit board (PCB) (ideally at only one point).

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| TPS65530ARSLR | ACTIVE | VQFN | RSL | 48 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -25 to 85 | TPS 65530A |  |
| TPS65530ARSLT | ACTIVE | VQFN | RSL | 48 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -25 to 85 | TPS 65530A |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS65530ARSLR | VQFN | RSL | 48 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65530ARSLT | VQFN | RSL | 48 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

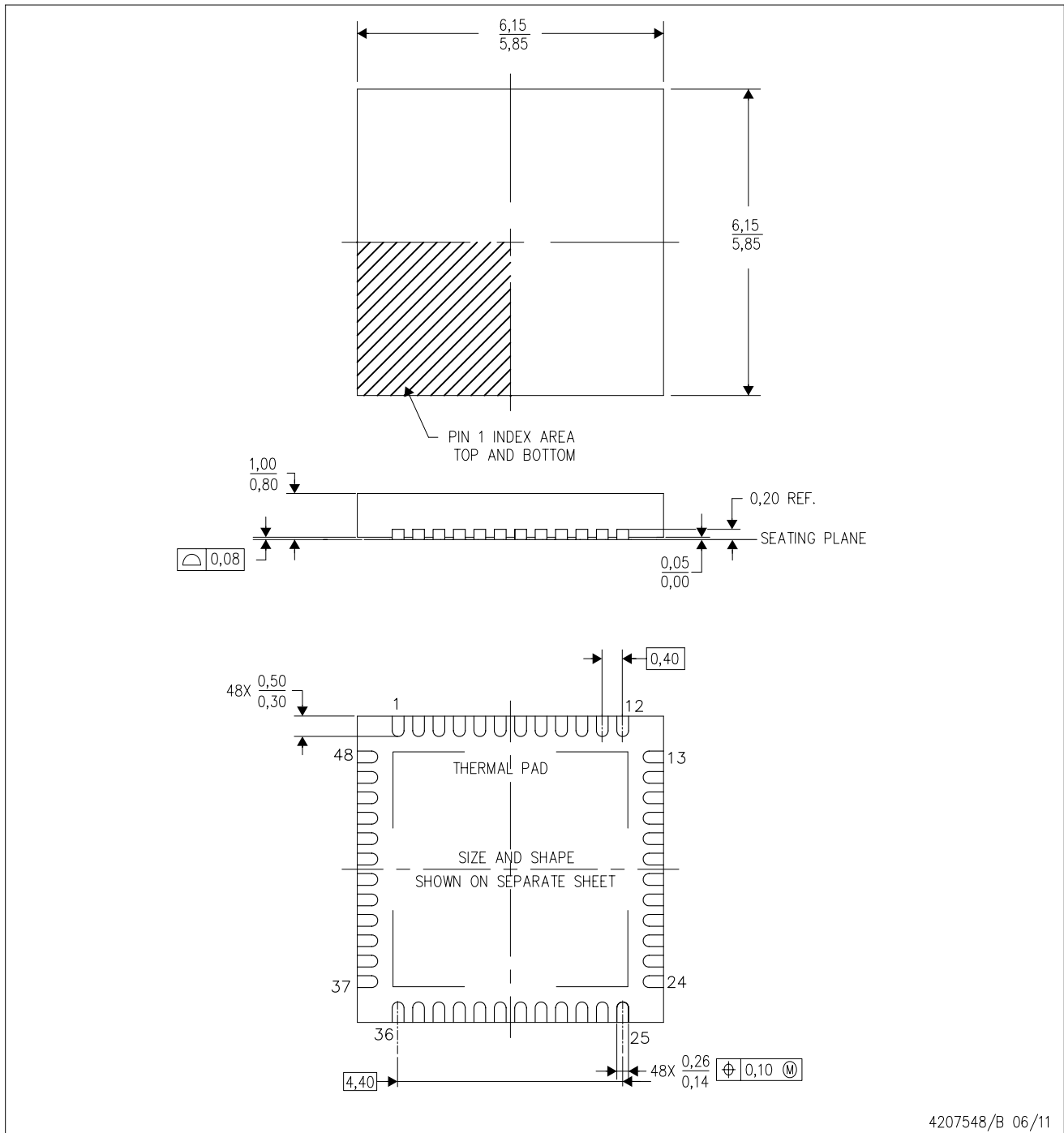

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS65530ARSLR | VQFN | RSL | 48 | 2500 | 367.0 | 367.0 | 38.0 |
| TPS65530ARSLT | VQFN | RSL | 48 | 250 | 210.0 | 185.0 | 35.0 |

MECHANICAL DATA

RSL (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RSL (S-PVQFN-N48)

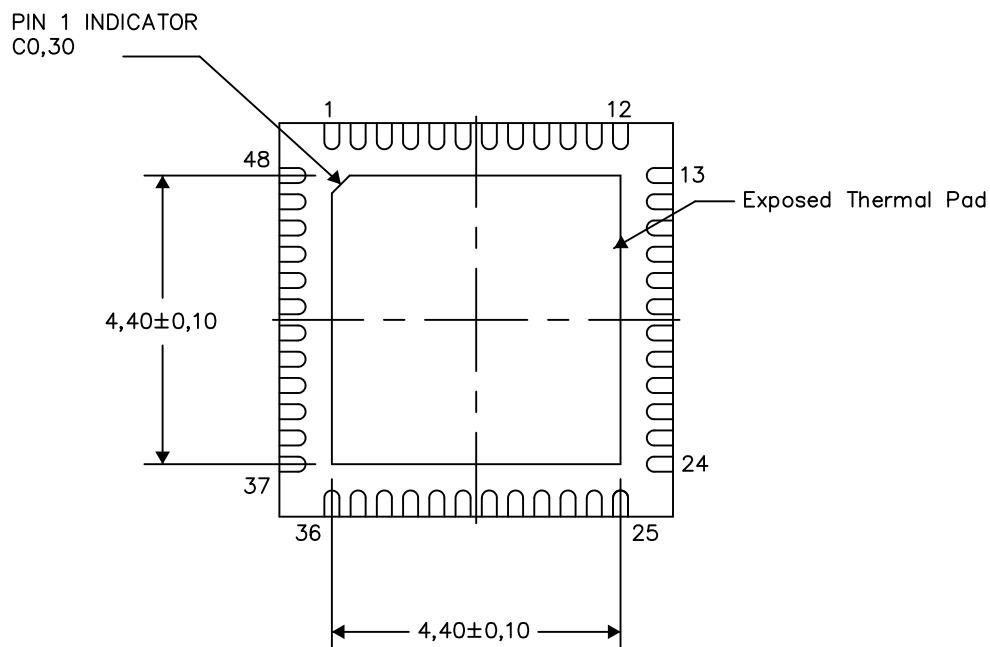
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

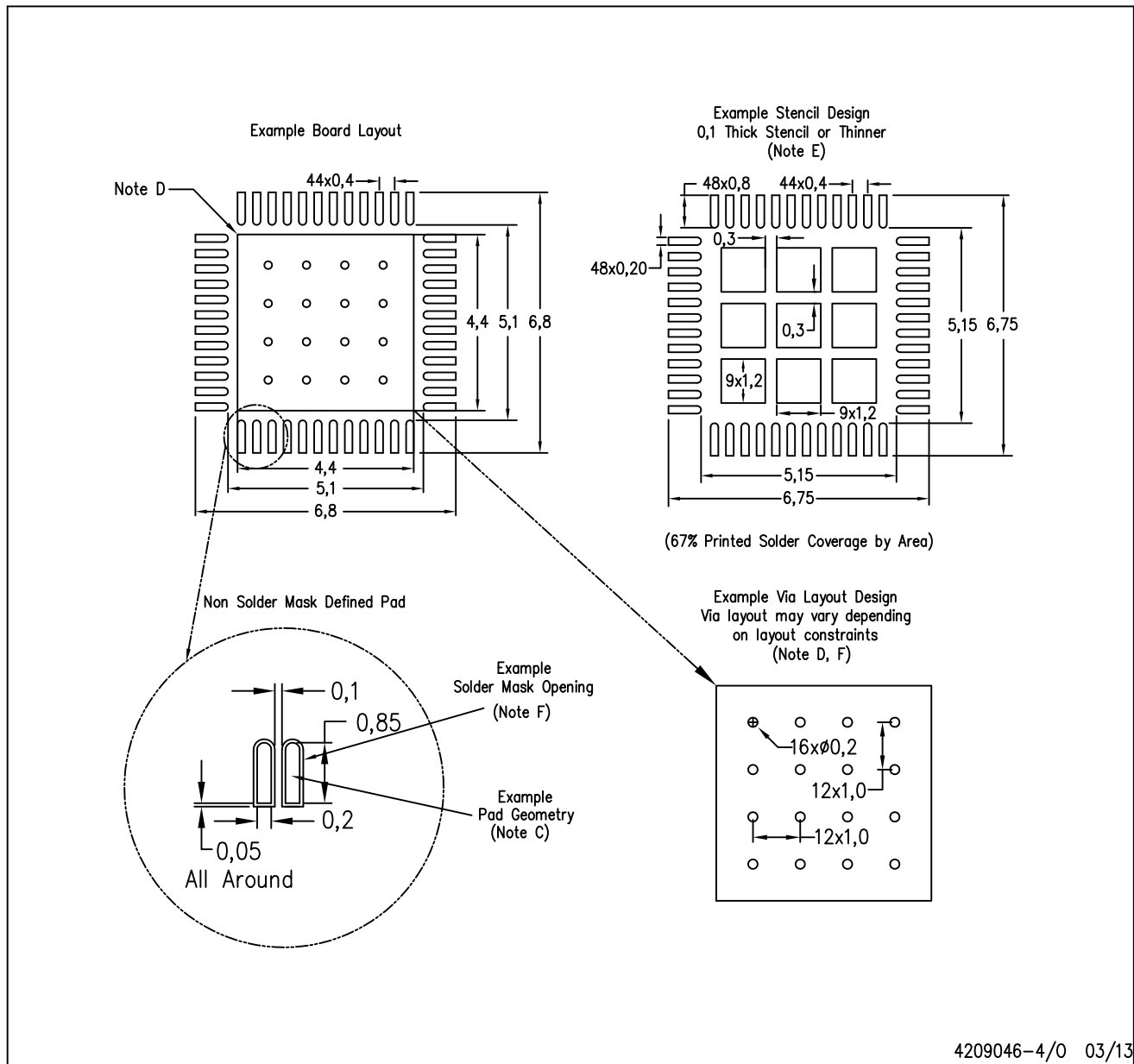
Exposed Thermal Pad Dimensions

4207841-2/P 03/13

NOTE: All linear dimensions are in millimeters

RSL (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SQN PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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