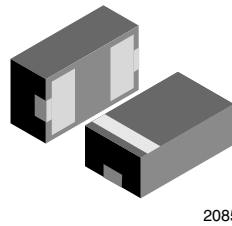
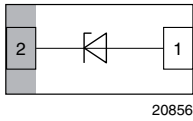


## Low Capacitance, Single-Line ESD Protection Diode



### MARKING (example only)



Bar = cathode marking  
 Y = type code (see table below)  
 X = date code

### DESIGN SUPPORT TOOLS



### FEATURES

- Ultra compact LLP1006-2L package
- Low package profile < 0.4 mm
- 1-line ESD protection
- High surge current acc. IEC 61000-4-5  $I_{PPM} > 3$  A
- Low leakage current  $I_R < 0.1$   $\mu$ A
- Low load capacitance  $C_D = 0.9$  pF
- ESD immunity acc. IEC 61000-4-2  $\pm 15$  kV contact discharge  $\pm 15$  kV air discharge
- Soldering can be checked by standard vision inspection; no X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



ORDERING INFORMATION			
DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VBUS051BD-HD1	VBUS051BD-HD1-GS08	8000	8000

PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VBUS051BD-HD1	LLP1006-2L	A	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS VBUS051BD-HD1				
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5; $t_p = 8/20$ $\mu$ s; single shot	$I_{PPM}$	3	A
Peak pulse power	Acc. IEC 61000-4-5; $t_p = 8/20$ $\mu$ s; single shot	$P_{PP}$	45	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	$V_{ESD}$	$\pm 15$	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		$\pm 15$	kV
Operating temperature	Junction temperature	$T_J$	-55 to +145	°C
Storage temperature		$T_{STG}$	-55 to +150	°C

PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)

This Vishay product is protected by one or more United States and international patents.

<b>ELECTRICAL CHARACTERISTICS VBUS051BD-HD1</b> (Ratings at 25 °C ambient temperature, unless otherwise specified)						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{\text{channel}}$	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	$V_{\text{RWM}}$	-	-	5	V
Reverse voltage	At $I_{\text{R}} = 0.1 \mu\text{A}$ ; pin 2 to pin 1	$V_{\text{R}}$	5	-	-	V
Reverse current	At $V_{\text{R}} = V_{\text{RWM}} = 5 \text{ V}$ ; pin 2 to pin 1	$I_{\text{R}}$	-	< 0.01	0.1	$\mu\text{A}$
Reverse breakdown voltage	At $I_{\text{R}} = 1 \text{ mA}$ ; pin 2 to pin 1	$V_{\text{BR}}$	6.9	7.9	8.7	V
Reverse clamping voltage	At $I_{\text{PP}} = 3 \text{ A}$ ; acc. IEC 61000-4-5; pin 2 to pin 1	$V_{\text{C}}$	-	-	16	V
Forward clamping voltage	At $I_{\text{F}} = 3 \text{ A}$ ; acc. IEC 61000-4-5; pin 1 to pin 2	$V_{\text{F}}$	-	3.4	4	V
Capacitance	At $V_{\text{R}} = 0 \text{ V}$ ; $f = 1 \text{ MHz}$ ; pin 2 to pin 1	$C_{\text{D}}$	-	0.9	1.3	pF

### APPLICATION NOTE

The VBUS051BD-HD1 is an ESD protection device with the characteristic of a Z-diode with a high ESD immunity and a very low capacitance which makes it usable for high frequency applications like USB2.0 or HDMI.

With the VBUS051BD-HD1 one high speed data line can be protected against transient voltage signals like ESD (electro static discharge). Connected to the data line (pin 2) and to ground (pin 1) negative transients will be clamped close below the ground level while positive transients will be clamped close above the 5 V working range. The clamping behavior of the VBUS051BD-HD1 is bidirectional but asymmetrical (BiAs) and so it offers the best protection for applications running up to 5 V.

### TYPICAL CHARACTERISTICS ( $T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$ , unless otherwise specified)

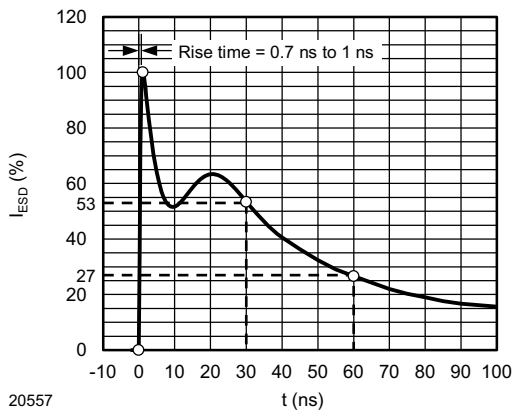


Fig. 1 - ESD Discharge Current Wave Form  
acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

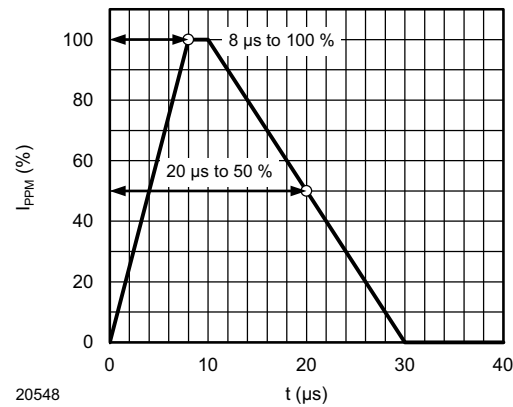


Fig. 2 - 8/20  $\mu\text{s}$  Peak Pulse Current Wave Form  
acc. IEC 61000-4-5

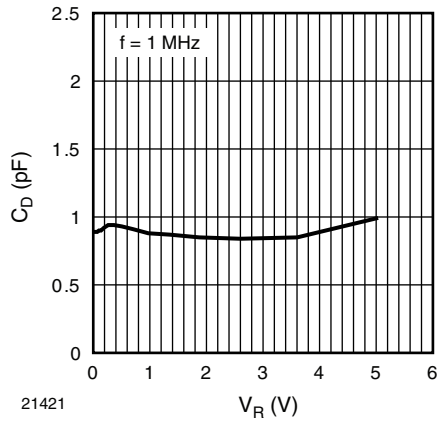


Fig. 3 - Typical Capacitance  $C_D$  vs. Reverse Voltage  $V_R$

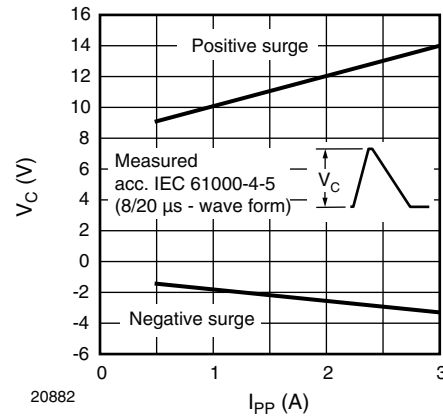


Fig. 6 - Typical Peak Clamping Voltage  $V_C$  vs. Peak Pulse Current  $I_{PP}$

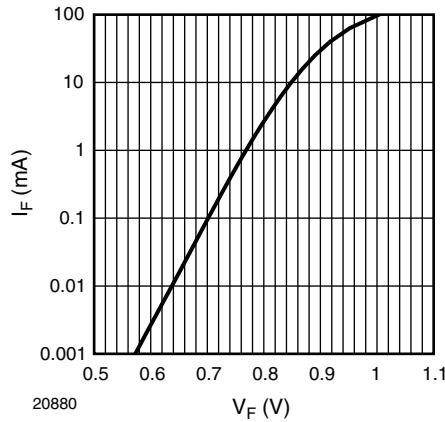


Fig. 4 - Typical Forward Current  $I_F$  vs. Forward Voltage  $V_F$

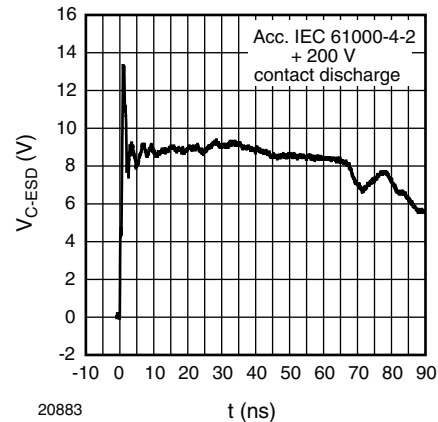


Fig. 7 - Typical Clamping Performance at + 200 V Contact Discharge (acc. IEC 61000-4-2)

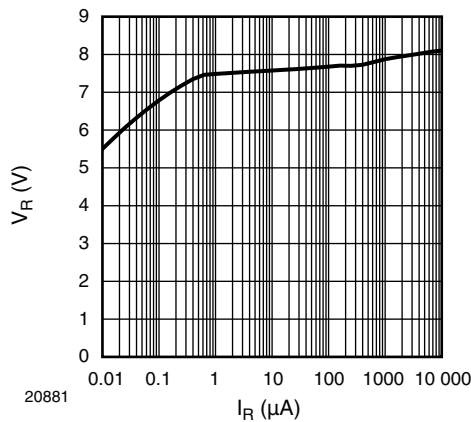


Fig. 5 - Typical Reverse Voltage  $V_R$  vs. Reverse Current  $I_R$

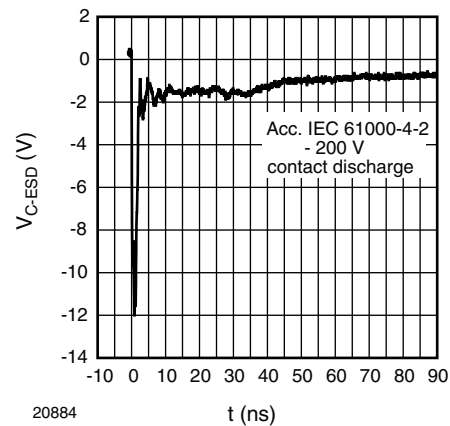


Fig. 8 - Typical Clamping Performance at - 200 V Contact Discharge (acc. IEC 61000-4-2)

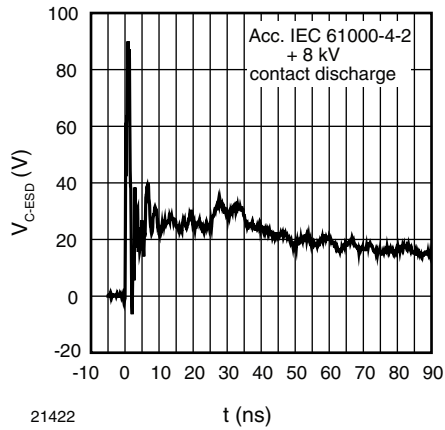


Fig. 9 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

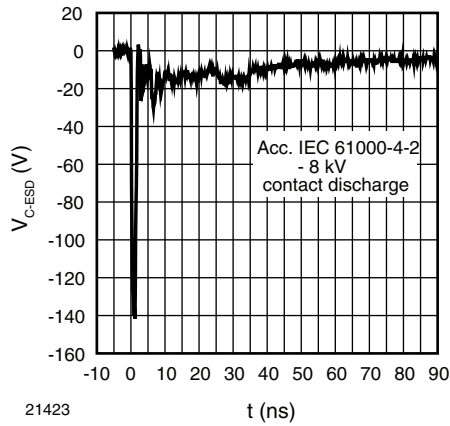


Fig. 10 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

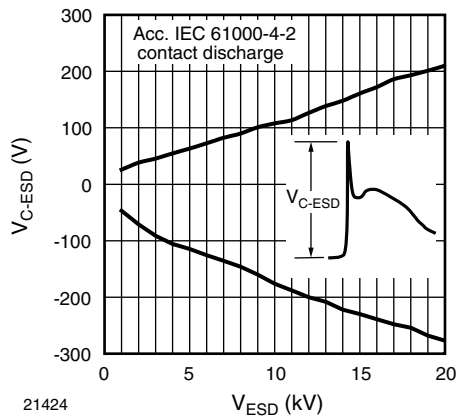
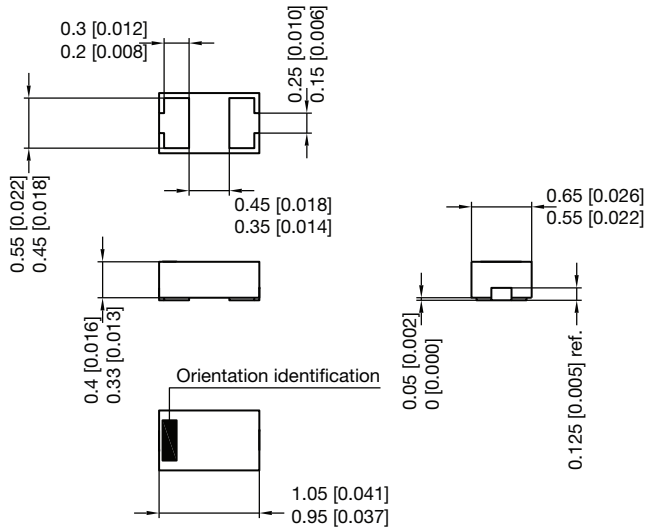


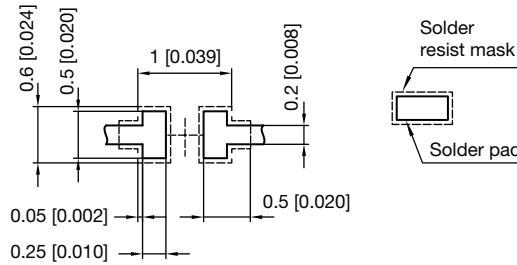
Fig. 11 - Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)



**PACKAGE DIMENSIONS** in millimeters (inches) **LLP1006-2L**

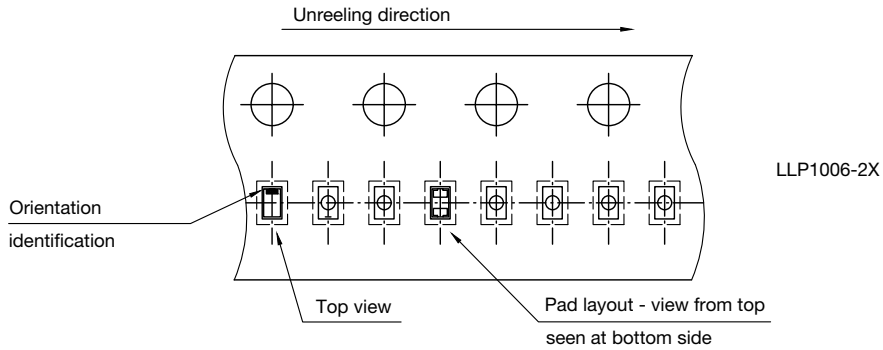


Foot print recommendation:



Pad Design Patented:  
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20812



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02.05.2017  
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