PHD97NQ03LT



N-channel TrenchMOS logic level FET

Rev. 01 — 24 March 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Fast switching
- Lead-free packing
- Logic level threshold

- Low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- Computer motherboard high frequency DC-to-DC convertors
- Switched-mode power supplies
- Voltage regulators

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	25	V
I_D	drain current	$T_{mb} = 25 ^{\circ}\text{C}; V_{GS} = 10 \text{V};$ see <u>Figure 1</u> ; see <u>Figure 3</u>	-	-	75	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	107	W
Dynamic	Dynamic characteristics					
Q_{GD}	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A};$ $V_{DS} = 12 \text{ V}; \text{ see } \frac{\text{Figure 9}}{\text{Figure 10}};$	-	1.9	-	nC
Static ch	Static characteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 7}}{\text{see } \frac{\text{Figure 8}}{\text{otherwise}}}$	-	5.3	6.3	mΩ



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain	mb	D
3	S	source		$G \longrightarrow A$
mb	D	mounting base; connected to drain	1 3	mbb076 S
			SOT428 (SC-63; DPAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHD97NQ03LT	SC-63; DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage	$T_j \ge 25$ °C; $T_j \le 175$ °C; $R_{GS} = 20$ kΩ	-	25	V
V_{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see <u>Figure 1</u>	-	69	Α
		V _{GS} = 10 V; T _{mb} = 25 °C; see <u>Figure 1</u> ; see <u>Figure 3</u>	-	75	Α
I _{DM}	peak drain current	$t_p \le 10 \mu\text{s}; \text{ pulsed}; T_{mb} = 25 ^{\circ}\text{C}; \text{ see } \frac{\text{Figure 3}}{}$	-	300	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	107	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-dr	ain diode				
Is	source current	$T_{mb} = 25 ^{\circ}C$	-	75	Α
I _{SM}	peak source current	$t_p \le 10 \ \mu s$; pulsed; $T_{mb} = 25 \ ^{\circ}C$	-	240	Α
Avalanche	ruggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 35 A; V_{sup} ≤ 25 V; unclamped; t_p = 0.1 ms; R_{GS} = 50 Ω	-	60	mJ

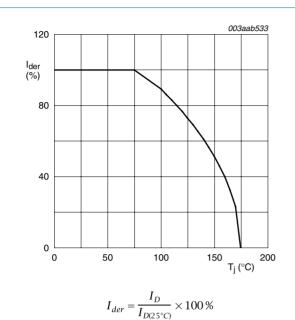
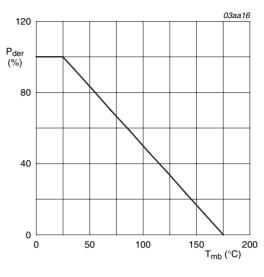
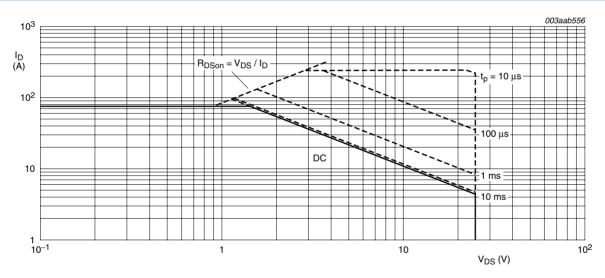


Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



 $T_{mb} = 25 \,^{\circ}C; I_{DM}$ is single pulse

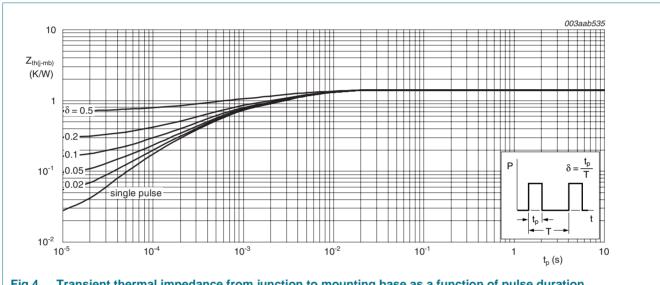
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

Thermal characteristics

Thermal characteristics Table 5.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4		-	-	1.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint	[1]	-	75	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air



6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	25	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	22	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see <u>Figure 5</u> ; see <u>Figure 6</u>	1.3	1.7	2.15	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 175$ °C; see <u>Figure 5</u>	0.7	-	-	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see Figure 5	-	-	2.6	V
I _{DSS}	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see <u>Figure 7</u> ; see <u>Figure 8</u>	-	10.1	12	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 7</u> ; see <u>Figure 8</u>	-	8	10.6	mΩ
		$V_{GS} = 10 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 25 \text{ °C}$; see Figure 7; see Figure 8	-	5.3	6.3	mΩ
I _{DSS}	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 ^{\circ}\text{C}$	-	-	100	μΑ
R_G	gate resistance	f = 1 MHz	-	1.5	-	Ω
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 12 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; see <u>Figure 9</u> ; see <u>Figure 10</u>	-	11.7	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 4.5 \text{ V}$	-	10.2	-	nC
Q _{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	6.2	-	nC
Q _{GS1}	pre-threshold gate-source charge	see <u>Figure 9</u> ; see <u>Figure 10</u>	-	3.4	-	nC
Q _{GS2}	post-threshold gate-source charge		-	2.8	-	nC
Q _{GD}	gate-drain charge		-	1.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}$; $V_{DS} = 12 \text{ V}$; see <u>Figure 9</u> ; see <u>Figure 10</u>	-	3.1	-	V
C _{iss}	input capacitance	$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 ^{\circ}\text{C}; \text{ see } \frac{\text{Figure 11}}{\text{Comparison}}$	-	1570	-	pF
		$V_{DS} = 0 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$	-	1800	-	pF
Coss	output capacitance	$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	380	-	pF
C _{rss}	reverse transfer capacitance	T _j = 25 °C; see <u>Figure 11</u>	-	160	-	pF

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.5 Ω ; V_{GS} = 4.5 V;	-	18	-	ns
t _r	rise time	$R_{G(ext)} = 5.6 \Omega$	-	33	-	ns
t _{d(off)}	turn-off delay time		-	20	-	ns
t _f	fall time		-	12	-	ns
Source-di	rain diode					
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 12</u>	-	0.87	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	38	-	ns
Q _r	recovered charge	$V_{DS} = 30 \text{ V}$	-	14	-	nC

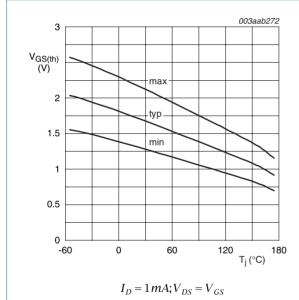


Fig 5. Gate-source threshold voltage as a function of junction temperature

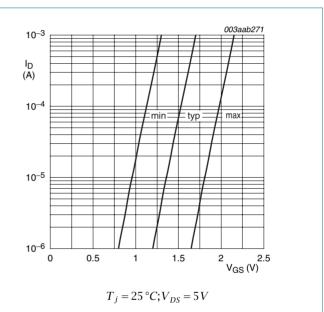


Fig 6. Sub-threshold drain current as a function of gate-source voltage

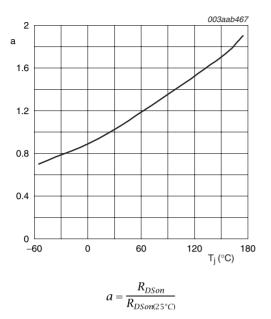
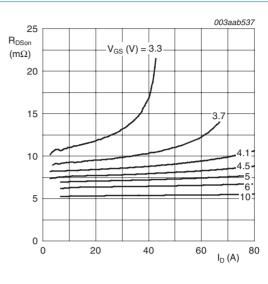


Fig 7. Normalized drain-source on-state resistance factor as a function of junction temperature



 $T_j = 25^{\circ}C$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values

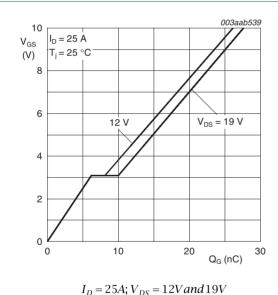


Fig 9. Gate-source voltage as a function of gate charge; typical values

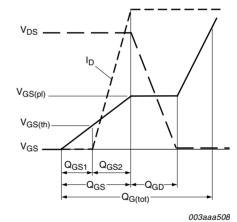


Fig 10. Gate charge waveform definitions

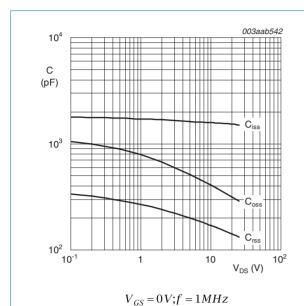
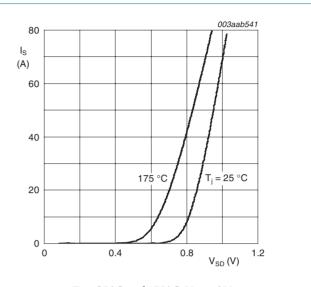


Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $T_j = 25$ °C and 175°C; $V_{GS} = 0V$

Fig 12. Source current as a function of source-drain voltage; typical values

7. Package outline

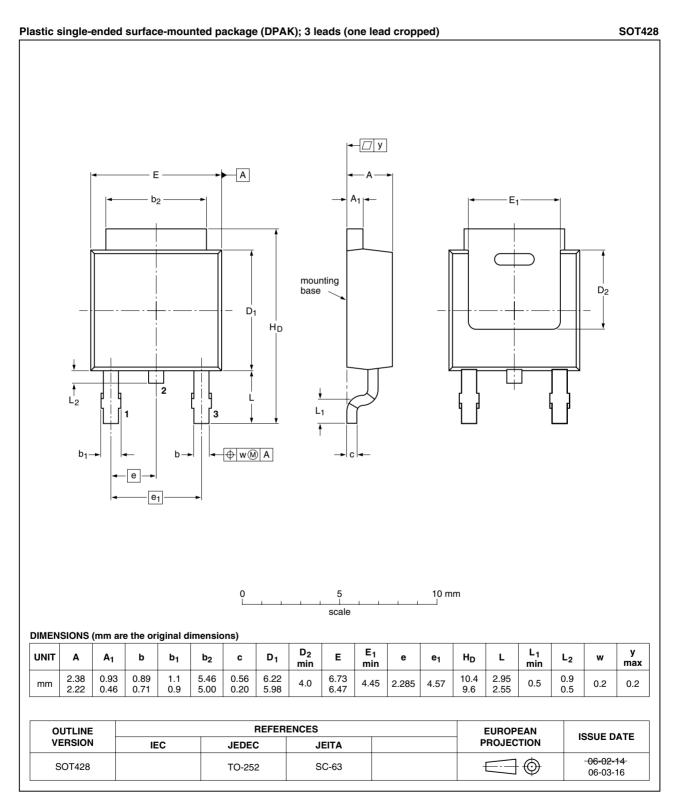


Fig 13. Package outline SOT428 (DPAK)



8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD97NQ03LT_1	20090324	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions"
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