

STSJ25NF3LL

N-CHANNEL 30V - 0.0085 Ω - 25A PowerSO-8™ LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STSJ25NF3LL	30 V	<0.0105 Ω	25 A

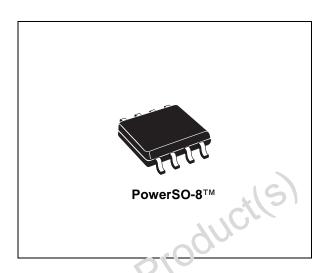
- TYPICAL R_{DS}(on) = 0.0085 Ω @ 10V
- TYPICAL Q_q = 24 nC @ 4.5 V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- IMPROVED JUNCTION-CASE THERMAL RESISTANCE

DESCRIPTION

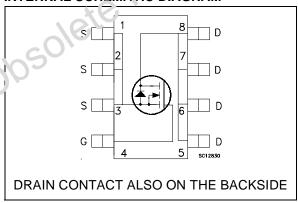
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature SizeTM" strip-based process. This silicon, housed in thermally improved SO-8TM package, exhibits optimal on-resistance versus gate charge tradeoff plus lower $R_{thj-c.}$



■ SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE P 3s



INTERNAL SCHEMATIC DIAGRAM



AESOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V_{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	30	V
V _G S	Gate- source Voltage	± 16	V
I _D	Drain Current (continuous) at T _C = 25°C (*)	25	A
I _D	Drain Current (continuous) at T _C = 25°C (#)	12	A
I _D	Drain Current (continuous) at T _C = 100°C	16	A
I _{DM} (•)	Drain Current (pulsed)	100	A
P _{tot}	Total Dissipation at $T_C = 25^{\circ}C$ Total Dissipation at $T_C = 25^{\circ}C$ (#)	70 3	W

^(•) Pulse width limited by safe operating area.

^(*) Value limited by wires bonding

THERMAL DATA

1 '	Thermal Resistance Junction-case Max (*)Thermal Resistance Junction-ambient Max	1.8 42	°C/W °C/W
T_j	Maximum Operating Junction Temperature Storage Temperature	150 -55 to 150	°C °C

^(*) When mounted on FR-4 board with 0.5 in² pad of Cu.

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_{C} = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$	I _D = 250 μA	10	4O		V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V V _{GS} = 4.5 V	I _D = 12.5 A I _D = 12.5 A	e Y	0.0085 0.011	0.0105 0.013	Ω Ω

DYNAMIC

Ţ	Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
,	g _{fs} (*)	Forward Transconductance	V _{DS} =15 V I _D = 12.5 A		20		S
·	C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1 MHz$, $V_{GS} = 0$		1650 540 130		pF pF pF
0	osole	te Proc.					

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	$\begin{aligned} &V_{DD} = 15 \text{ V} & I_{D} = 12.5 \text{ A} \\ &R_{G} = 4.7 \Omega & V_{GS} = 4.5 \text{ V} \\ &(\text{Resistive Load, Figure 1}) \end{aligned}$		23 156		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} =15V I _D =25A V _{GS} =4.5V (see test circuit, Figure 2)		24 8.5 12	33	nC nC nC

SWITCHING OFF

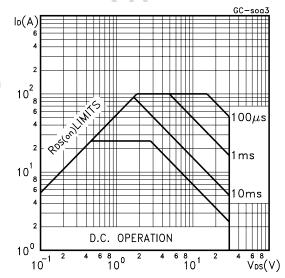
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(off)} t _f	Turn-off Delay Time Fall Time	$\begin{aligned} &V_{DD} = 15 \text{ V} & I_D = 12.5 \text{ A} \\ &R_G = 4.7\Omega, &V_{GS} = 4.5 \text{ V} \\ &(\text{Resistive Load, Figure 3}) \end{aligned}$		27 28		ns ns

SOURCE DRAIN DIODE

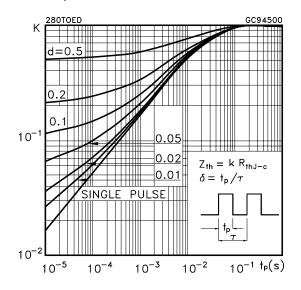
Symbol	Parameter	Test Con	ditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				400	25 100	A A
V _{SD} (*)	Forward On Voltage	I _{SD} = 25 A	V _{GS} = 0	OY		1.2	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 25 \text{ A}$ $V_{DD} = 25 \text{ V}$ (see test circuit,	di/dt = 100A/ μ s T _j = 150°C Figure 3)	(o	40 50 2.5		ns nC A

^(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Safe Operating Area

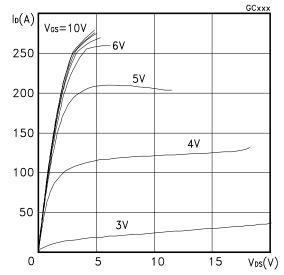


Thermal Impedance

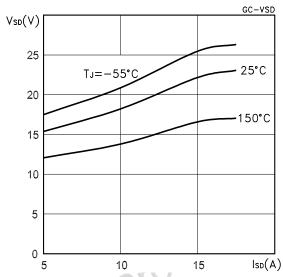


^(•)Pulse width limited by safe operating area.

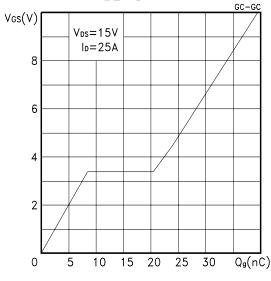
Output Characteristics



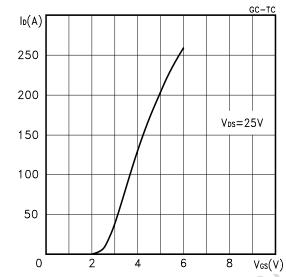
Transconductance



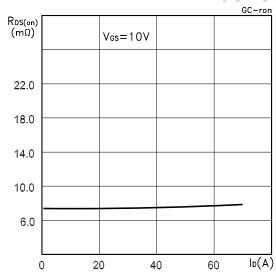
Gate Charge vs Gate-source Voltage



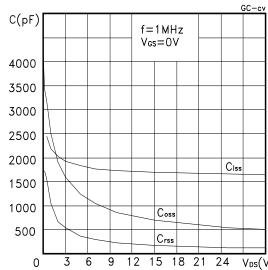
Transfer Characteristics



Static Drain-source On Resistance

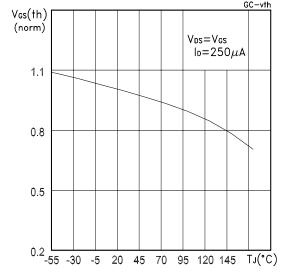


Capacitance Variations

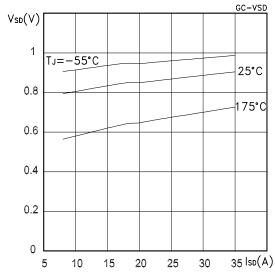


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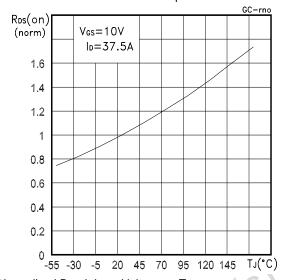
Normalized Gate Threshold Voltage vs Temperature



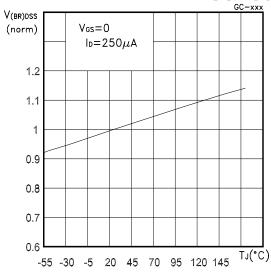
Source-drain Diode Forward Characteristics



Normalized on Resistance vs Temperature



Normalized Breakdown Voltage vs Temperature.



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Fig. 1: Switching Times Test Circuits For Resistive Load

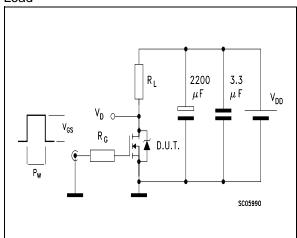


Fig. 2: Gate Charge test Circuit

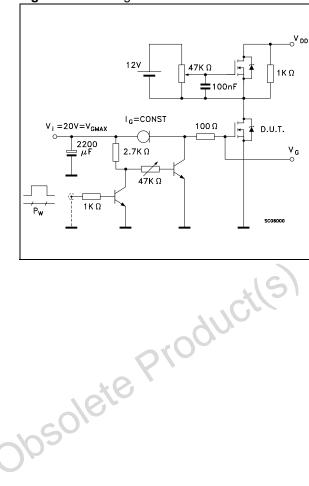
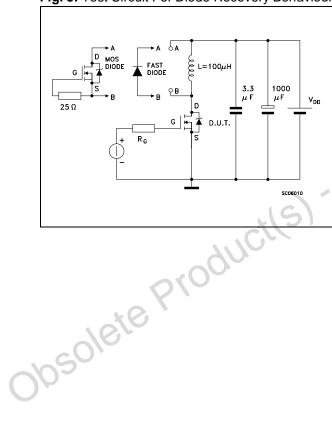


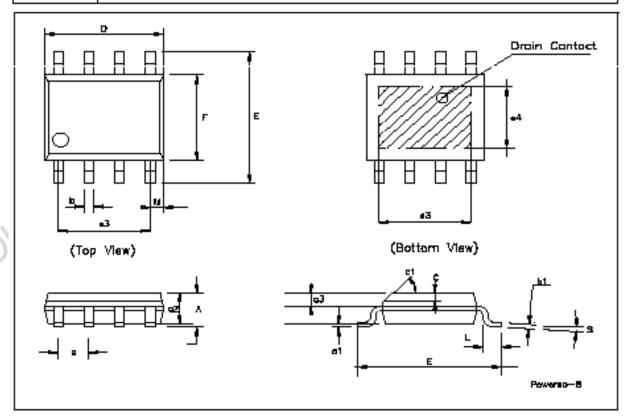
Fig. 3: Test Circuit For Diode Recovery Behaviour



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PowerSO-8™ MECHANICAL DATA

DIM.		mm.		inch			
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.	
Α			1.75			0.068	
a1	0.1		0.25	0.003		0.009	
a2			1.65			0.064	
a3	0.65		0.85	0.025		0.033	
b	0.35		0.48	0.013		0.018	
b1	0.19		0.25	0.007		0.010	
С	0.25		0.5	0.010		0.019	
c1			45°	(typ.)			
D	4.8		5.0	0.188		0.196	
E	5.8		6.2	0.228		0.244	
e		1.27			0.050		
63		3.81			0.150		
e4		2.79			0.110		
F	3.8		4.0	0.14		0.157	
L	0.4		1.27	0.015		0.050	
M			0.6			0.023	
S			8° (r	nax.)	•	•	



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